Greg P. Semeraro, PhD

18 Royal Birkdale Court
Penfield, New York 14526
(585) 402-9550 (cell)
semeraro@ieee.org

Core Expertise

- Mentoring / Leading
- System Engineering
- System Architecture
- Project Management
- Instruction / Teaching
- Statistical Analysis
- Exploratory Data Analysis
- Real-Time Systems (H/W & S/W)
- Real-Time Operating Systems
- Embedded Software Design
- Multi-threaded Software Design
- Software Architecture
- Embedded Linux / uCLinux
- Linux Kernel-Level Programming
- CPU/MCU Microarchitecture
- Digital Hardware Design
- FPGA / CPLD Design
- VHDL / Verilog
- Hardware / Software Co-Design
- Problem Solving / Debugging
- Optimization / Performance Analysis

Education

Doctor of Philosophy in Electrical (Computer) Engineering, University of Rochester, October 2003 GPA:4.0/4.0

Dissertation: Greg P. Semeraro. *Multiple Clock Domain (MCD) Microarchitecture Design, Analysis and Performance*. Doctoral dissertation, University of Rochester, Electrical and Computer Engineering Department, August 2003.
Advisers: Dr. David H. Albonesi (primary), Dr. Michael Huang, Dr. Martin Margala and Dr. Michael L. Scott.

Master of Science in Computer Engineering, Rochester Institute of Technology, May 1997 GPA:3.4/4.0

Thesis: Greg P. Semeraro. *Evolution of Solutions to Real-Time Problems*. Master's thesis, Rochester Institute of Technology, Department of Computer Engineering, April 1997.
Advisers: Dr. Roy Czernikowski (primary) and Dr. Tony Chang.

Bachelor of Science in Computer Engineering, Boston University, May 1988 GPA:3.3/4.0, *cum laude*

Professional Employment

***Principal Engineer and Partner,* AppliedLogix / Re:Build AppliedLogix, 2020-2023**

Hardware / Firmware / Software / FPGA RTL Design / FPGA Testbench Design Engineer / Architect. Architected and designer for complex embedded systems specializing in Xilinx FPGA devices – both SoC and RTL designs – for both large and small organizations. Designed real-time embedded firmware for high-performance imaging devices and Windows device control software.

***Principal System Architect,* IDEX Biometrics ASA, 2016-2020**

Fingerprint Sensor ASIC Products. System Architect fingerprint scanner product line for biometric smart-card (BSC) payment and identity card applications. Focused on design and specification of system-level architecture, power and temporal performance system model development and hardware / firmware trade-off analysis.

***Senior Staff Architect, Display Integration Architect*, Atmel Corp, 2015-2016**

In-Cell Touch / Display ASIC Products. System Architect for revolutionary in-cell touch / display product line for high resolution mobile, tablet and notebook LCD display modules which allow simultaneous touch and display operation – impossible with all previous architectures from all suppliers. Focused on design and specification of module-level power management integrated circuit (PMIC) device and power management approaches.

***Independent Consultant*, GPS Engineering Consulting, LLC, 2006-Present (re-activated Nov. 2014-Apr. 2015)**

In-Cell Touch / Display ASIC Products. Develop novel in-cell architecture approaches for Atmel Corporation to enter the in-cell touch / display ASIC market. Work with geographically diverse team and develop specifications and system-level analysis tools to facilitate the creation of new in-cell products which meet the needs of LCM customers.

***Embedded System Architecture Manager*, Synaptics Inc., 2011-2014**

Touch / Display Driver IC (TDDI) ASIC Products. Technical Lead / System Architect for world's first combination touch / display driver ASIC products (TD4260, TD4291 and TD4191). Responsible for system-level customer requirements analysis, system architectural design and partitioning, advanced algorithm analysis, development and prototyping, analysis techniques and tool development, resource allocation and initial customer engagement adaptations, customizations and support.

***Independent Consultant*, GPS Engineering Consulting, LLC, 2006-Present (active through 2011)**

Embedded Fuel Cell Data Acquisition Electronic Device. Architected and managed the development of embedded firmware which acquired individual fuel cell performance characteristics and energy consumption data used to provide load balancing and lifetime management of overall fuel cell array.

Embedded Linux-Based Medical Imaging Electronics Device. Lead the design and develop embedded uClinux system infrastructure for advanced wireless medical imaging device. Provide support and assistance for board bring-up and development including VHDL-based CPLD subsystem. Provide performance analysis and optimization of embedded Linux

device drivers to meet project and system timing requirements. Ported Linux device drivers from x86 CPU to embedded platform (Analog Devices Blackfin processor). Provide estimates, project planning and business analysis.

Hand-Held Medical Equipment Design. Provide overall project consulting regarding cost and manufacturability of medical treatment product. Responsible for the board level digital hardware design, 250k FPGA design (entirely designed and implemented in VHDL), embedded real-time control software (designed and implemented in C) and Man-Machine Interface (MMI) design (designed and implemented using the EasyGui development environment). Provide on-going technical consulting regarding product enhancements.

Miniature Embedded Audio Electronic Device. Designed embedded software for miniature embedded audio device using Atmel AVR microcontroller with microphone, SD-Card (FAT file system) and custom sensor interfaces. Provided analysis, design review and recommendations for hardware architecture.

USB-Based Consumer Electronics Device. Provided software (MS Windows XP and Windows Vista) USB device driver support. Provided real-time embedded firmware design, development and support for very high volume consumer electronics device. Provided analysis and design for manufacturing cost reduction. Provided analysis and support for follow-on product planning.

Advanced Consumer Electronics DSL Modem. Designed hardware and embedded diagnostic firmware for an advanced, remote-powered DSL modem. Responsible for overall project lead including management and estimation. Responsible for working with customer to establish and evolve system requirements for second generation product.

Adjunct Faculty, Rochester Institute of Technology, Department of Software Engineering, 2011

Principles of Concurrent Software Systems. Undergraduate course in modeling, designing and implementing concurrent systems using a modeling language / infrastructure to develop and understand concurrent execution behavior and Java / C++ to develop and test program implementations.

Senior Engineer, Carestream Health, 2009-2011

Embedded Linux-Based Medical Imaging Electronics Device. Technical lead for DRX1 Digital Imaging detector design and architecture. Responsible for project planning, architectural design, resource allocation and follow-on product embedded software design and development.

Assistant Professor, Rochester Institute of Technology, Department of Computer Engineering, 2003-2006

Real-Time Operating System Design. Graduate course in the design of a real-time operating system (RTOS) kernel. This course covers all aspects of RTOS design including system initialization of peripheral devices, data structure design for process management, inter-process communication primitive design and implementation and scheduling algorithm fundamentals.

High Performance Architectures. Graduate course taught in a seminar format, centered on continuous, active participation of students in analyzing and understanding the design of modern high-performance computer architectures.

Computer Organization. Undergraduate course in the information transfer and transformations that occur in a computer, with emphasis on the relations between computer architecture and organization. Topics include design levels and their respective primitives, modules and descriptive media, register transfer and micro-operations, basic computer organization and design, central processor organization, control unit and microprogramming, memory organization, and input-output organization.

Applied Programming. Undergraduate course in numerical algorithm design and implementation in the C language. A primary focus of the course is programming in memory and / or computing power constrained environments, i.e., embedded systems. Topics include root finding, solutions to systems of simultaneous equations, floating-point arithmetic algorithms and fixed-point arithmetic properties and characteristics.

Assembly Language Programming. Undergraduate course in 68000 assembly language. The course covered general programming techniques (instruction classes and usage) as well as interrupt driven input/output programming concepts and device driver design. The focus is on the basic programming techniques needed for embedded and real-time assembly language programming.

MS Thesis Advising. Adviser for Master of Science in Computer Engineering thesis. Responsible for defining research problem scope appropriate for MS student, managing the activities and schedule of the thesis and editing and directing the creation of the MS thesis document.

David R. Cox. Distributed SystemC Simulation. Master's thesis, Rochester Institute of Technology, Department of Computer Engineering, August 2005. Advisers: Dr. Greg Semeraro, Dr. Roy Czernikowski and Dr. Muhammad Shaaban.

Scott C. Warner. Linux OS Emulator and an Application Loader for a High Performance Microarchitecture Simulator. Master's thesis, Rochester Institute of Technology, Department of Computer Engineering, May 2005. Advisers: Dr. Greg Semeraro, Dr. Roy Czernikowski and Dr. Juan Cockburn.

Harry J. Eisenbise. RITSim: Cache Modeling and Simulation. Master's thesis, Rochester Institute of Technology, Department of Computer Engineering, April 2005. Advisers: Dr. Greg Semeraro, Dr. Muhammad Shaaban and Dr. Marcin Lukowiak.

David L. Morse. Feasibility Analysis of Correlation Based Prefetching Using Digital Signal Processing. Master's thesis, Rochester Institute of Technology, Department of Computer Engineering, August 2004. Advisers: Dr. Greg Semeraro, Dr. Juan Cockburn and Dr. Muhammad Shaaban.

James D. Remus. Statistical Closed-Loop Process Scheduling. Master's thesis, Rochester Institute of Technology, Department of Computer Engineering, August 2004. Advisers: Dr. Greg Semeraro, Dr. Roy Czernikowski and Dr. Juan Cockburn.

Adjunct Instructor, University of Rochester, Department of Electrical and Computer Engineering, 2000-2003

Introduction to Computers and Programming. Undergraduate course in C/C++ and computer organization. The course covers Unix/Linux programming commencing with basic programming in the C/C++ language and concluding with the introduction of

Object Oriented Programming (OOP) concepts. Solely responsible for the development and presentation of the course and instruction of graduate and undergraduate Teaching Assistants.

***Scientist*, University of Rochester, Department of Electrical and Computer Engineering, 2000- 2003**

Linux System Administrator. Responsible for the installation, configuration and maintenance of Linux computer systems in the Advanced Computer Architecture Laboratory (ACAL). The laboratory was used for microarchitecture research simulation, typically on a 24/7 basis.

***Principal Engineer*, Harris Corporation, RF Communications Division, Radio Products Engineering Department, 1992-2000**

Strategic Exciter Development Software Group Leader. Responsible for the supervision and management of as many as six software engineers. Provided technical leadership and design oversight for the development of this embedded, object-oriented, real-time software (C++). Designed and implemented a complex, real-time, non-linear control system for 10k Watt HF transmitter (Matlab/Simulink and C on a Digital Signal Processor). Responsible for product planning, estimation and tracking of all software development activities.

HF Modem Group Leader. Responsible for the supervision and management of two software engineers and one engineering aide. Provided technical leadership and design leadership for the development of product enhancements in the embedded, real-time software of the HF modem product line (C and 80x86 Assembly Language). Participated in product planning, estimation and tracking of all software and hardware development activities. Designed 80386/EX based video Capture, Compression and Communication ISA Bus card. Designed and implemented low-level hardware test software (80386 protected mode Assembly Language). Designed and implemented embedded, real-time software for the control of a 1000 Watt HF power amplifier (C). Designed 80186 based transmitter control module and MIL-STD-1553 dual redundant, Ethernet-like, interface module. Designed and implemented associated embedded, real-time, low-level hardware control software (i.e., driver) for custom real-time operating system (C and 80x86 Assembly Language).

***Adjunct Faculty*, Rochester Institute of Technology, Department of Computer Engineering, 1997-1999**

Design Automation of Digital Systems. Graduate course concerning all aspects of digital system design automation tools and techniques. The entire design, implementation and manufacturing process flow was discussed with emphasis on the use of the VHDL language for design description and implementation.

Digital System Design for Computer Engineers. Undergraduate course concerning the design of synchronous and asynchronous sequential logic systems. An introduction to language-based design description techniques was included, in addition to discussions concerning all theoretical and practical aspects of sequential circuit design and implementation.

***Computer Architecture Engineer*, PAR Government Systems Corporation (PGSC), 1990-1992**

Designed high-performance computer architectures and consulted on performance and architectural issues related to digital signal processing (DSP) within advanced vision system designs. Designed and implemented concurrent software using VHDL for the design of an IEEE-754 compliant floating point Digital Signal Processor (DSP). Responsible for the design of a combination double precision and dual single precision floating point adder (approximately one-third of 300k gate chip). Informally taught VHDL to engineers responsible for other aspects of the DSP design. Created the syllabus for and taught a college-level Ada programming course to approximately fifteen engineers; covered all aspects of the Ada programming language in approximately six weeks (two-hour lectures, twice per week).

***Adjunct Faculty*, Utica College of Syracuse University, Department of Mathematics and Computer Science, 1991-1992**

Assembly Language Programming. Undergraduate course concerning all aspects of 80x86 Assembly Language programming and the IBM PC/AT (ISA Bus) computer architecture. All aspects of assembly language programming were discussed from low-level hardware access to high-level, structured design techniques. Emphasis was placed on the appropriate use of assembly language within the personal computer architecture context.

***Product Design Engineer*, Bull HN Information Systems Incorporated, Custom & Special Products Division, Hardware Development Group, 1988-1990**

Designed custom hardware and embedded real-time software for mini-computer and ISA Bus peripheral products. Designed mini-computer quad-, streaming-, tape drive controller real-time firmware (68000 Assembly Language). Designed ISA Bus encryption / communication card which provided eight full duplex, 9600 baud secure communication channels using the Data Encryption Standard (DES) algorithm and integrated communication ports. Specialized in ISA Bus design.

***Adjunct Teaching Fellow*, Boston University College of Engineering, Department of Manufacturing Engineering, 1989-1990**

Pascal Programming for Engineers I & II. Off-semester, undergraduate courses which covered all aspects of the Pascal programming language. In addition, data structure design and large scale software development concepts were introduced. Solely responsible for material preparation and presentation as well as course administration.

***Undergraduate Teaching Assistant*, Boston University College of Engineering, Department of Manufacturing Engineering, 1985-1988**

Pascal Programming for Engineers I & II. Undergraduate course which covered all aspects of the Pascal programming language. Prepared and lectured twice weekly two-hour course work review sessions. Lecture material aligned with professor's lecture but was independently developed. Supervised the actions of fifteen other teaching assistants for the course.

Professional Awards and Honors

IEEE Computer Society Technical Committee on Computer Architecture 2022 High-Performance Computer Architecture (HPCA) Test of Time Award

Awarded for most influential work 20+ years after publication for PhD dissertation work published at the 2002 HPCA Conference titled "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling"

Voted “Most Effective Teacher” by Rochester Institute of Technology Computer Engineering Class of 2006

Elected to the grade of Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), January 2006

Nominated for 2005 Richard and Virginia Eisenhart Provost's Award for Excellence in Teaching, December 2005

Ph.D. dissertation work chosen as a "Top Pick for 2003" and published in "Special issue of the most industry relevant and significant papers of the year in computer architecture", IEEE Micro, December 2003

Awarded Outstanding Performance as a Teaching Assistant, Boston University, College of Engineering, May 1988.

Memberships in Professional Societies

Rochester Business Alliance, Member, 2007 – 2009

American Society for Engineering Education (ASEE), Professional Member, 2003 – 2018

Institute of Electrical and Electronics Engineers (IEEE), Senior Member, 1999 – Present

IEEE Computer Society (IEEE-CS), 1999 – Present

IEEE Education Society (IEEE-ES), 2002 – 2018

Order of the Engineer, 1988 – Present

Professional Service as Referee

Invited Panelist

Panelist for National Science Foundation (NSF) Foundations of Computing Processes and Artifacts (CPA). Washington, DC, June 2004. Reviewed 6 proposals (of 17 submissions). The 11 member panel met to rank proposals and provide recommendation(s) for funding to NSF.

Invited Reviewer

Innovations 2006: World Innovations in Engineering Education and Research Journal. International Network for Engineering Education and Research, January 2006. iNEER.

Microcontrollers: Motorola MC68HC12. Freescale, Inc., November 2005. Book chapter reviewer.

Steven C. Chapra. Numerical Methods, 5th ed. McGraw Hill, February 2005. Book chapter reviewer.

Special Issue on Network Processors for Future High-Performance Systems and Applications. In IEEE Micro, June 2004.

Genetic and Evolutionary Computation Conference. Real-World Applications Subcommittee, Orlando, Florida, July 1999. GECCO-99. Program Review Committee Member.

Guest Reviewer (invited by program committee member to review on his/her behalf)

International Symposium on Performance Analysis of Systems and Software. Austin, Texas, October 2005. ISPASS-2005.

International Conference on Computer Design. San Jose, CA, May 2005. ICCD-2005.

Workshop on Complexity Effective Design, in conjunction with the 29th International Symposium on Computer Architecture. Munich, Germany, May 2004. WCED-2004.

The 30th Annual International Symposium on Computer Architecture. January 2003. ISCA-2003.

Transactions on Very Large Scale Integration Systems. IEEE, August 2002.

Workshop on Complexity Effective Design, in conjunction with the 29th International Symposium on Computer Architecture. Anchorage, Alaska, May 2002. WCED-2002.

John Hennessy and David Patterson. Computer Architecture: A Quantitative Approach, 3rd Edition. Morgan Kaufmann, June 2001. Book chapter analyzer and researcher.

International Symposium on Performance Analysis of Systems and Software. Tucson, Arizona, November 2001. ISPASS-2001.

Workshop on Complexity Effective Design, in conjunction with the 28th International Symposium on Computer Architecture. Goteborg, Sweden, June 2001. WCED-2001.

International Workshop on Power-Aware Computer Systems. Cambridge, MA, September 2000. PACS-2000.

Workshop on Complexity Effective Design, in conjunction with the 27th International Symposium on Computer Architecture. Vancouver, British Columbia, June 2000. WCED-2000.

Publications

James Remus and Greg Semeraro. Statistical Closed-Loop Process Scheduling. In *Proceedings of the 1st Workshop on Operating System and Architectural Support for the on-demand IT Infrastructure*, Boston, MA, October 2004. OASIS.

Greg Semeraro, David H. Albonesi, Grigorios Magklis, Michael L. Scott, Steven Dropsho, and Sandyha Dwarkadas. Hiding Synchronization Delays in a GALS Processor Microarchitecture. In *Proceedings of the 10th IEEE International Symposium on Asynchronous Circuits and Systems*, Hersonissos, Crete, Greece, April 2004. ASYNC-2004.

Greg Semeraro, David Albonesi, Steven Dropsho, Grigorios Magklis, and Michael L. Scott. Improving Application Performance by Dynamically Balancing Speed and Complexity in a GALS Microprocessor. In *Proceedings of the 2nd Workshop on Application Specific Processors*, San Diego, CA, December 2003. WASP-2.

David H. Albonesi, Rajeev Balasubramonian, Steven G. Dropsho, Sandyha Dwarkadas, Eby G. Friedman, Michael C. Huang, Volkan Kursun, Grigorios Magklis, Michael L. Scott, Greg Semeraro, Padip Bose, Alper Buyuktosunoglu, Peter W. Cook, and Stanley E. Shuster. Dynamically Tuning Processor Resources with Adaptive Processing. *IEEE Computer (Special Issue on Power-Aware Computing),* 36(12):49-58, December 2003.

Grigorios Magklis, Greg Semeraro, David H. Albonesi, Steven G. Dropsho, Sandhya Dwarkadas, and Michael L. Scott. Dynamic Voltage and Frequency Scaling for a Multiple Clock Domain Microprocessor. *IEEE Micro (Microarchitecture "Top Picks" 2003),* 23(6), December 2003.

Greg P. Semeraro. The Future of Literacy for Electrical and Computer Engineers. In *Proceedings of the 2003 ASEE St. Lawrence Section Annual Meeting*, Kingston, Ontario, Canada, October 2003.

Grigorios Magklis, Michael L. Scott, Greg Semeraro, David H. Albonesi, and Steven G. Dropsho. Profile-based Dynamic Voltage and Frequency Scaling for a Multiple Clock Domain Microprocessor. In *The Proceedings of the 30th International Symposium on Computer Architecture*, San Diego, California, June 2003. ISCA 2003.

Greg Semeraro, David H. Albonesi, Steven G. Dropsho, Grigorios Magklis, Sandhya Dwarkadas, and Michael L. Scott. Dynamic Frequency and Voltage Control for a Multiple Clock Domain Microarchitecture. In *The Proceedings of the 35th Annual Symposium on Microarchitecture*, Istanbul, Turkey, November 2002. IEEE/ACM. MICRO-35.

Steven Dropsho, Alper Buyuktosunoglu, Rajeev Balasubramonian, David H. Albonesi, Sandhya Dwarkadas, Greg Semeraro, Grigorios Magklis, and Michael L. Scott. Integrating Adaptive On-Chip Storage Structures for Reduced Dynamic Power. In *Proceedings of the Eleventh International Conference on Parallel Architectures and Compilation Techniques*, Charlottesville, Virginia, September 2002. PACT-2002.

Greg Semeraro, Grigorios Magklis, Rajeev Balasubramonian, David H. Albonesi, Sandhya Dwarkadas, and Michael L. Scott. Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling. In *The Proceedings of the Eighth International Symposium on High-Performance Computer Architecture*, Boston, Massachusetts, February 2002. HPCA-8.

Greg P. Semeraro and David C. Vallese. Non-Linear Control of a High Power Transmitter. In *The Proceedings of the Eleventh Annual International Conference on Signal Processing Applications and Technology*, Dallas, Texas, October 2000. ICSPAT-2000.

Greg P. Semeraro. Evolutionary Analysis Tools for Real-Time Systems. In *Proceedings of the Sixth International Symposium of Modeling, Analysis and Simulation of Computer and Telecommunication Systems, Tools-Track (Addendum)*, Montreal, Canada, July 1998. MASCOTS-98.

Greg P. Semeraro. Evolutionary Approach to Real-Time Analysis. In *Proceedings of the Third Annual Conference of Genetic Programming, Symposium on Genetic Algorithms*, pg. 133, Madison, Wisconsin, July 1998. GP-98.

Patents

Multiple Clock Domain Microprocessor. David Albonesi, Greg Semeraro, Grigorios Magklis, Michael L. Scott, Rajeev Balasubramonian and Sandhya Dwarkadas. Filed January 2004, Issued August 2006. U.S. Patent Nos. 7,089,443 & 7,739,537.

Matrix Sensor for Image Touch Sensing. Petr Shepelev, Christopher A. Ludden, Jeffrey Lukanc, Stephen L. Morein, Greg P. Semeraro and Joseph Kurth Reynolds. Filed January 2014, Issued March 2015. U.S. Patent No. 8,970,537.

Capacitive Sensing Using a Matrix Electrode Pattern. Jeffrey Lukanc, Stephen L. Morein, Christopher A. Ludden, Greg P. Semeraro, Joseph Kurth Reynolds, Petr Shepelev, Thomas Mackin. Filed December 2014, Pending.

End-User Self-Service Biometric Card Failure Analysis. Greg P. Semeraro, Application Pending.