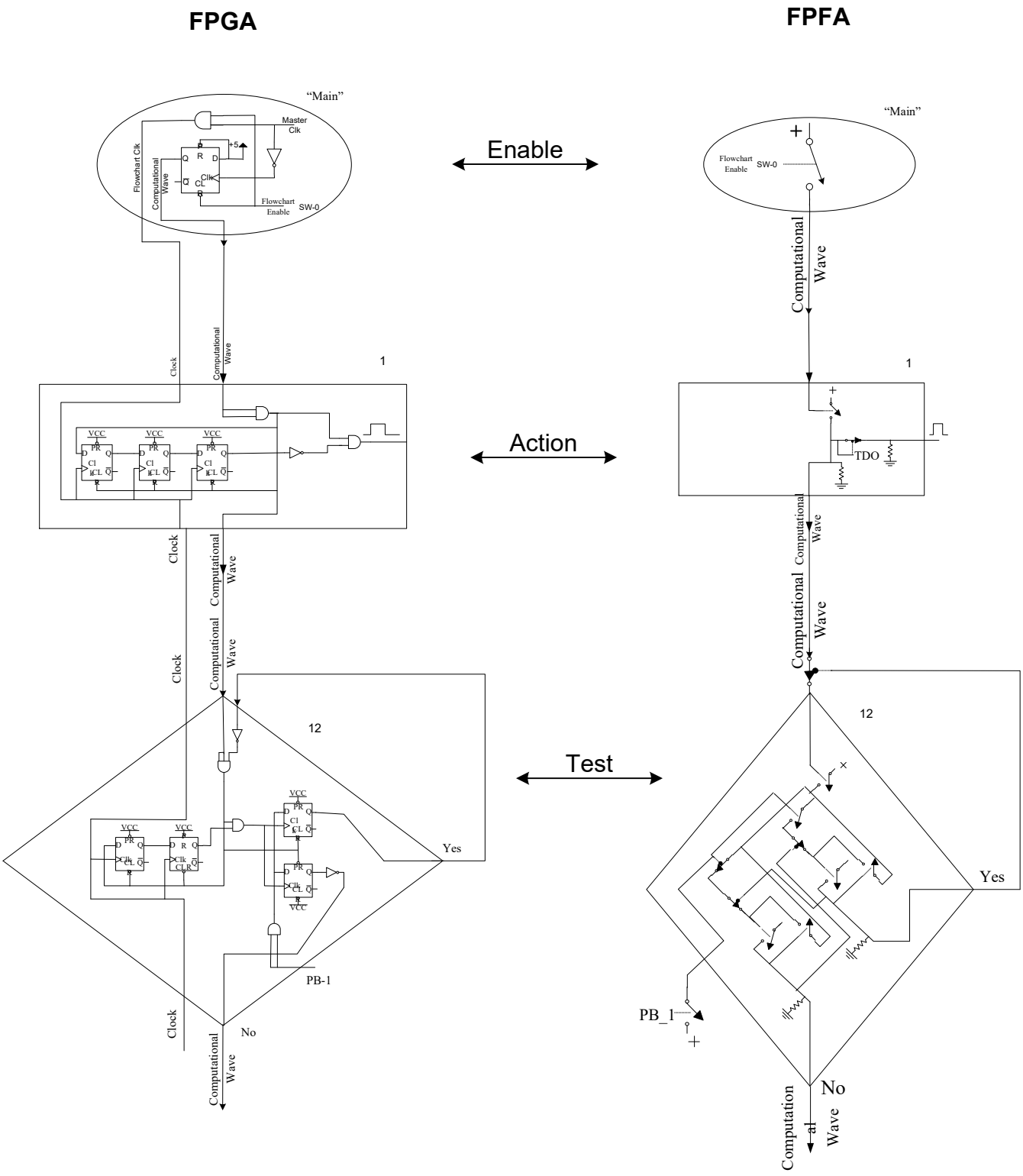
Flowpro Machines as Configurable Hardware

US Patent No. 10,181,003 “Processing Circuits for Parallel Modeling and Execution”

January, 2022



An Overview of Flowpro Computational Machines as Configurable FPGA and FPFA Hardware

Introduction

This overview provides a brief explanation and comparison of the implementation of the new configurable hardware option FPFA (Field Programmable Flowpro Array) versus the current standard for configurable hardware FPGA (Field Programmable Gate Array). As further introduction of the comparison, you will recognize that FPFA logic is configured into AE (Atomic Element) cells while the FPGA references the current terminology of a CLB (Configurable Logic Block) cell.

Conceptually the advantages of an FPFA over an FPGA are primarily power, processing speed, processing density and ease-of-use.

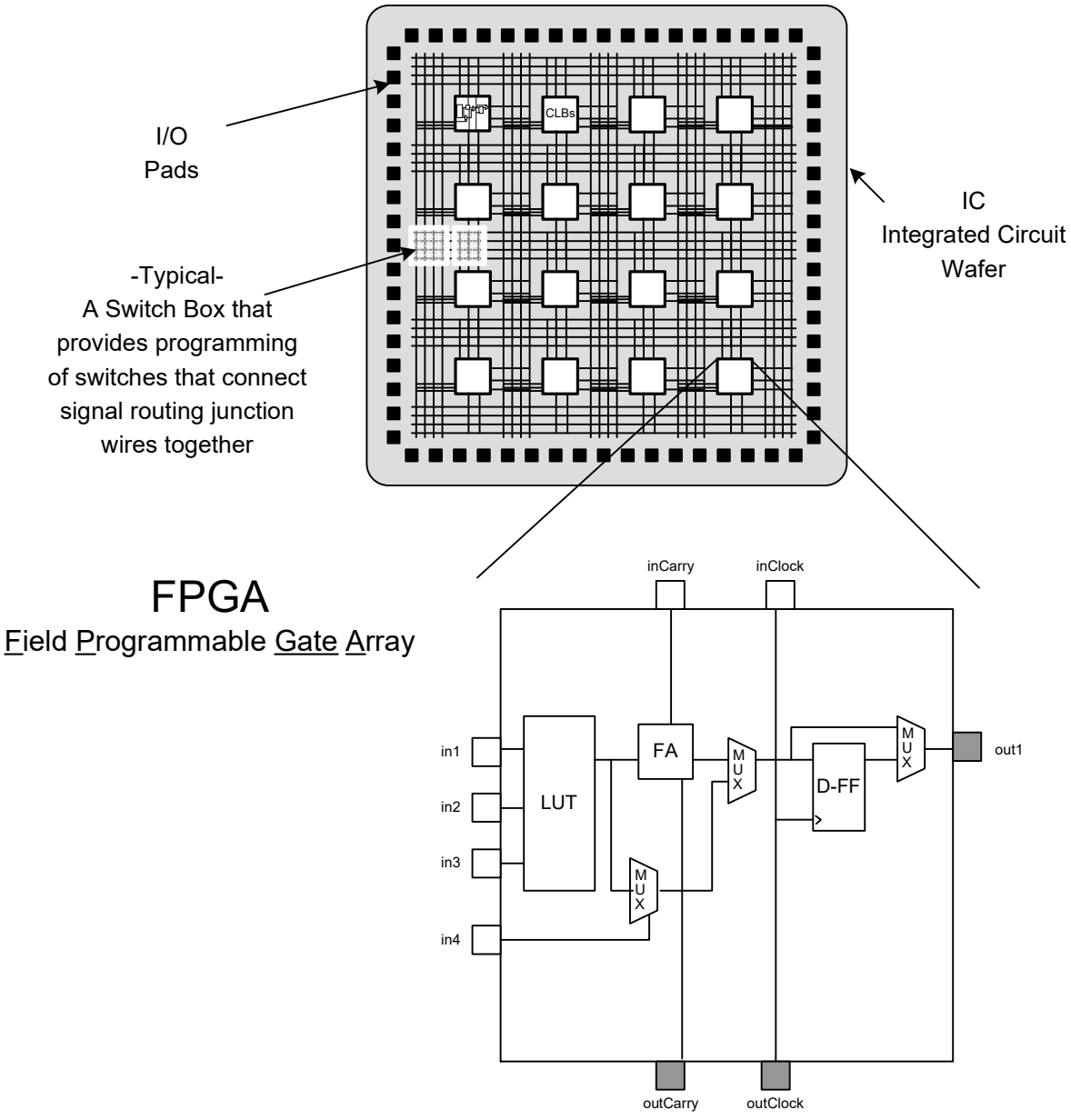
FPFA's power advantage stems from the fact that they are clock-less, implemented with a smaller cell size and that AE cells only need to draw power when they are processing.

Processing density is influenced by Cell size, wiring complexity and also by design input. Wiring between cells is simpler with a FPFA because the flowcharts are small and flowchart elements flow from one to another in their layout. Flowpro Software has shown through numerous applications that a parallel design approach actually uses less logic for equivalent applications. Higher processing density allows FPFAs to take better advantage of Die and Wafer area. This allows FPFAs to compete more closely with an ASIC's (Application Specific Integrated Circuit) power advantage.

Patent 10,181,003 describes in detail the ease-of-use advantages of Flowpro Software flowcharts as a parallel programming language and a parallel processing system. Parallel high level flowcharts are created on a PC describing a process or function and the flowcharts are compiled to a data file. This data file can now be executed on a PC for simulating the application or synthesized to hardware for propagating, i.e. running, as parallel flowcharts on an FPFA or even on a standard FPGA as shown in the patent. Synthesizing the data file to an FPFA may not require a third-party synthesizer because the same basic cell structure is repeated over and over again for any and all applications. The wiring algorithm is the key part of synthesis to an FPFA. Once the flowcharts are in an FPFA, “What You See” on the PC is “What You Get” in the FPFA.

FPFAs and FPGAs do not have to exist in isolation. As shown in patent 10,181,003 a combination of Boolean and other compute structures is simple and straightforward. FPFA flowcharts can control other systems and other systems can control flowcharts. When optimizing for speed there will be situations with advantages to each structure.

Currently the term Configurable Hardware is primarily associated with FPGA integrated circuits. FPGA development systems provide software that allows programming and re-programming of fixed hardware components into complete systems. In effect, rewiring together the same standard hardware circuits to produce a new function. This can be done over and over again, producing a new function each time. These standard circuits are laid out in a grid pattern and each Cell, sometimes called a Tile, is identical and is called a CLB (Configurable Logic Block, See figure 1). It is the programming of switches that will connect wires between CLBs that make an FPGA configurable hardware. The CLBs are fixed but the wires between them are configurable, hence, configurable hardware. By using the FPGA vendor software an FPGA user's software application is automatically synthesized, i.e. converted, to CLBs with proper wiring between them. The synthesized program is downloaded to the FPGA which configures the hardware within it.



CLB - Configurable Logic Block Tile (Cell)

Figure 1

A Flowpro Machine is a 'decision flowchart' or multiple 'decision flowcharts' that conform to specific rules of construction and execution when implemented in an integrated circuit, chemical or biological substrate. Flowpro Machines as configurable hardware was introduced with US patent 10,181,003, January 2019. A Flowpro Machine with configurable standard hardware circuits and programmable wiring is called an FPFA (Field Programmable Flowpro Array) or sometimes called a Field Programmable Flowchart Array. In an FPFA integrated circuit (see figure 2) the CLB cells are replaced with AE (Atomic Element) cells but the FPFA is also configured with programmable wiring. An FPFA development system provides programming, reprogramming and monitoring of the FPFA.

AE verse CLB

Referring to figure 1 and figure 2, AE cells are smaller physically than CLBs and require less area on the integrated circuit. The actual design of the CLB varies from manufacturer to manufacturer, some more complicated than others, and most are larger than an AE. There are a number of reasons for this but mainly because CLBs are clock driven and AEs are clock-less, also referred to as asynchronous. This is a major advantage of FPFAs over FPGAs, because it simplifies the design of configurable chips by not having to route a clock signal to every cell. Another advantage is that AEs are true parallel structures and although CLBs can be made pseudo-parallel they are almost always tied to a clock signal. Another advantage of an AE over a CLB is that AEs allow for multiple independent functions per cell and CLBs traditionally do not. FPFA's full development cycle has many advantages over FPGAs as is detailed in US patent 10,181,003.

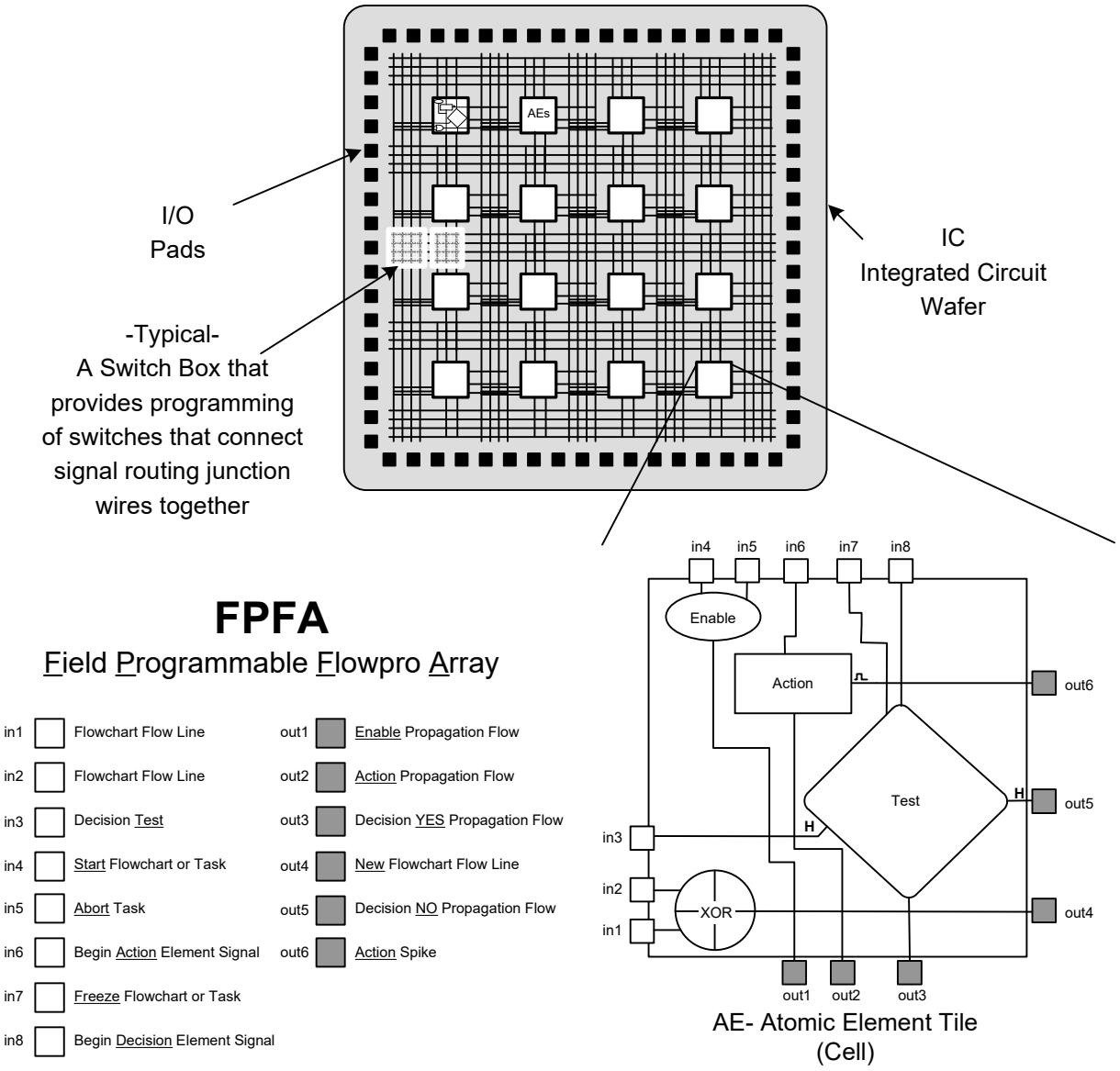


Figure 2

AE details

The programming of an FPFA consists of creating truly parallel Flowpro Machine flowcharts and synthesizing those flowcharts into AEs with the wiring configured. As the patent states, any computation (a program) can be realized by only using the 4 flowchart elements, Enable, Action, Test and Task structures. Referring to figure 3, The Enable oval (in4) is used to begin (enable) a flowchart or task operation and the Abort (in5) is used to turn off the enable. If power is removed from the Enable line all flowchart elements within that flowchart or Task will become disabled and not run. This is a major advantage of AEs because they do not need to draw power when they are not running.

The flowchart Freeze input (in7) connected to Decision elements is used to pause a flowchart or Task Object operation at the executing Decision element. When the Freeze signal is active, all Decision elements hold their status until the Freeze signal is not active. Flowcharts and tasks will begin operation from the paused Decision element.

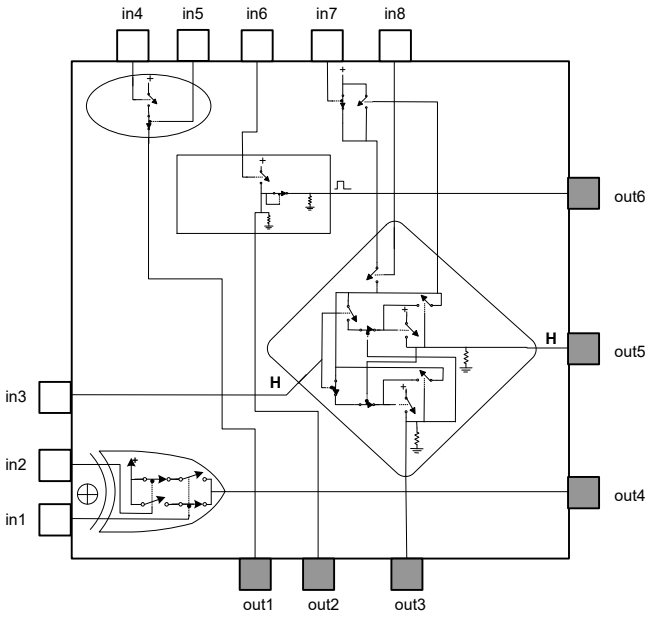
Propagation flows out of the Enable and into the first block of the flowchart or Task. The Action element generates a spike signal and passes the propagation flow to the next block. Action spikes are used to turn on (T.ON) and turn off (T.OFF) outputs, internal bit variables, counters, timers etc. The Decision element latches propagation flow through the YES or NO path which are in turn connected to other elements. The circuits within these elements are taken directly from the patent and represent 'ideal' switches and circuit structures and not implemented circuits.

The exclusive-or element of an AE cell is used to control propagation flow to an element that has multiple flow lines connected to it. The basic tenet of a Flowpro Machine is that the transition of OFF to ON as the propagation flow signal enters an element causes that element to perform its function and pass the propagation flow to the next element. The exclusive-or of flowlines to an element that already has propagation flow through it will reset (ON to OFF transition) the propagation flow. This will initiate another scan of propagation flow through elements as the propagation flow transitions from OFF to ON again.

FPFA

Field Programmable Flowpro Array

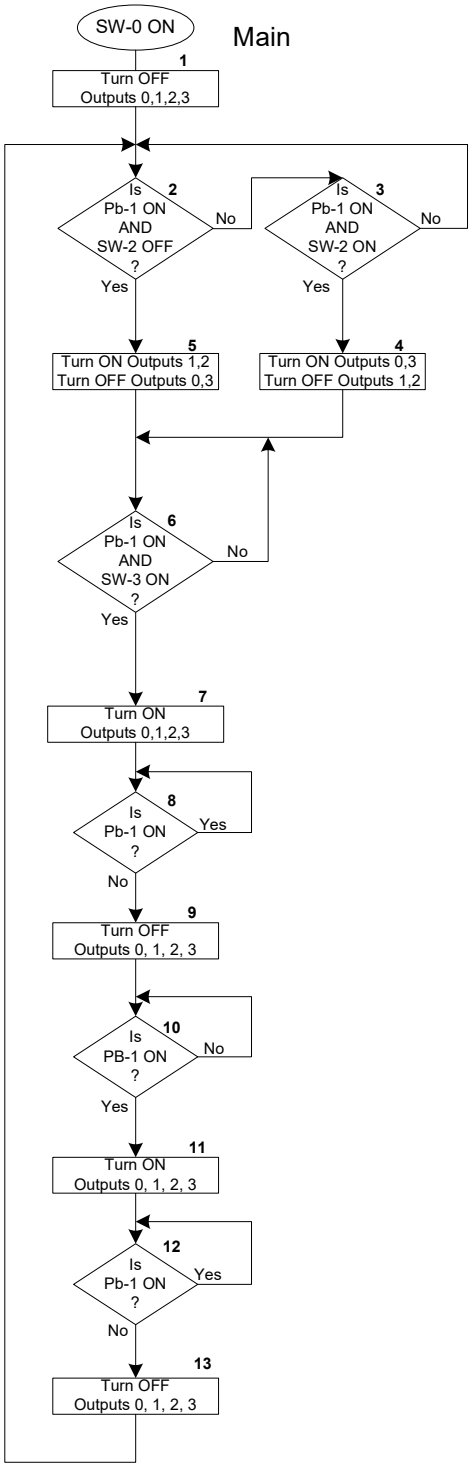
in1	Flowchart Flow Line	out1	Enable Propagation Flow
in2	Flowchart Flow Line	out2	Action Propagation Flow
in3	Decision Test	out3	Decision YES Propagation Flow
in4	Start Flowchart or Task	out4	New Flowchart Flow Line
in5	Abort Task	out5	Decision NO Propagation Flow
in6	Begin Action Element	out6	Action Spike
in7	Freeze Flowchart or Task		
in8	Begin Decision Element		



AE- Atomic Element Tile (Cell)

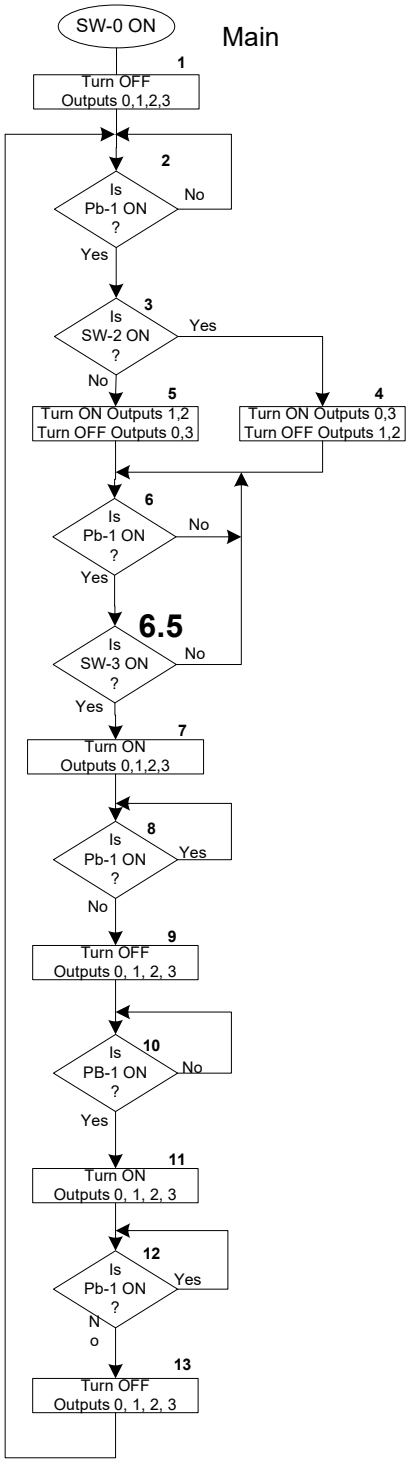
Figure 3

Please refer to the two flowcharts of figure 4. The flowchart on the left (4A) with Boolean expressions used in elements 2, 3 and 6 are converted to event flow before entering the flowchart into the development system. As outlined in the patent, Boolean expressions and State Logic are not required by a Flowpro Machine to solve any computation. Although, combining Boolean gate structures with Flowpro Machines may have potential advantages by using fewer transistors than event flow. The flowchart 4B can now be synthesized directly into an FPFA.



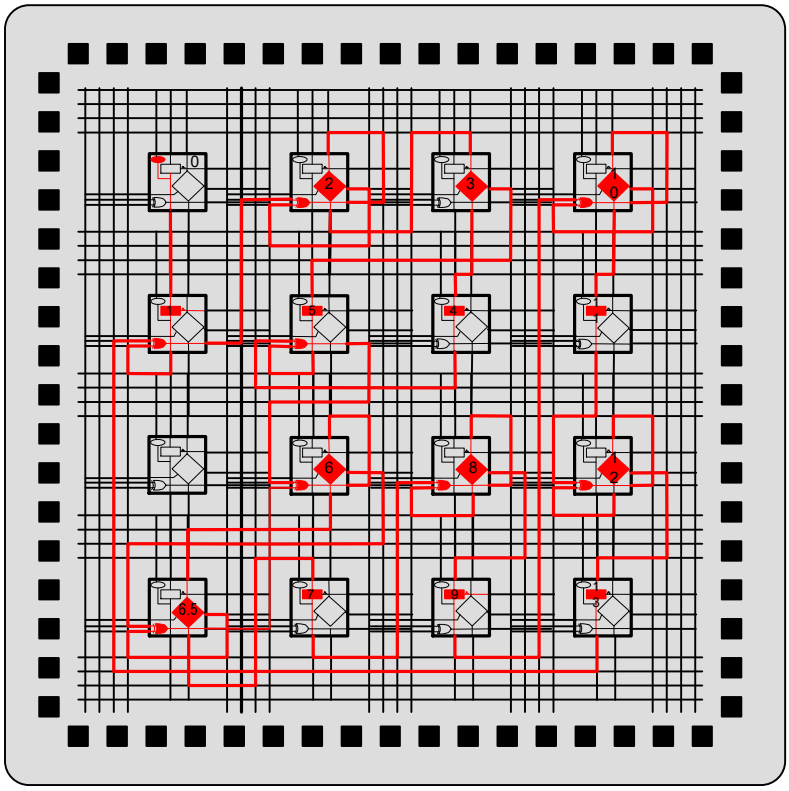
(A)

Figure 4

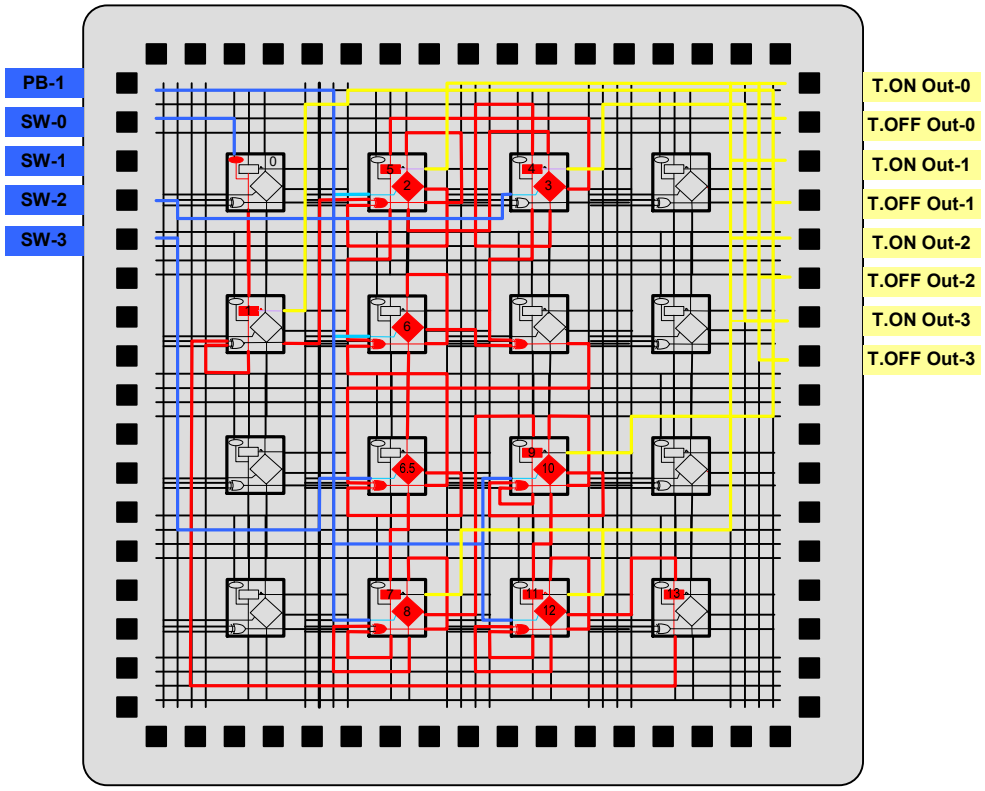


(B)

Referring to figures 4 and 5 shows that the synthesis of the flowchart MAIN into an FPFA is almost a 1 to 1 process and probably does not require the use of Verilog or third-party synthesizers. The keys to implementing this technology are the parallel asynchronous (clock-less) flowcharts and a sophisticated wiring algorithm. The top wafer is an example of the synthesis of 'Main' that only uses one element per tile to emphasize the 1 to 1 synthesis of a Flowpro Machine. The bottom wafer example synthesis takes advantage of using more than one element per tile (Packing) with I/O wiring added.



Wafer
Without Packing
Elements
15 Cells



Wafer
With Packed
Elements
11 cells

Figure 5

Figure 6 is an example of functionally specifying the same operation as figure 4 but by using two parallel asynchronous flowcharts to perform the function. In this example the original flowchart (6A) is encapsulated into a Flowpro Machine Task Object and renamed “Output Control” (6B). Figure 6C shows the Task Object after selecting the object. Figure 6D is the new “Main” flowchart that controls the operation of the “Output Control” Task Object. Notice that there is a Start Task Enable and a Done Task Object. The Done Task allows testing of the Task Object to determine if it has completed its operation or not. A Task begins operation when the propagation flow signal enters the Enable (Start) element. A task will run continuously or until the propagation flow is removed from the Start element by using the Abort Task flowchart control element. The Flowpro Machine elements that have a 3-D quality represent that there is more code within them. In a development environment selecting a 3-D element navigates to the next level flowchart which in turn can call more and more parallel or synchronous levels of task control. Parallelism is a computational quality of its own.

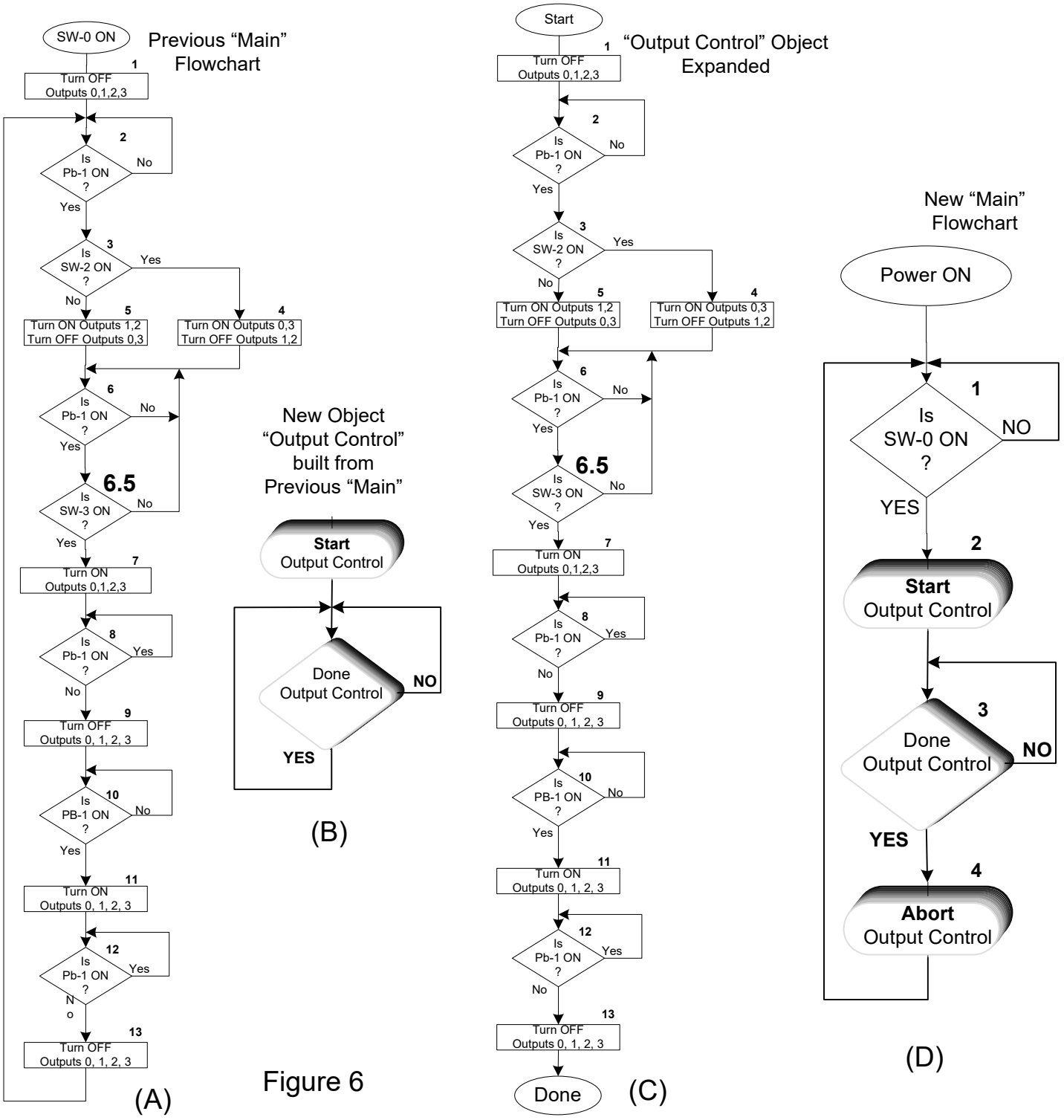


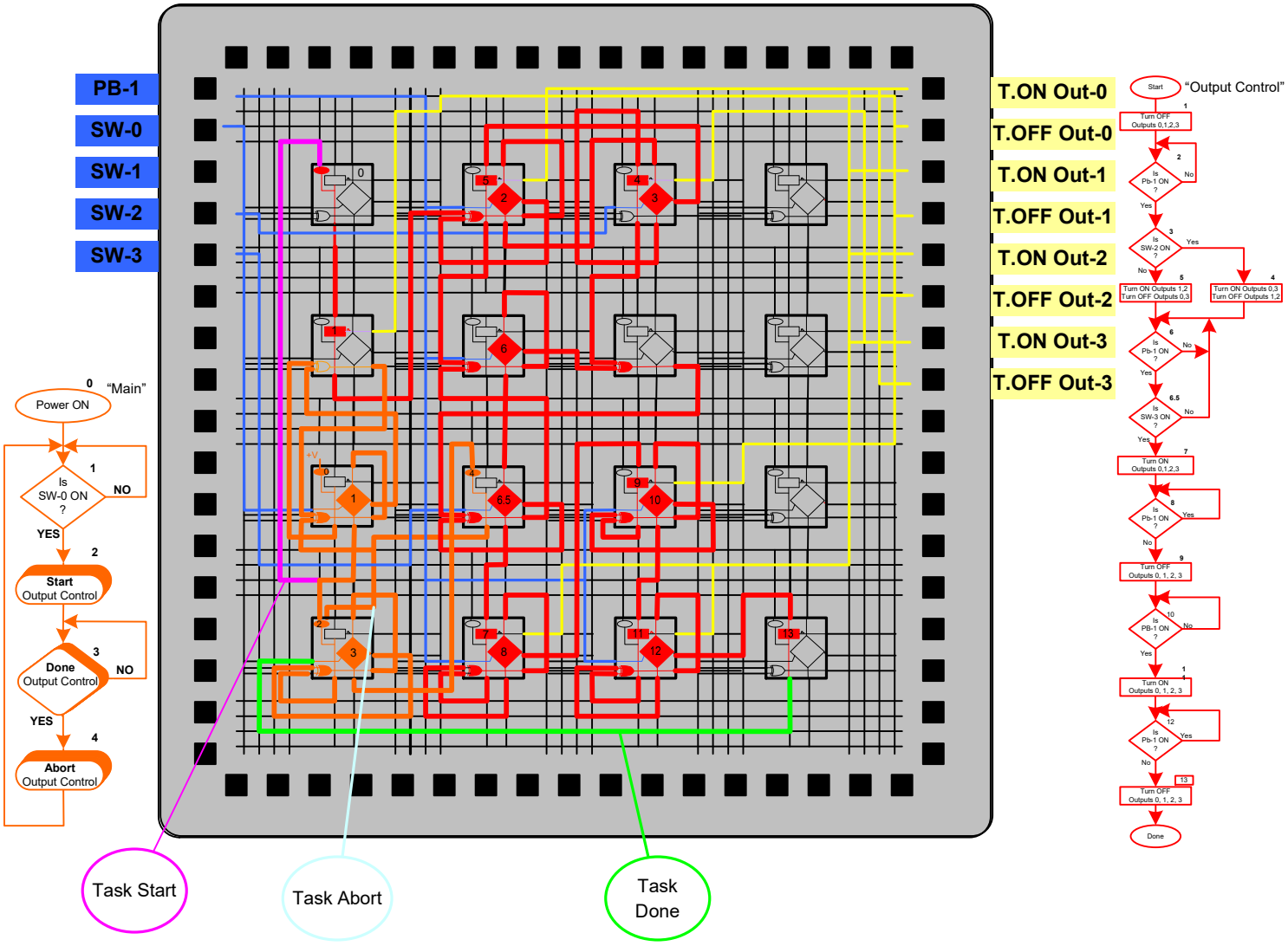
Figure 6

Synthesis Layout Description

Figure 7 shows the synthesis layout with flowchart 'Main' using orange lines and flowchart “Output Control” using redlines. Zooming into figure 7 and referencing the flowcharts while following the connection wires between cells, shows that the synthesis is a straight-forward process for all encapsulated Flowpro Machine Objects and the running of those objects in an FPFA.

Monitoring Running Flowpro Machines

Monitoring and troubleshooting executing flowcharts is a well-defined mature process supported by multiple manufacturers and is especially true for Flowpro Machines. A key point in troubleshooting Flowpro Machines is knowing where each flowchart is executing and the status of variables. As the flowcharts are entered into a PC monitor points are allocated to flowchart decision element flowlines. Using a technique similar to programmable wiring, monitor points can be configured during the synthesis process. Programmable monitor Cells (Tiles) could be strategically placed throughout an FPFA to transmit monitor point status back the PC.



Example of two parallel Flowpro Machines connected within an FPFA and with Flowpro Machine "Main" (orange) calling and terminating Flowpro Machine "Outputs Control" (red).

Figure 7