Making Intelligent Material Decisions

Wednesday Nov 9th, 2022

PCB Carolina 2022

INSULECTRO

PCEA Printed Circuit Engineering Association

PCE-EDU, Inc. Printed Circuits Engineering Education

Mike Creeden CID+ Background

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- Insulectro – Technical Director Design Education
- PCEA - Printed Circuit Engineering Association - Vice Chair
- PCE-EDU, Inc. - Certified Curriculum Author & Instructor
- IPC-CID+ Curriculum - Primary Contributor & Instructor
- Chairman IPC-2221/2222 Standards Committee
- Founder of San Diego PCB, Design, LLC
- PCB Designer 45 Years - "*I Love PCB Design*"

Today's Circuit Engineer Must Meet 3 Competing Perspectives for Success

Design For:

- DF*Solvability*
- DF*Performance*
- DF*Manufactuability*

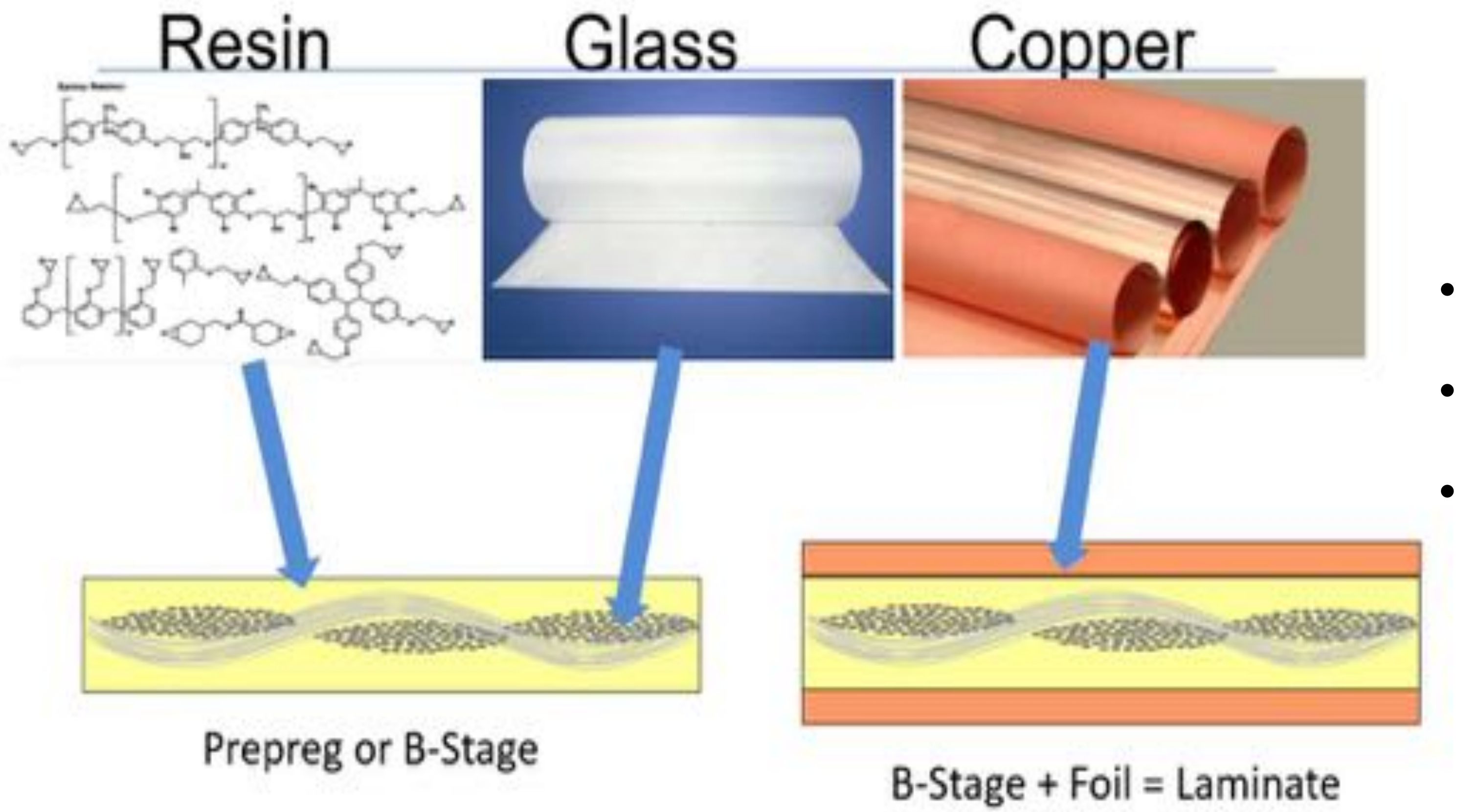
Skill set to solve the placement and route of our circuit.
Often with complex (HDI) High Density Interconnect and master this on your CAD Tool

Signal Integrity/EMC
Power Delivery
Thermal

DFX (DFM) all considerations producing high yield and lower cost

THE RESULT Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing

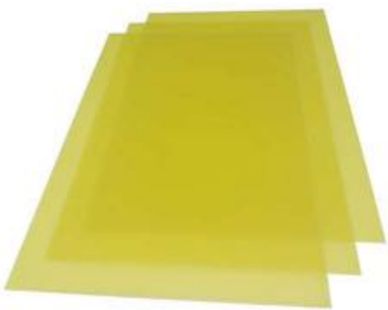
PCB Rigid Laminates - Composites



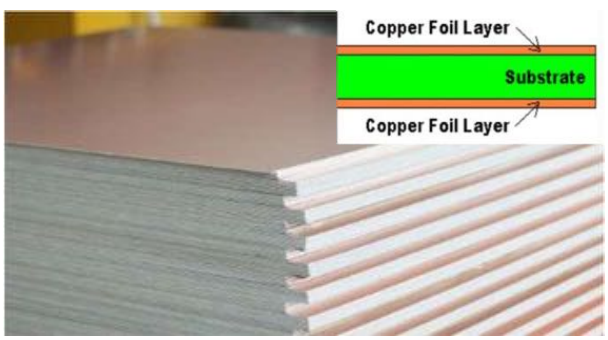
- Resin – Bonding
- Glass – Rigidity
- Copper - Conductivity

Each component plays a role in providing the right properties for the design.

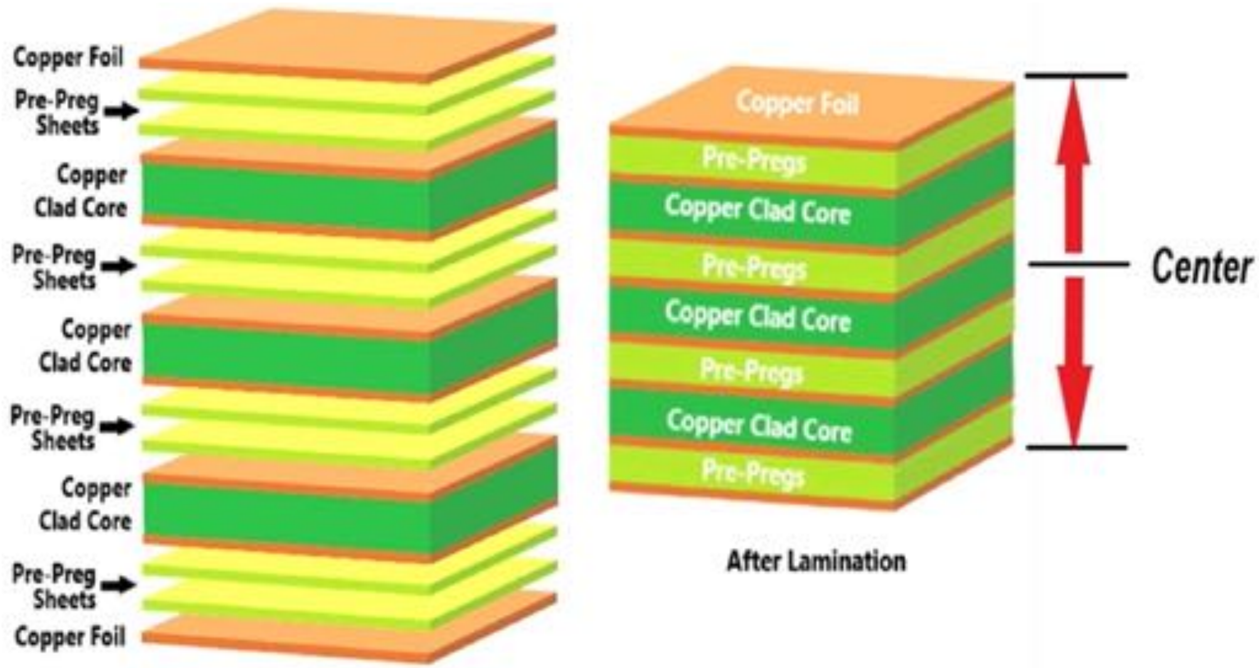
Epoxy Materials Construction



Prepreg “B-Stage”



Copper Clad Core “C-Stage”



Bare Board 8-Layer Alternating Construction - Center Outward, Balanced on Both Sides

Material Standard Panel Sheet

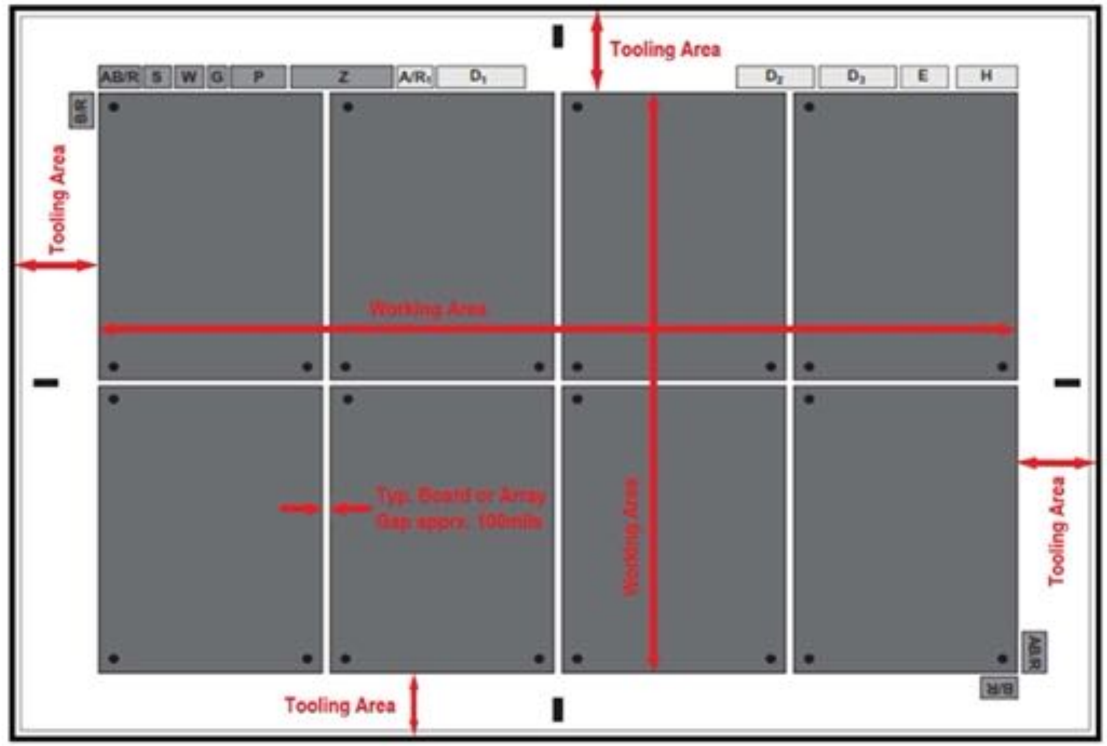
PCB Carolina 2022

Both the Prepreg and Core are sold in **standard sheet sizes** and cut into working panel sizes, **18” x 24” is called the full panel size**

Half panel is 12” x 18” which helps for smaller volume runs, less waste

Prepreg and **Core** come in **many varieties and thicknesses**

Tooling area around **outer edges**, **working area** for **boards or array** of boards **separated by a gap** between



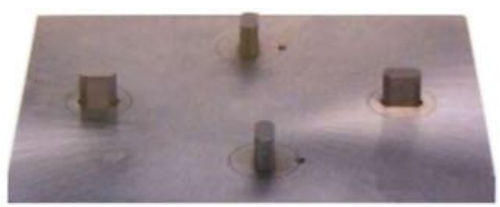
18” x 24” Fabrication Panel Sheet, Working Area and Tooling Area

Lamination Press

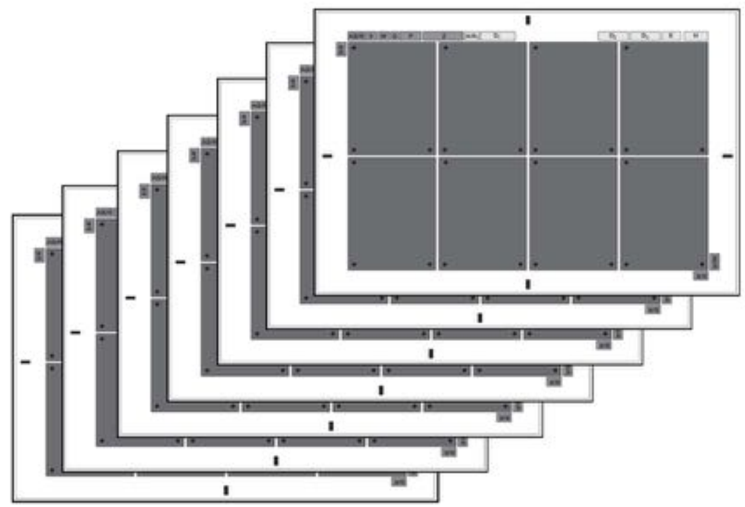
Sheets layered and stacked together, one layer at a time, with a **pin-align system to aid in the layer-to-layer registration**.

Special handling is utilized for the process. The **lamination press heats and compresses the stack of materials together** with a measured time cycle to cure the material and thus bond them together.

Lamination Press



Lamination Base Plate with Pin Alignment

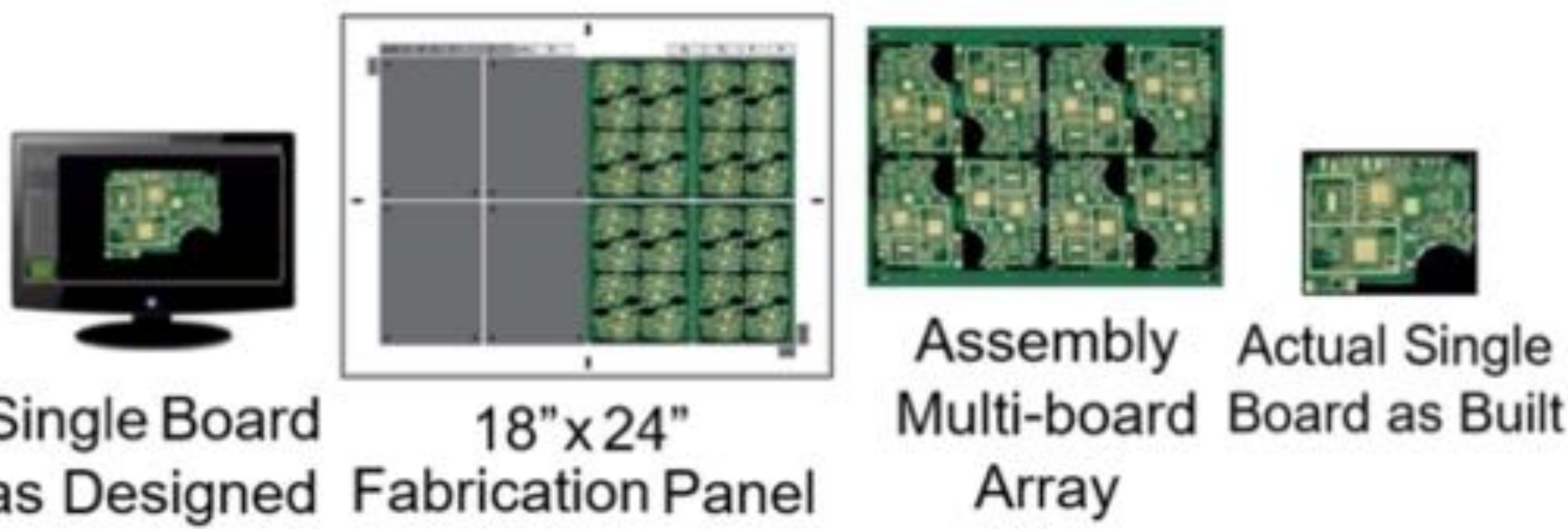


Sheets layered and stacked

Bare Board Construction Basics

Sheets layered and stacked together, one layer at a time,
with a pin-align system to aid in the layer-to-layer registration.

Tooling area around the edges for coupons and other manufacturing aids, leaving a remaining working area. **This is where panel utilization is achieved**. Multiple images, either single boards or many boards on an assemble array, are located with separation of about 100mils.



IPC-4101/126 Specification Sheet

Physical Parameters –

- **(Tg) Glass Transition** – Where **resin turns from a semi-solid state to a rubbery viscous state,** important factor with high layer count boards, observed at lower end of the thermal lamination cycle
- **(Td) Decomposition Temperature** – Where **material breaks down from excess heat,** important factor multiple laminations & thermal excursions, observed at higher end of all thermal excursions such as lamination, solder, product environment and usage

SPECIFICATION SHEET

SPECIFICATION SHEET #:	IPC-4101/126	
REINFORCEMENT:	*1:* Woven E-glass	*2:* N/A
RESIN SYSTEM:	***Primary:*** Epoxy	
	Secondary 1: Multifunctional epoxy	***Secondary 2:*** Modified Epoxy or Non-Epoxy (max. wt. 5%)
FLAME RETARDANT MECHANISM:	RoHS Compliant Bromine	***Minimum UL94 Requirement:*** V-0
FILLERS (>5%):	Contains inorganic fillers	
ID REFERENCE:	***UL/ANSI:*** FR-4/126	
GLASS TRANSITION (T_g):	170 °C minimum	
UL MAX. OPERATING TEMP:	130 °C	

LAMINATE REQUIREMENTS

Laminate Requirement	Specification <0.50 mm [0.0197 in]	Specification ≥0.50 mm [0.0197 in]	Units	Test Method	Ref. Para.
1. Peel Strength, minimum A. Low profile copper foil and very low profile copper foil – all copper weights >17 µm [0.669 mil]. B. Standard profile copper foil 1. After thermal stress 2. At 125 °C [257 °F] 3. After process solutions C. All other foil – composite	0.70 [4.00] 0.80 [4.57] 0.70 [4.00] 0.55 [3.14] AABUS	0.70 [4.00] 1.05 [6.00] 0.70 [4.00] 0.80 [4.57] AABUS	N/mm [lb/in]	2.4.8 2.4.8.2 2.4.8.3	3.9.1.1 3.9.1.1.1 3.9.1.1.2 3.9.1.1.3
2. Volume Resistivity, minimum A. C-96/35/90 B. After moisture resistance C. At elevated temperature E-24/125	10^6 – 10^3	– 10^4 10^3	MΩ-cm	2.5.17.1	3.11.1.3
3. Surface Resistivity, minimum A. C-96/35/90 B. After moisture resistance C. At elevated temperature E-24/125	10^4 – 10^3	– 10^4 10^3	MΩ	2.5.17.1	3.11.1.4
4. Moisture Absorption, maximum	–	0.5	%	2.6.2.1	3.12.1.1
5. Dielectric Breakdown, minimum	–	40	kV	2.5.6	3.11.1.6
6. Permittivity at Frequency, maximum (Laminate & laminated prepreg)* 1 MHz 1 GHz 10 GHz	5.4 5.2 AABUS	5.4 5.2 AABUS	–	2.5.5.2/ 2.5.5.3 2.5.5.9 2.5.5.5	3.11.1.1 3.11.2.1
7. Loss Tangent at Frequency, maximum (Laminate & laminated prepreg)* 1 MHz 1 GHz 10 GHz	0.035	0.035	–	2.5.5.2/ 2.5.5.3 2.5.5.9 2.5.5.5	3.11.1.2 3.11.2.2
8. Flexural Strength, minimum A. Length direction B. Cross direction	– –	415 [60,190] 345 [50,040]	N/mm² [lb/in²]	2.4.4	3.9.1.3
9. Flexural Strength at Elevated Temperature, length direction, minimum	–	–	N/mm² [lb/in²]	2.4.4.1	3.9.1.4
10. Arc Resistance, minimum	60	60	s	2.5.1	3.11.1.5
11. Thermal Stress 10 s at 288 °C [550.4 °F], minimum A. Unetched B. Etched	Pass Visual Pass Visual	Pass Visual Pass Visual	rating	2.4.13.1	3.10.1.2
12. Electric Strength, minimum (Laminate & laminated prepreg)	30	–	kV/mm	2.5.6.2	3.11.1.7 3.11.2.3
13. Flammability (Laminate & laminated prepreg)	V-0 minimum	V-0 minimum	rating	UL94	3.10.2.1 3.10.1.1
14. Glass Transition Temperature	–	170 minimum	°C	2.4.24 2.4.25	3.10.1.6
15. Decomposition Temperature	–	340 minimum	°C	2.4.24.6 (5% wt loss)	3.10.1.8

Epoxy Laminates - Physical Parameters, CTE

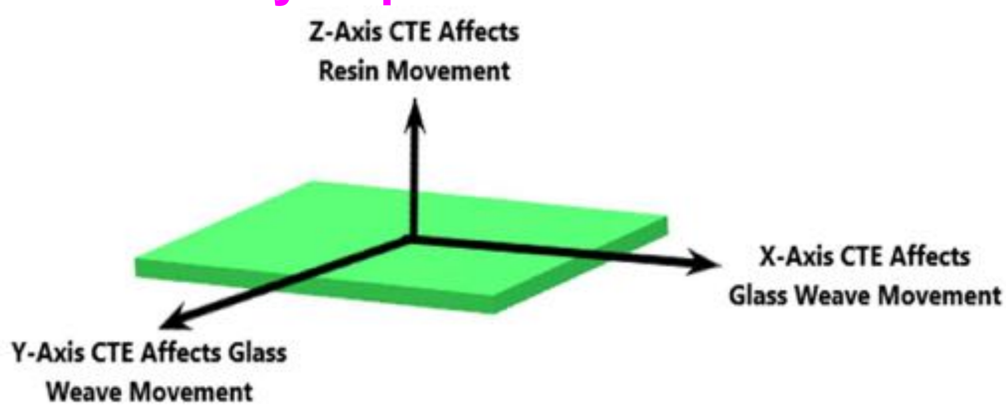
Physical Parameters – (continued)

CTE percentage of movement material may experience, measured as a **parts-per-million ratio, over temperature (PPM/°C)**

Boards are thin in the Z-Axis as compared to the X/Y-Axis therefore, **Z-Axis can be of greater concern,** especially true of small metalized plated via holes

- **X/Y-Axis = Glass weave movement**
  Concern for warpage threatening solder joints & damage to traces
- **Z-Axis = Resin movement**
  Greater concern, as it threatens the reliability of plated holes

(CTE) Coefficient of Thermal Expansion in X/Y & Z Axis



IPC4101/126 Specification Sheet

Electrical Parameters –

- **Dielectric Constant (Er or Dk)** aka. **permittivity or relative permittivity (Er),** ratio of capacitance of electrodes in a specific material, critical for impedance calculations Noted that *approximate* ***Dk* of resin is 3.0** & **glass weave about 5.0, resultant equaling a Dk4.0**
- **Dielectric Losses (Df)** is the **absorption of electromagnetic energy** by the board material in a varying electric field, critical for minimizing db loss calculations, high value to RF circuits

Several other significant factors considered for RF circuits discussed next slide

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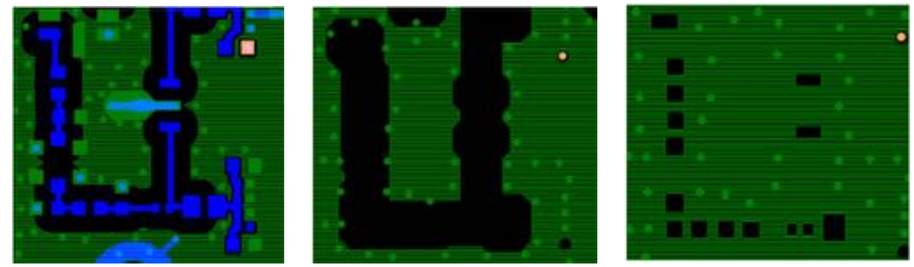
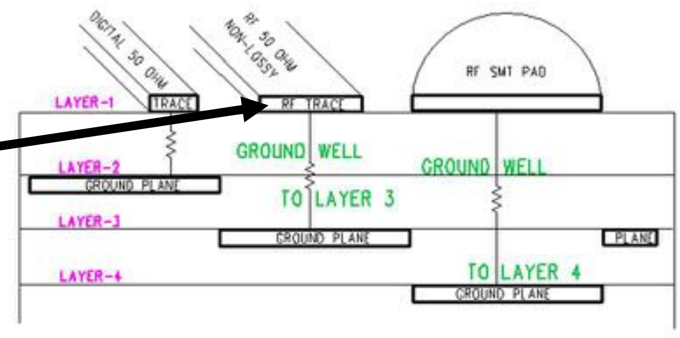
Routing – RF Circuits

Design Practices to Reducing Loss



RF Keep-outs & Ground-wells on: L1 L2 L3



3 Factors Contribute to Insertion Loss (Df):

1. **Wide Traces** = with matching dielectric thickness
2. **Copper Profile** = Rz .7um - 18um (.1-.2 dB loss/cm)
3. **Material Dissipation Factor** = Df .0009 to .020

At 10Ghz - 80% of all loss, dominated by trace width and copper roughness, measured (dB/cm)

Laminate Material Data Sheets

https://insulectro.com/

Typical Values Table

Property		Typical Value	Units Metric (English)	Test Method IPC-TM-650 (or as noted)
Glass Transition Temperature (Tg) by DSC		200	°C	2.4.25C
Decomposition Temperature (Td) by TGA @ 5% weight loss		360	°C	2.4.24.6
Time to Delaminate by TMA (Copper removed)	A. T260 B. T288	>60	Minutes	2.4.24.1
Z-Axis CTE	A. Pre-Tg B. Post-Tg	50 - 70 250 - 350	ppm/°C	2.4.24C
X/Y-Axis CTE	Pre-Tg	12	ppm/°C	2.4.24C
Thermal Conductivity		0.45	W/m·K	ASTM E1952
Thermal Stress 10 sec @ 288°C (550.4°F)	A. Unetched B. Etched	Pass	Pass Visual	2.4.13.1
Dk, Permittivity	A. @ 2 GHz B. @ 10 GHz	3.00	–	2.5.5.5
Df, Loss Tangent	A. @ 2 GHz B. @ 10 GHz	0.0017	–	Bereskin Stripline
Volume Resistivity	C-96/35/90	1.33×10^{7}	MΩ-cm	2.5.17.1
Surface Resistivity	C-96/35/90	1.33×10^{5}	MΩ	2.5.17.1
Dielectric Breakdown		45.4	kV	2.5.6B
Arc Resistance		139	Seconds	2.5.1B
Electric Strength (Laminate & laminated prepreg)		45 (1133)	kV/mm (V/mil)	2.5.6.2A
Comparative Tracking Index (CTI)		3 (175-249)	Class (Volts)	UL 746A ASTM D3638
Peel Strength	1 oz. EDC foil	1.0 (5.7)	N/mm (lb/inch)	2.4.8.3
Flexural Strength	A. Length direction B. Cross direction	49.0 39.0	ksi	2.4.4B
Tensile Strength	A. Length direction B. Cross direction	31.0 24.0	ksi	ASTM D3039
Poisson's Ratio	A. Length direction B. Cross direction	0.183 0.182	–	ASTM D3039
Moisture Absorption		0.1	%	2.6.2.1A
Flammability (Laminate & laminated prepreg)		V-0	Rating	UL 94
Relative Thermal Index (RTI)		130	°C	UL 796

Physical, Electrical, & Environmental Parameters
Enabling Defect Free Mfg. &
Performance Requirements

isola

Astra® MT77

Ultra Low Loss, RF/MW Laminate and Prepreg

Tg 200°C Td 360°C Dk 3.00 Df 0.0017

IPC-4103 /17 UL - File Number E41625

Astra® MT77 materials are a breakthrough, very low-loss dielectric constant (Dk) product for millimeter wave frequencies and beyond.

PRODUCT FEATURES

Industry Recognition
- UL File Number E41625
- RoHS Compliant

Performance Attributes
- Lead-free assembly compatible

Processing Advantages
- FR-4 process compatible
- Short lamination cycle
- Reduced drill wear
- No plasma desmear required
- Good flow and fill
- Dimensional stability
- Multiple lamination cycles
- Any layer technology compatible
- HDI technology compatible
- VIPPO design compatible

PRODUCT AVAILABILITY

Standard Material Offering: Laminate
- 2.5, 5, 7.5, 10, 12.5, 15, 20, 30, 60 mil (0.0635, 0.127, 0.1905, 0.254, 0.3175, 0.381, 0.510, 0.760, 1.50 mm)

Copper Foil Type
- HVLP (VLP2) ≤2.5 micron Rz JIS, 1 oz and below is standard

Copper Weight
- ½ to 2 oz (18 to 70 µm) available
- Thinner copper foil available

Standard Material Offering: Prepreg
- Roll or panel form
- Tooling of prepreg panels

Astra MT77 laminate materials exhibit exceptional electrical properties which are very stable over a broad frequency and temperature range. Astra MT77 is suitable for many of today's commercial RF/microwave printed circuit designs. It features a dielectric constant (Dk) that is stable between -40°C and +140°C at up to W-band frequencies. In addition, Astra MT77 offers an ultra-low dissipation factor (Df) of 0.0017, making it a cost-effective alternative to PTFE and other commercial microwave laminate materials.

Key applications include long antennas and radar applications for automobiles, such as adaptive cruise control, pre-crash, blind spot detection, lane departure warning and stop and go systems.

PRODUCT ATTRIBUTES

TYPICAL MARKET APPLICATIONS

ORDERING INFORMATION:

Contact your local sales representative or contact info@isola-group.com for further information.

Isola Group
6565 West Frye Road Chandler, AZ 85226 Phone: 480-893-6527
Fax: 480-893-1409

Isola Asia Pacific
(Hong Kong) Ltd 12/F, Kin Sang Commercial Centre, 49 King Yip Street, Kwun Tong, Kowloon, Hong Kong Phone: 852-2418-1318
Fax: 852-2418-1533

Isola GmbH
Isola Strasse 2 D-52348 Düren, Germany Phone: 49-2421-8080
Fax: 49-2421-808164

Let someone pick your component values? NO!
Why let someone pick values of your materials?
Pick materials to suit your needs.
Making a Technically Appropriate Material Choice!

Technically Appropriate Material Choice

All these are /126

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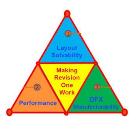
https://insulectro.com/

Circuit Design Types:

- ❑ **Physical Properties**
- ❑ **Electrical Properties**

Isola's Product Ladder

Rigid Laminates:



DF-Solvability:

HDI, uTraces, µVias

DF-Performance:

SI, EMI, PDN, Thermal

DF-Manufacturability:

CTE, Plating, CU surface, Process, Reliability

Product	Tg by TMA	Td	Dk	Df	LP Foil	PIM Sensitive applications	IPC Slash Sheets, Comments and Recommended Bit Rate/ Frequency range	Number of lamination cycles	Compatible with for Hybrid Builds	Replaces These products
185HR	180	340	4.01	0.02	N/A	N	Low cost Lead Free solder compatible FR4 PCB 2 to 3 GHz	3 to 4	I-Tera MT40, Tachyon 100G, Astra MT77	Panasonic R-1755V and R-1655V
370HR	180	340	4.04	0.021	N/A	N	Legacy High rel and lead free compatible FR4 2 to 3 GHz max	3 to 4	I-Tera MT40, Tachyon 100G, Astra MT77	Panasonic R-1755V and R-1655V
FR408HR	190	360	3.68	0.0092	Available	N	Multifunctional low loss resin up to 12 GHz	3 to 4	I-Tera MT40, Tachyon 100G, Astra MT77	Nelco N4000-13 and 13EP
I-Speed®	180	360	3.64	0.006			IPC-4101 /98 /99 /101 /126		185HR, 370HR, 408HR, I-	Panasonic Megtron 4
I-Tera® MT40	200	360	3.45	0.0031						
I-Tera® MT40 (RF/MW)	200	360	3.30/ 3.45/ 3.60/ 3.75	0.0028 0.0035						
TerraGreen®	200	390	3.44	0.0039						
TerraGreen® (RF/MW)	200	390	3.45	0.0032						
IS300MD	190	390	3.06	0.0033						
IS680	200	360	2.80-3.45	0.0025-0.0035						
IS680 AG	200	360	3.00 / 3.38 / 3.45 / 3.48	0.0020 0.0029						
Tachyon® 100G	200	360	3.02	0.0021						
Astra® MT77	200	360	3	0.0017						

ACCORDING TO
IPC-4101

		/40	/41	/97	/98	/99	/101	/102	/126	/129	/134	/140
THERMAL RELIABLE	IS400			●	●	●	●					
	185HR				●	●	●		●			
	370HR				●	●	●		●			
	IS550H											●
HIGH SPEED DIGITAL	IS415				●	●	●		●			
	FR408HR				●	●	●		●			
	I-SPEED®				●	●	●		●			
	TERRAGREEN®											
	I-TERA® MT40							●				
	TACHYON® 100G							●				
	TERRAGREEN® 400G										●	
SPECIALTY PRODUCTS	P95/P25	●	●									
	P96/P26	●	●									

Conductive Metals - Copper

Copper is readily available and comes with several properties:

Thickness measured in ounces based on amount of copper hammered out flat, to cover one square foot, measurement origin from roofing industry

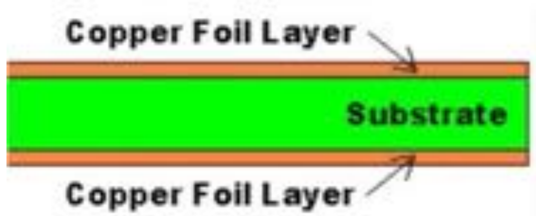
- One ounce of copper foil **(1 OZ CU)** common established thickness approximately 36 microns **(.0014)**
- Copper foil & copper clad material is available in several common thicknesses ranging **in thickness of 1/2, 1/4 and 1/8 OZ Cu**
- Commonly available with **thick usage sizes, i.e., 4, 3, and 2 OZ Cu**

Copper Produced on Drums,
Sheets of Clad Cores and Foils

Copper Foil Weights and Thickness

IPC-4562 also provides guidance and classification per Table 1-1 in section 1.2.6 for most standard copper thicknesses as shown in this similar table

Copper Foil



Copper Clad Core

Micron	IPC	Oz	Mil	Inch	oz/ft²
1µm			0.039	0.000039	
1.5µm	C			0.000059	
2µm	B		0.078	0.000078	
3µm	A	**1/12oz**	0.118	0.00011	0.085 oz
4µm			0.157	0.00015	
5µm	E	**1/8oz**	0.196	0.00019	0.148 oz
6µm			0.236	0.00023	
7µm			0.275	0.00027	
8µm			0.314	0.00031	
9µm	Q	**1/4oz**	0.354	0.00035	0.249 oz
10µm			0.393	0.00039	
12µm	T	**3/8oz**	0.472	0.00047	0.375 oz
18µm	H	**1/2oz**	0.708	0.00066	0.5 oz
27µm	M	**3/4oz**	1.06	0.001	0.75 oz
35µm	1	**1oz**	1.377	0.00133	1 oz
53µm		**1.5oz**	2.08	0.002	
70µm	2	**2oz**	2.755	0.0027	2 oz
105µm	3	**3oz**	4.133	0.0041	3 oz
140µm	4	**4oz**	5.511	0.0055	4 oz

Copper Foil Weights and Thickness

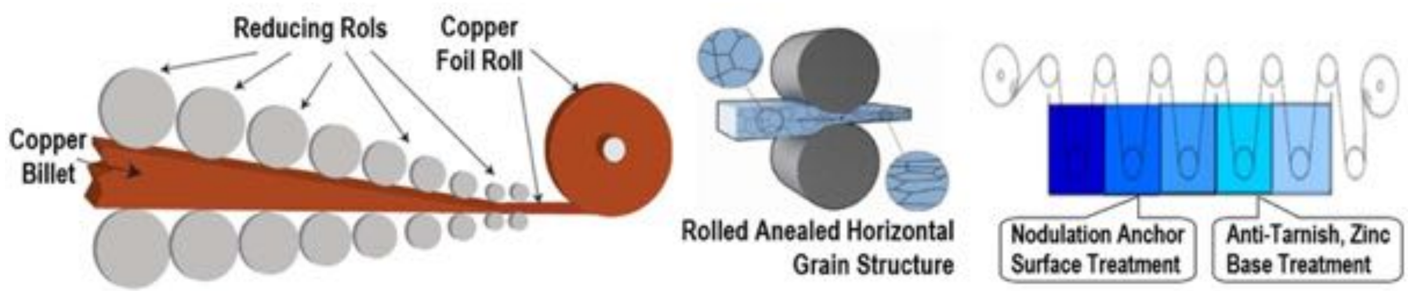
Copper Production Types

Copper produced on rolled drum , further sold in sheets

Copper is **affixed to dielectric material, referred to as copper clad**, also comes as an **unattached copper sheets, called foil copper**

Because copper foil sheets are so thin, often they are supported with aluminum handling plates that are temporarily attached

While in construction, copper is being **pressed onto a drum creating a grain structure**, along with **varied surface roughness** on **each side**, and lastly it also is produced with **several surface finishes for manufacturing purposes**



Copper Production Rolled Drum, Pressed, and Surface Treatments

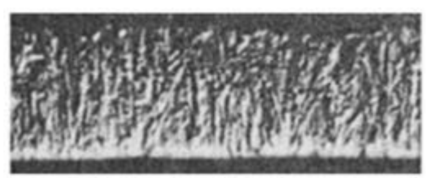
Copper Production Types (1 of 2)

Manufactured in two basic types: **Electro Deposited (ED) or Rolled Annealed (RA)**

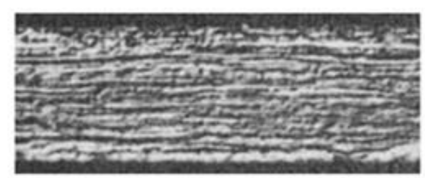
Four major properties that define the construction and usage capabilities

1. **Definition and Manufacturing Method:**
   - **Electro-Deposited (ED)** - which is made from **CuSO4 solution**, by using electrolysis method, made Cu2+ (An ionic identifier of copper) dip into spinning cathode rolls and stripping, producing ED Copper Foil
   - **Rolled Annealed (RA)** - which is made from **high purity copper (>99.98%)**, using a **high-pressure process**, **creating a flattened grain structure** (A.k.a. Wrought)
2. **Form:**
   - **ED Copper - has a vertical grain structure**, for **rigid constructions**
   - **RA Copper - has a horizontal grain structure**, for **flex constructions**

Grain Structures:
ED=Vertical,
RA=Horizontal



ED Cu Vertical Grain



RA Cu Horizontal Grain

Copper Surface Profile and Finish

- **A sheet of copper has two surface sides**, different **finishes** & surface **profiles**
- **Copper clad has two sheets of copper pre-attached to a laminate base**
- **Copper foil is one stand-alone sheet**
- One side typically has a **smooth profile**, and other side is a **rough profile** as shown below

Rough profile serves the purpose of *adhering the metal to the resin system* within the dielectric insulating material used between layers

Various Copper Profiles - Smooth Side and Rough Side

Copper – Skin Effect

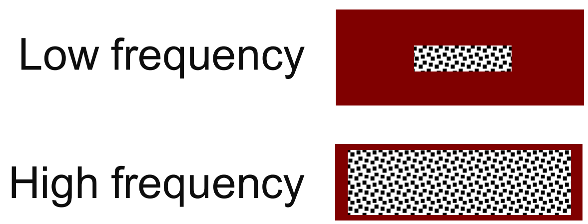
High Frequency Effects

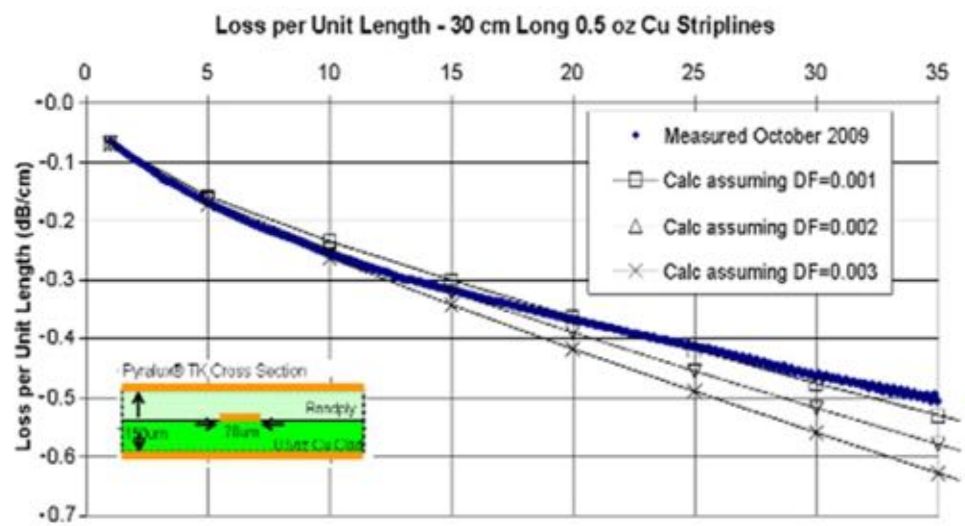
- As frequency increases, current concentrates toward copper outer edges
- When roughness of copper surface becomes close to wavelength of signal, loss increases
- This begins to be a big factor at frequencies of 10 GHz and higher

Rules of Thumb

- Thicker copper has slightly lower loss and wider lines have lower loss
- Effects of oxide treatments are hard to accurately predict, generally effect at higher frequencies
- Skin effect has a bigger impact on stripline than microstrip since field is concentrated on top and bottom of line instead of mostly the bottom

Cu Trace Cross Sections
(dark areas show highest field density)





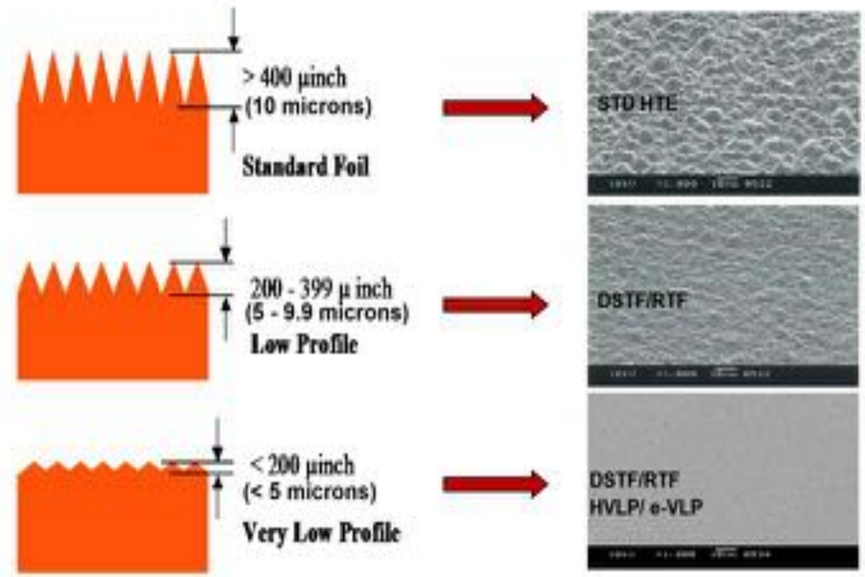
Copper Surface Roughness

Measurement for roughness referred to as, ***Copper Roughness (Rz),*** measuring overall maximum macro surface roughness on rough side

Copper Roughness (Rz), a.k.a, ***Ten Point Height***, average absolute value, **five highest peaks and five lowest valleys**, in microns.

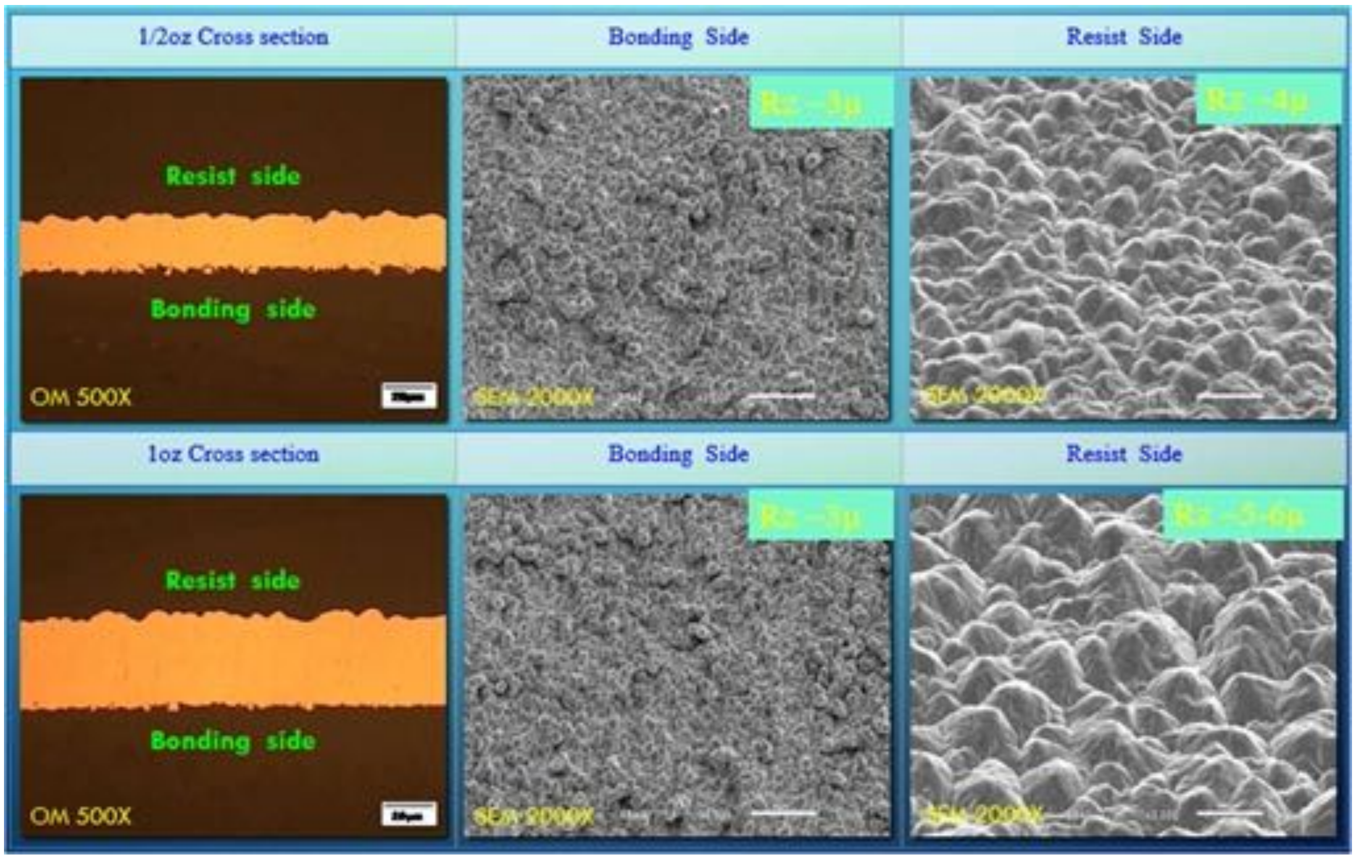
A.k.a. ***Roughness Surface Area Ratio (RSAR)***

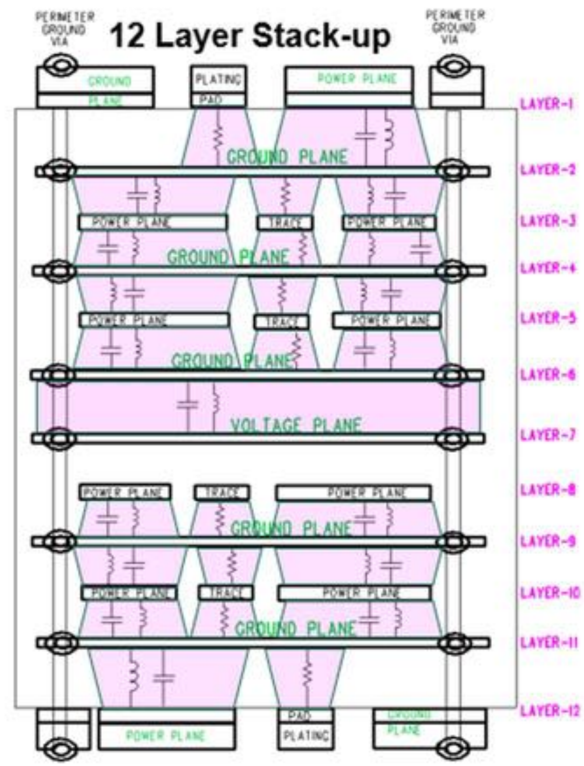
- **Standard foil,** similar roughness on inner layer side & RSAR of 0.3 to 0.4
- RA of 0.3 to 0.4 microns & Rz of 3-4 microns, smooth foil on resist side
- **Very Low Profile (VLP)** with Rz 3-4 microns and **Hyper Very Low Profile (HVLP)** copper foils, 2-3 microns Rz both sides is common



Electrodeposited Copper Foil Side Treatments

Grade 3 Foil – Reverse or Drum Side Treated



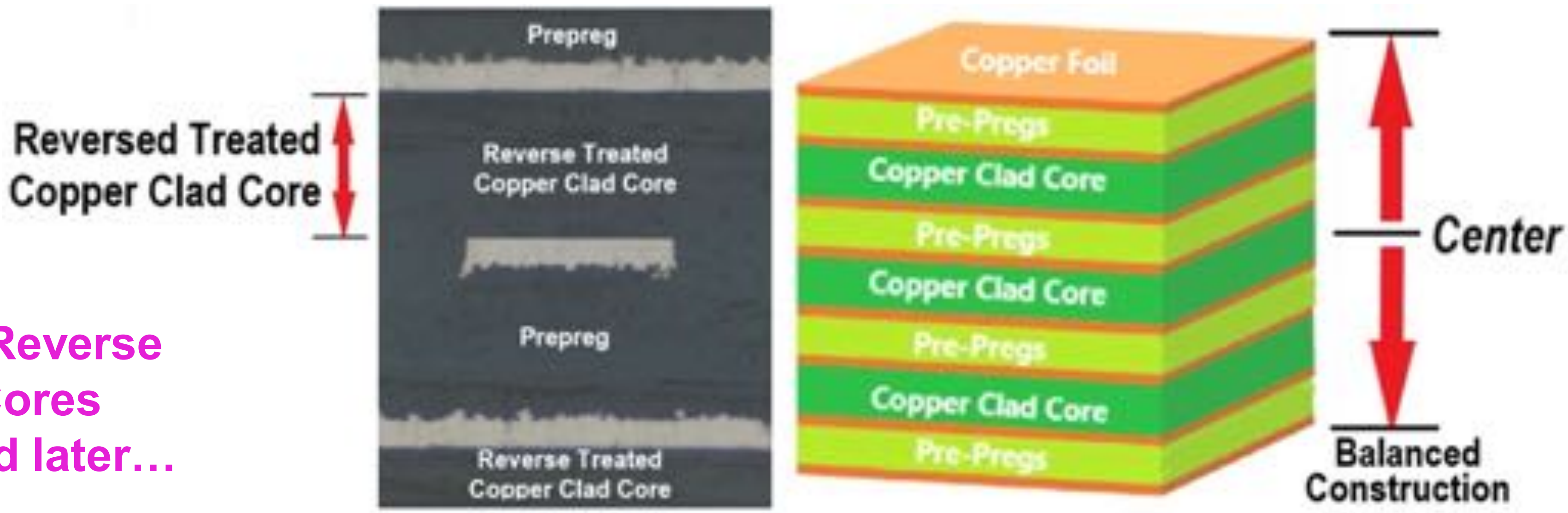


Reverse Treated Copper Clad Core

Most copper clad cores have reverse treat copper on both sides

This **helps with adhesion to adjacent prepreg layers on both sides** using an alternating **core-prepreg-core-prepreg method for a balanced constructions**

Prepregs are the glue between copper clad cores and foils are used on the outer layer with a foil construction

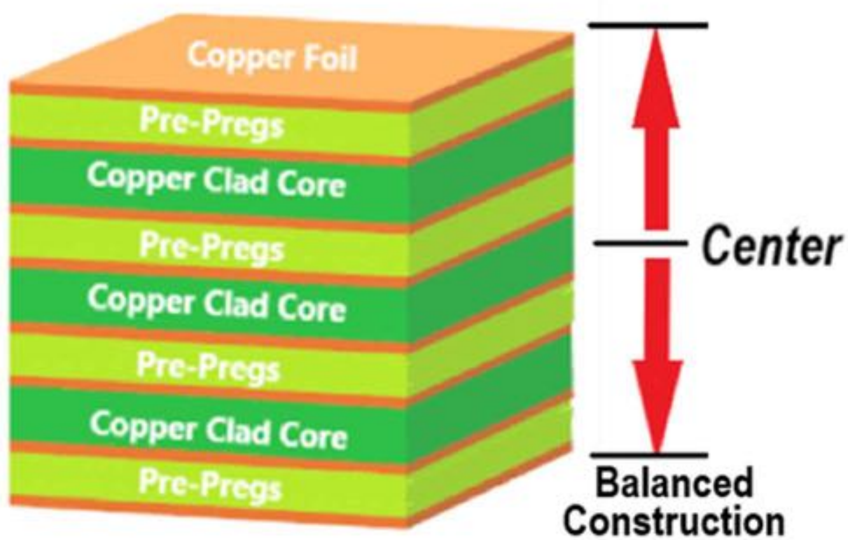


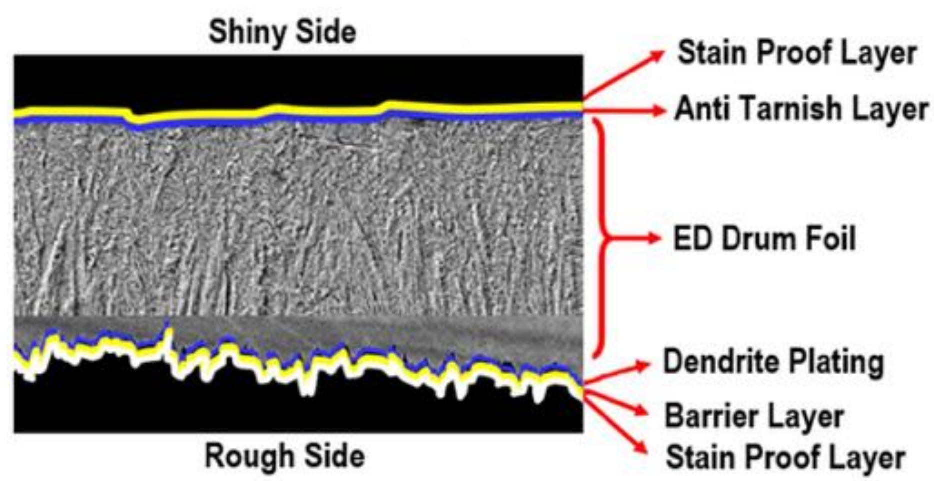
Value of Reverse Treated Cores discussed later…

Chemical Treated Foils

Chemical treated foils involve **treatment of electro deposited copper surfaces**, treatment layers are **thin coatings, improve base foil adhesion** to dielectrics and **add corrosion resistance** which **makes shiny side rougher** than it was before, can be **used in high-speed applications**

- **Reverse Treat or Double Treat** foil typically has RSAR of 1.0 to 1.2, RA of 0.7 to 0.8 microns and Rz of 8-10 microns on one or both sides of the foil

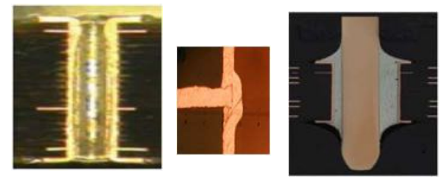




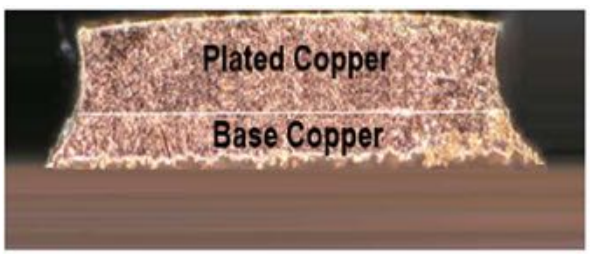
Electro-Plated Copper Holes

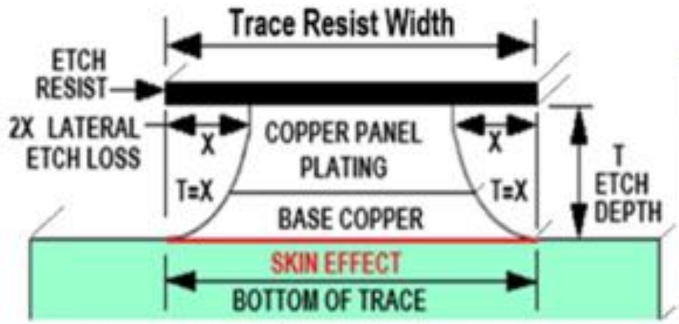
Used to plate drilled holes to bring connectivity from one layer to another or many, **two basic uses for plated holes**:

- **Vias** part of the Z-Axis connectivity and
- **Plated component Thru-Hole (TH) pins**

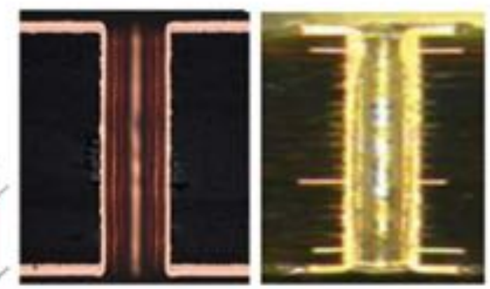


Plating step will inadvertently add an accumulated metal thickness to the layers at that step, whenever applied, will occur for every plated drill process and must be **accounted for when used across the entire panel, called panel plate**, or **selectively, called button plate, where only holes are plated**





Outer Layer Trace after Panel Plate and Etch


Panel Plating, Producing Plated Thru-Holes

Cross Section of Panel Plating, from Producing Plated Thru-Hole

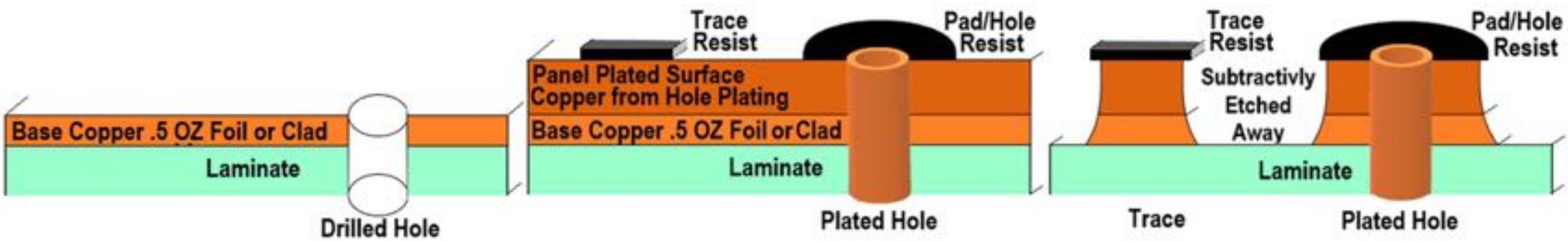
Subtractive Process - Base and Plated Copper

Historically common & **cost-effective process** used to establish metal patterns on PCBs

Subtractive process - full sheet of base copper is on a laminate layer, holes drilled then plated, results in a **thick deposition of panel plated copper on top of the base copper**

Then **etch process strips away unwanted metal**, leaving resultant copper trace, which is **often trapezoidal in shape**, can cause **problems for producibility and performance**

Fabricators Make Spaces not Traces…



Subtractive Process – Resultant Trapezoidal Shaped Trace

How Thick are the Copper Hole Walls???

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Hole wall thickness stipulated IPC Class 1, 2, or 3, many process steps to produce a thru-hole, robust & reliable plated metalized hole wall, **drill hole will often be over-sized,** allow for, process steps for plating wall thickness

Ref. IPC 2221, IPC-A-600, & IPC-6012

Requirements may be waived in a condition known as, ***As Agreed Between User and Supplier (AABUS)***

Ductility - characteristic when copper is deposited into drilled holes during plating process, **allows some Z-Axis movement during thermal stresses**

Difference between electro-plated copper & electro-deposited sheet copper

1. Surface & Hole Copper Plating Minimum Requirements - Buried Vias > 2 Layers, Through-Holes, and Blind Vias

Minimum Cu Plating Wall Thickness	IPC Class 1	IPC Class 2	IPC Class 3
Average – cont. or wrap onto outer	20µm (.00078)	20µm (.00078)	25µm (.00098)
Thinnest Area	18µm (.00071)	18µm (.00071)	20µm (.00078)
Wrap Cu plating for filled PTHs	AABUS	5µm (.00020)	12µm (.00047)

2. Surface & Hole Copper Plating Minimum Requirements - Microvias (Blind and Buried)

Minimum Cu Plating Wall Thickness	IPC Class 1	IPC Class 2	IPC Class 3
Average – cont. or wrap onto outer	12µm (.00047)	12µm (.00047)	12µm (.00047)
Thinnest Area	10µm (.00040)	10µm (.00040)	10µm (.00040)
Wrap Cu plating for filled PTHs	AABUS	5µm (.00020)	6µm (.00024)

3. Surface & Hole Copper Plating Minimum Requirements for Buried via cores (2 layers)

Minimum Cu Plating Wall Thickness	IPC Class 1	IPC Class 2	IPC Class 3
Average – cont. or wrap onto outer	13µm (.00051)	15µm (.00060)	15µm (.00060)
Thinnest Area	11µm (.00043)	13µm (.00051)	13µm (.00051)
Wrap Cu plating for filled PTHs	AABUS	5µm (.00020)	7µm (.00028)

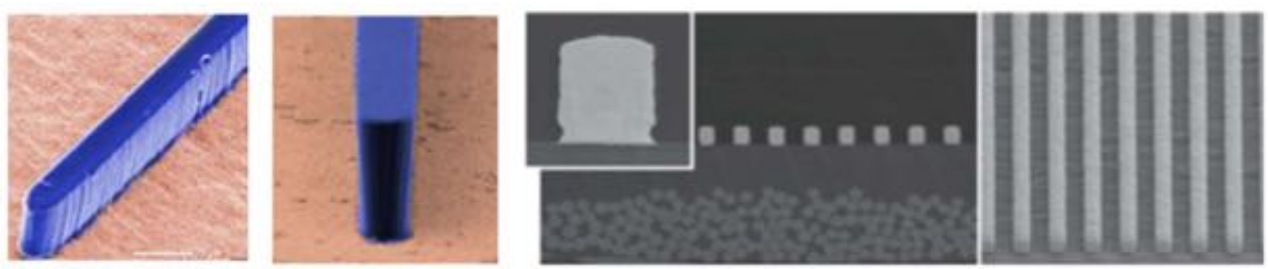
Minimum Plating Wall Requirements

Additive Process (Discuss problematic Issue)

Copper is used to **build up metal on surface** of dielectric, couple variations to this type of fabrication process, used in package design and cell phone industry

- **Semi Additive Process (SAP)** - Metalized processes begin with a **thin seed layer of electroless copper, <1.5 um**, chemical process, then buildup additive copper until metal thickness is achieved, **results in an orthogonal trace geometry**
- **Modified Semi Additive Process (mSAP)** - Photo-imageable circuit pattern on **Ultra Thin Foil (UTF) >1.5um**, pattern defined by resist layer, flash etched, then additive ED process build up on UTF, subtractive process removes copper foil with no circuitry, build up process additive copper until metal thickness achieved, **reliable µtraces widths <3.0mils vertical trace**

Modified Semi-Additive Process (mSAP) – Consistent Vertical Width

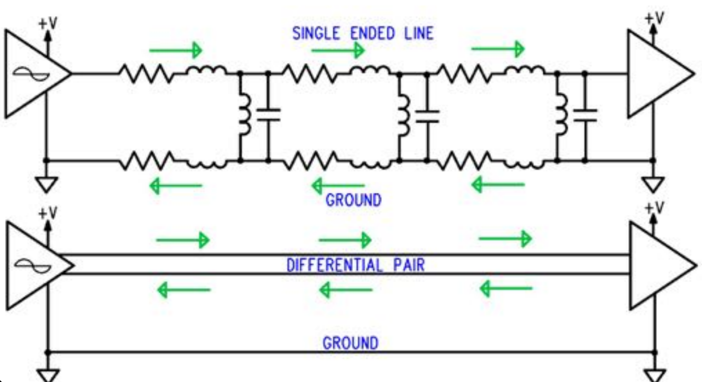


Signal Energy in the Dielectric

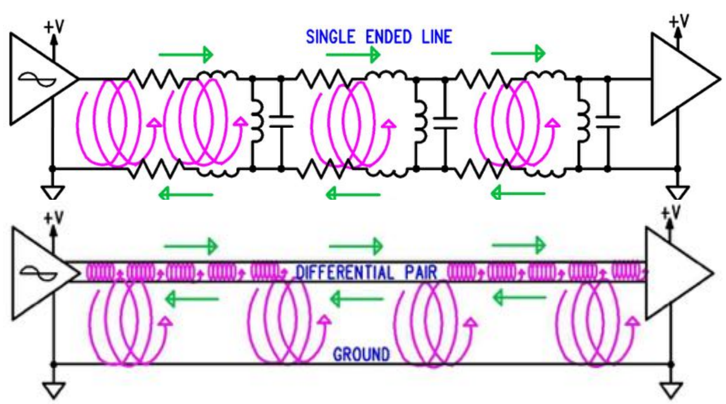
Signal Propagation and Return (energy moving forward & back)
However, it is not forward and back, rather, the energy field is
immediate between trace and plane in the dielectric material

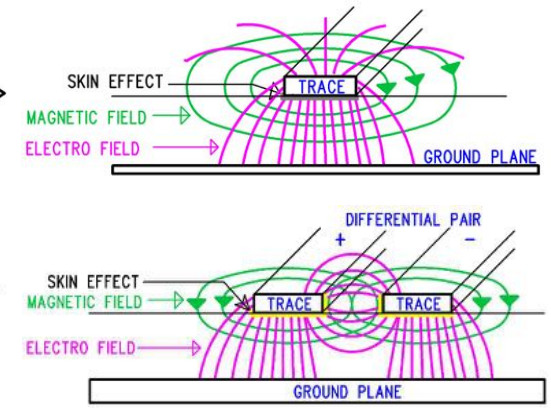
"Materials are part of the circuit"

Not forward and back



Fields exist in the dielectric





Understanding Electro & Magnetic (EM) Fields

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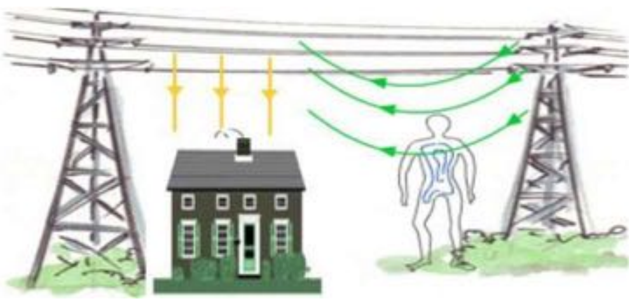
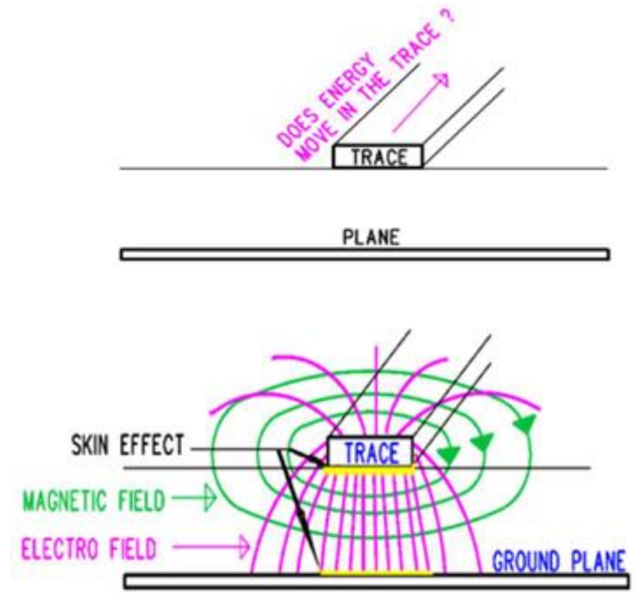
Where does the energy exist, is it in the trace?
NOOOOO! ---→





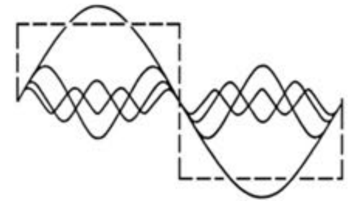
- Energy fields exists between the trace and the plane (return path) **within the dielectric material**
- Why this is important – you're not just connecting a route, rather **you are managing an EM field**

Opposites Attract

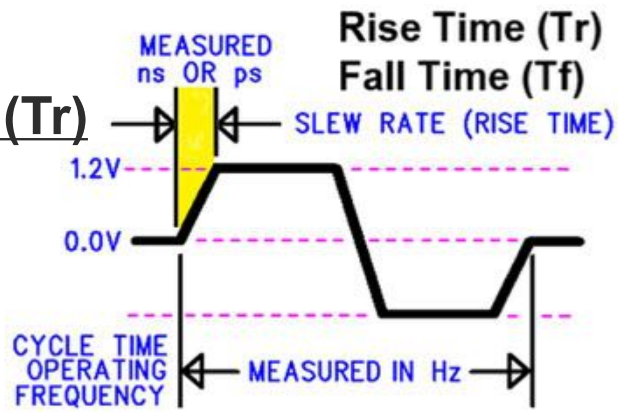
GND Best Return Path - GND net not the only metal that can serve as a return path **but is always the best metal layer,** PWR nets will serve as a return path but not a good one, **don't confuse impedance reference & best return path**

Similar but Different

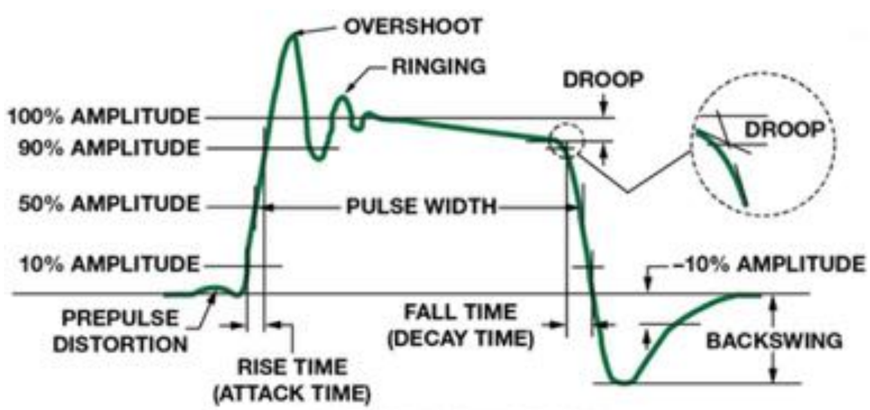
Signal Integrity Issues



Rise Time (Tr)

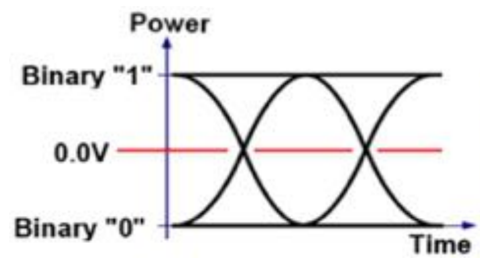


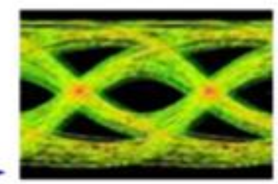
Ideal vs. Actual

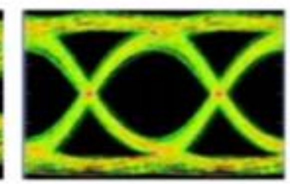


POSITIVE PULSE WAVEFORM

Trace length equal to ¼ of the Rise Time (Tr) signal integrity issues such as reflections start to occur with any impedance discontinuities





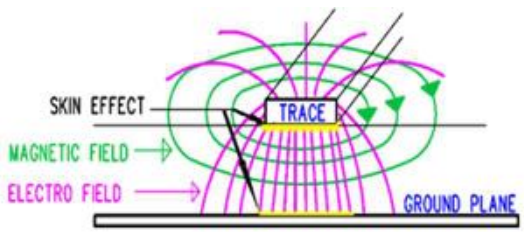


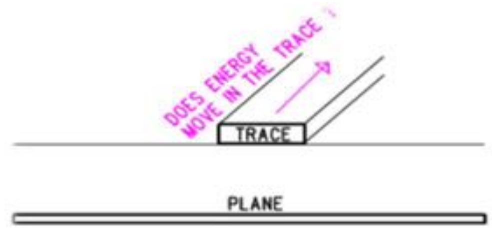
Eye Diagram

- One pulse - left image
- Billions of pulses per sec. - right image

GND (0.0V) Most Important Net

- Copper Sheets have Two Sides (Skin deep)
- Signal Energy is in the material

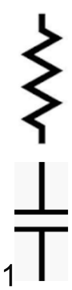




No BLACK MAGIC Secret for Stack-ups

- **GND (0.0V) reference every signal**
- **GND (0.0V) reference every PWR**

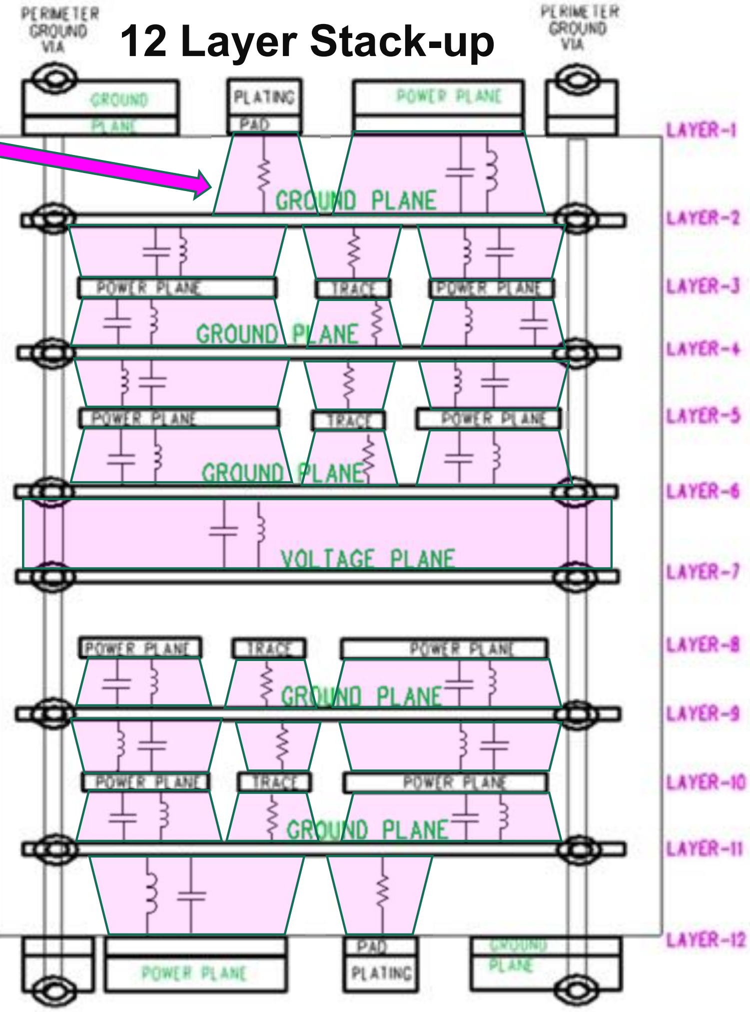
When defining a Stack-up:



- Sketch a resistor symbol from your signal layer to an adjacent uninterrupted GND plane
- Sketch a capacitor symbol from your voltage layer to an adjacent uninterrupted GND plane

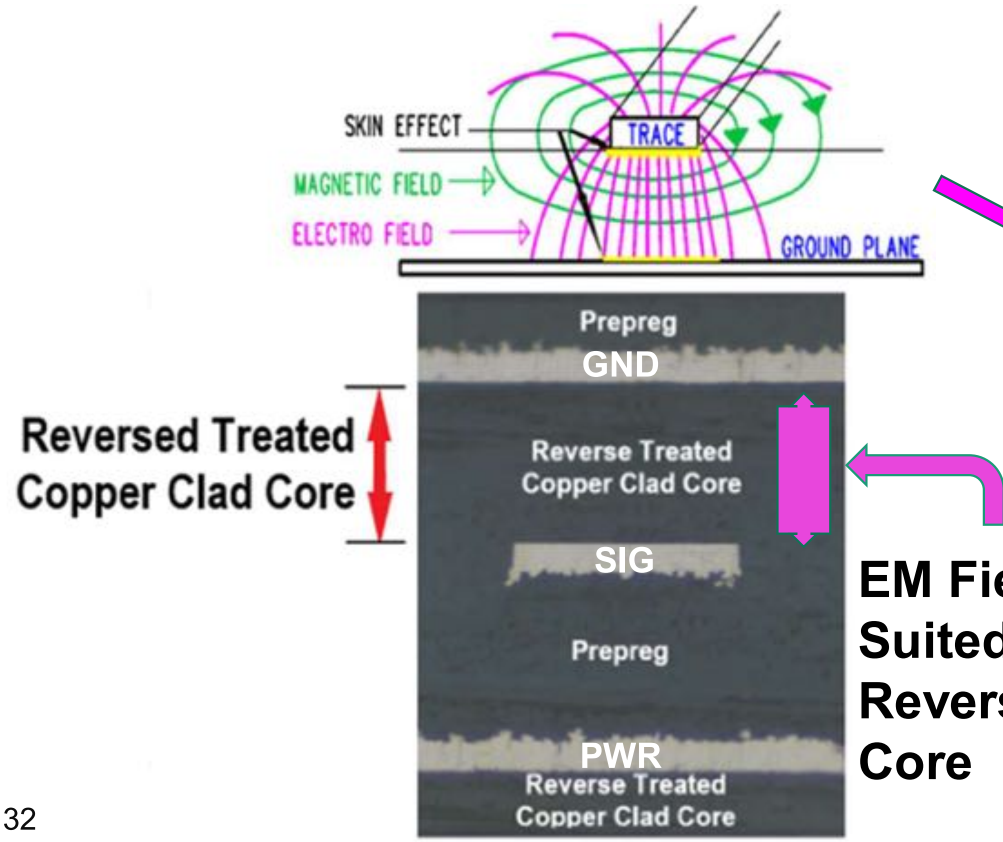
Determining a Stack-up

12 Layer Stack-up



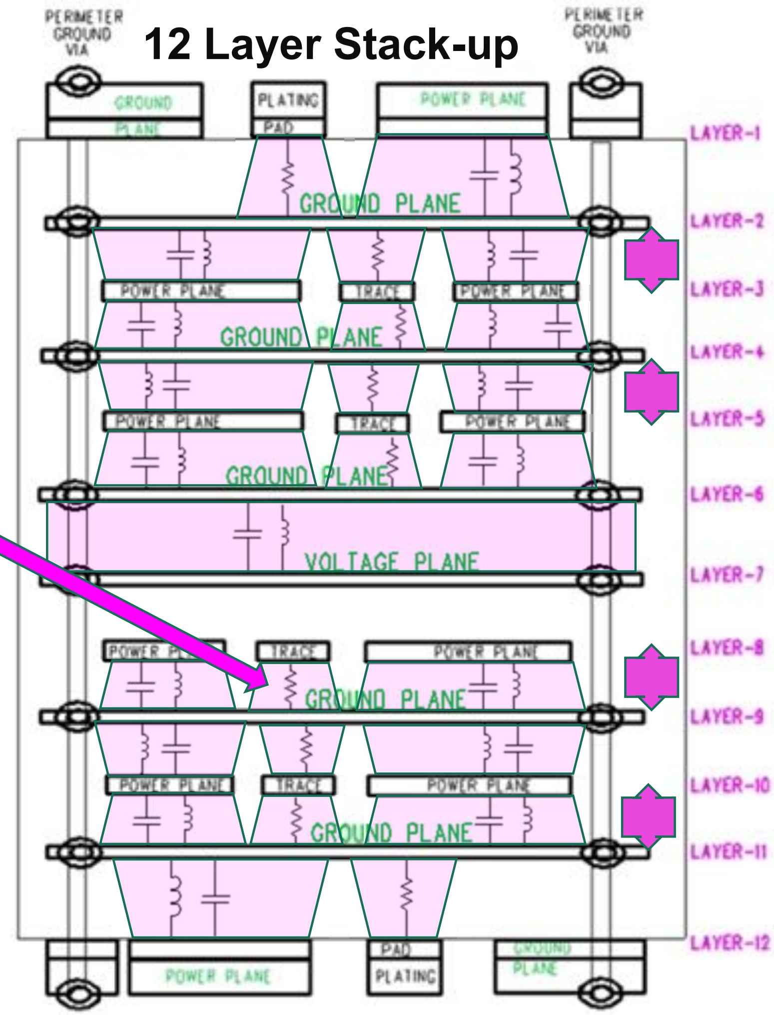
Reversed Treated Copper Clad Cores

Signal Energy is in the Material, **Plan EM Field Locations** using Low Tooth Profile, Reversed Treated, Copper Clad Cores i.e.; L2-3, L4-5, L8-9, L10-11 (As shown)



EM Field is Better Suited Between Reverse Treated Core

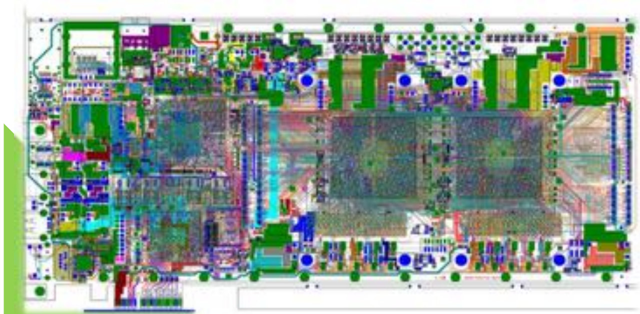
Determining a Stack-up



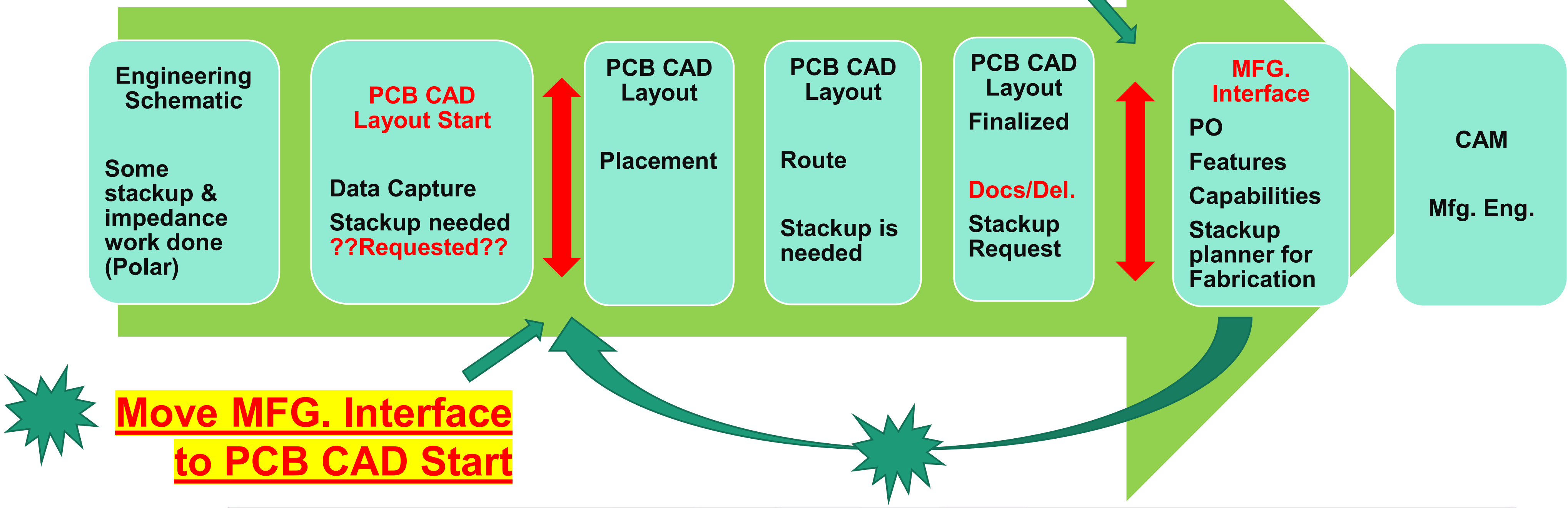
Start Mfg. PO Day 1 of CAD

When Does MFG. Interface Occur?

- Stackup Design Requested?
  OEM PO Locked-in?
- Ensure Robust Mfg. Build
  Proactive or Reactive Solutions



Too Late to Make Needed Changes for Producibility



Move the Collaboration Point to the Start of Layout

Printed Circuit Engineering – Start Data

Stackup Design

Design-Request vs. Fabricator Stack-up with Manufacturing Tolerance Allowances

CAD Design by: ____________________.
12layer Class 2
FR370HR RoHS

Overall board thickness to be 1.57mm (.062) as required.
Surface finish NI/AU
½ oz CU on all layers, plate outers 1.4mils, and plate drill layers as required

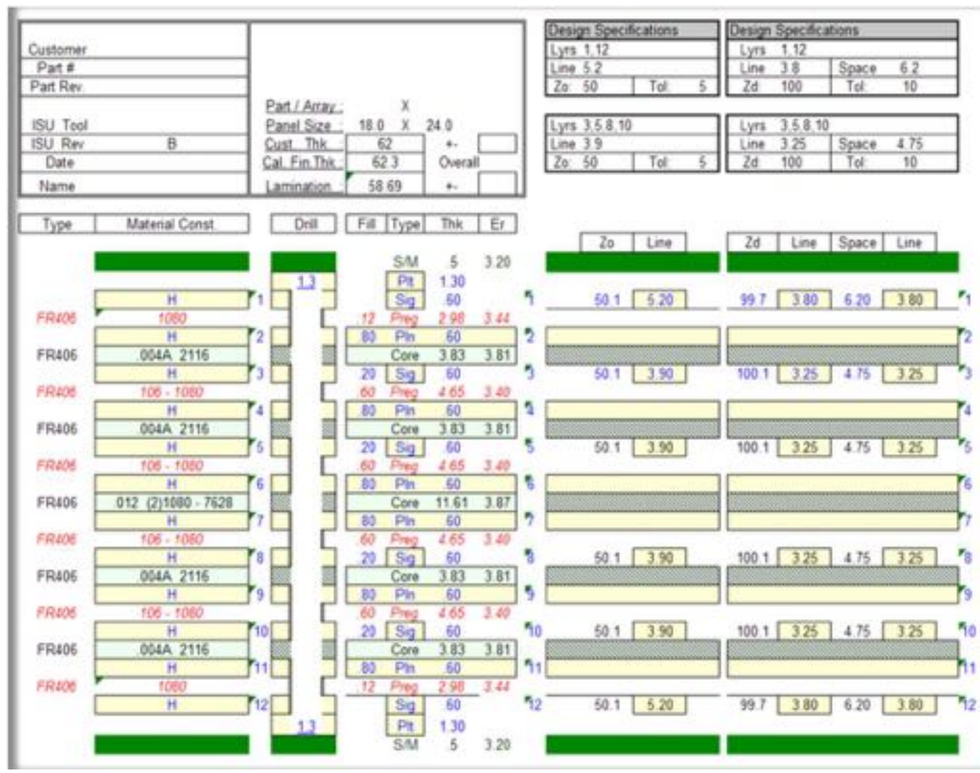
Mech. Thru via L1-L12 .020pad/.010drill
Via in Pad, non-conductive fill, coplanar finish

Impedance designed features: routed on .1mm grid

- 50 ohm +/- 10% .00394 Trace & space Layers 3, 5, 8, 10
- 50 ohm +/- 10% .005 Trace & space Layers 1, 12
  Differential pairs routed on .1mm grid with a .2mm differential pitch
- 100 ohm +/- 10% Differential Pairs - approximately .0033 Trace & .0046 space
  - Used on Layers 3, 5, 8, 10
- 100 ohm +/- 10% Differential Pairs - approximately .0045 Trace & xxxx space
  - Used on Layers 1, 12

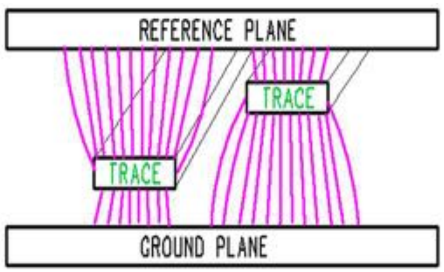
12 Layer Stack-up Single-Stripline
Layer 1 Top GND/PWR & -.00_ trace-via fanout, a few diff-pairs
Layer 2 GND
Layer 3 Signal/PWR
Layer 4 GND
Layer 5 Signal/PWR
Layer 6 GND
Layer 7 PWR
Layer 8 Signal/PWR
Layer 9 GND
Layer 10 Signal/PWR
Layer 11 GND
Layer 12 Bottom PWR/GND & .00_via fanout, a few diff-pairs

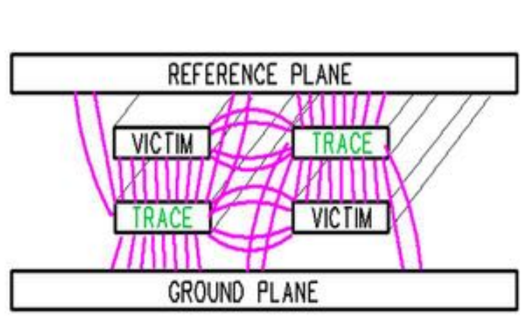
Sample Stack-up Request to be Submitted to Production Fabricator

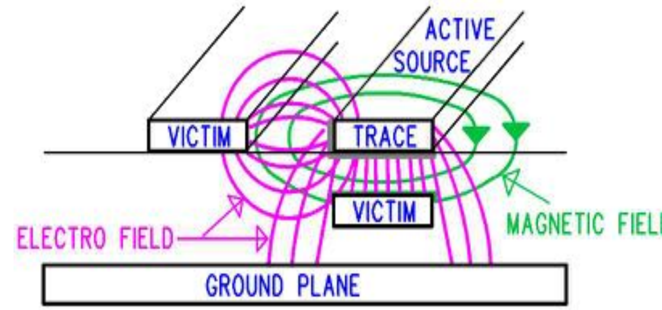


Sample Stack-up provided by Production Fabricator

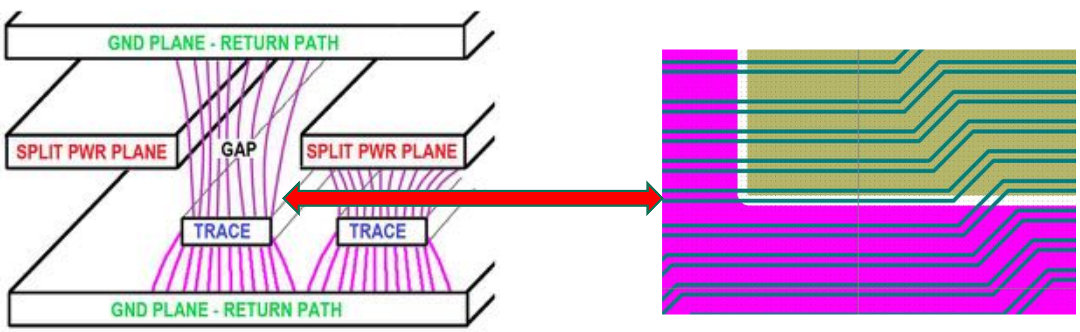
Avoid Crosstalk and Impedance Mis-match

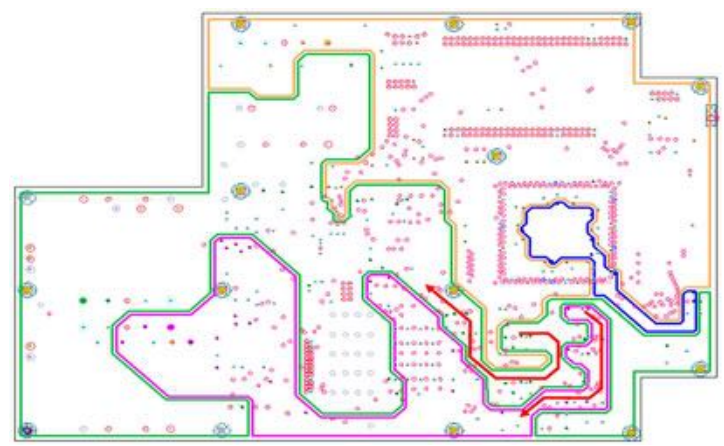






Planned vs. Actual, instead of two traces routed, 4 traces are routed.
The actual routing did not equal the modeled topology,





Routing Over *Split Gap* in PWR Planes will cause **Impedance Mis-match**

Stackup – Routing over Split in Planes

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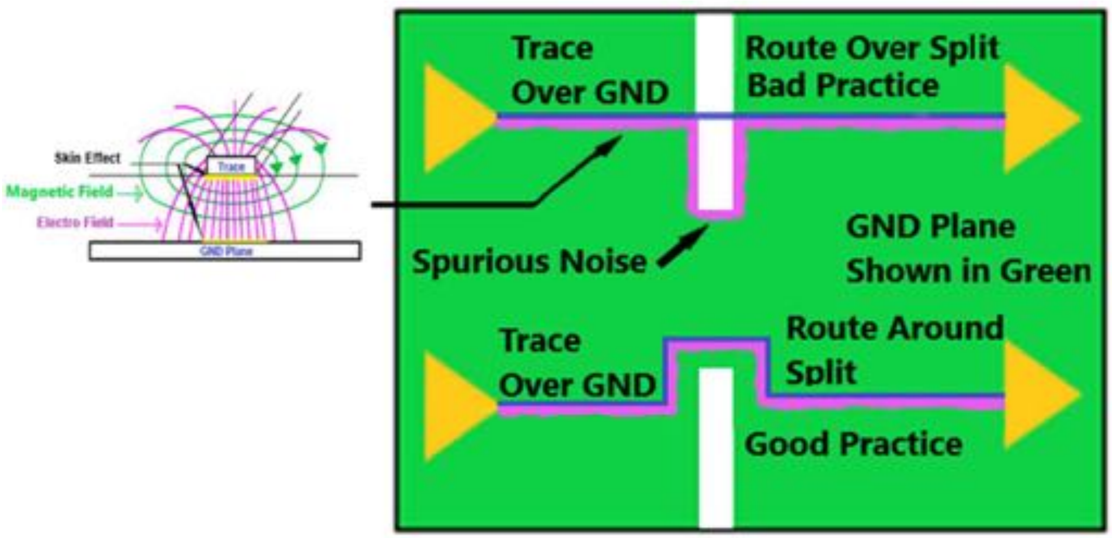
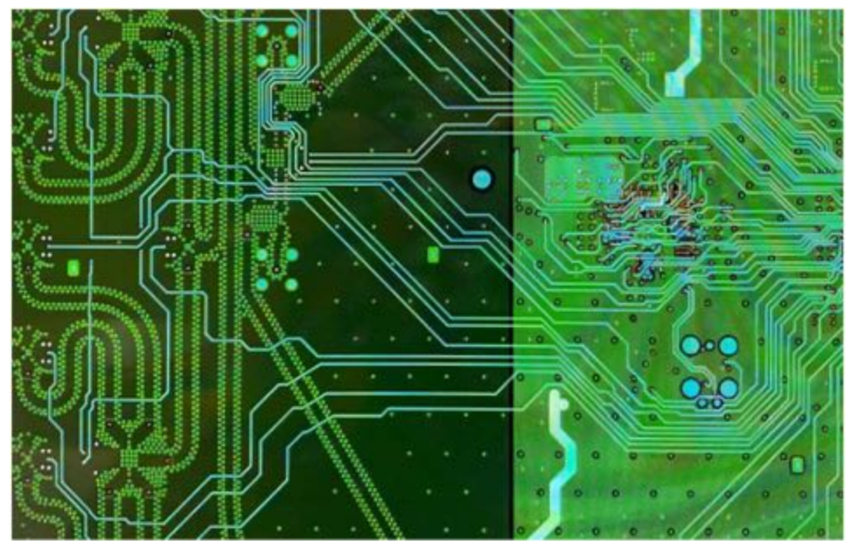
Return layer always a continuous layer, if signal routing **crosses a split** in the return plane, **field energy cannot flow with signals**, will find another path

Separation between signal and its return, **creates interference/EMI problems**

- **Avoid signals routing over two different GNDS**

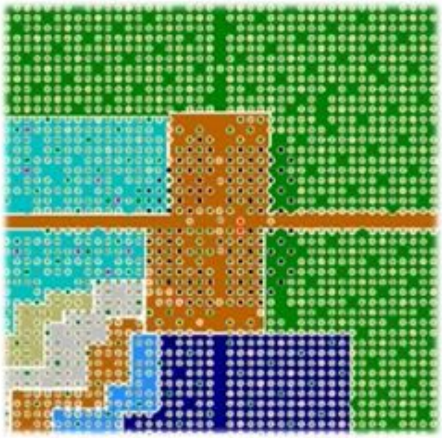


Return Energy Field Pink - Follows Blue Trace Around the Split Plane, Not Follow Over



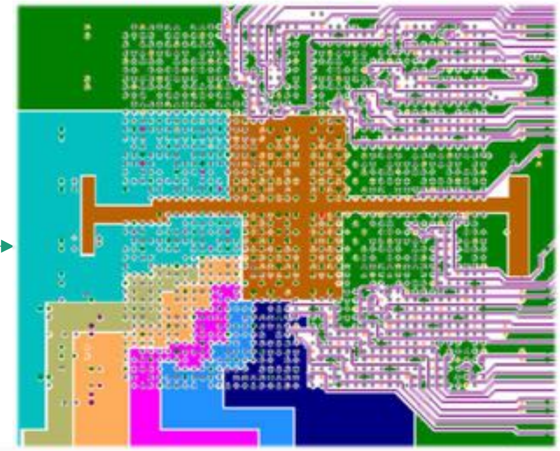
Signals Should Never Cross Over Two GND Return Paths

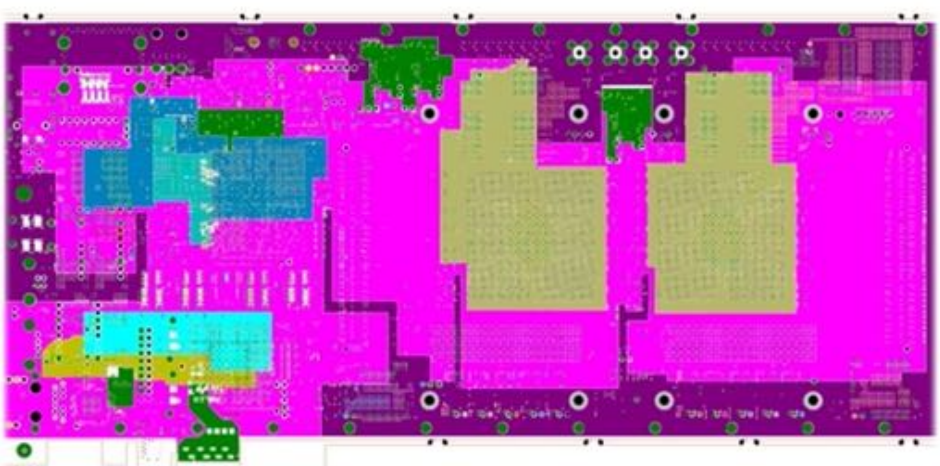
Split PWR Planes & Uninterrupted GND Return Planes



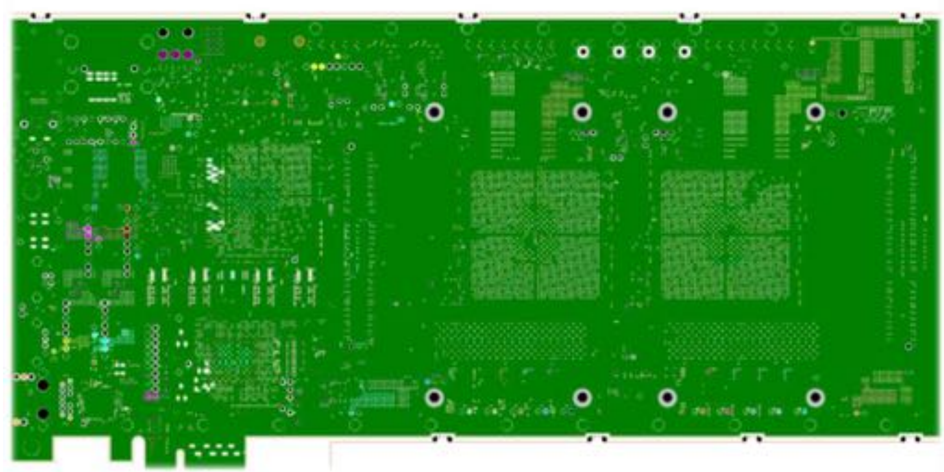
All Split PWR Planes can have dual usage; PWRs & Traces

Split PWR Planes Under a BGA Help to **Balanced Copper**



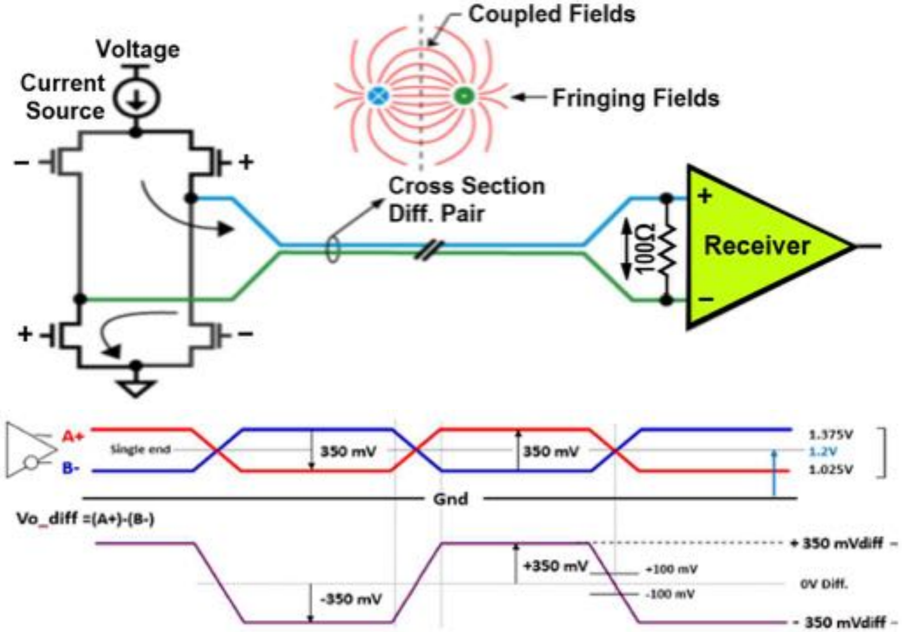


Split PWR Plane



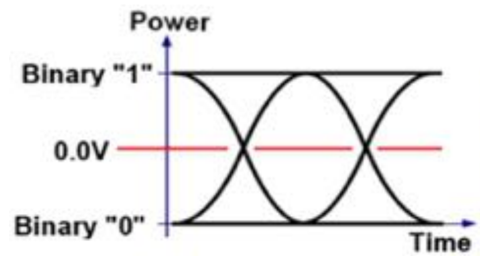
Uninterrupted GND Return Plane

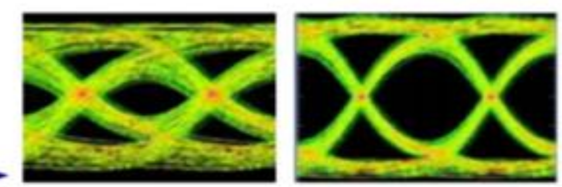
Differential Pair Routing – Signal Integrity Issues



Pair of wires (Twisted pair) or two traces on a PWB, circuit **responds to electrical difference between two signals**, rather than difference between a single wire and GND, aka. single ended mode

Any Impedance discontinuity caused by routing in a transmission line on one signal in the pair, can cause an SI issue and system failure

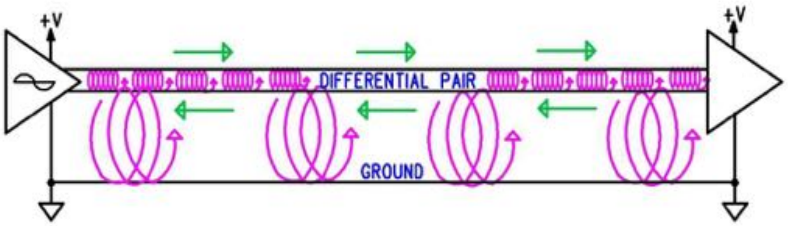


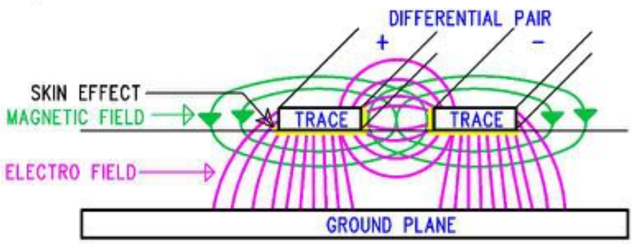


Eye Diagram

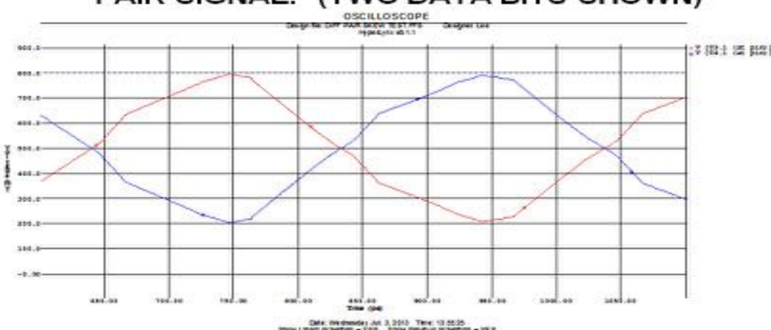
- One pulse, left images
- Billions of pulses per sec., right image

Differential Pairs and Skew



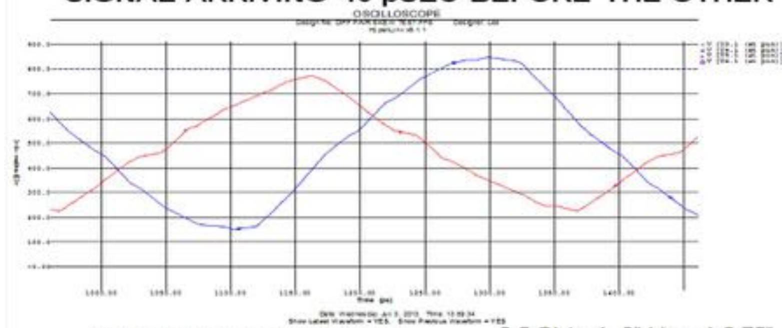


A PERFECTLY ALIGNED 2.5 Gb/S DIFFERENTIAL PAIR SIGNAL. (TWO DATA BITS SHOWN)



2.5 Gb/S, 2 each 3" Lines

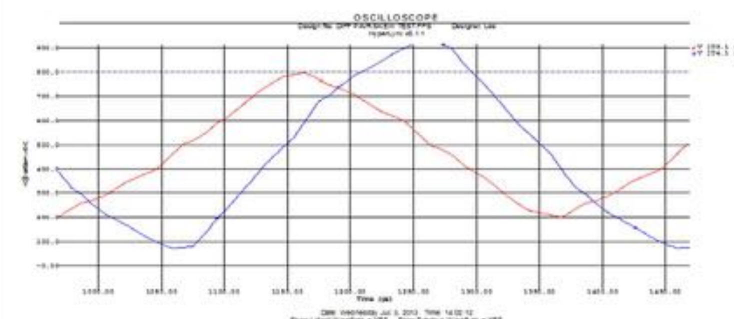
A 2.5 Gb/S DIFFERENTIAL PAIR WITH ONE SIGNAL ARRIVING 40 pSEC BEFORE THE OTHER



Note how eye is not as open as perfectly aligned signal pair.

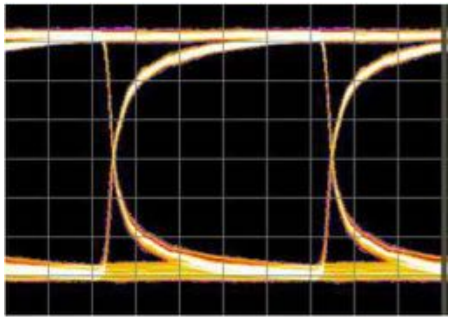
2.5 Gb/s, 1- 3" Line, 1-2.75" Line, Delta = 40 pSec

A 2.5 Gb/S DIFFERENTIAL PAIR WITH ONE SIGNAL ARRIVING 80 pSEC BEFORE THE OTHER

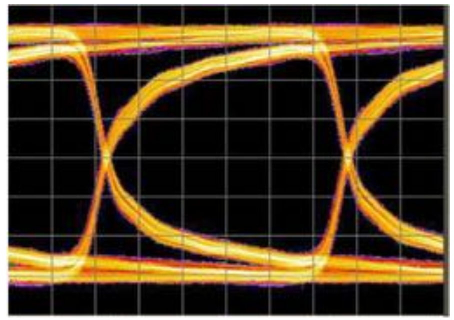


Note how eye is almost closed.

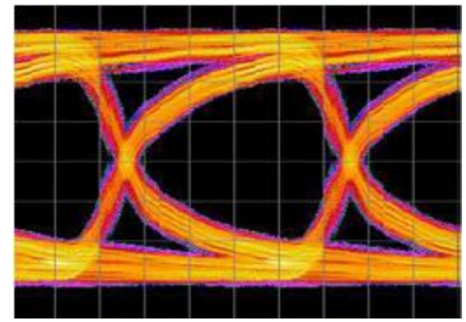
High-Speed Differential Pair Eye Diagrams 4” Stripline FR4



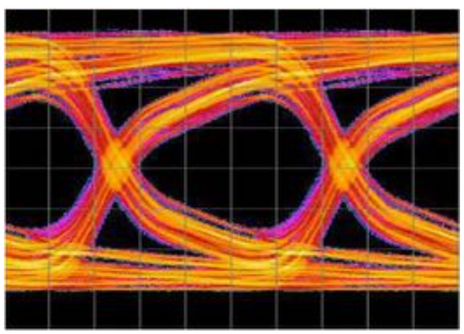
1 Gbps



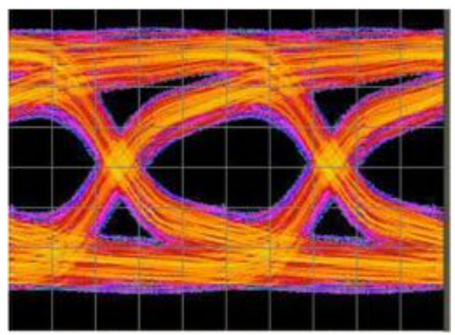
3 Gbps



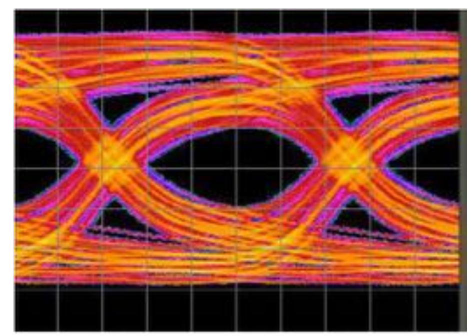
5Gps



8 Gbps



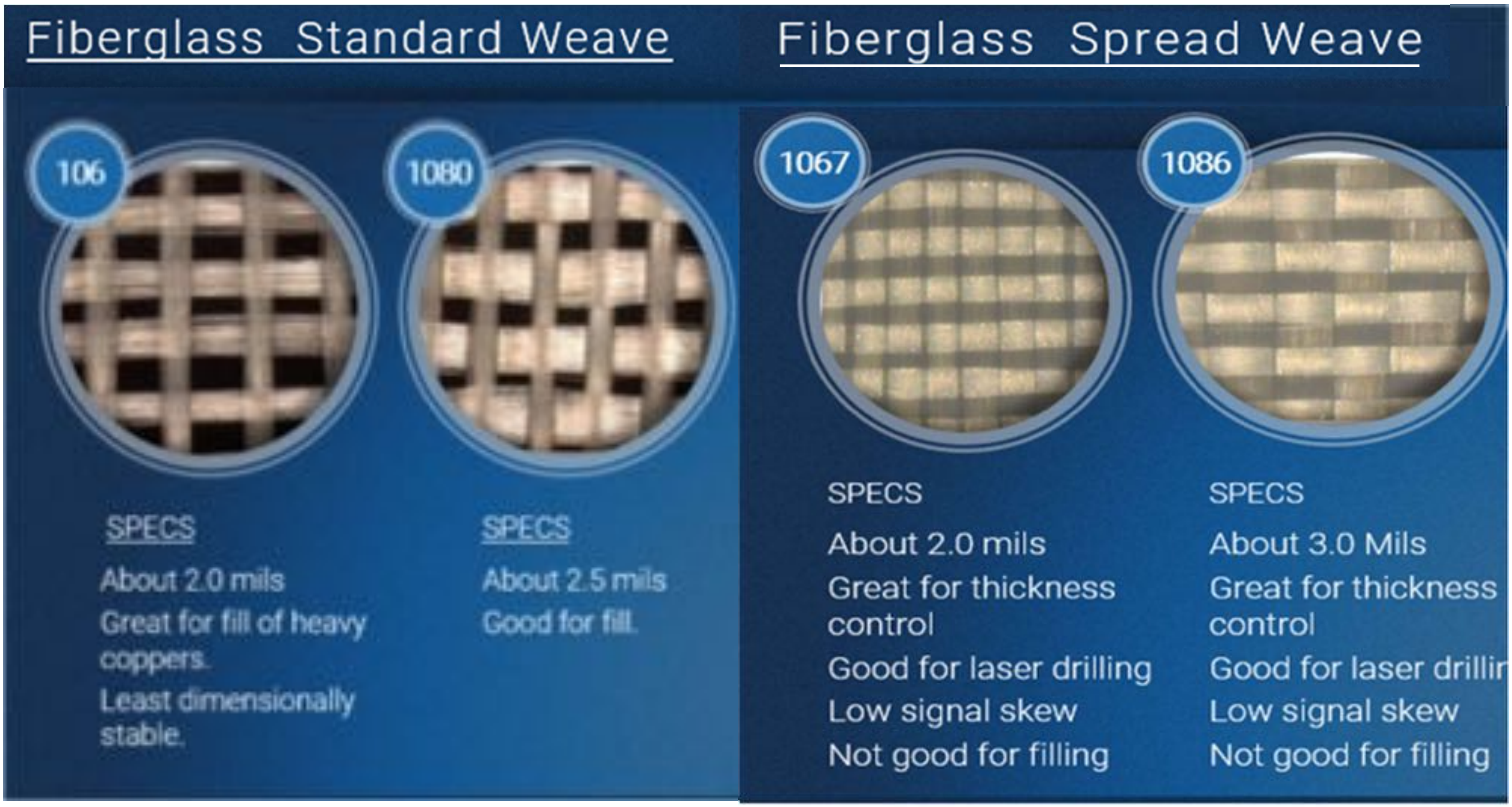
10 Gbps



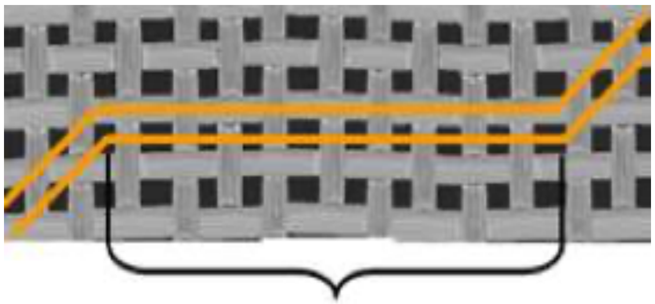
12.5 Gbps

Using a lower loss material will open the “eye” at higher speeds.

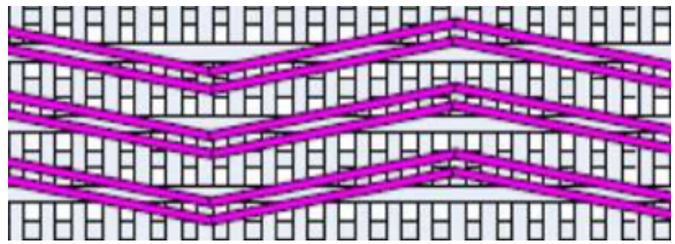
Glass Reinforced Laminate Weave Patterns - Standard & Spread



Differential Pair Routing – Fiber-weave Effect



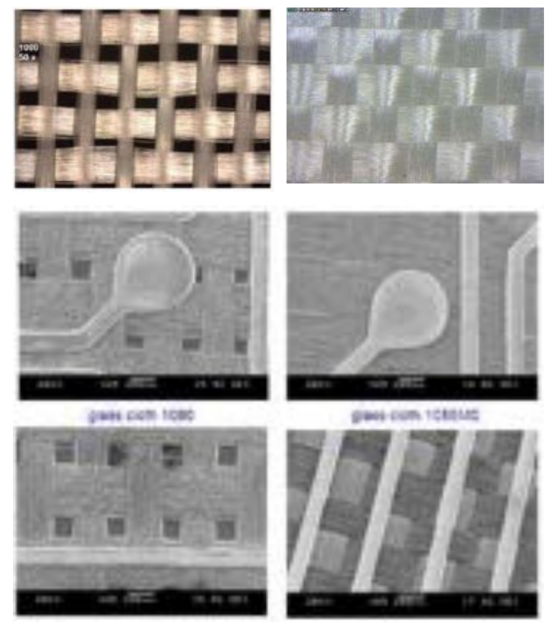
Fiber-weave Effect



Fiber-weave Routing is an Inconsistent Solution

Standard Weave 1080 Loose

Spread Weave 1086 Spread



Over 2.4Ghz Consider Spread-weave Glass

Fiberweave Routing vs. Spread Weave Material

- Std FR4 (i.e.1080): Fabric Weave and Resin have different Dk's, one trace routed over glass and the other trace over resin, results in a mismatched impedance
- Spread Weave: Provides a consistent Dk and will ensure a matched characteristic impedance for both signals in the diff-pair

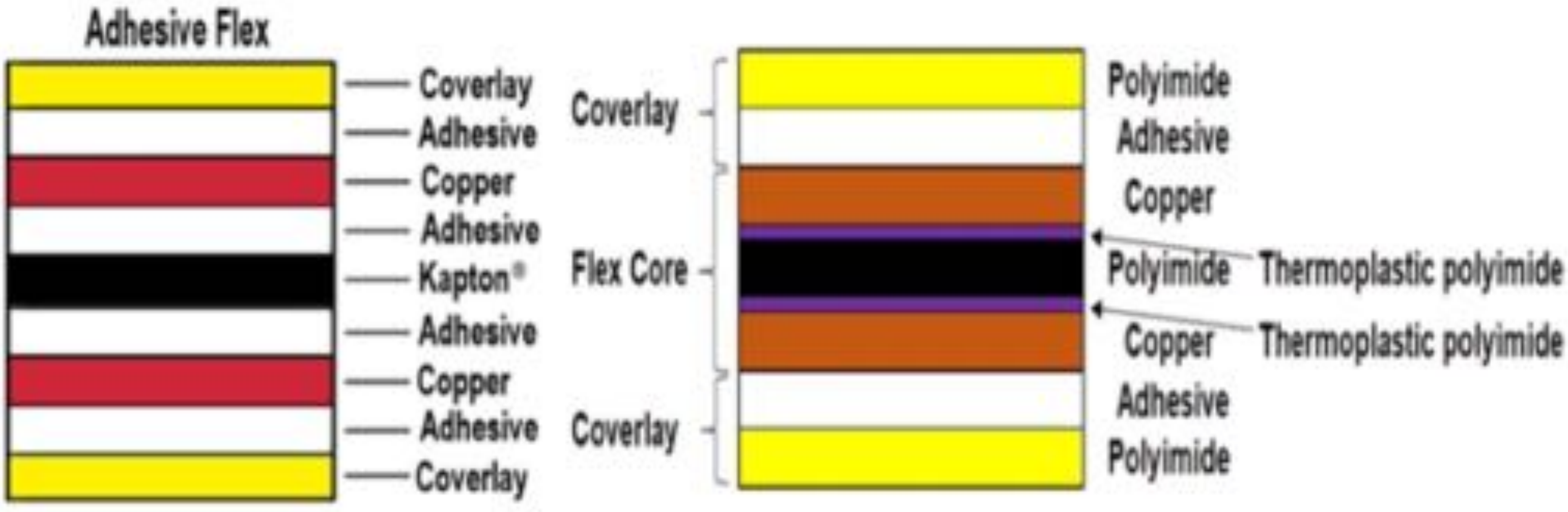
Isola's spread weave product families:

370HR® I-Tera®MT40 I-Speed®

Astra®MT77 Tachyon®100G

Flex Materials and Construction
Adhesive or Adhesiveless

DuPont's Unique Polyimide Technology provides very low loss and very high peel strength

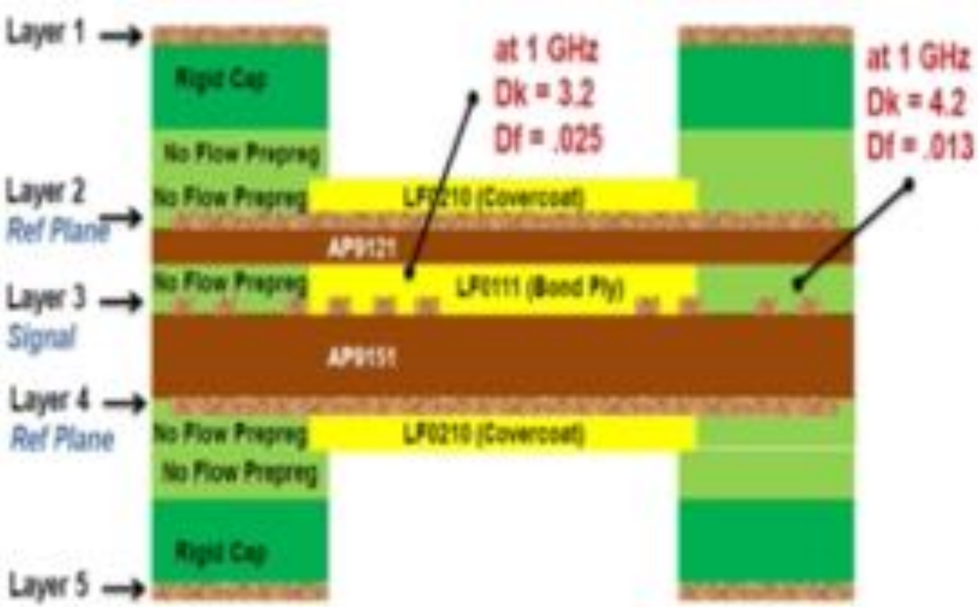


Adhesive Flex Materials and Construction

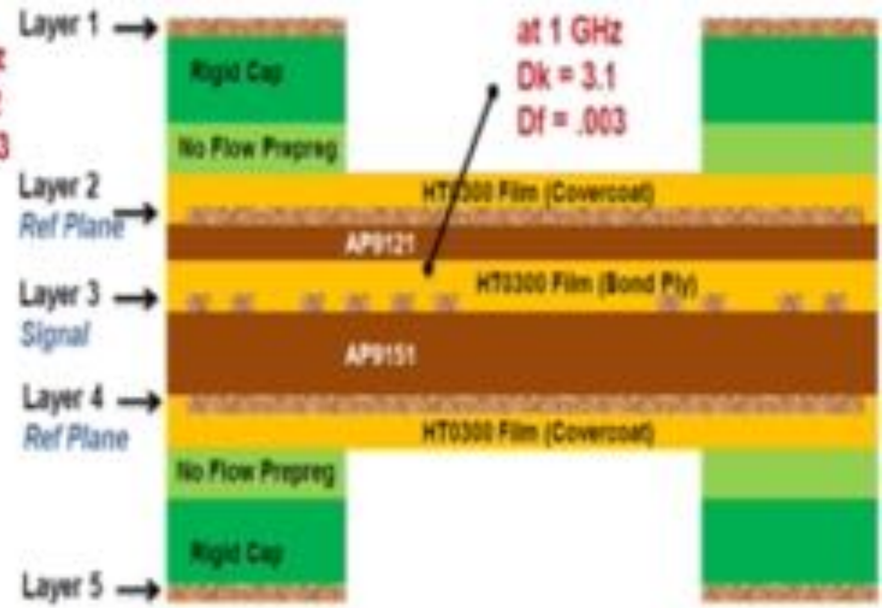
Adhesiveless Flex Materials and Construction

PCB Carolina 2022

Adhesive or Adhesiveless Flex Materials and Construction



Adhesive Rigid-Flex-Rigid Materials and Construction



Adhesiveless Rigid-Flex-Rigid Materials and Construction

Electrical & Physical Properties of DuPont Flex Dielectric Films

Property	Unit	Method	Kapton® HN	Pyralux® AP	Pyralux® AG	Pyralux® HT Bondfilm	Pyralux® TK
Thicknesses	mil	–	1 - 5	1 - 6	1 - 2	1-4	2 – 4
Dk @ 10 GHz	–	Method 2.5.5.5	3.4	3.2	3.2	3.0	2.5
Df @ 10 GHz	–	Method 2.5.5.5	0.010	0.002 - 0.003	0.007	0.003	0.002
% Moisture uptake	%	Method 2.6.2	2.8	0.8	0.8	0.8	0.6
CTE (x-y axis)	ppm/°C	50 to 250 °C	20	25	17-20	25	27
CTE (z axis)	ppm/°C	50 to 250 °C	115	90	90	90	102
Peel strength	N/mm	IPC-TM650	N/A	2.0 (ED) 1.6 (RA)	2.0 (ED) 1.6 (RA)	N/A	1.2 (RA)
Tg	°C	DMA	360 - 410	220	230	220	270
Tm	°C	DSC	–	–	–	–	300
Flammability	–	UL94	V-0	V-0	V-0	V-0	V-0

Material – Summary

Technically Appropriate Materials

- **Don't Let someone select your component values, don't let them select your Material Values**

Solvability:

- Layer Count Reduction
- Thin Overall Boards, Flex-Rigid
- Micro Feature designs, including HDI

Performance:

- High-Speed, RF and Antenna - Signal Integrity, Thermal, EMI/EMC, & Power Delivery

Manufacturability:

- High Yield = Low Cost
- High Process Producibility
- High Quality and Reliability

PCE-Edu, Inc. Introduces: *PCE Professional Curriculum*

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www.pce-edu.com

- After registration, student kit mailed (textbook), read chapters 1-6 approximately 2-4 weeks prior to scheduled 40-hour interactive class.
- **In 2023 enrollment cost will be $2,995. Significantly more cost effective than the few similar certifications currently on the market.**
- Following the class, you may take the exam for certification.
- **Online, open book, timed exam.**
- Lifetime Certification ponsored/recognized by **PCEA** trade association.
- **Classes taught live in-person or offered using the Zoom platform, whereby students are required to have appropriate AV equipment: Headphones, microphone, camera on a dedicated computer.**

Review Comments by Lee Ritchey:

"I've had time to review the textbook. It is the best book of its kind that I have ever seen. Very nice work!"

"I'll be showing it at my classes from now on...

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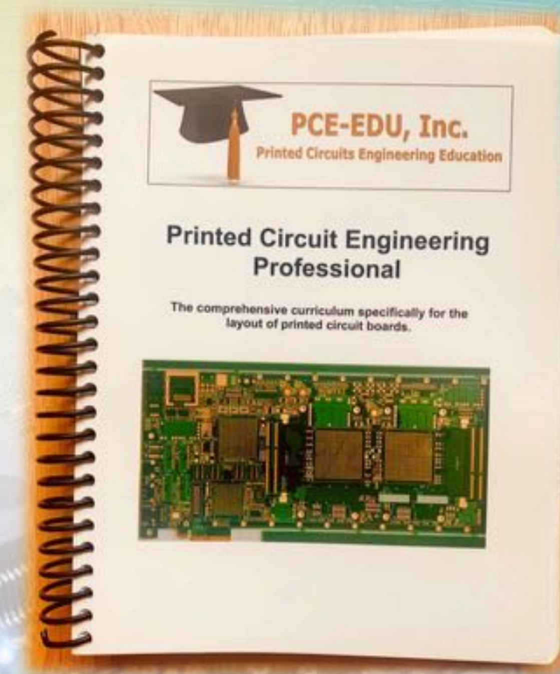

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LinkedIn

Thank You!

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