PCB Carolina 2022

110922RC

EMC, SI, and PI Impact of Embedded Capacitance and High-Performance Copper in RF and High Speed Digital Devices

November 9, 2022

PCB Carolina
McKimmon Center, Raleigh, NC

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OAK-MITSUI TECHNOLOGIES

ABSTRACT:

With miniaturization, higher speeds, and more device complexity, today's RF and high-speed digital devices require more precise filtering, improved signals, and power with less noise. This discussion will focus on how the lowest profile coppers can improve SI, how ultra-thin coppers can be used to make more precise circuits and features, and how extremely thin and high Dk dielectrics improve EMC, SI and PI.

WE WILL LOOK AT:

- Intro to electro deposited copper and embedded capacitance materials
- Impact of Very Smooth Profile Copper on Transmission
- MicroThin and RF
- Embedded Capacitance for RF and Digital and impact on EMC
- Wrap up

Sharper Images are Good!

Hubble Webb

Southern Ring Nebula

Hubble Webb

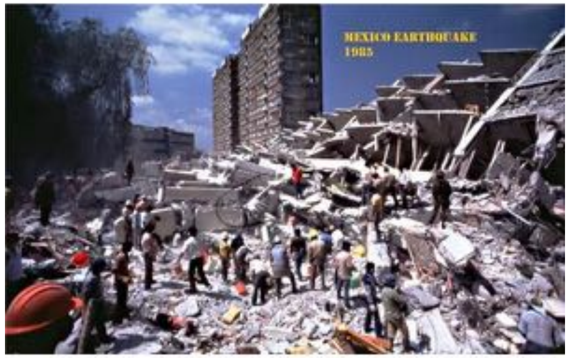
Pillars of Creation

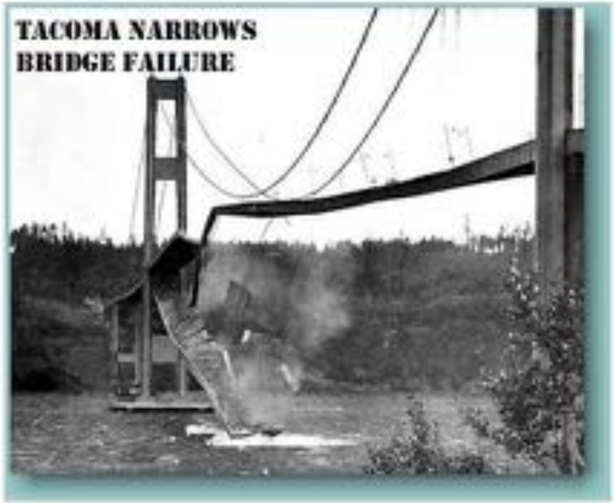
Credits: NASA, ESA, CSA, STScI; Joseph DePasquale (STScI), Anton M. Koekemoer (STScI), Alyssa Pagan (STScI)

High Resolution for Better Signals….this guy looks Bad!

Eugenijus Kavaliauskas/Nikon Small World

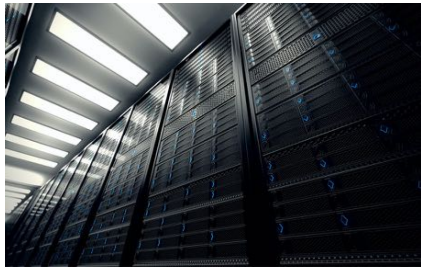
Resonance is Bad!

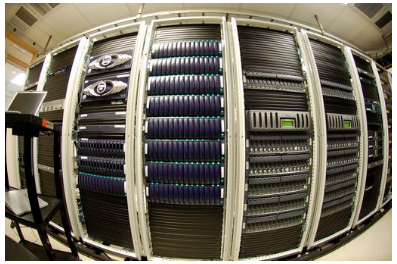




Embedded Capacitance and Advanced Copper is Good!


Routers


Servers
(Cloud computing)

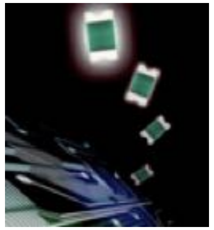

SSD storage


Super computers


Military

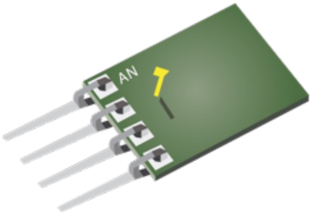

Aerospace

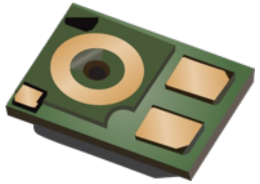

Drones


Organic Capacitor chip
Diplexers, RF Filters


Medical


IC testers


Modules


MEMS Microphones
(Size 2.5mmx3.5mm)


Automotive

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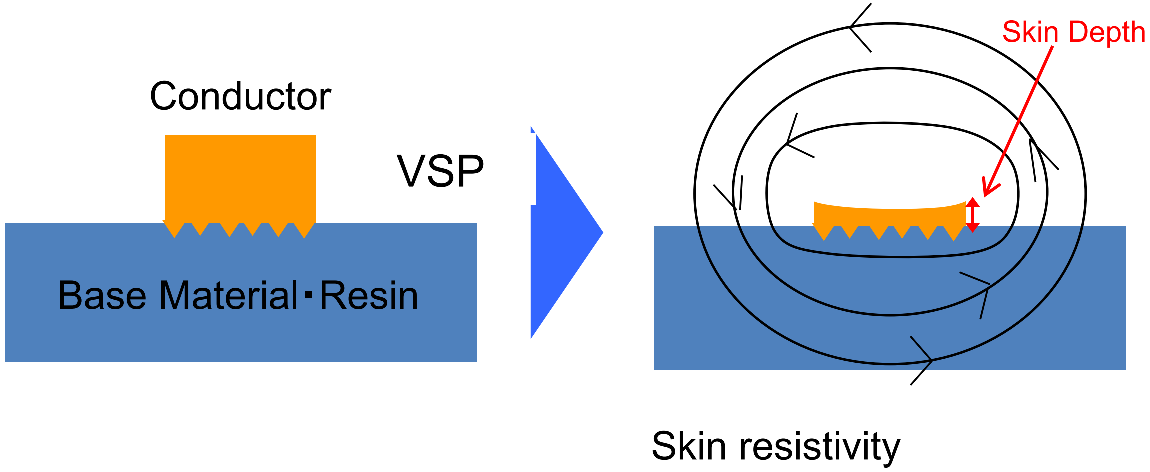
Very Smooth Profile Copper and RF

Skin Effect

At higher frequency range, the signal currency runs at the surface of copper foil（Skin Effect）.
The depth in which signal currency runs is called “Skin Depth”.
The Skin Depth can be calculated by the formula:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} = \frac{0.066}{\sqrt{f}}$$

f=frequency



Skin resistivity

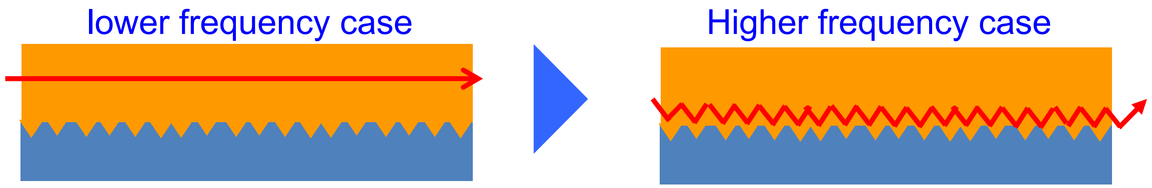
Frequency(GHz)	Skin Depth(um)
0.1	6.6
1	2.1
10	0.7
20	0.5
40	0.3
100	0.2

Higher frequency
⇒ More Skin effect

More affected by conductor surface conditions
In case of higher conductor roughness, wire length becomes longer in effect.

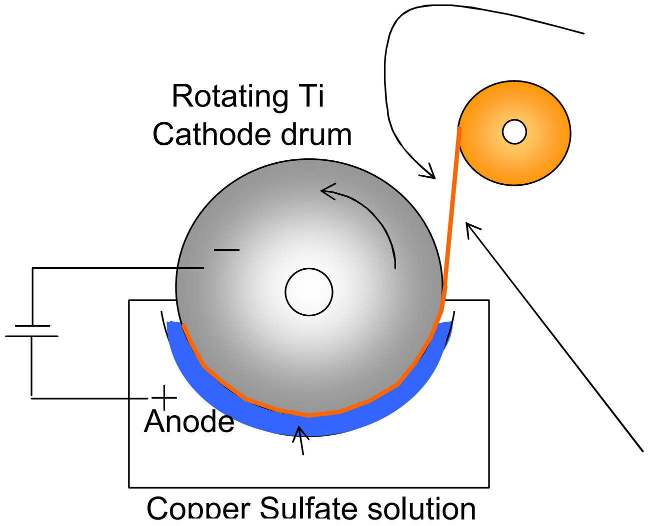
Increased Signal Loss

Image of signal currency flow



Low conductor roughness proved to improve Signal Loss.

• Making Smoother Copper

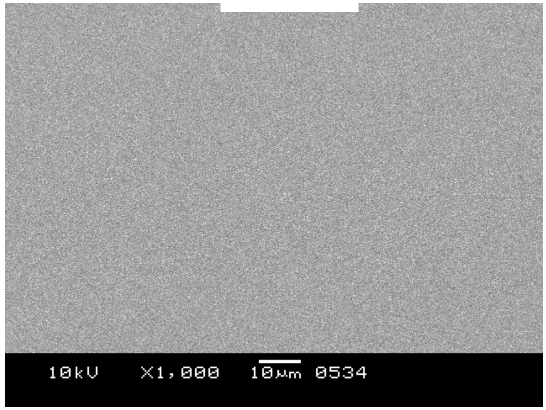


Surface topography

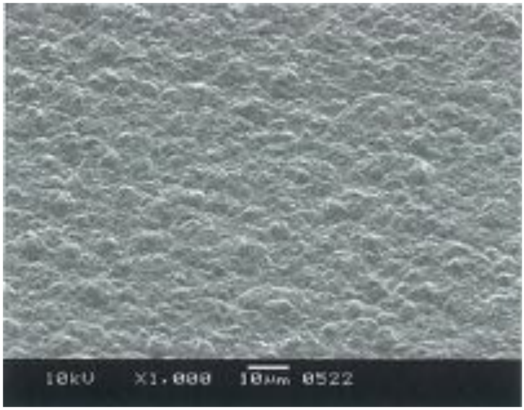
Drum side

Deposited side

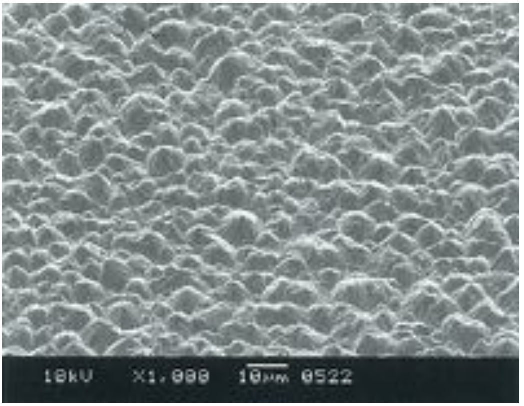
VSP®



VLP™



Conventional ED foil



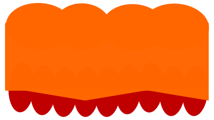
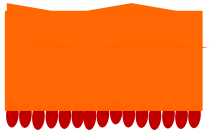
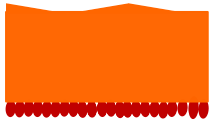
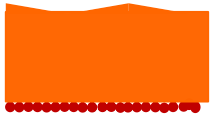
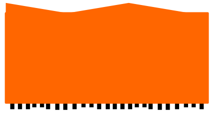
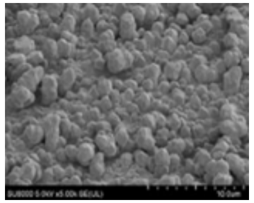
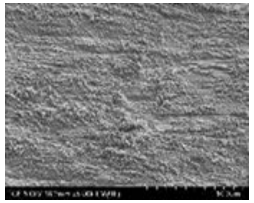
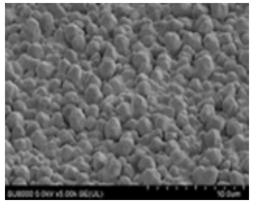
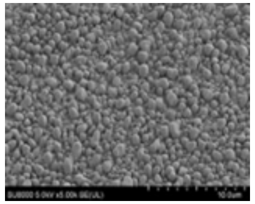
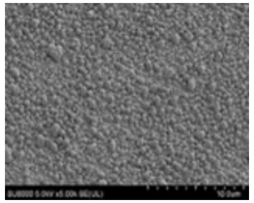
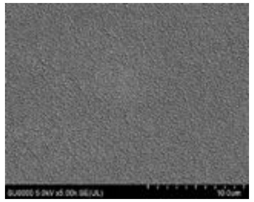
VSP

Very Smooth Profile

Standard Copper Foil

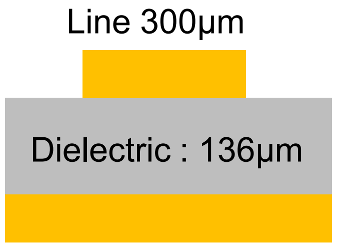
MITSUI KINZOKU TAKING FULL ADVANTAGE OF MATERIAL INTELLIGENCE MITSUI 2007

Surface Roughness, Rz

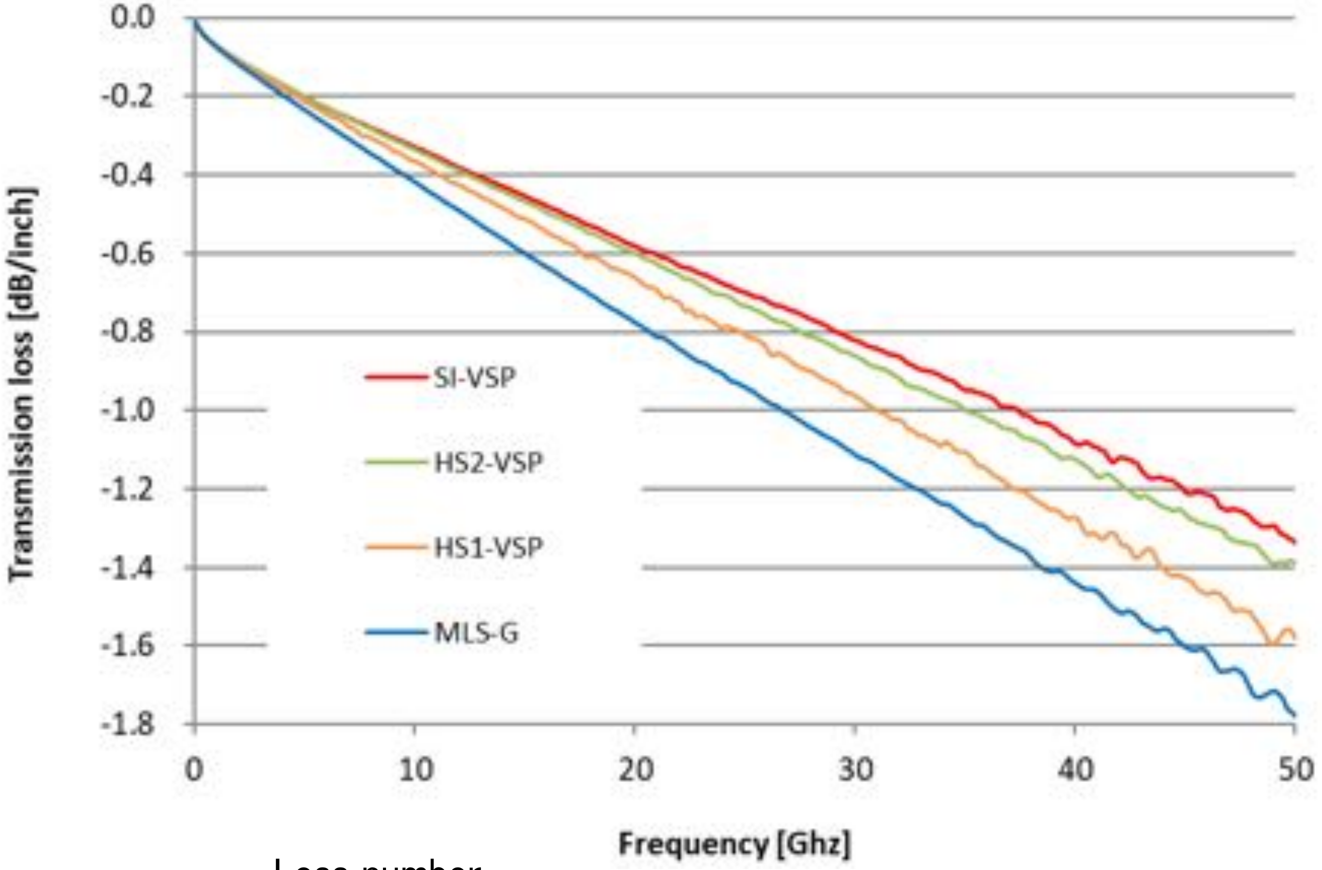
	MLS-G	MLS-G3	HS-VSP	HS1-VSP	HS2-VSP	SI-VSP
Base copper	3.2um  1.3um (Drum side)	3.2um  1.3um (Drum side)	1.3um (Drum side)  0.5um	1.3um (Drum side)  0.5um	1.3um (Drum side)  0.5um	1.3um (Drum side)  0.5um
After treated copper	 2.5um	 1.3um	 1.8um	 1.3um	 0.8um	 0.5um
Bonding side SEM image						

Transmission Loss

Dielectric : Low loss Prepreg 136um, Dk 3.08, Df 0.0027
Cu thickness : 18 μ m Impedance : 50 Ω
Measurement mode : Microstrip Line / Single


Line 300μm

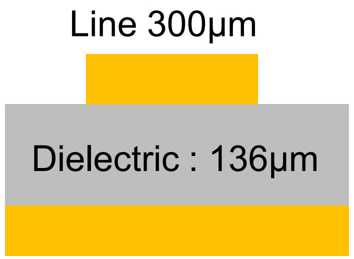
Dielectric : 136μm

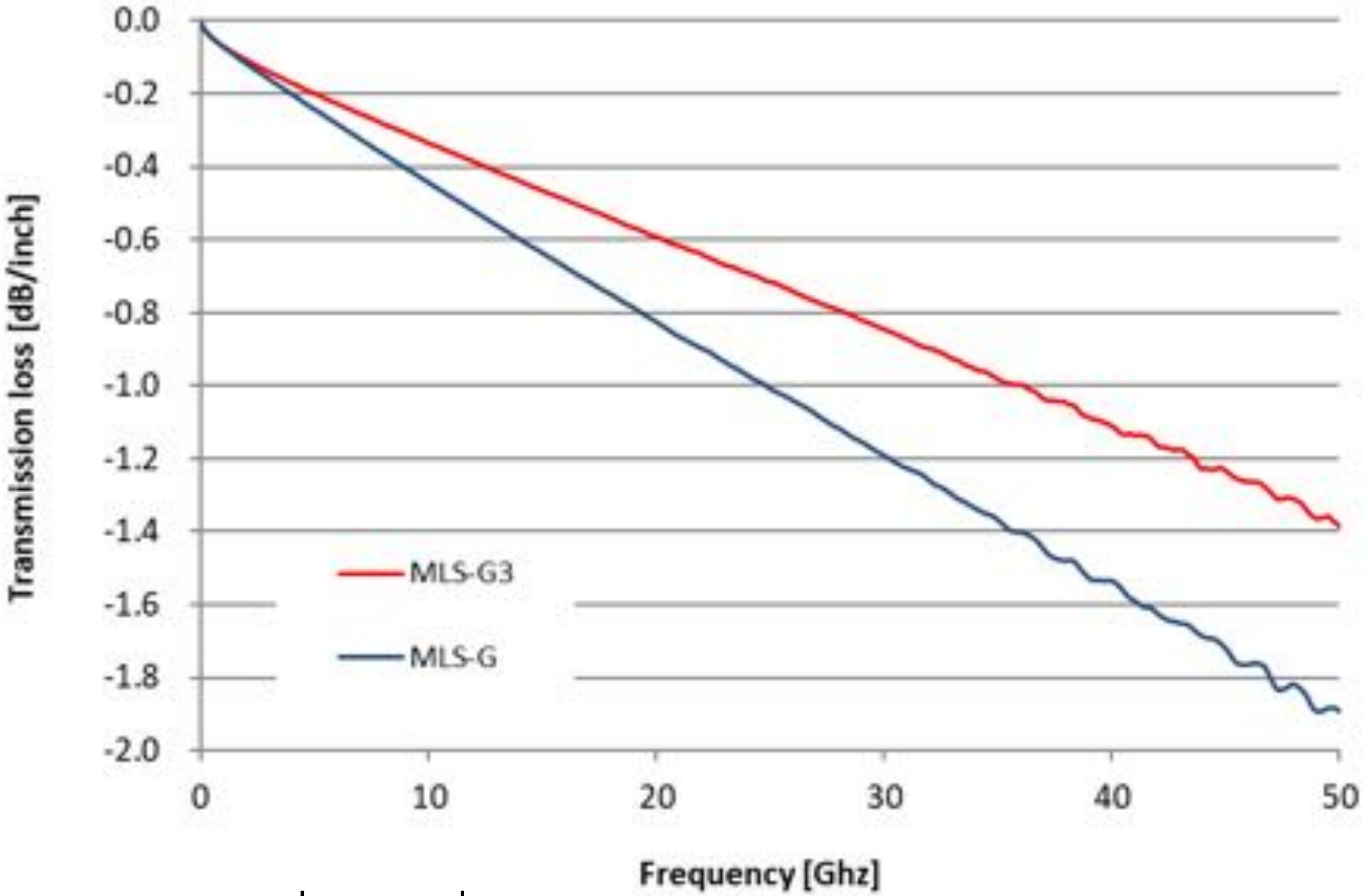


Loss number
(Good) SI-VSP < HS2-VSP < HS1-VSP < MLS-G (Bad)

Transmission Loss of RTF

Dielectric : Low loss Prepreg 136um, Dk 3.08, Df 0.0027
Cu thickness : 18 μm Impedance : 50 Ω
Measurement mode : Microstrip Line / Single


Line 300µm
Dielectric : 136µm

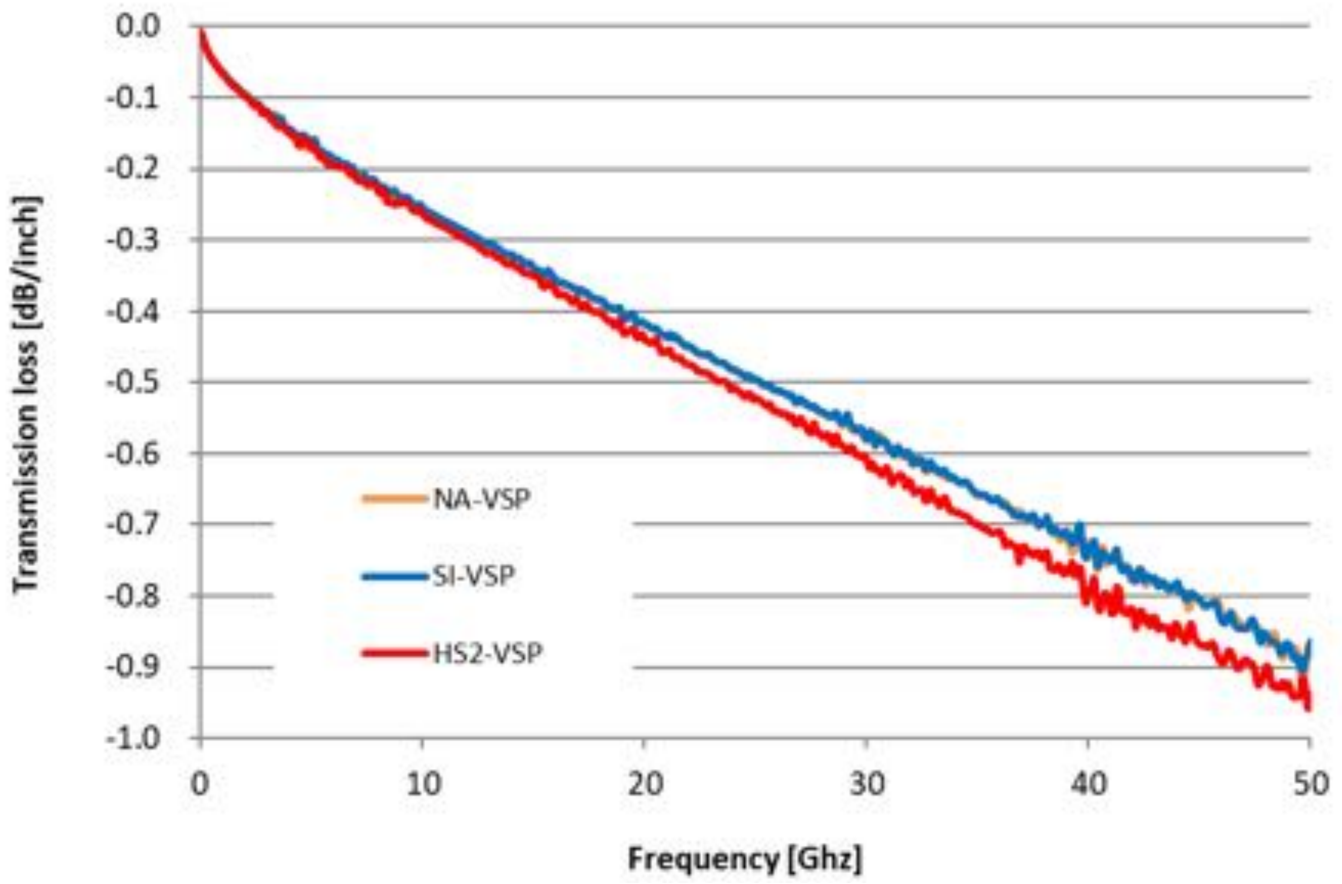


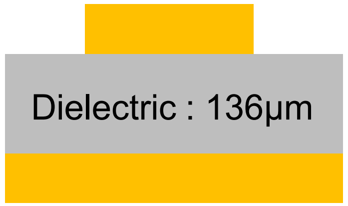
Loss number

(Good) MLS-G3 << MLS-G (Bad)

Transmission Loss, lowest profile copper comparisons

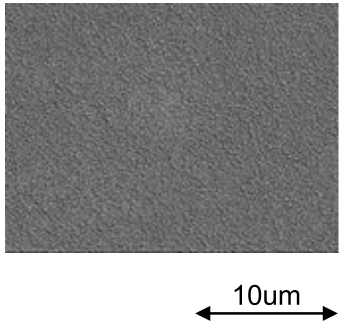
Dielectric : Low loss Prepreg 136um, Dk 3.4, Df 0.002
Cu thickness : 18µm Impedance : 50Ω
Measurement mode : Microstrip Line / Single





NA-VSP
= without nodule

SI-VSP



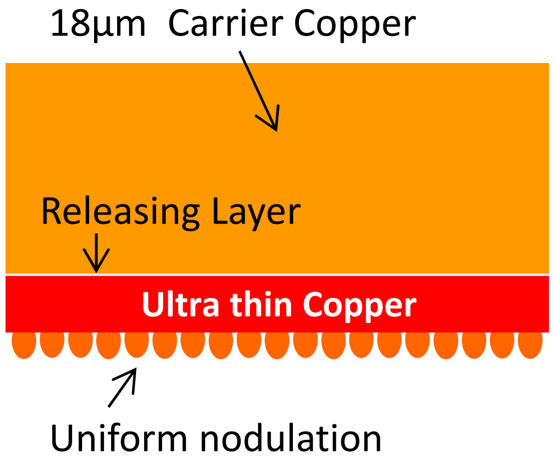
MicroThin and RF

Thin Copper in RF Applications

Useable for very fine pitch pattern under L/S=30/30µm formation by MSAP*.

*MSAP: Modified Semi-Additive Process

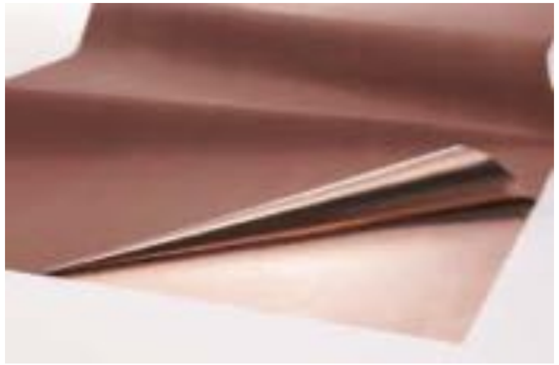
MicroThin™



Variations		Surface roughness [µm]	Target L/S by MSAP	Thickness [µm]			
				1.5	2	3	5
Standard	MT18SD-H	Rz 3.0	30/30µm			●	●
Low Profile	MT18Ex	Rz 2.0	25/25µm	●	●	●	●
Very Low Profile	MT18FL	Rz 1.3	15/15µm	●	●	●	

Thin Copper in RF Applications

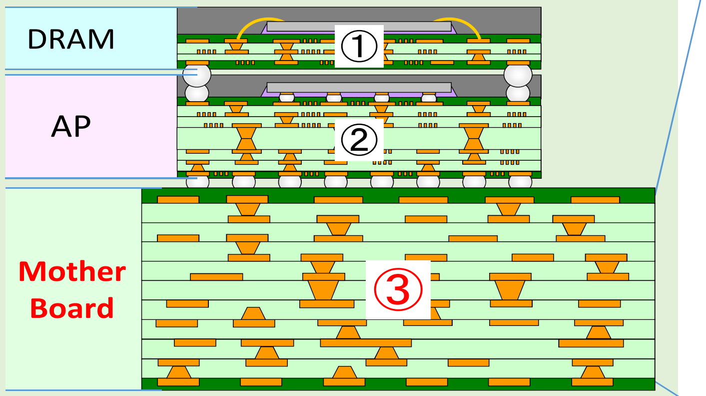
Coverage of MSAP has spread from IC substrate to Smartphone Motherboard



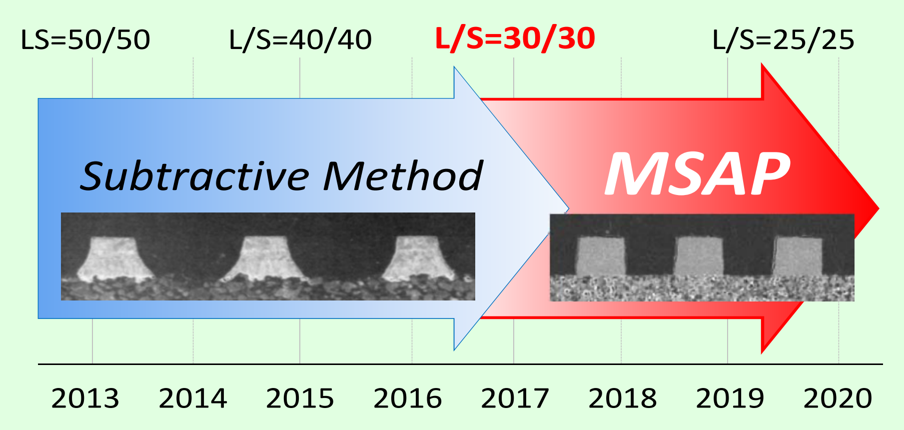
IC Substrate
- DRAM ①
- Application Processor ②

Smartphone Motherboard ③

【Cross section of Smartphone】



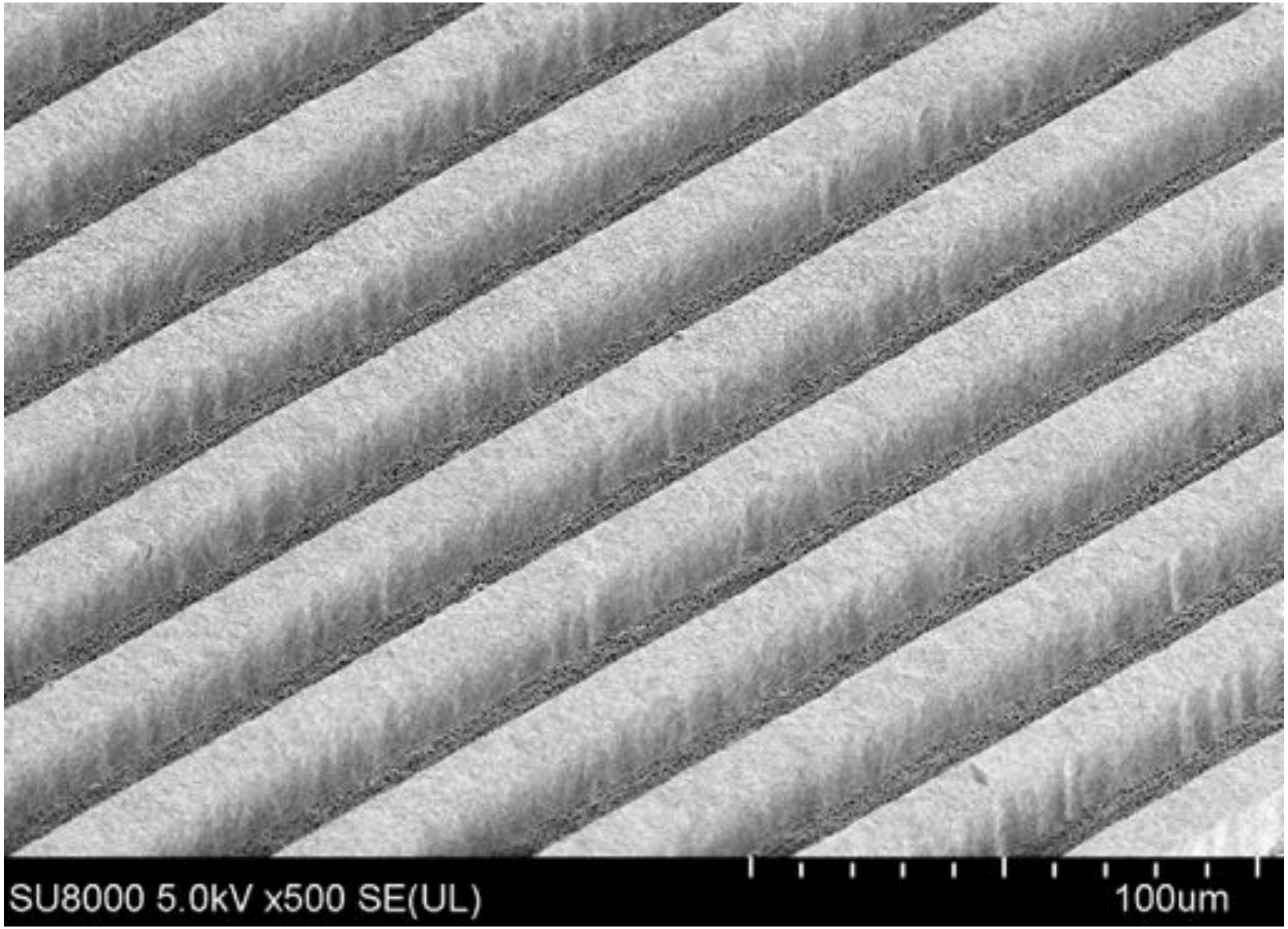
Change of patterning method on Mother Board



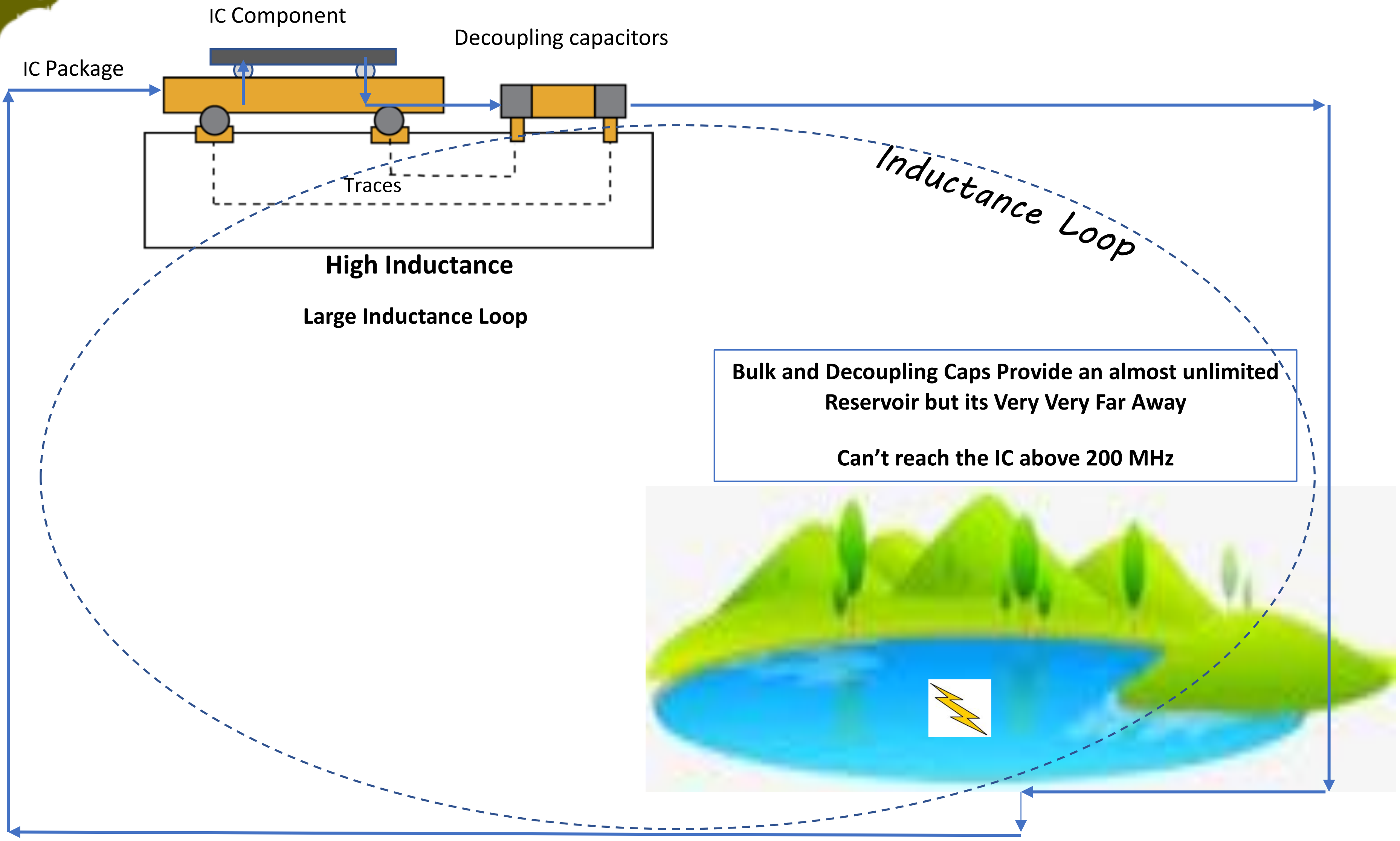
Reason for using MSAP for Smartphone Motherboard
- ✓ Miniaturization and densification of Mother Board to enlarge battery space.
- ✓ Narrower BGA ball pitch to improve the function of IC package
- ✓ Improvement of signal characteristics in high speed signal

MicroThin

SEM High Resolution Image/ 12 micron Lines and 12 micron Spaces



Embedded Capacitance and RF, PI, and EMC



High Inductance

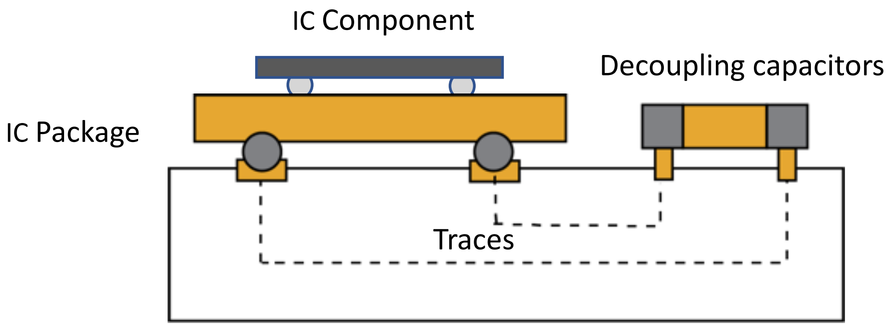
Large Inductance Loop

Bulk and Decoupling Caps Provide an almost unlimited Reservoir but its Very Very Far Away

Can’t reach the IC above 200 MHz

- Concept of Ultra Thin Embedded Capacitance Laminates

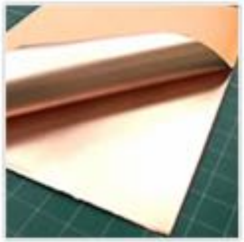
Traditional Surface Mount Decoupling capacitor design



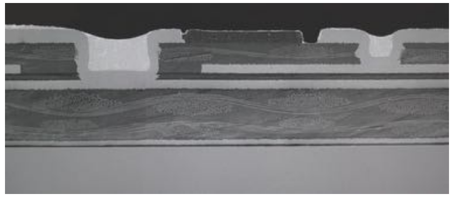
High Inductance

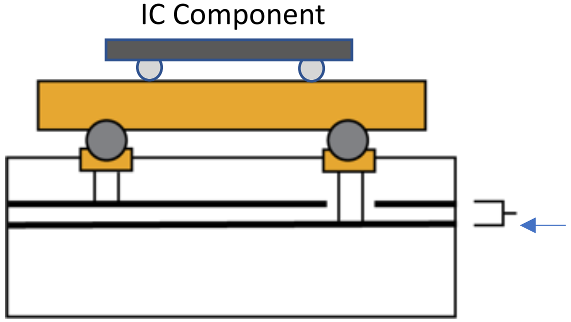
Instead you can do this

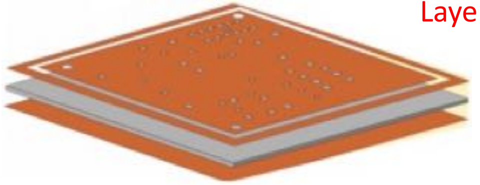
Embedded capacitor design



FaradFlex® laminate







Capacitance Layer

Low Inductance

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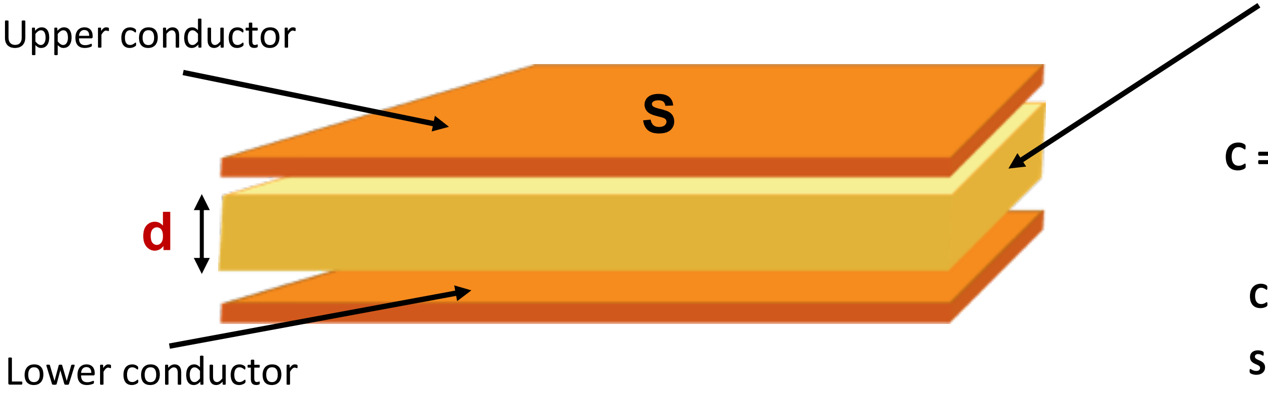
Why Embedded Capacitance and Thin Dielectrics?

- ❖ Better PDN (Power Delivery Network)
- ❖ More design space
- ❖ Low inductance
- ❖ Low impedance
- ❖ Reduced noise

- ❖ Lower Profile
- ❖ Can remove most 0.1µF and 0.01 µF decoupling capacitors
- ❖ Weight reduction
- ❖ Higher reliability
- ❖ In some designs better thermal transfer

• What is a Planar Capacitor?

Conductive plane pair with dielectric separation



Dielectric material: **D_k Dielectric Constant or Relative Permittivity ε_r**

$$C = \frac{K*D_k*S}{d}$$

C = Capacitance (Farads)

S = Area of plates

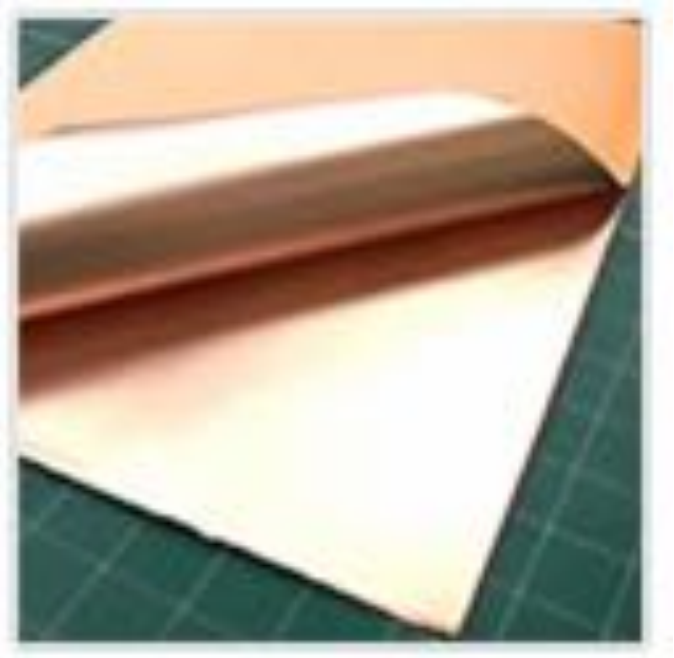
D_k = Dielectric constant of material between plates

K = Constant

d = Thickness between plates

EMBEDDED CAPACITANCE LAMINATE CONSIDERATIONS

When Designing the PCB: Two Factors That Determine Capacitance Of A Laminate



Dk of the Material- Dielectric Constant- Capacitance is directly proportional to the Dk
HIGHER Dk IS BETTER!

Thickness of the dielectric- Capacitance is inversely proportional to thickness
THINNER IS BETTER!

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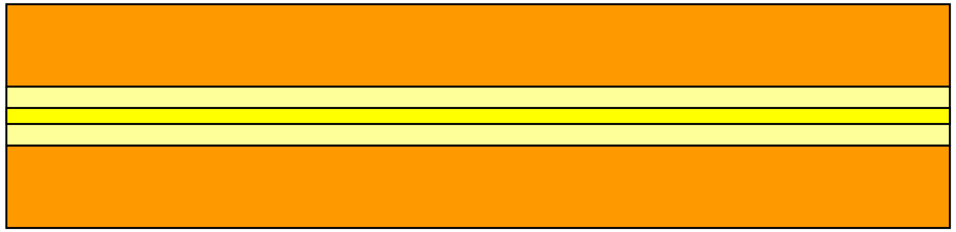
Embedded Capacitance Materials

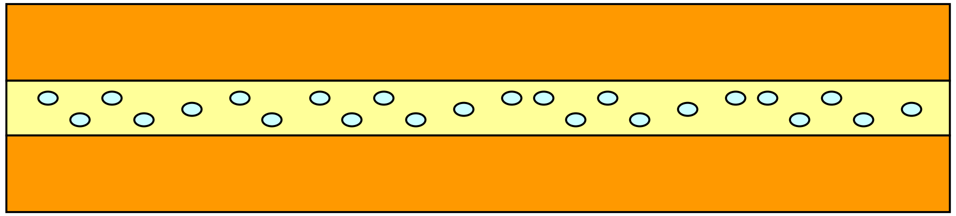
Types of Embedded Capacitance Laminate

Used in Shared Planar Applications

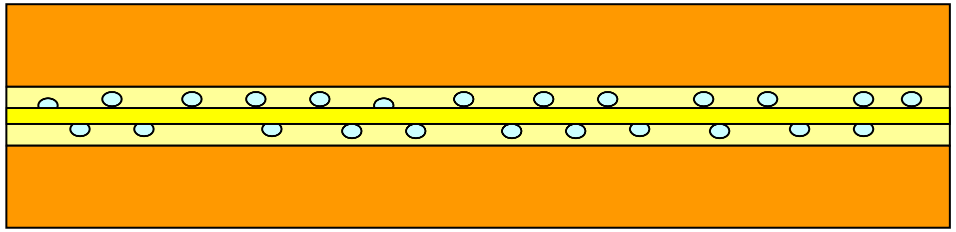
1. Polymer film and resin



2. Filled resin “non-supported”

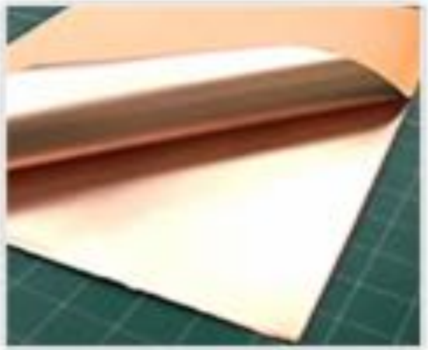


3. Polymer film with filled resin



Laminate constructed with:

- **Copper (from 2 oz to as thin as 3 micron)**
- **Epoxy or other type resin bonded to a high performance polymer film**
- **Thicknesses from 25 micron to as thin as 3 micron**
- **D_k from 3.5 to as high as 30**



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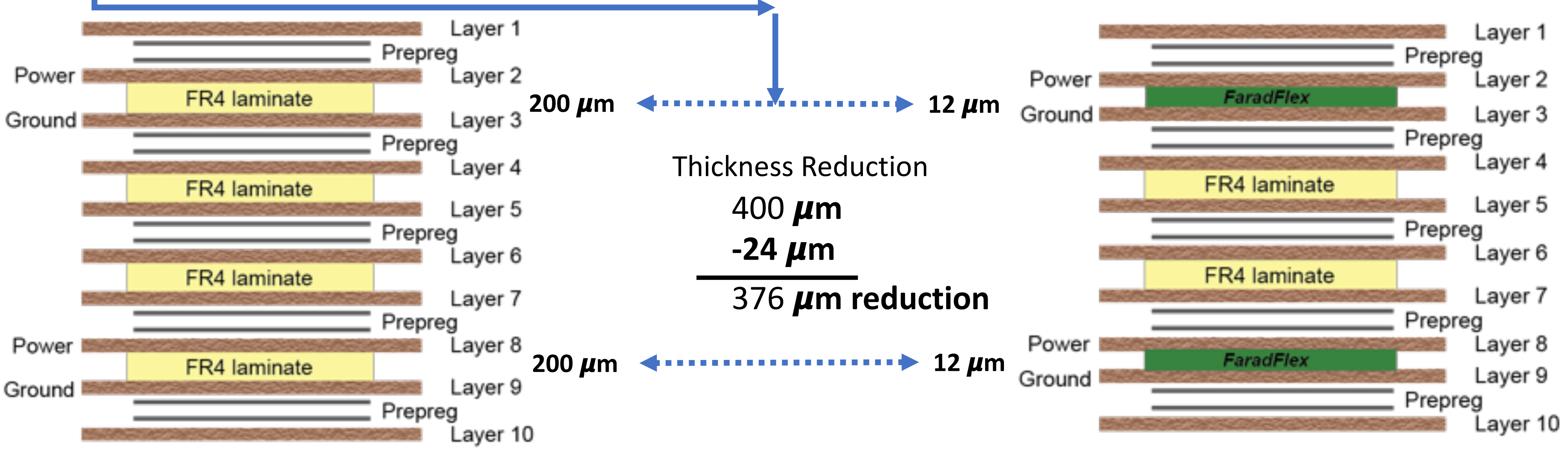
- Why Embedded Capacitance and Thin Dielectrics?

FaradFlex® is much thinner than other cores

Z-axis of the PCB can be reduced or more layers put in the same thickness

Replace existing power/ground layers with ***FaradFlex®***
for use as power distribution layer

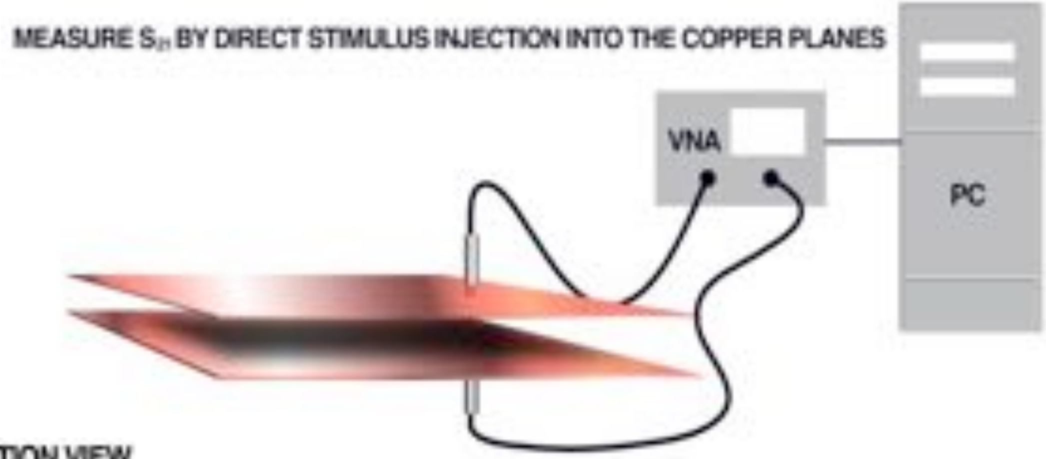
10 layer stack-up with 2 power-ground layers at **L2/L3** and **L8/L9** (using ***FaradFlex®*** in the power-ground allows for embedded capacitance)

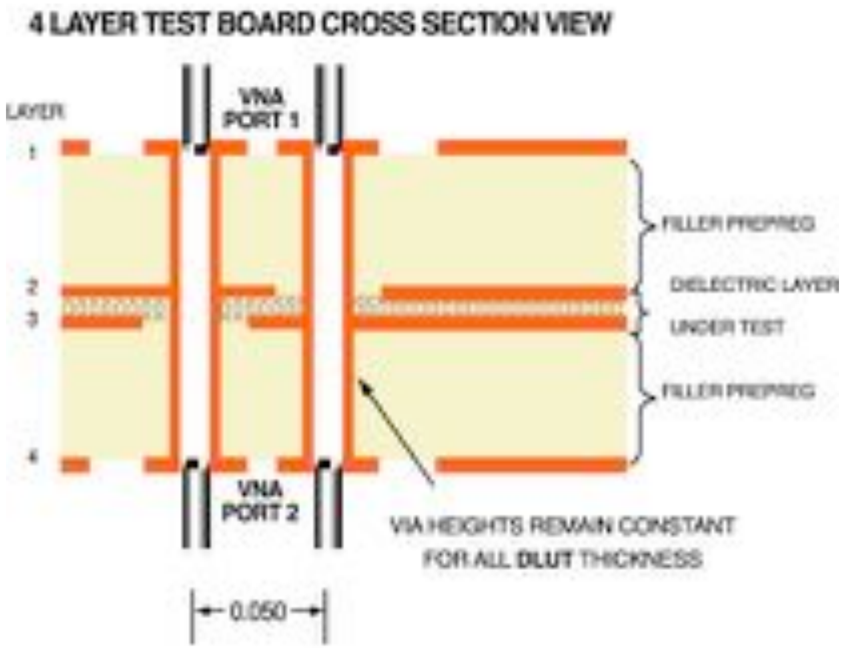


Thickness Reduction

$$\begin{array}{r} 400\ \mu m \\ -24\ \mu m \\ \hline 376\ \mu m \text{ reduction} \end{array}$$

- Bare Board Impedance Measurement





Courtesy of Oracle

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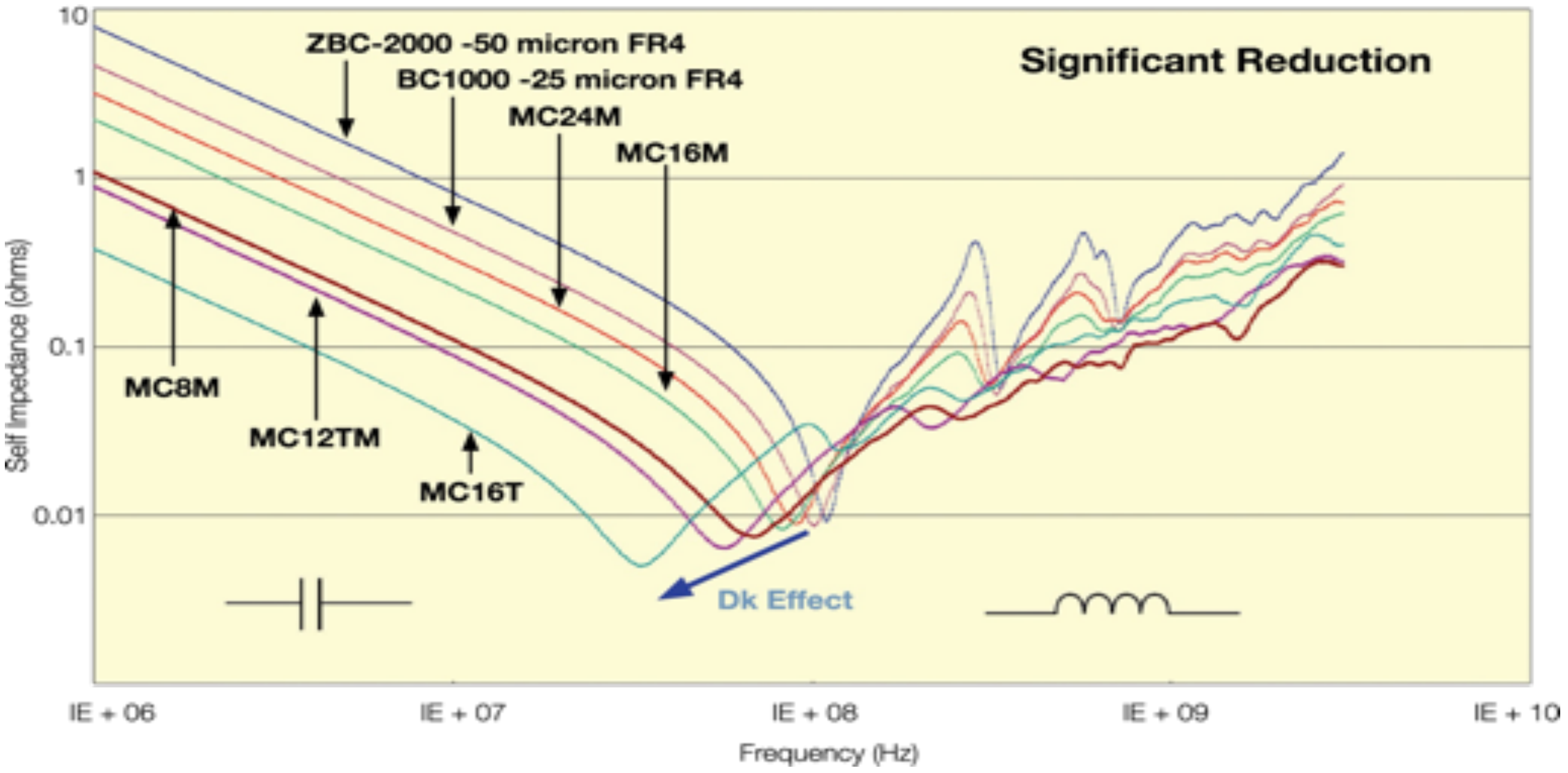
• PCB Electrical Performance

Discrete capacitors of 0.1µF have a resonance frequency of about 15 MHz
Discrete capacitors of 0.01µF have a resonance frequency of about 40 MHz



Thinner Dielectrics and
Higher Dk = Lower Impedance

Thinner Dielectrics =
Lower Impedance

Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
MC24M	40
MC8M	124
MC12TM	180
MC16T	440

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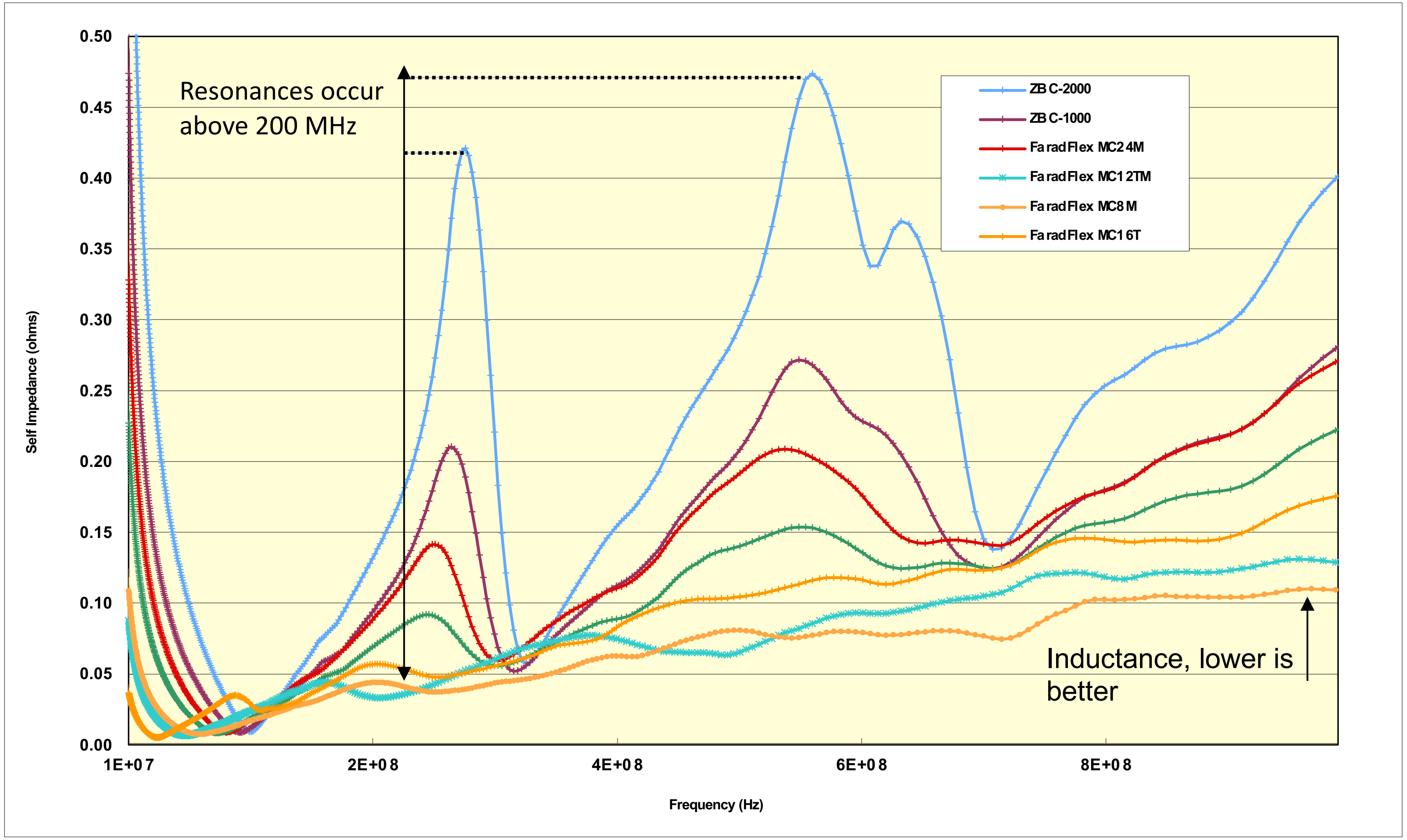
• PCB Electrical Performance (Up to 1 GHz)



Resonances occur above 200 MHz

Inductance, lower is better

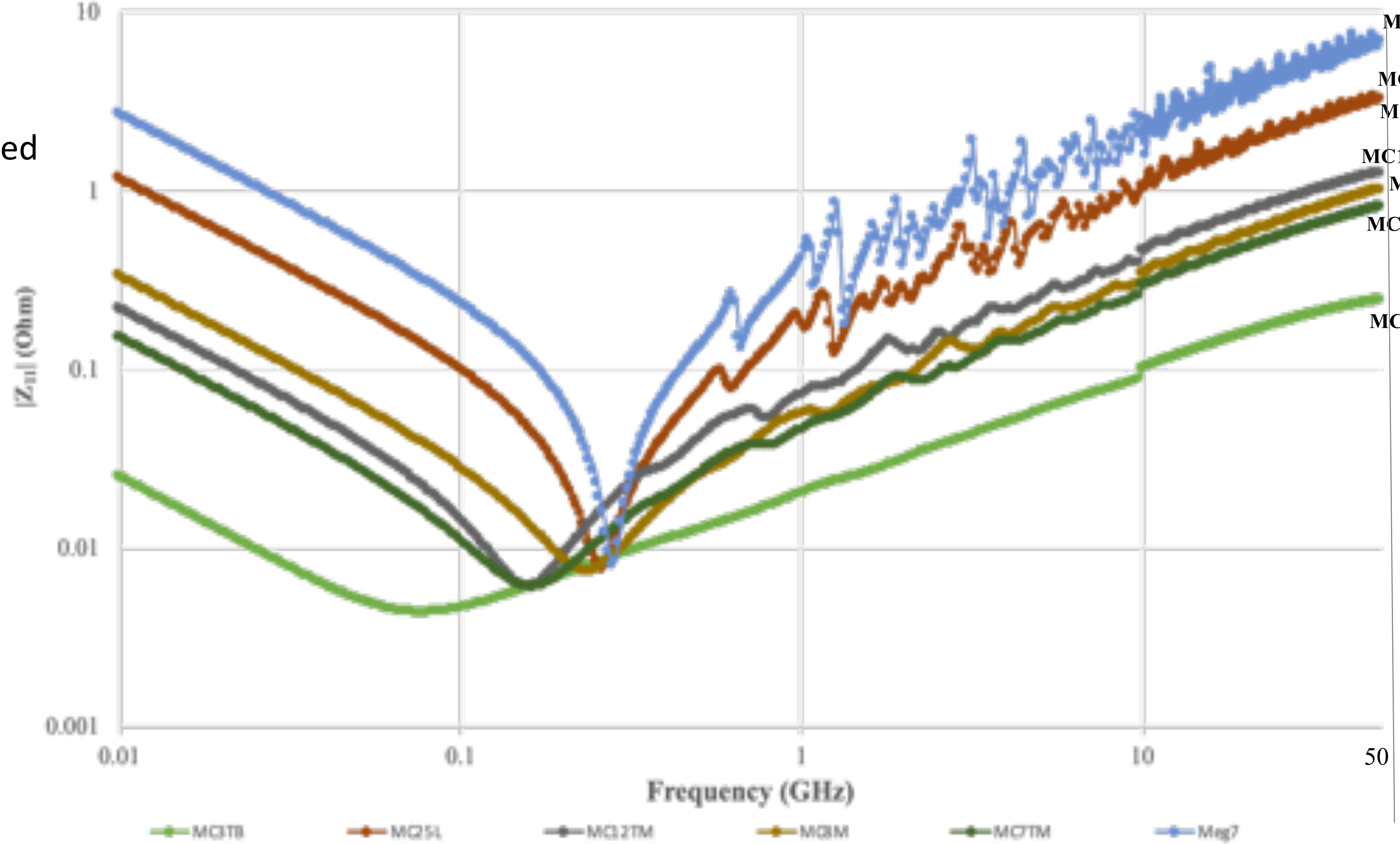
Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
MC24M	40
MC8M	124
MC12TM	180
MC16T	440

FARADFLEX®
OAK-MITSUI TECHNOLOGIES

PCB Electrical Performance (Up to 50 GHz, simulated)

PI Improved



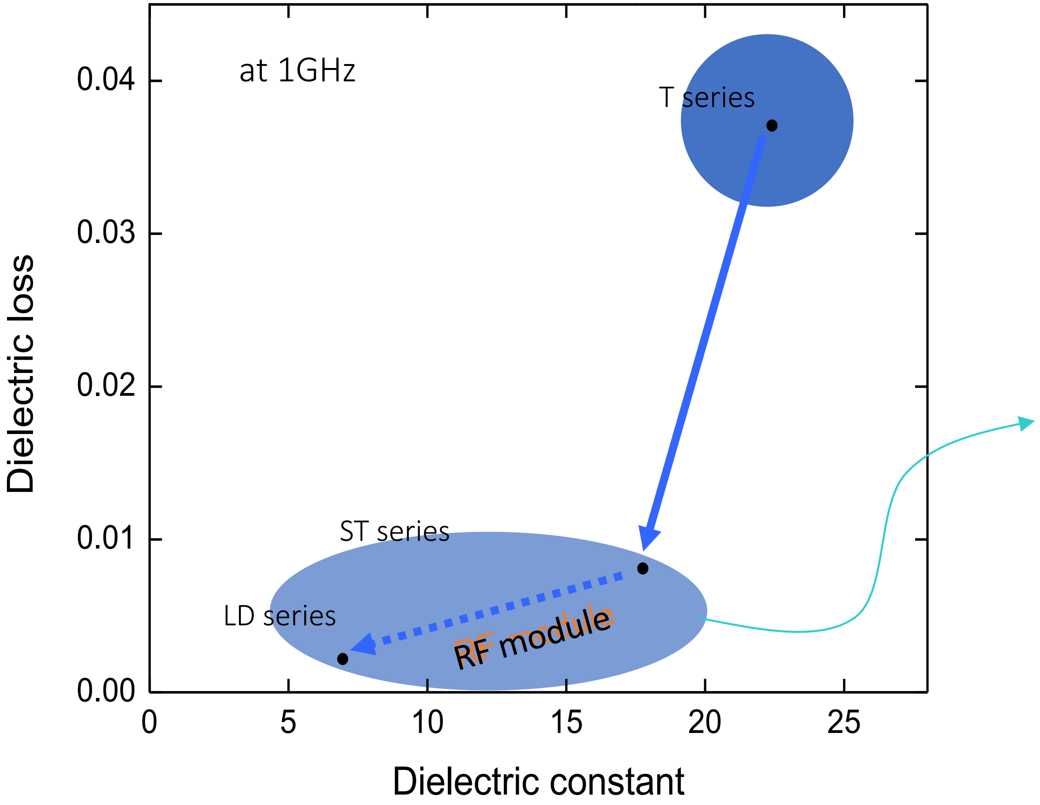
Meg 7	50 micron
MC25L	25 micron
MC24M	22 micron
MC12TM	12 micron, high Dk
MC8M	8 micron,
MC7TM	7 micron, high Dk
MC3TB	3 micron, high Dk

Thinner is Better!

Lower Inductance
Lower resonance

Embedded Capacitance Materials for RF

High DK and/ or Low Df



Main application:

→ LPF, BPF, Diplexer

→ RF module

Fig. 1. Low dielectric loss (DF) FaradFlex, “ST” & “LD” series for RF module

Dk & DF vs Frequency (1 GHz – 10 GHz)

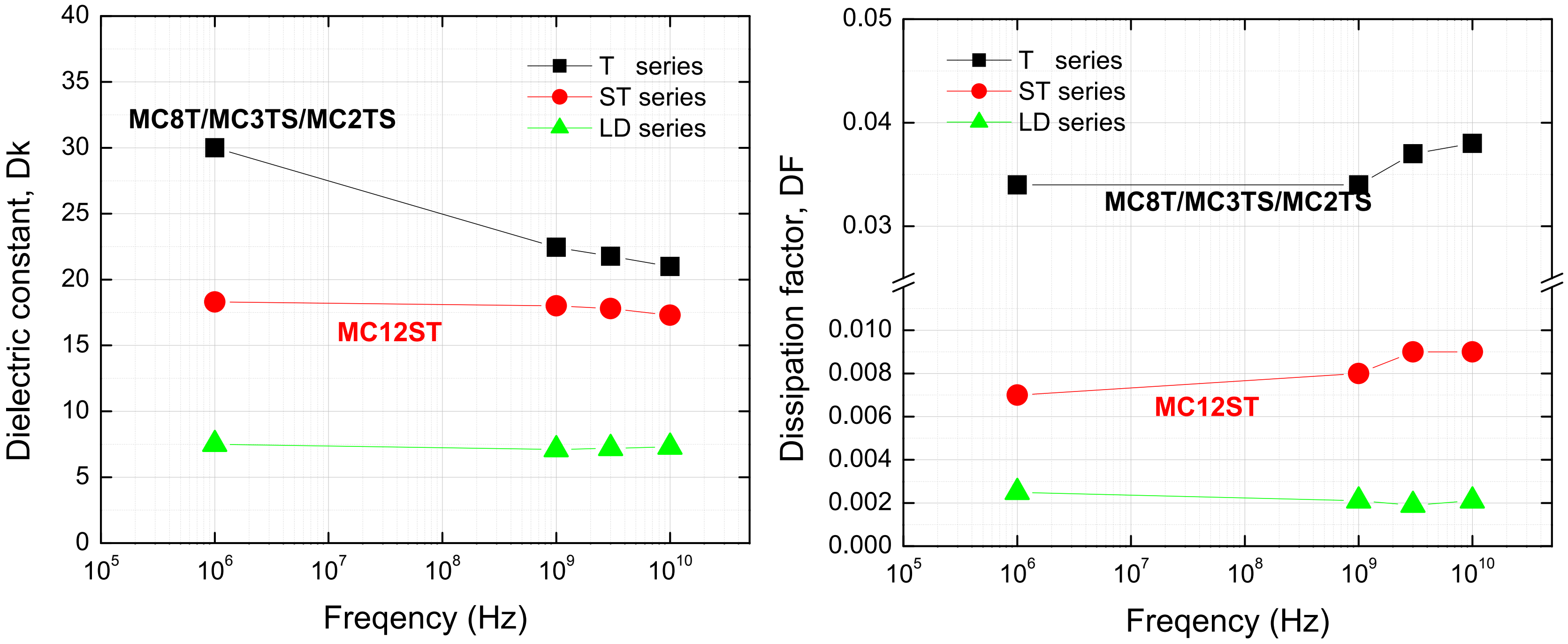
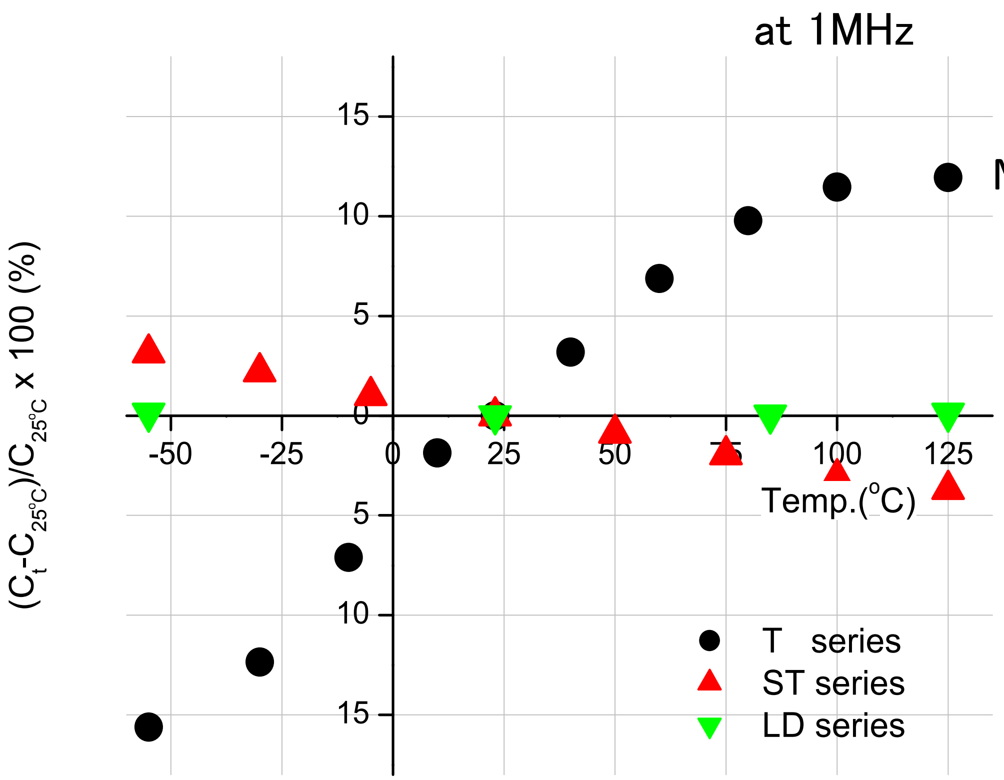


Fig. Dk and DF vs frequency at GHz of FaradFlex materials

Embedded Capacitance Materials and RF

Temperature Dependence of Capacitance



MC8T/MC3TB

MC12LD improved temperature stability

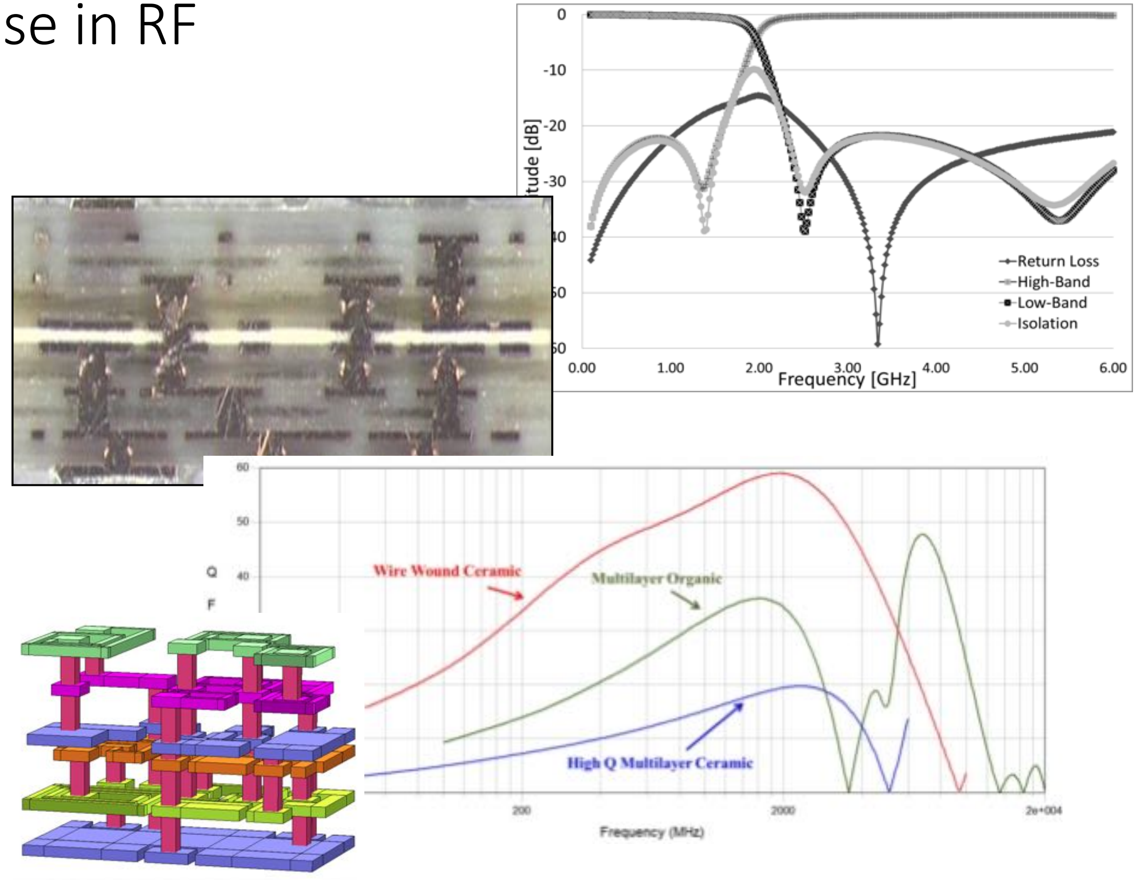
MC12ST

Embedded Capacitance for RF

Low Loss MC12LD for use in RF

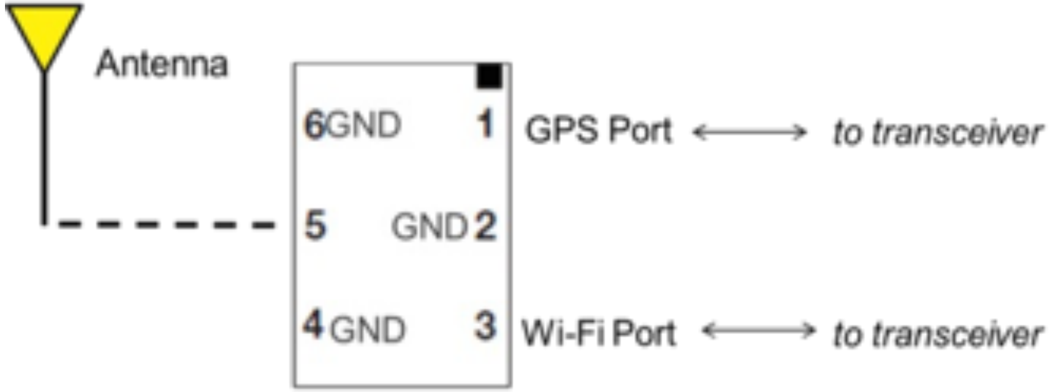
For use in:

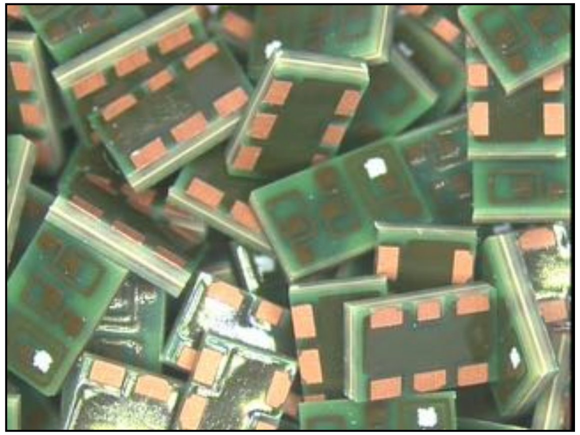
- Inductors
- Diplexers
- Capacitors
- Filters



Diplexer

- A device containing 2 RF filters and one I/O port.
- Enables 2 RF transceivers to operate on 1 RF antenna.

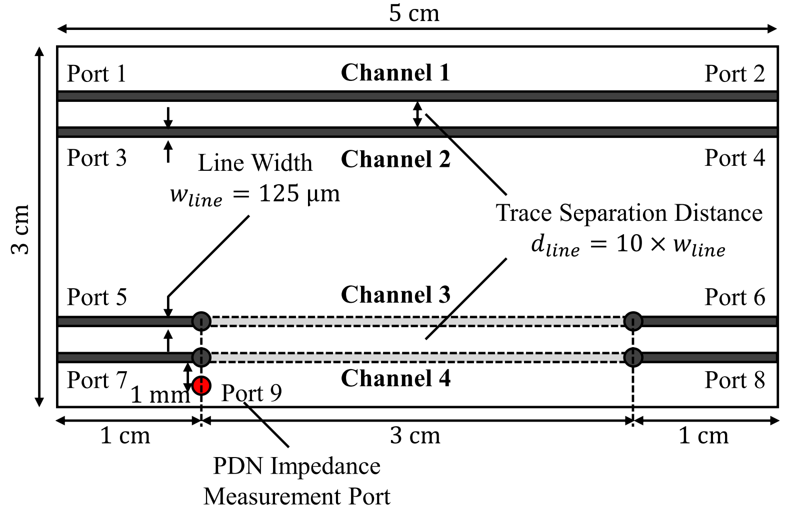


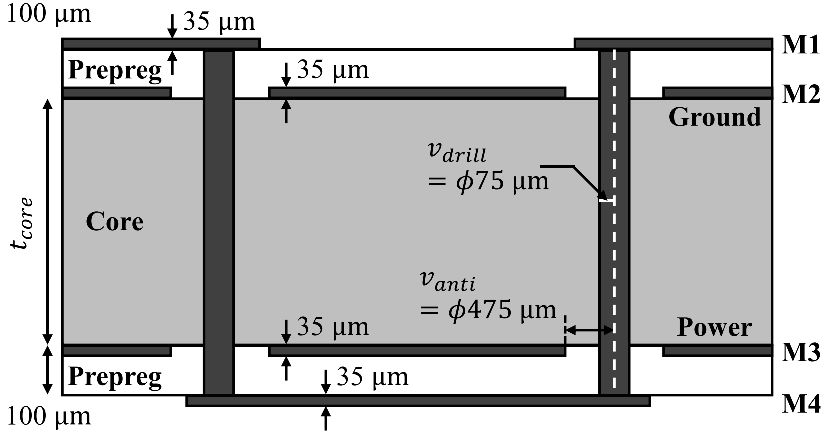


Important Parameters

- Low insertion loss at each center frequency.
- High rejection of out of band frequencies.
- Size.

Cross Talk- Impact on High Speed Signaling

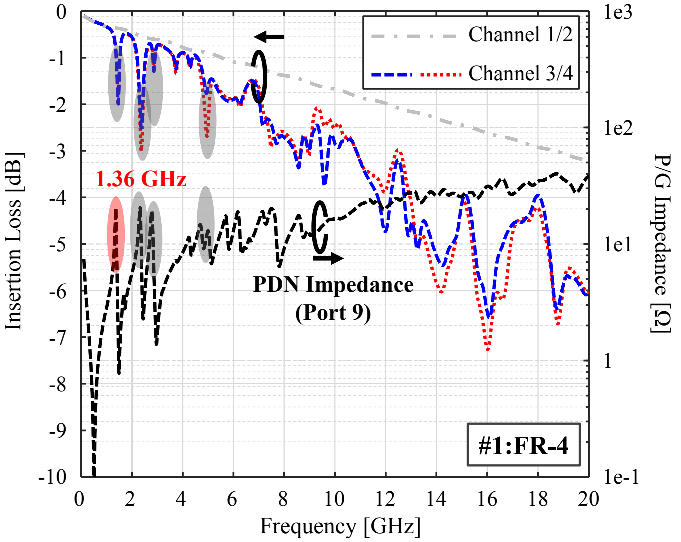


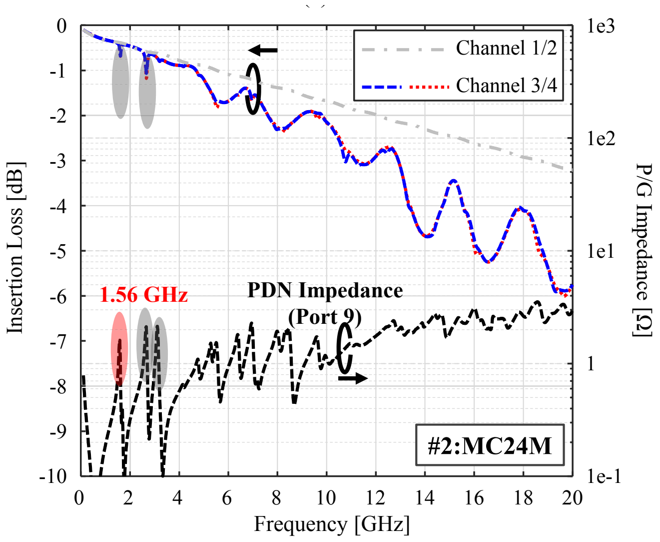


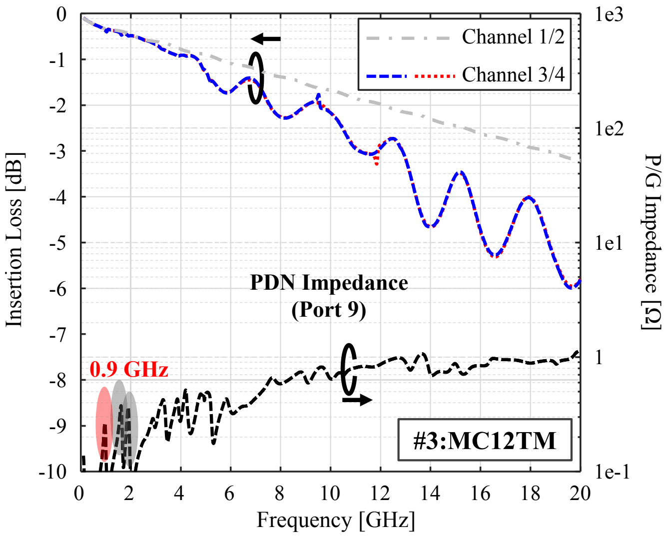
	#1	#2	#3
Name	FR-4	MC24M	MC12TM
Thickness t_{core}	300 **µm**	24 **µm**	12 **µm**
Relative Permittivity ε_r (@ 1 GHz)	4.4	3.5	9.5
Loss Tangent $\tan\delta$ (@ 1 GHz)	0.020	0.016	0.020

Permission from Taiki Kitazawa, Nara Institute of Science and Technology, Graduate School of Information Science

Cross Talk- Impact on High Speed Signaling







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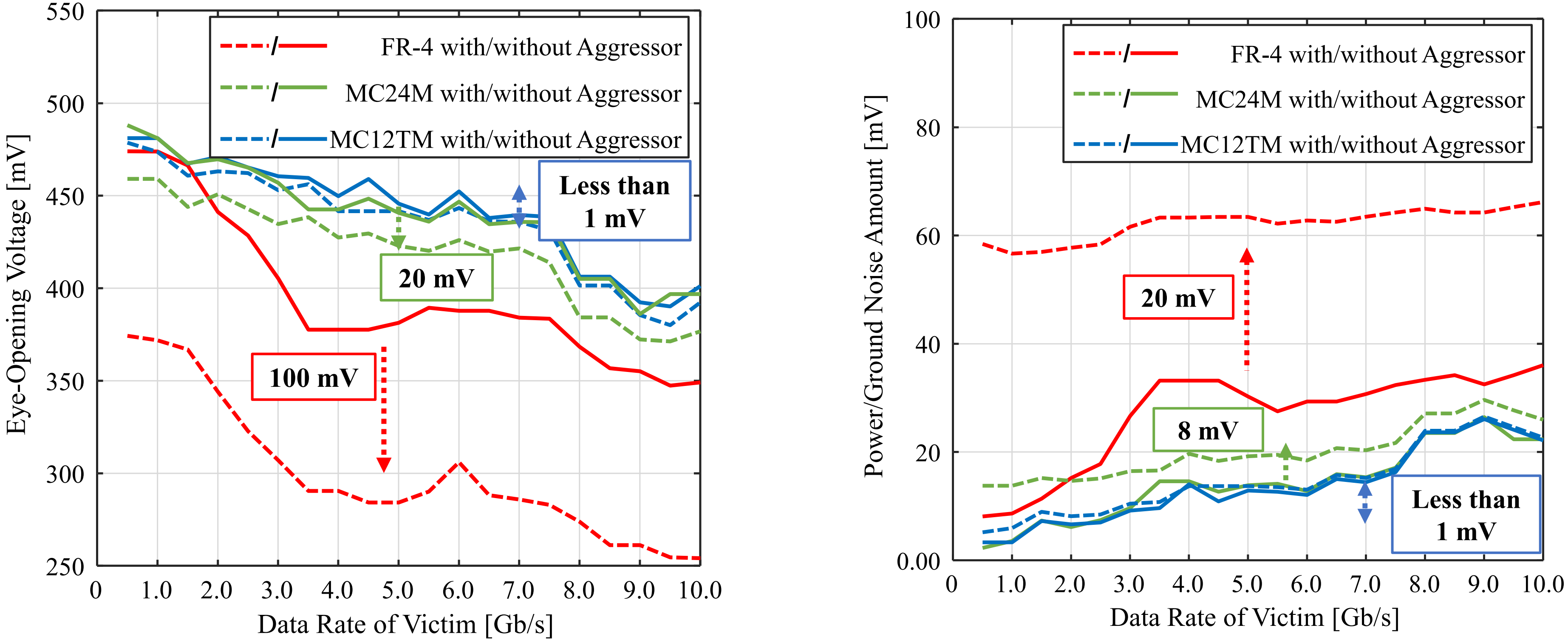
Cross Talk- Impact on High Speed Signaling

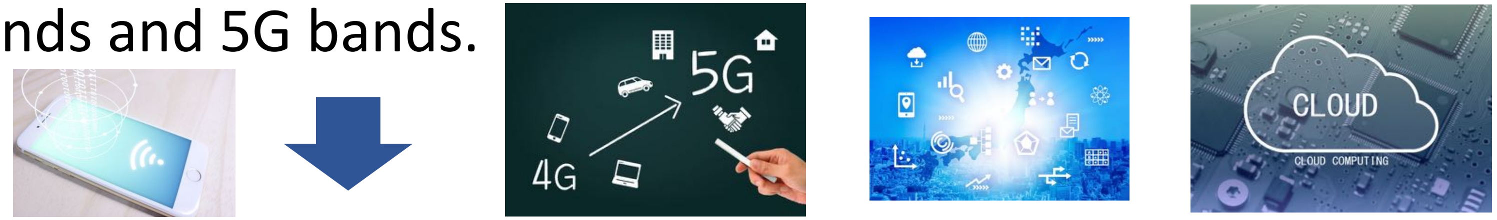


Permission from Taiki Kitazawa, Nara Institute of Science and Technology, Graduate School of Information Science

- Background

Technical Background

- EMI problems are getting more critical as frequency goes higher and higher.
- IoT devices are getting smaller, so resonance frequency from PDN becomes higher.
- This would affect Wi-Fi bands and 5G bands.

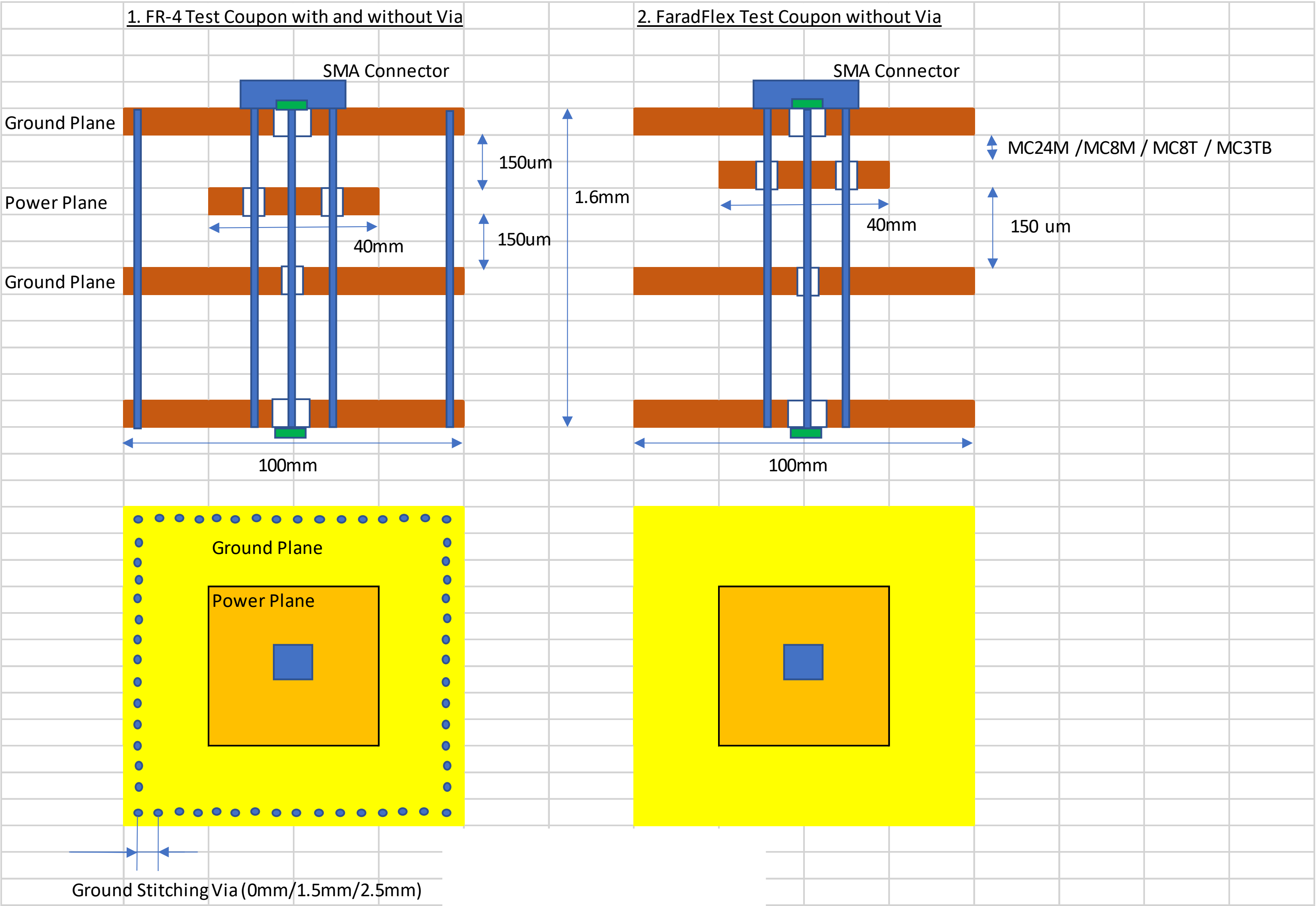


- Sometimes, ground stitching via or edge plating is used to mitigate EMI from PDN.
- But these solutions would end up with cost increase.
- Also for higher frequency, it won’t work well due to via pitch limitation.

Research Theme

- ➢ Find a solution for mitigating higher frequency EMI using high Dk material for PDN.
- ➢ Find if we could eliminate stitching via and edge plating with high Dk material.

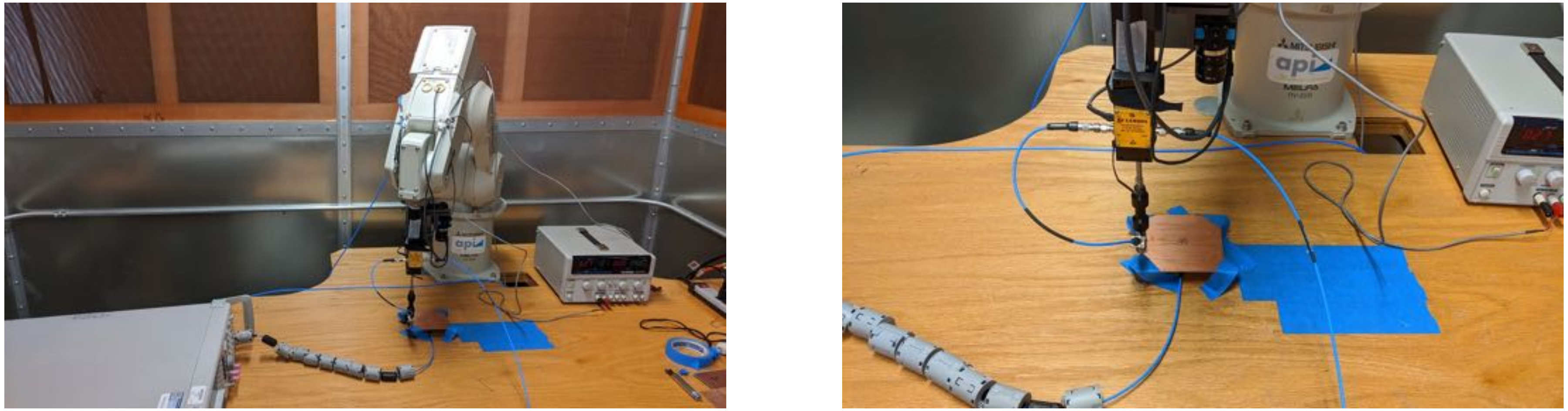
Stack-ups: Via Stitch versus Embedded Capacitance



Near Field EMI Measurements (study removing via stitch from design by replacing with embedded capacitance)

Test Equipment:

1. Near-field EMI Scanner (SmartScan 350 from API) with Ez Probe
2. Signal Generator (Anritsu 68369A)
3. Spectrum Analyzer (Anritsu MS2760A)

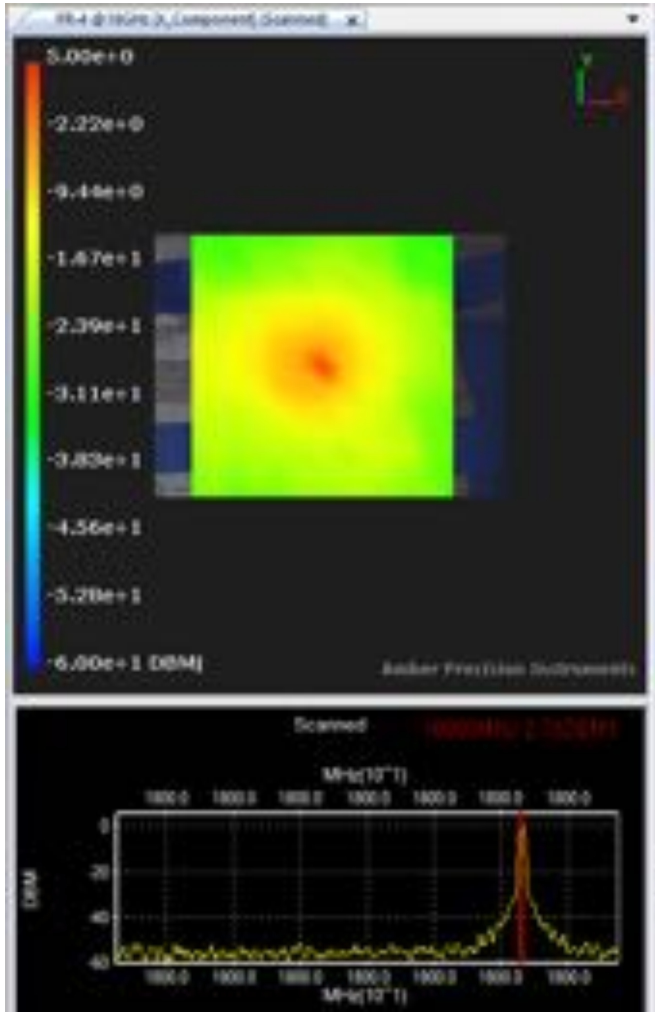


Test Condition:

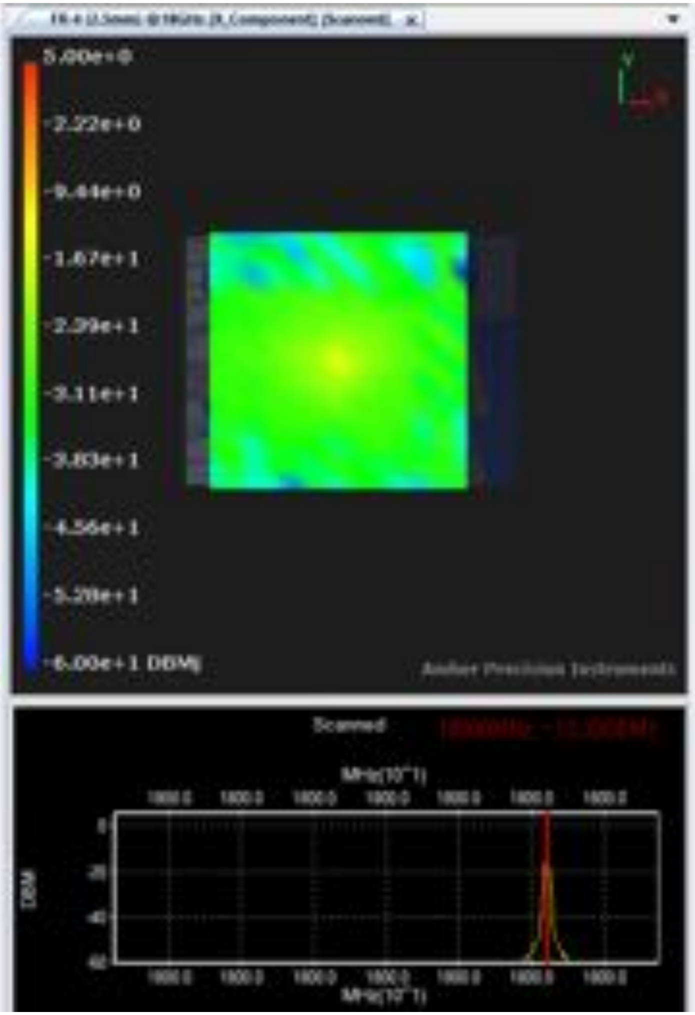
1. Scan Frequency : 500MHz/1GHz/6GHz/18GHz/40GHz
2. Output Power : 15dBm@500MHz/10dBm@1GHz/7dBm@6-40GHz

18GHz Measurement Results

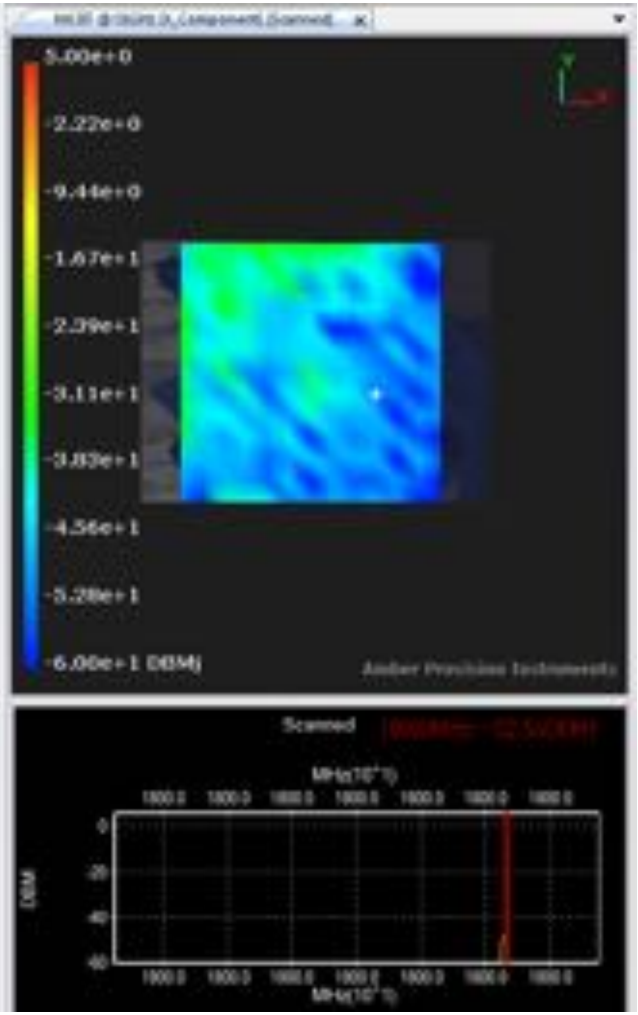
FR-4 (No Via)



FR-4 (2.5mm Pitch Via)



MC8T (No Via)



Near-field Measurement Result Summary

Material	500MHz	1GHz	6GHz	18GHz	40GHz
FR-4 (No Via)	-51.24	-63.32	-41.03	2.76	-38.29
FR-4 (2.5mm Pitch Via)	-56.38	-68.8	-47.45	-13.33	-44.11
MC8M (No Via)	-66.24	-67.44	-48.44	-25.01	-47.74
MC8T (No Via)	-66.27	-68.93	-51.05	-31.26	-59.28

Thank You!

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www.faradflex.com