PCB 3.0

What does the future hold?

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The Future

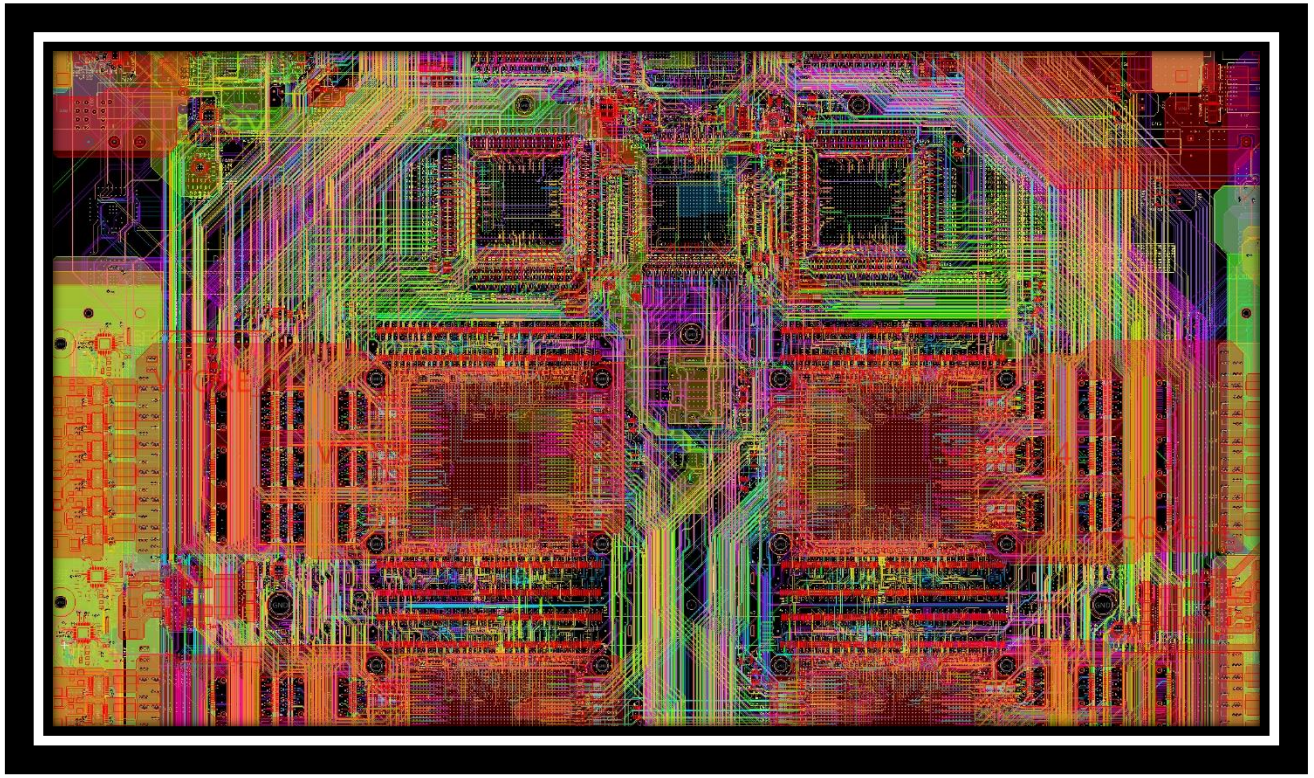
Who am I…and why am I giving this talk?

PCB 1.0 The bad ole days

PCB 2.0 The here and now

- What is PCB 2.0
  - The act of putting together a 3D puzzle bound by Time, Physics and Manufacturing limitations.

And yes, it is ART



Palladium Z1

PCB 2.0 Short Cummings

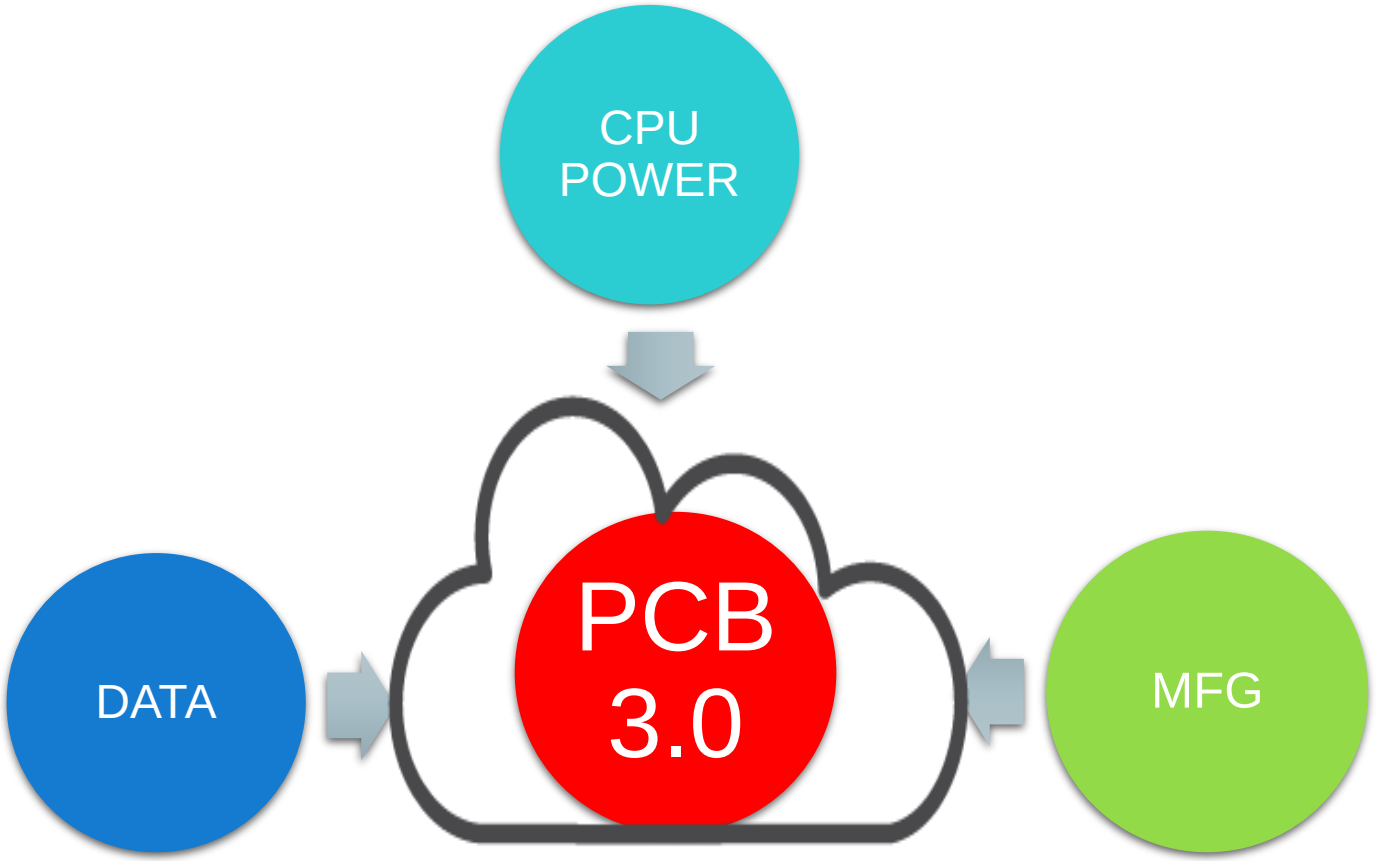
- Design Change
  - ECO’s and parallel design is a way of life
- Supply Chain Woo's
  - They are a challenge…and they are ALWAYS present
- PCB ROT (Rule of Thumb) and Dogma
  - We compensate for lack of simulation by ROT and Dogma
- Time to Market
  - Never enough time…

Measuring the risk

$$\textbf{RISK} = \frac{\textbf{((Design Changes)2*(Team Size)) + (Coffee Intake and Lack of Sleep)}}{\textbf{Quoted Time Factor}}$$

Welcome to PCB 3.0

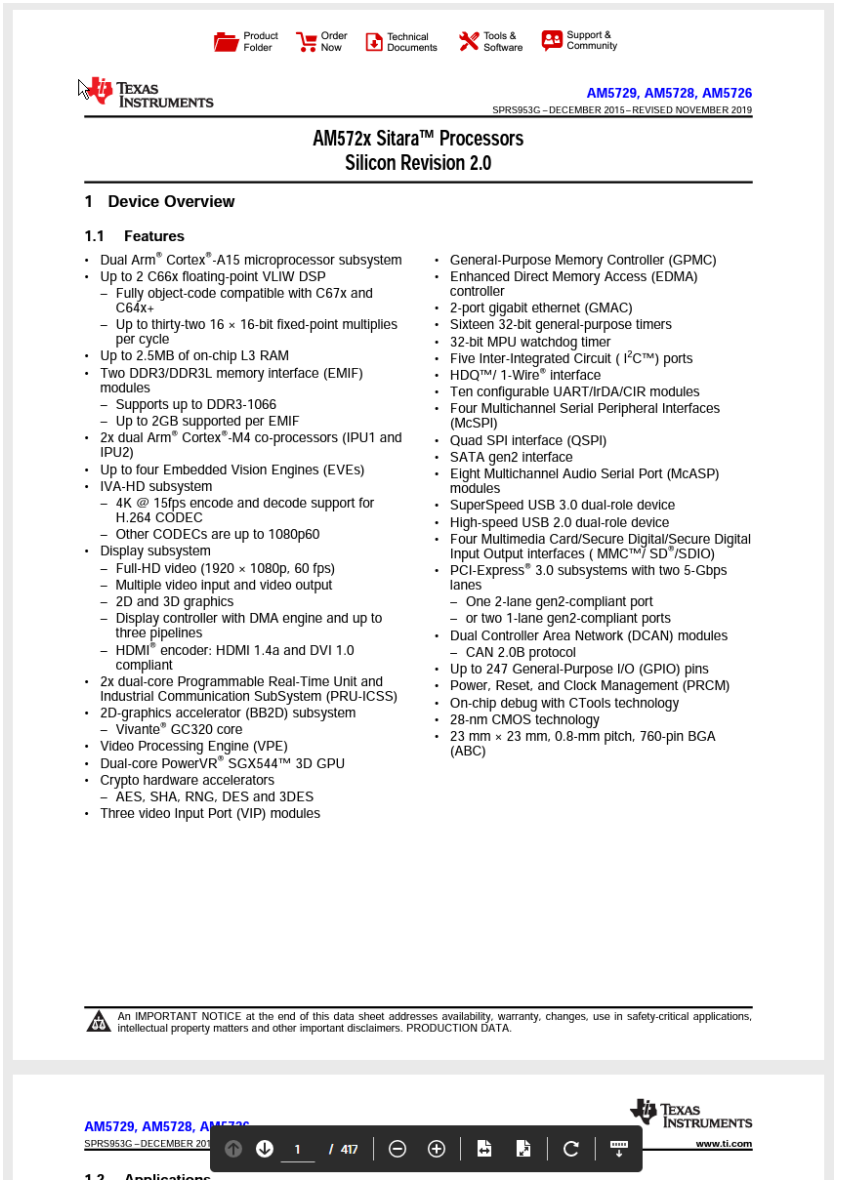
- Like many evolutions, there are several things that need to come together.



DATA

Datasheet

- Datasheet, it all starts here
  - Standardized Digitized format that our tools can digest quickly
  - Give the electrical/thermal/power requirements NOT physical space and trace



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TEXAS INSTRUMENTS

AM5729, AM5728, AM5726

SPRS953G – DECEMBER 2015 – REVISED NOVEMBER 2019

AM572x Sitara™ Processors
Silicon Revision 2.0

1 Device Overview

1.1 Features

- Dual Arm® Cortex®-A15 microprocessor subsystem
- Up to 2 C66x floating-point VLIW DSP
  - Fully object-code compatible with C67x and C64x+
  - Up to thirty-two 16 × 16-bit fixed-point multiplies per cycle
- Up to 2.5MB of on-chip L3 RAM
- Two DDR3/DDR3L memory interface (EMIF) modules
  - Supports up to DDR3-1066
  - Up to 2GB supported per EMIF
- 2x dual Arm® Cortex®-M4 co-processors (IPU1 and IPU2)
- Up to four Embedded Vision Engines (EVEs)
- IVA-HD subsystem
  - 4K @ 15fps encode and decode support for H.264 CODEC
  - Other CODECs are up to 1080p60
- Display subsystem
  - Full-HD video (1920 × 1080p, 60 fps)
  - Multiple video input and video output
  - 2D and 3D graphics
  - Display controller with DMA engine and up to three pipelines
  - HDMI® encoder: HDMI 1.4a and DVI 1.0 compliant
- 2x dual-core Programmable Real-Time Unit and Industrial Communication SubSystem (PRU-ICSS)
- 2D-graphics accelerator (BB2D) subsystem
  - Vivante® GC320 core
- Video Processing Engine (VPE)
- Dual-core PowerVR® SGX544™ 3D GPU
- Crypto hardware accelerators
  - AES, SHA, RNG, DES and 3DES
- Three video Input Port (VIP) modules
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) controller
- 2-port gigabit ethernet (GMAC)
- Sixteen 32-bit general-purpose timers
- 32-bit MPU watchdog timer
- Five Inter-Integrated Circuit (I²C™) ports
- HDQ™/ 1-Wire® interface
- Ten configurable UART/IrDA/CIR modules
- Four Multichannel Serial Peripheral Interfaces (McSPI)
- Quad SPI interface (QSPI)
- SATA gen2 interface
- Eight Multichannel Audio Serial Port (McASP) modules
- SuperSpeed USB 3.0 dual-role device
- High-speed USB 2.0 dual-role device
- Four Multimedia Card/Secure Digital/Secure Digital Input Output interfaces (MMC™/ SD®/SDIO)
- PCI-Express® 3.0 subsystems with two 5-Gbps lanes
  - One 2-lane gen2-compliant port
  - or two 1-lane gen2-compliant ports
- Dual Controller Area Network (DCAN) modules
  - CAN 2.0B protocol
- Up to 247 General-Purpose I/O (GPIO) pins
- Power, Reset, and Clock Management (PRCM)
- On-chip debug with CTools technology
- 28-nm CMOS technology
- 23 mm × 23 mm, 0.8-mm pitch, 760-pin BGA (ABC)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

AM5729, AM5728, AM572...

SPRS953G – DECEMBER 201...

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1.2 Applications

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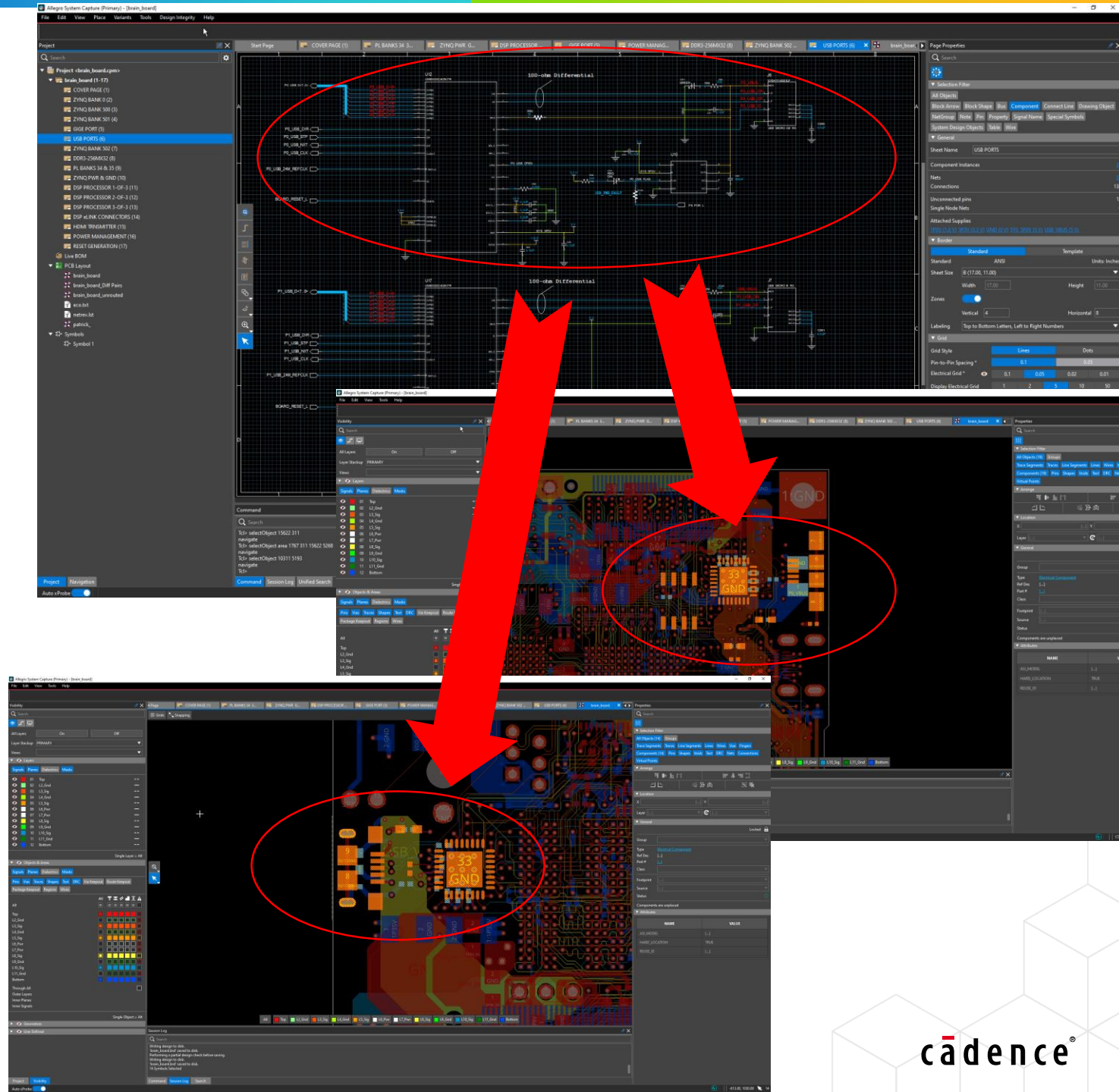
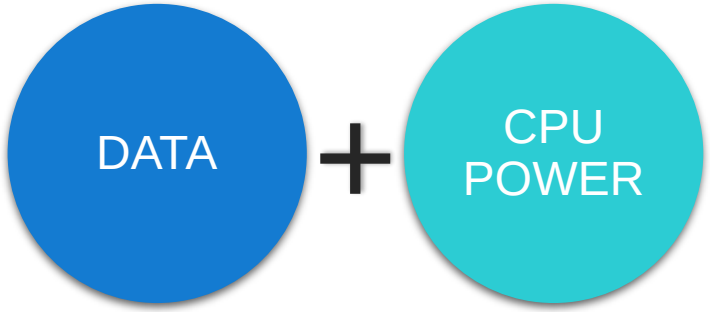
DATA

Intelligent Re-use

- Mining the data we have
  - Design Block
    - Defined by previous Schematics, Think G-Mail auto fill.
    - IP-Reuse- no need to define blocks
    - Design Driven by physics not rules
    - MFG History of blocks
  - Supply chain predictive analysis
    - Selection of Block based upon supply chain
    - As supply chain changes, the Blocks update





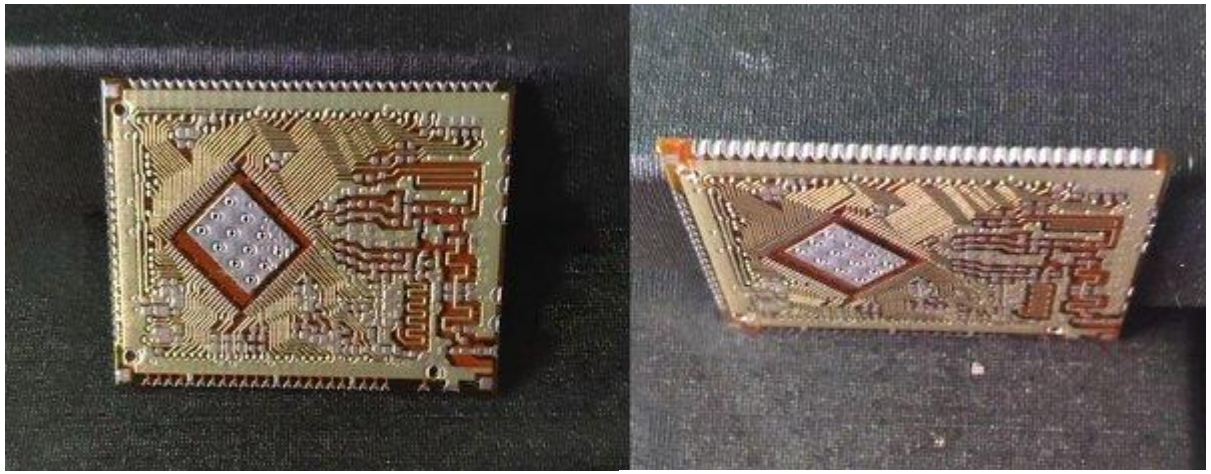
Simulation

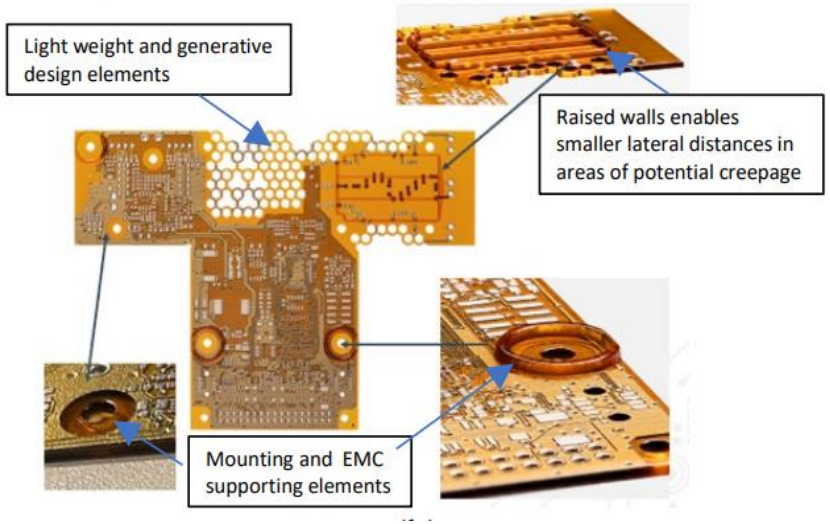
- Why do we simulate now?
- What is needed:
  - Good data in from datasheets,
  - Design Blocks from the schematics with electrical requirements
- The designs are based upon physics, not space and trace

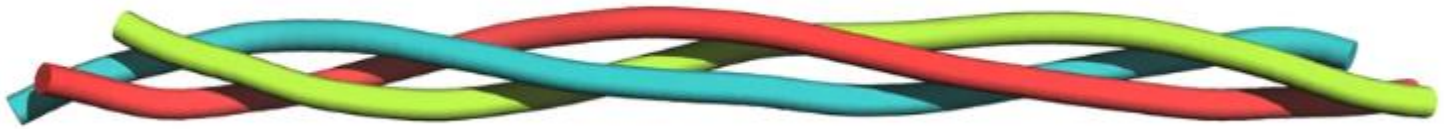
- Simulations run all the time in the back ground. (remember, this is all based in the cloud)
- Three levels of simulation
  - Modeless, quick real time checks as you are working
    - X-talk, Impendence, Reflection, IR Drop
  - 2D simulation
  - 3D sign off

MFG

AME (Additive Manufacturing Electronics)







MFG

Generative Design

CPU POWER

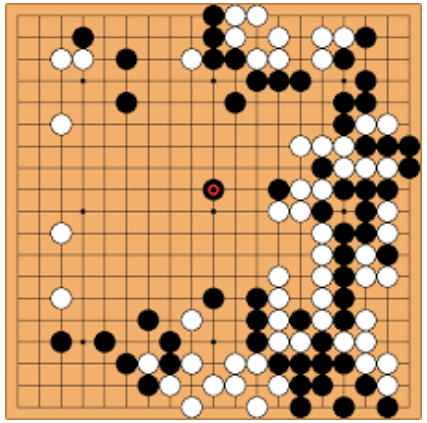
AI/ML for PCB Synthesis

- Why has this not been solved?
  - It is a big problem.

Chess

10^{44}

Go



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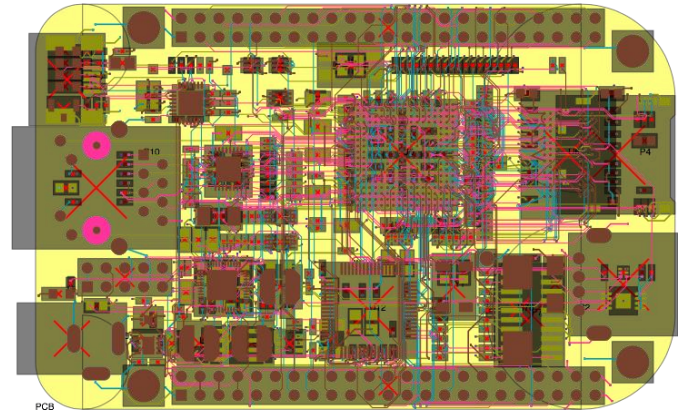
PCB Placement



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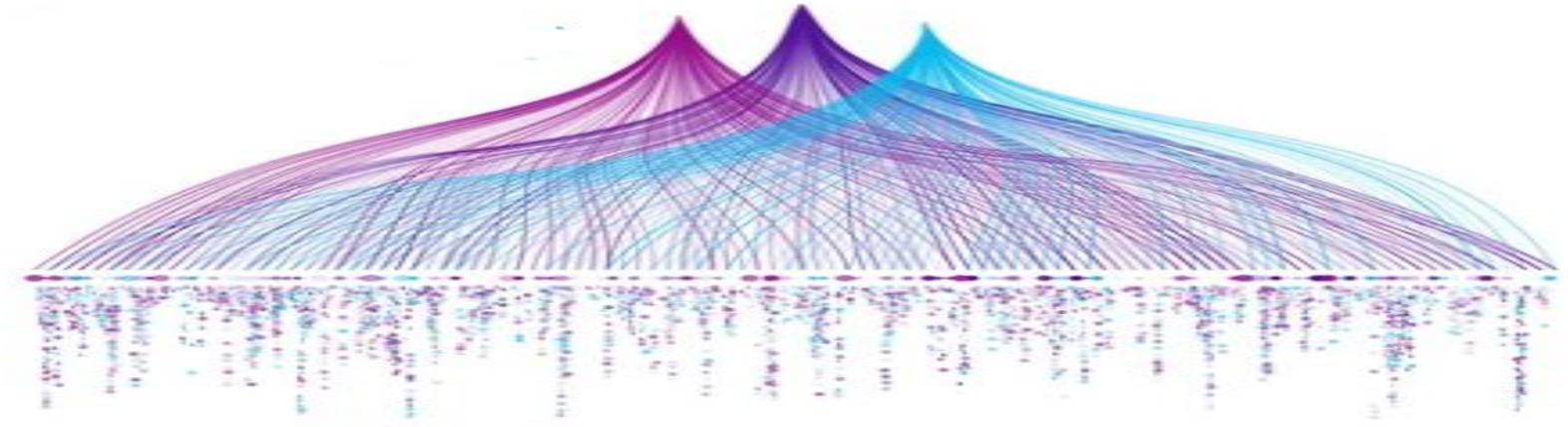
[* https://en.wikipedia.org/wiki/Game_complexity](https://en.wikipedia.org/wiki/Game_complexity)

Bringing it all together

All Cloud Based



DATA → CPU POWER → MFG → PCB 3.0

GOOD Datasheet Data
Block Data, IP-Reuse
Supply Chain

Cloud Based Power
Real Time Simulation
AI/ML application of Data

AME (3D Printing of PCB)
Generative Design