PCB Carolina 2022

PREES Laboratory
NC STATE UNIVERSITY
PACKAGING RESEARCH IN ELECTRONIC ENERGY SYSTEMS

Industry Inflection Point: Organic Substrates Outperform Ceramic in Power Modules

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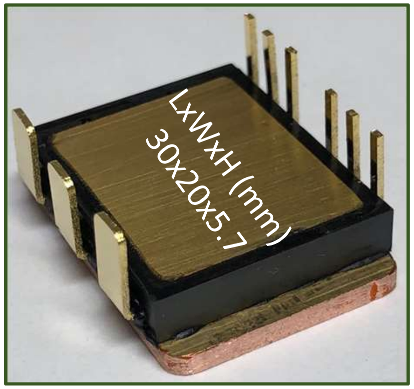
OUTLINE

ABSTRACT – An advanced epoxy-based insulated metal substrate (eIMS) uses a new high temperature, highly thermally conductive organic dielectric (ERCD) having characteristics of 40kV/mm breakdown, 10W/mK and operates at Tg≥300°C with a low modulus. And is used to create a two-sided GaN ½-bridge 450V/50A power module.

1. A bit of review about ceramic-based power modules
2. Review characteristics of Epoxy Resin Composite Dielectric (ERCD) ← *Think PCB*
3. Compare Ceramic to Organic ERCD
4. Introduce a double-side cooled GaN ½-bridge power module using an Epoxy Insulated Metal Substrate (*eIMS*), include a supply chain map
5. Impress audience with high-speed double-pulse-test results to show electrical module performance



PREES provides Open-Source Documentation of many of its designs.

The IPM designs reported here are available on our open-source design site:

https://go.ncsu.edu/prees_open_source

Provided are SolidWorks easm files and a pptx presentation of process steps.

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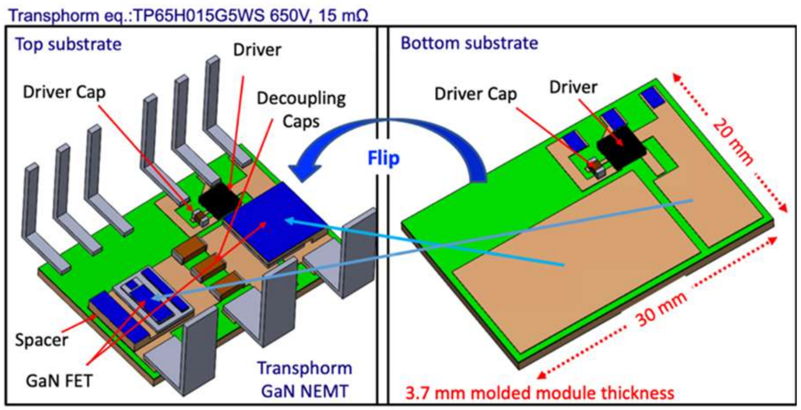
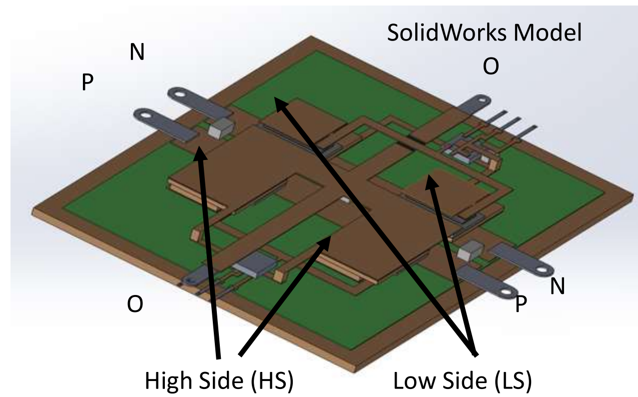
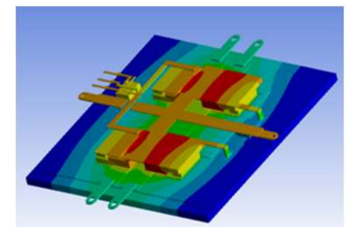
Open-Source Documents…

VIRTUAL DESIGNS 1A & 1B
PURSUED INTO PHASE-II
Single Die ½ - Bridge Module (Transphorm and GaN Syst dies)

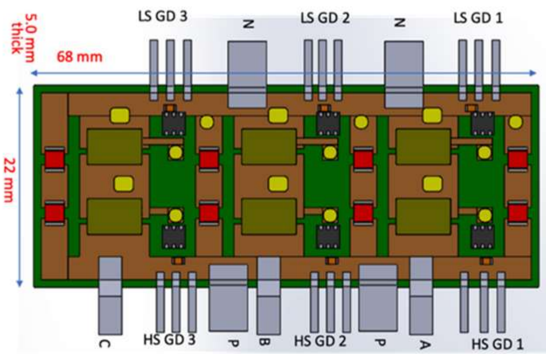


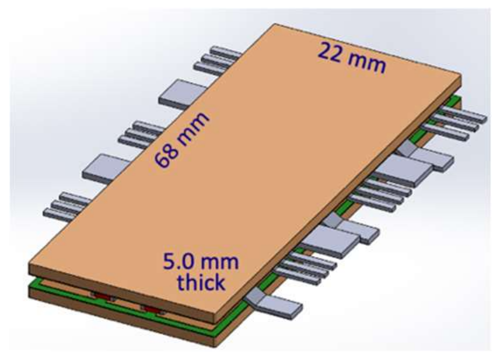
VIRTUAL DESIGN 2
Dual Dies in ½ - Bridge Module (Transphorm dies)

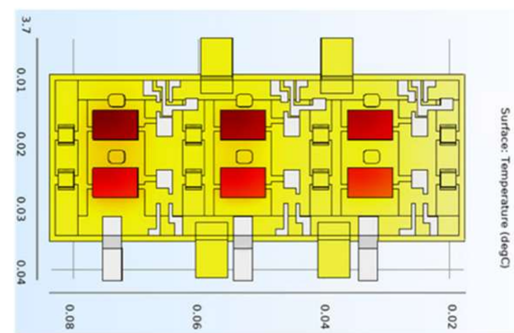




VIRTUAL DESIGN 3
Three Phase Bridge module (Transphorm dies)







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1. A bit of review about ceramic-based power modules

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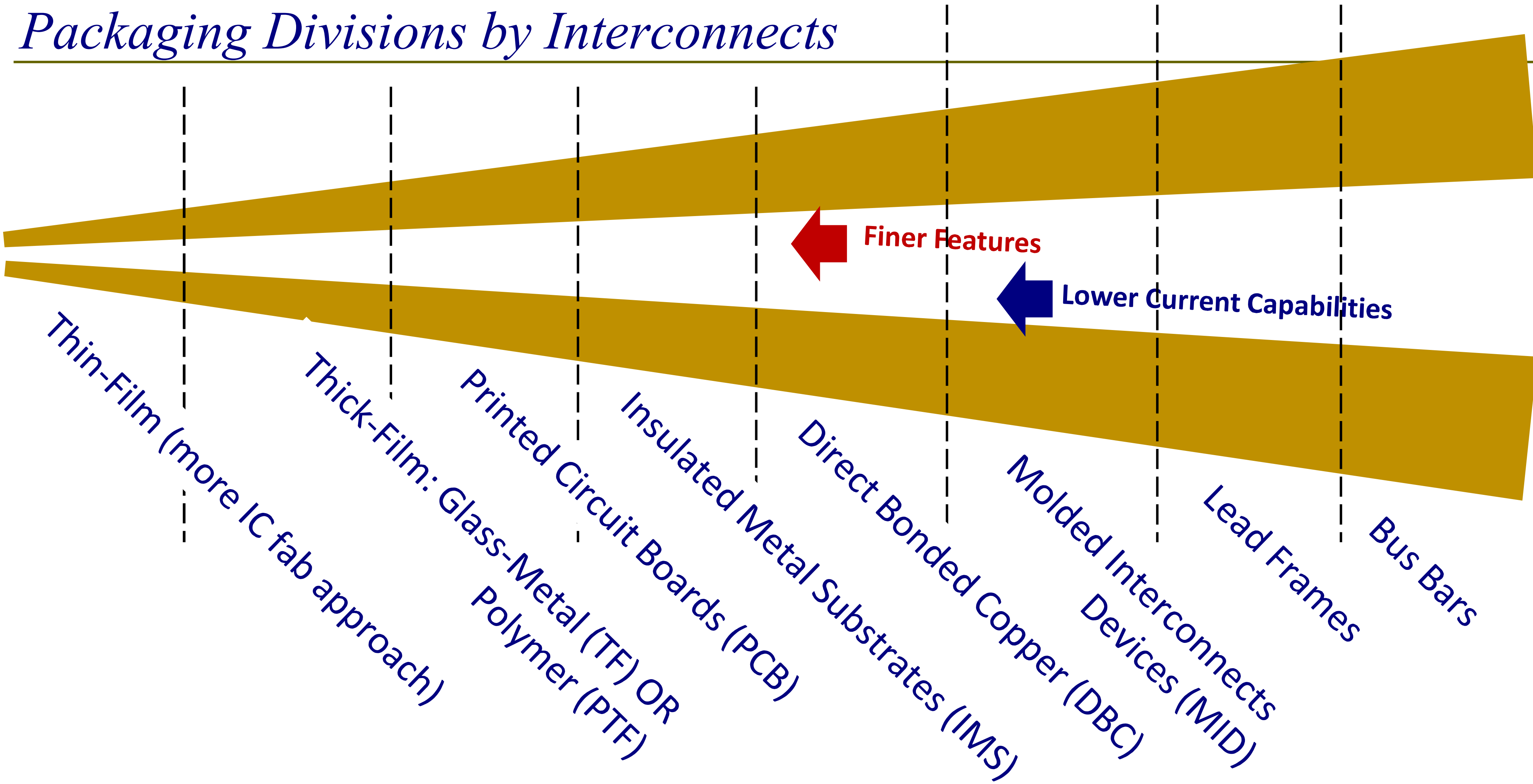
Packaging Divisions by Interconnects



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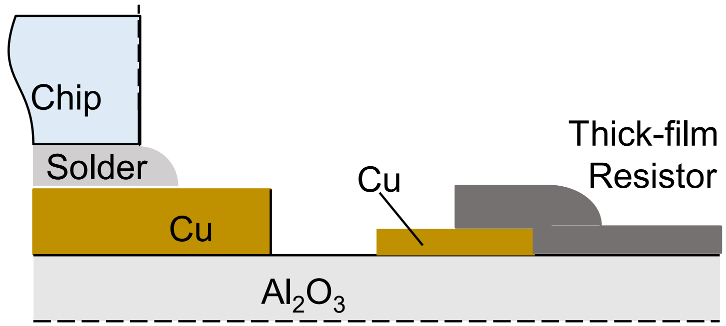
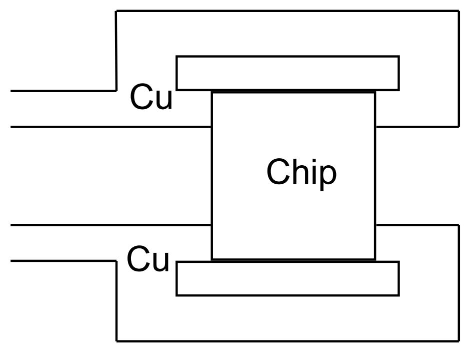
Plated Copper (Best for ≤125μm Cu thickness)

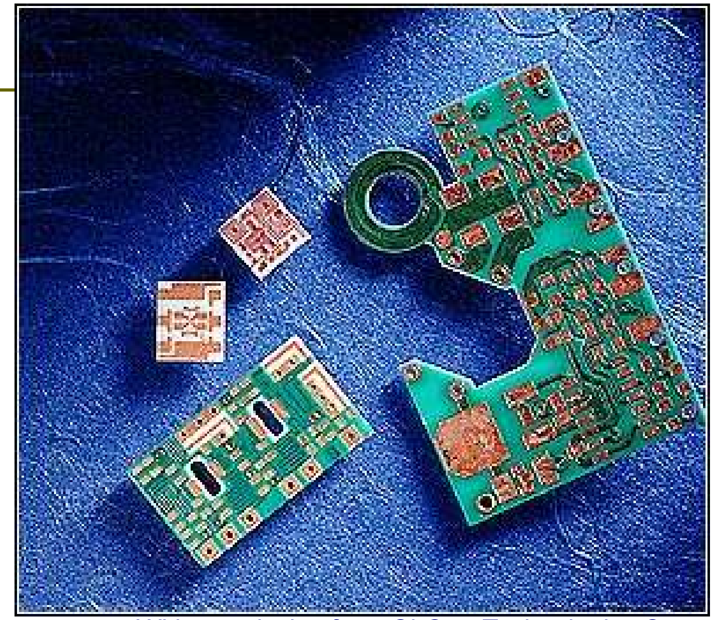
Attributes

* 50μm conductor separation
* ε_r = 9.4 or 13 pF/cm^2
* ρ = 1.72μΩ-cm   Copper
  25μm - 127μm thickness
  690μΩ/sq - 135μΩ/swq.
* R_θ = 2°C/W/cm^2 (*)
* Chip & Wire or SMT
* Some thermal interaction
* Ceramic based - mixed technology
  photo-patterned and plated;
  thick or thick-film
* Accommodates highly complex circuits



Top Down View





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Magnetics & ignition module

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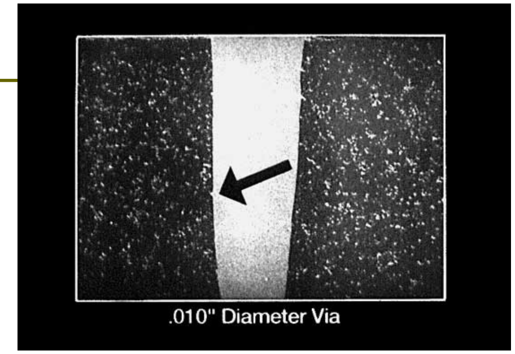
Plated Cu - Typical requirements

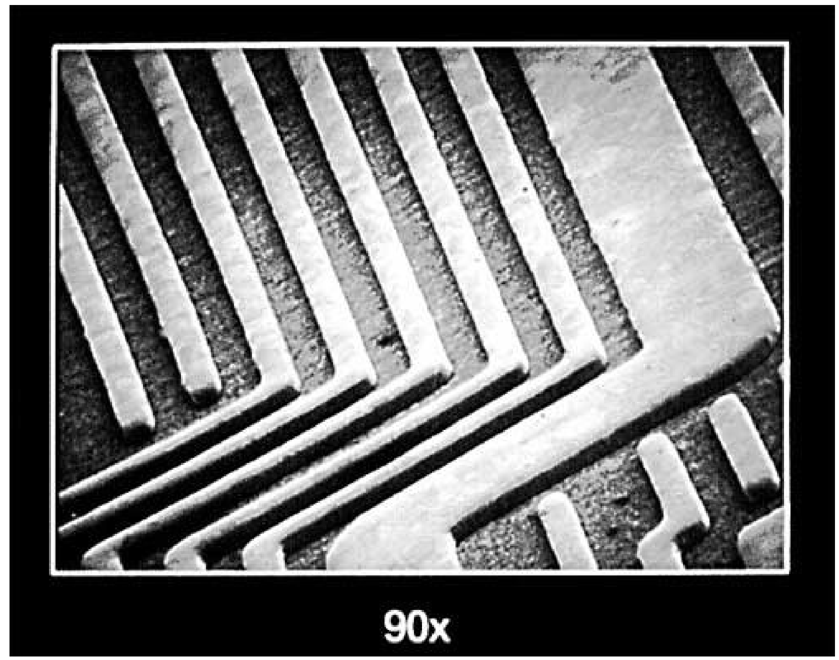


- Ceramic typically 96% Alumina
- Typical copper plating thickness:
  - Minimum .001” +/- .0003” , Maximum .003” +/- .001”
  - Perforations needed in copper patterns > .250” square.
- Preferred panel and substrate sizes:
  - 7” x 5” @ 25mils
  - 4.5” x 4.5” @ 15mils
  - 2” x 2” @ 10mils

Surface finish preparations typically

- Wire bondable ENIG (Electroless Nickel Immersion Gold).
- Immersion Au (3-5 microinches) with Ni diffusion barrier.
- Entek OSP over bare copper to promote solderability.
- Immersion Ag (3-5 microinches) to promote solderability

- For copper thickness of 1mil to 2 mil
  - minimum trace width .003” +/- .0005”
  - minimum space width .003”
    - For copper thickness of >2mil the
      - minimum trace width .004” +/- .0015”
      - minimum space width .004”



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Direct Bond Copper Process

Authors thank

Curamik® Electronics

A member of

AAVID
THERMAL TECHNOLOGIES, INC.

for providing information and photos

CIRCA 2003

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DCB Process

- Oxygen reduces the melting point of Cu from 1083°C to 1065°C (Eutectic melting temperature).
- Oxidation of copper foils or injection of oxygen during high temperature annealing (1065°C and 1080°C) forms thin layer of eutectic melt.
- Melt reacts with the Alumina by forming a very thin Copper-Aluminum-Spinel layer.
- Copper to copper is fused the same way.
- Copper-Aluminum-Nitride (AlN) DBC is possible. The AlN-Surface must be transformed to Alumina by high temperature oxidation.

Courtesy of Curamik Electronics, circa 2003

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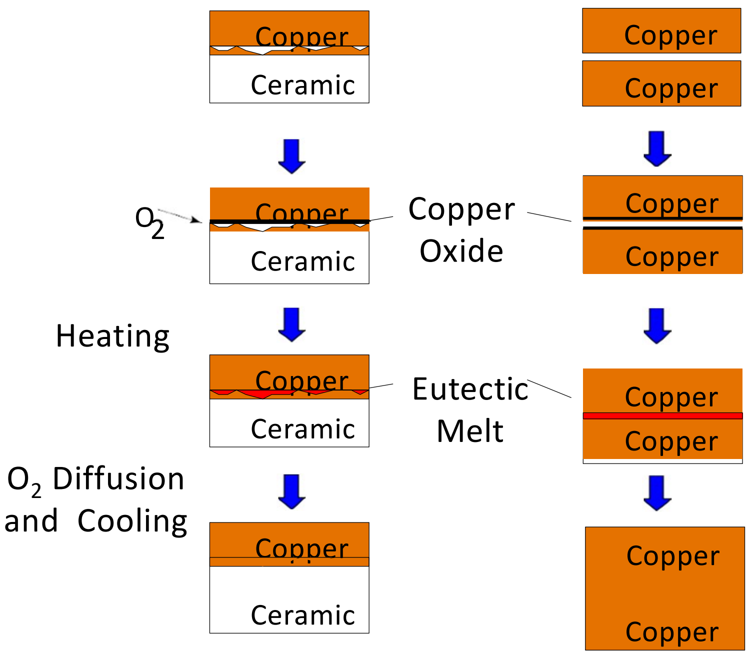
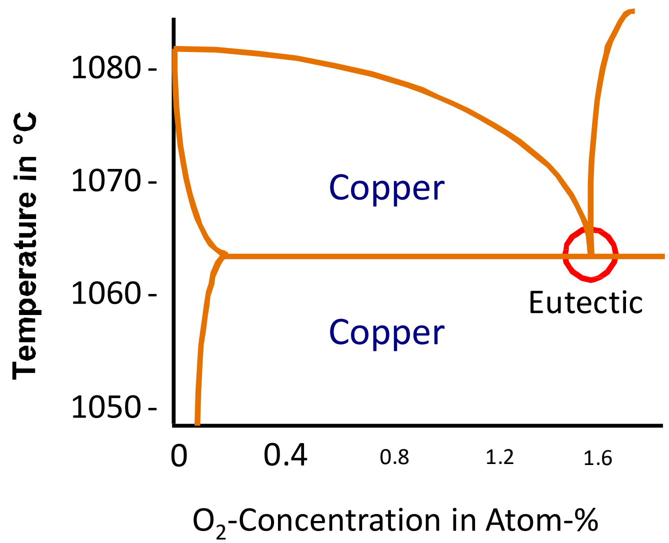
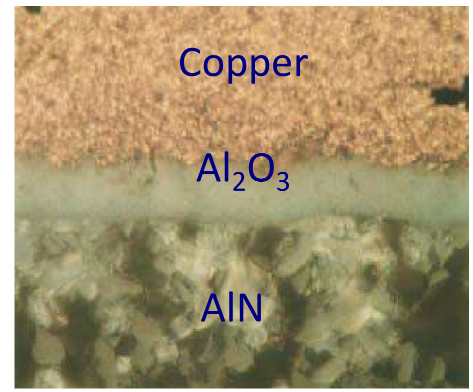
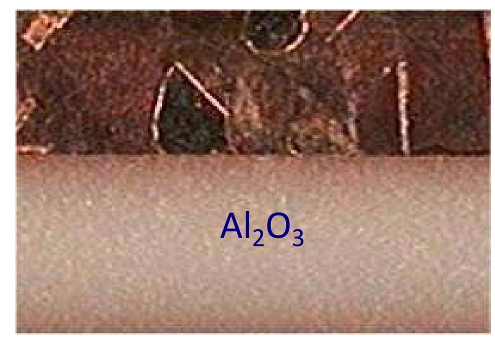
DBC Process









Courtesy of Curamik Electronics, circa 2003

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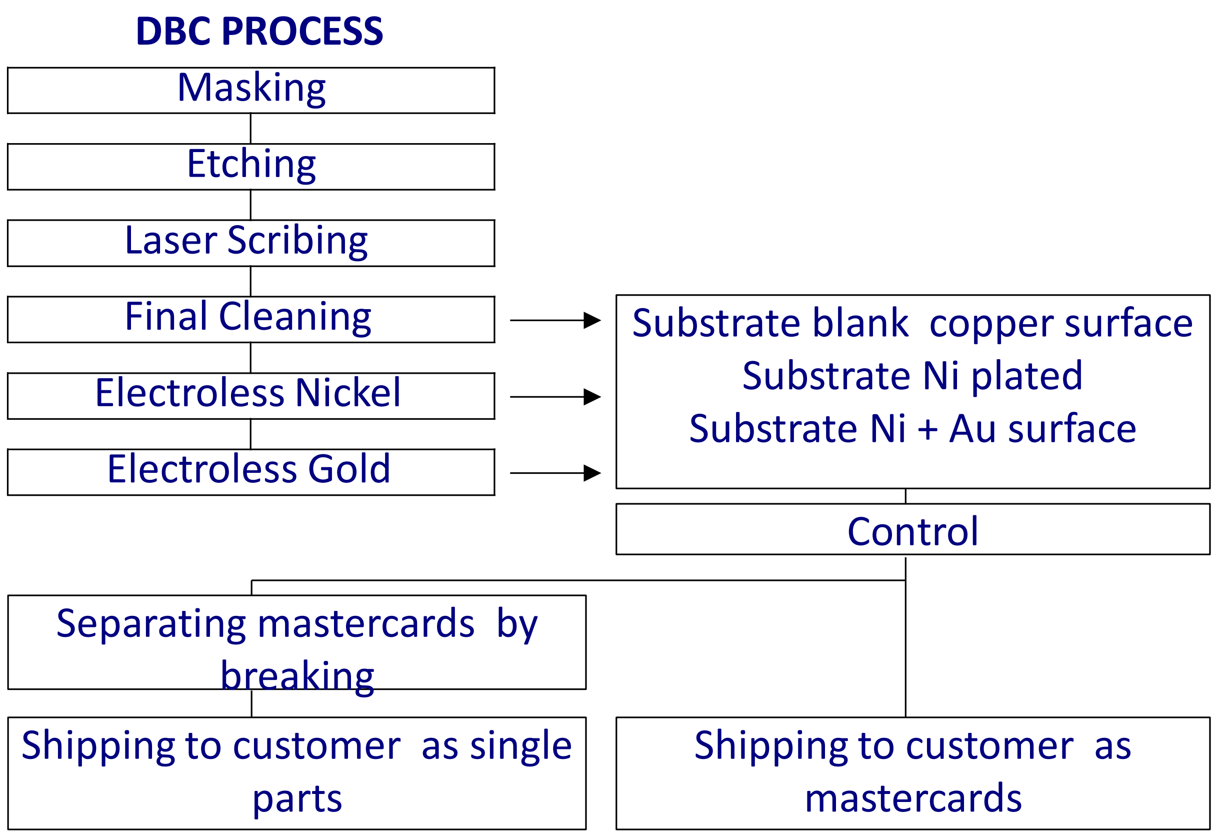
Flow Chart of DBC Circuit Processing



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Masking

- High precision screen printers for high volume
- Semiautomatic and fully automatic with pattern recognition
- Redundant equipment
- Photomasking for high density circuits
- Air conditioned clean rooms

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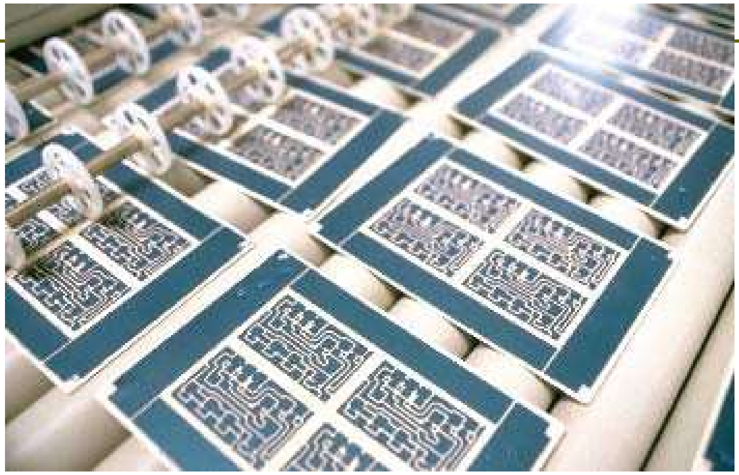
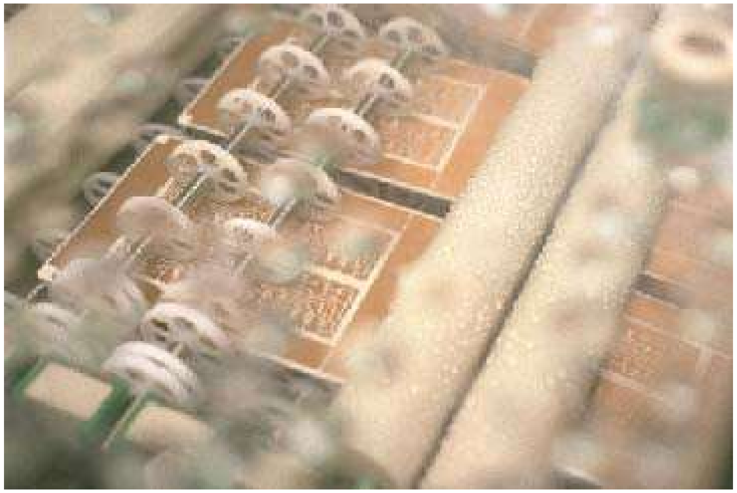
Etching

- Specially designed precision etchers for thick copper layers
- Automatic chemistry control
- Mask stripping integrated
- 3 separate high volume lines in operation
- Controlled by SPC





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Plating / Final Cleaning

- Fully automatic high volume plating line for electroless Ni + Au
- Controlled by SPC
- Final cleaning for Cu integrated
- Parallel backup lines
- Solderability and wire bond testing

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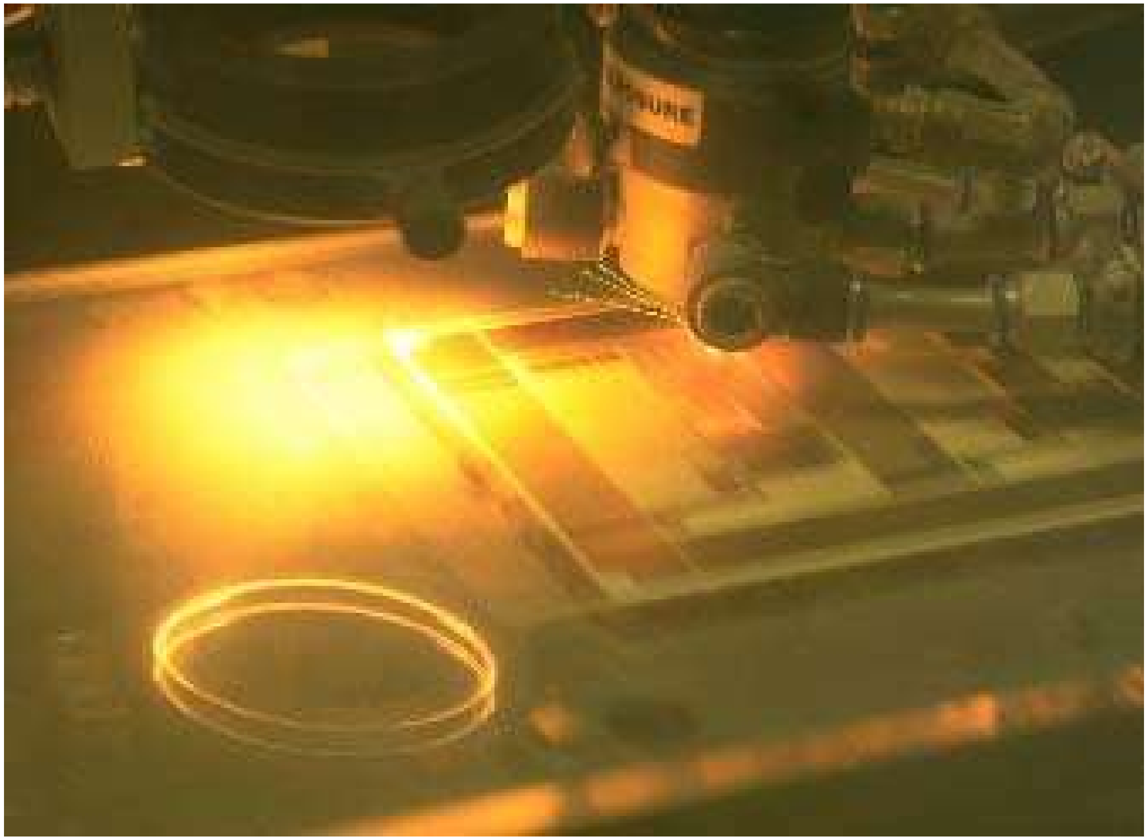
Laser Machining

- Fully automatic high precision CO2 lasers with pattern recognition
- Designed for high volume throughput
- Scribing and drilling
- Multiple equipment
- Controlled by SPC



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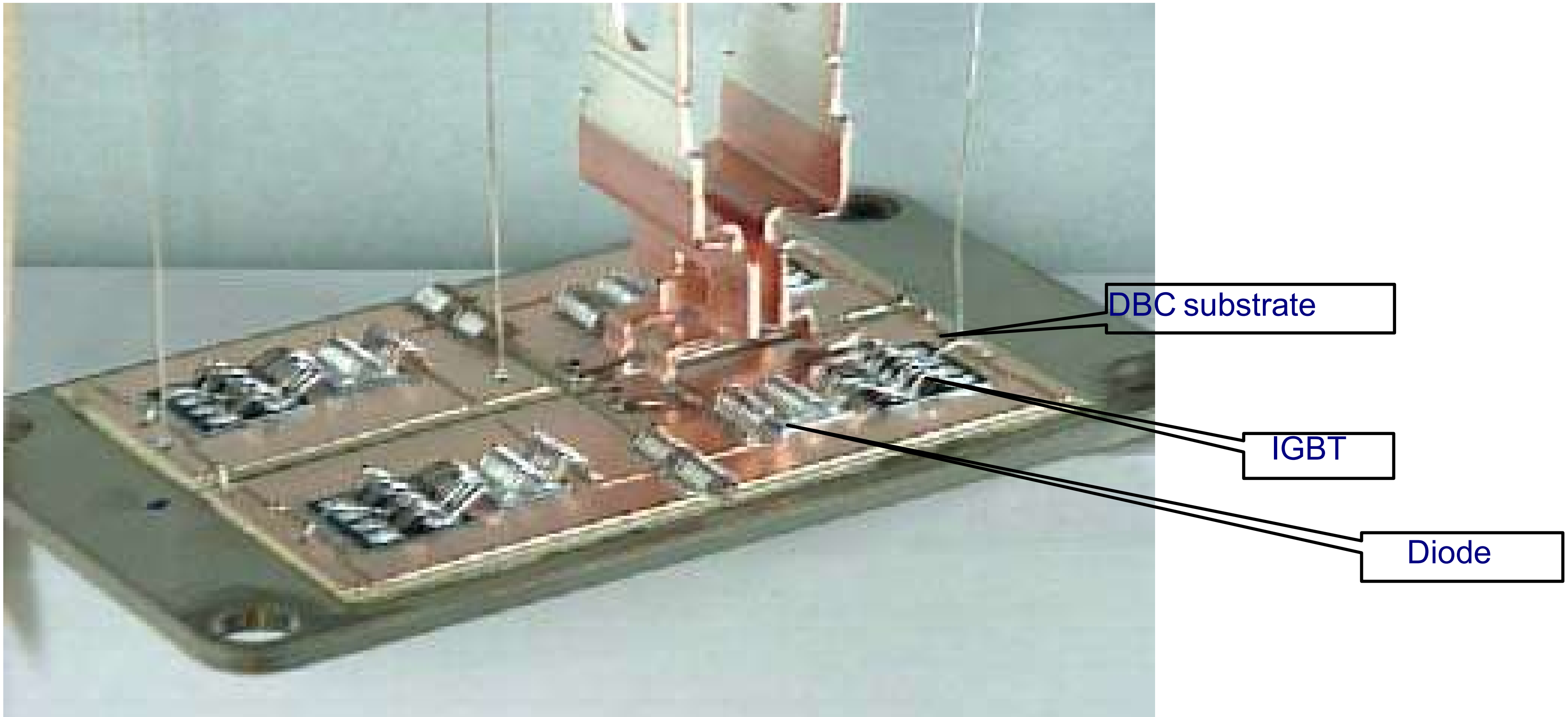
Single Switch Module

4 Substrates, 4 IGBT's and 4 Diodes



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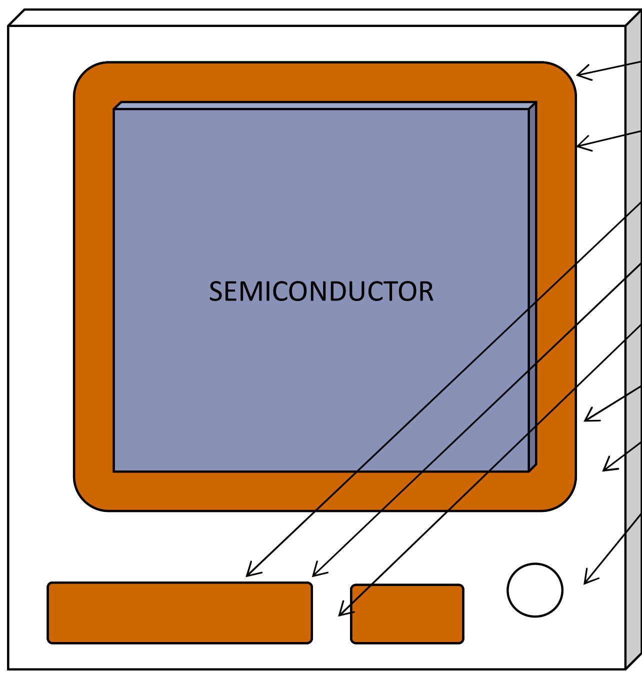
DBC Layout & Substrate Specifications



Thickness of Cu (not to exceed the ceramic thickness)	6–20 mil (10 mil typ.) 8–12 mil (10 mil typ.)	Direct-bonded Cu Active-brazed Cu
Tolerance for thickness	± 10%	
Minimum line width	20 mil 40 mil	6–10 mil Cu 10–20 mil Cu
Tolerance for length and width	±4 mil	
Minimum separation between conductors	20 mil 40 mil	<12milCu 12–20 mil Cu
Etch factors, a	3–10	Undercutting = *thickness*/a
Minimum distance from substrate edge	20 mil	V_{ISO} = 2,500 V
Hole	Hole ≥substrate thickness Edge of hole 0.060" from edge of substrate	
Camber	± (3–4 mil/linear inch)	

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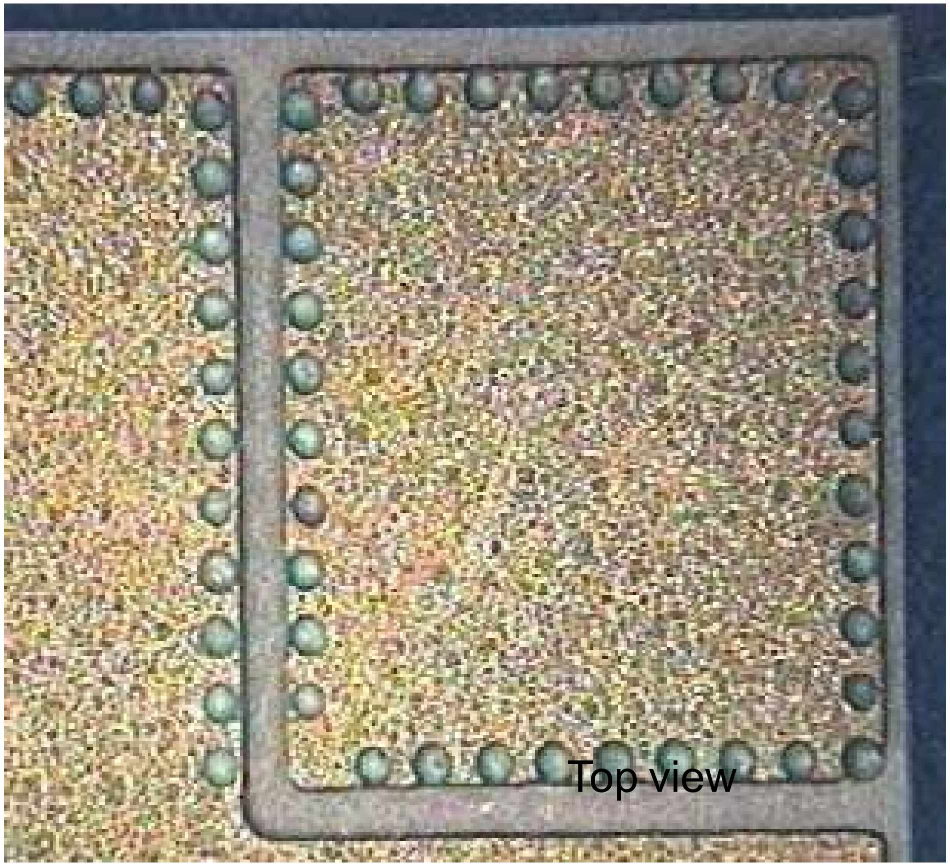
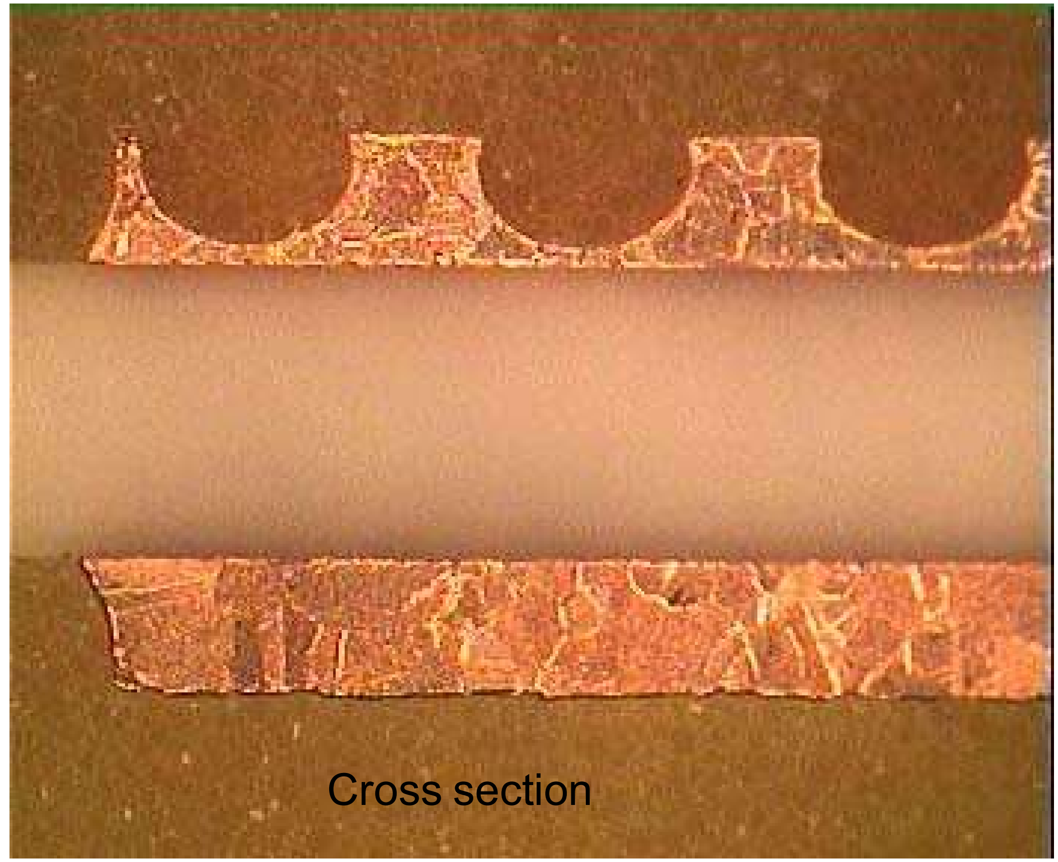
Dimple Design





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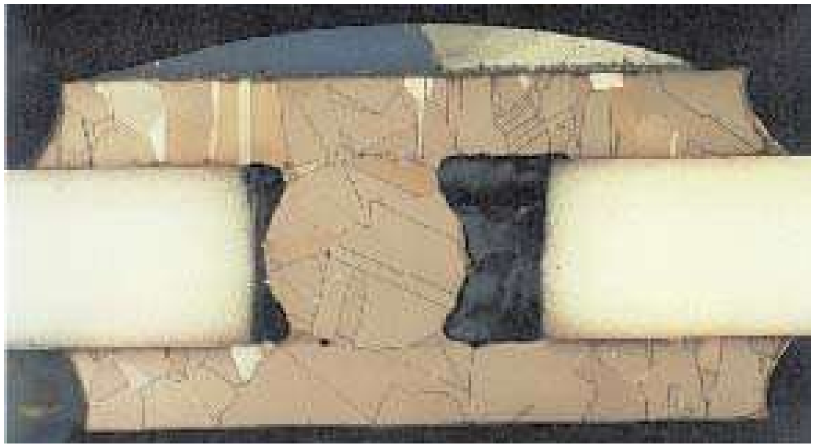
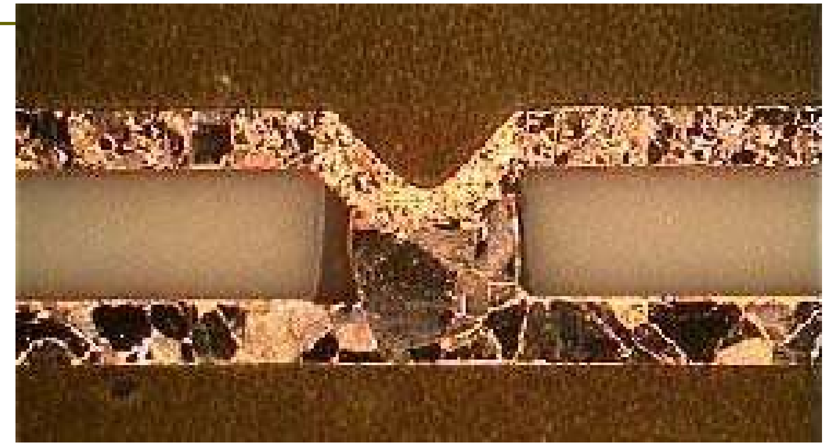
Via Technology

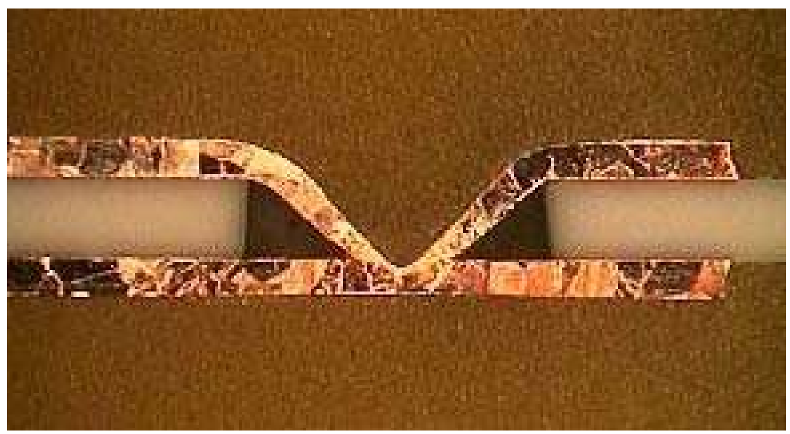


Both sides flat surface. Ceramic hole diameter min. 1.0mm R<100µΩ



One side flat surface. Ceramic hole diameter min. 1.0mm R<100µΩ

- High current front to back feed-through
  - 100 A / 100 µOhm
- For backside ground- plane or shield
- Both hermetic
- Can be used as thermal path also



One side flat surface low cost. Ceramic hole diameter 2.5mm (0.3mm copper layer) R<100µΩ

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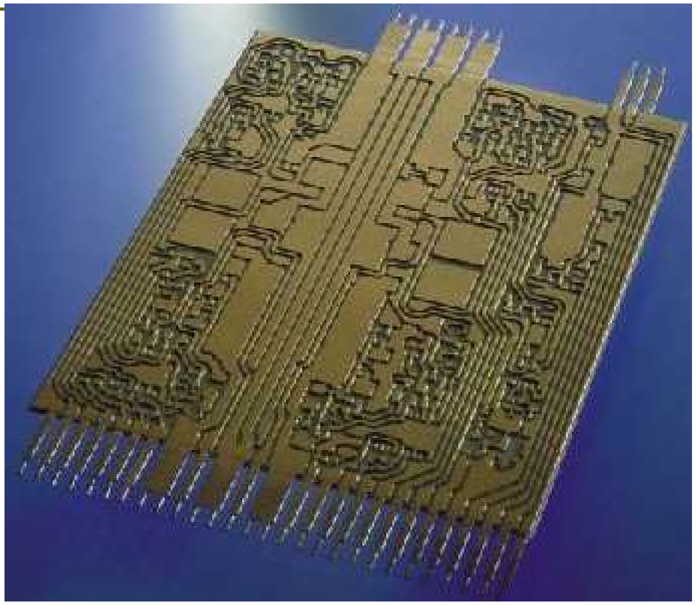
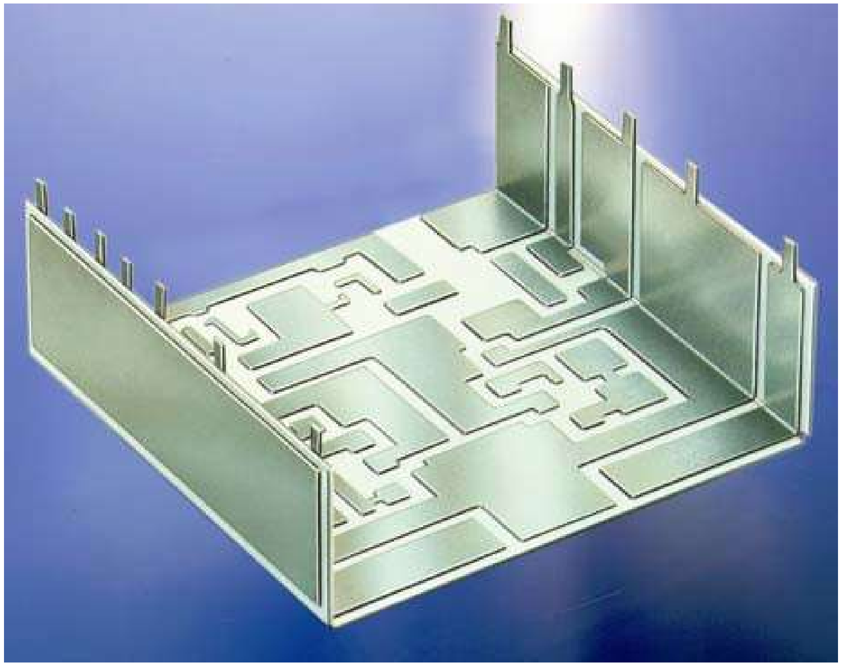
Integral Terminals

- Terminals made of same copper sheet as circuit
- High electrical conductivity due to solid metal w/o interface resistance
- Very high reliability





- For very high-density circuits
- Extremely reliable due to integral connectors
- Base for power
- Sidewalls for non-power components
- Assembled flat and bend up

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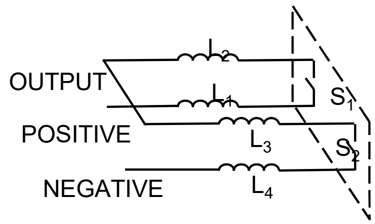
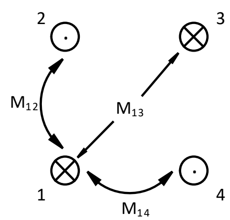
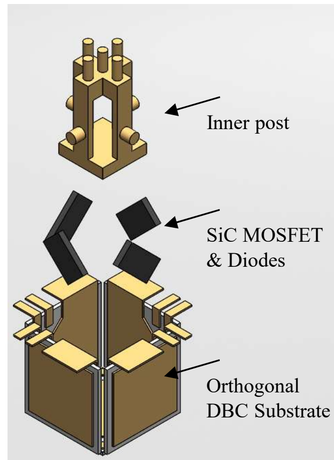
True-3D Module (Phase leg)

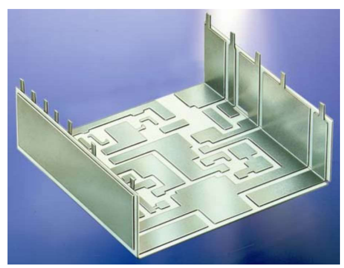


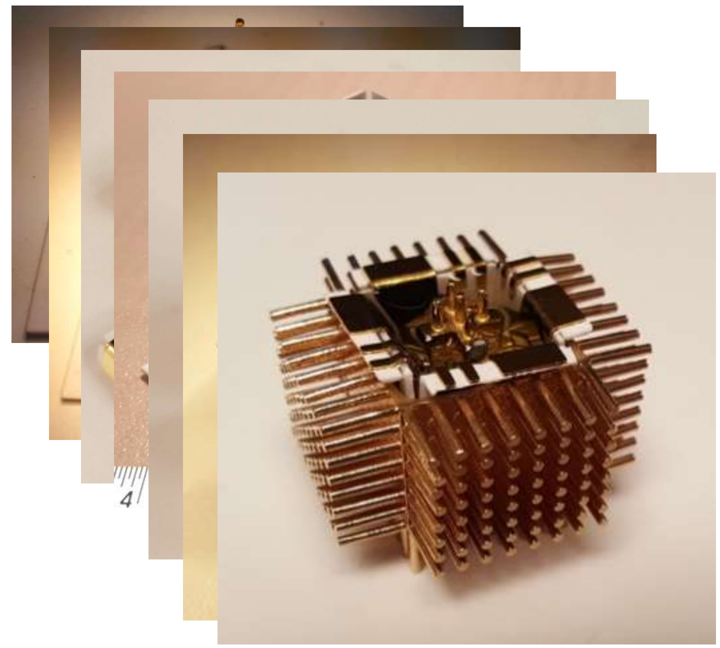
Current path in 3D, and Mutual inductance seen from L_1



$$L = \begin{bmatrix} L_1 & -M_{12} & M_{13} & -M_{14} \\ -M_{21} & L_2 & -M_{23} & M_{24} \\ M_{31} & -M_{32} & L_3 & -M_{34} \\ -M_{41} & M_{42} & -M_{43} & L_4 \end{bmatrix}$$







"3-D Prismatic Packaging Methodologies for Wide Band Gap Power Electronics Modules," Dissertation, Dr. Haotao Ke, North Carolina State University, Sept. 2017

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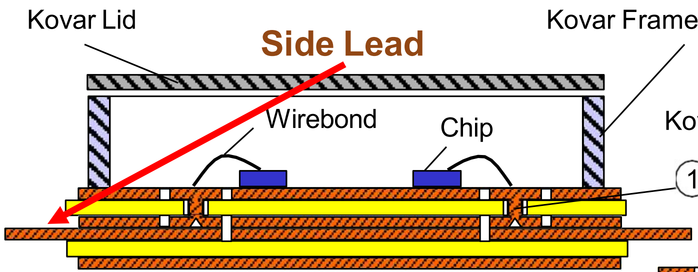
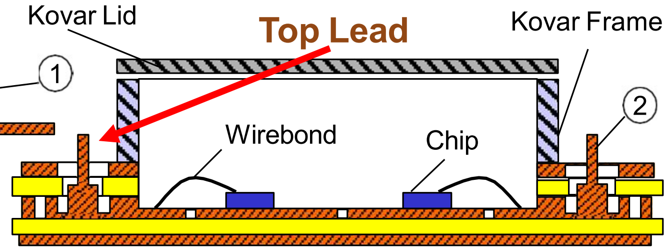
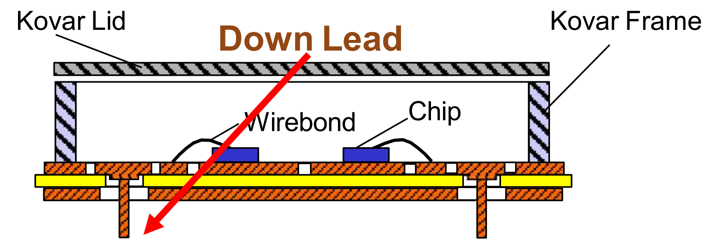
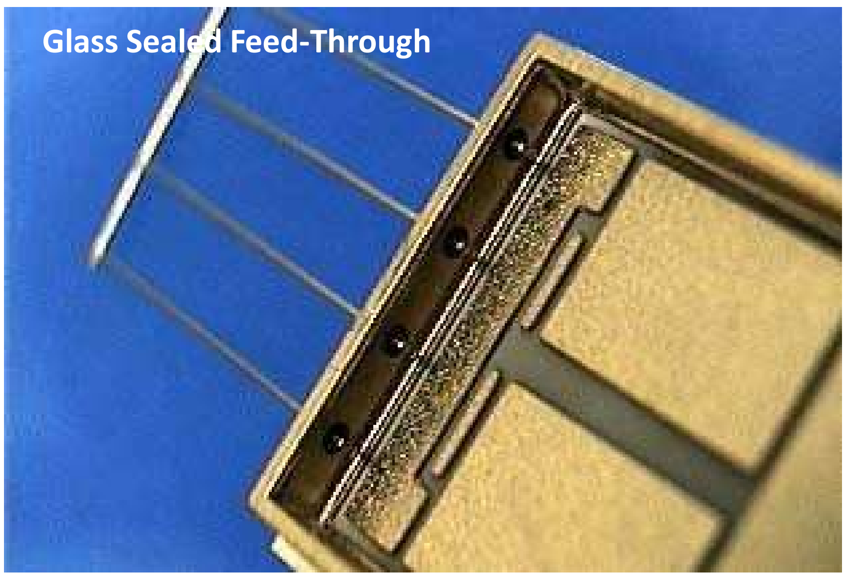
Package Types

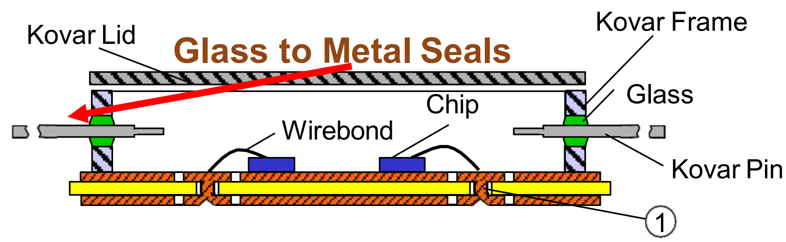
Ceramic | Copper | ① Via | ② Direct Bonded Pin

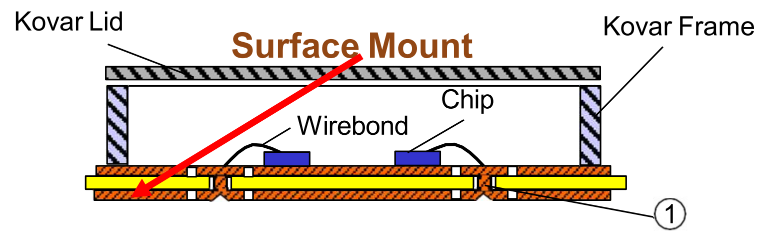












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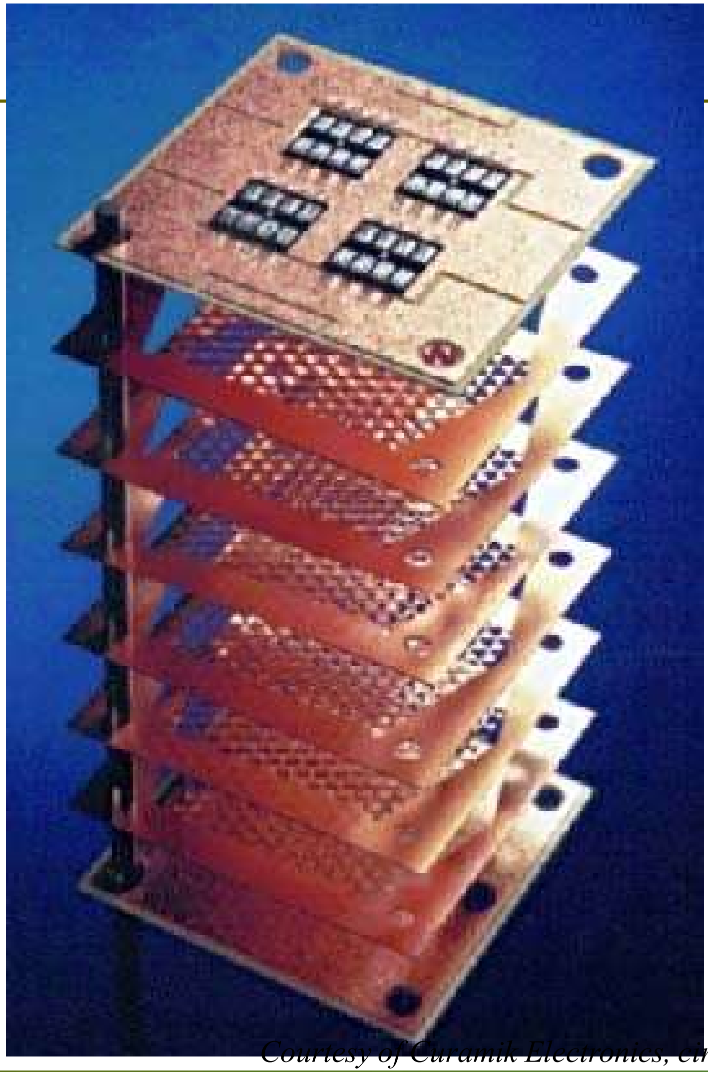
Fluid Cooled DBC

- Lowest thermal resistance of all available solutions for COB (Chip On Board)
- R_{th} from 0.08 to 0.02 °C/W using Al_2O_3 or AlN
- Power dissipation up to 3 kW on 2” x 2”
  - $3kW/4in^2$ ($750W/in^2 = 116W/cm^2$)
- Extremely compact design
- Modular system assembly



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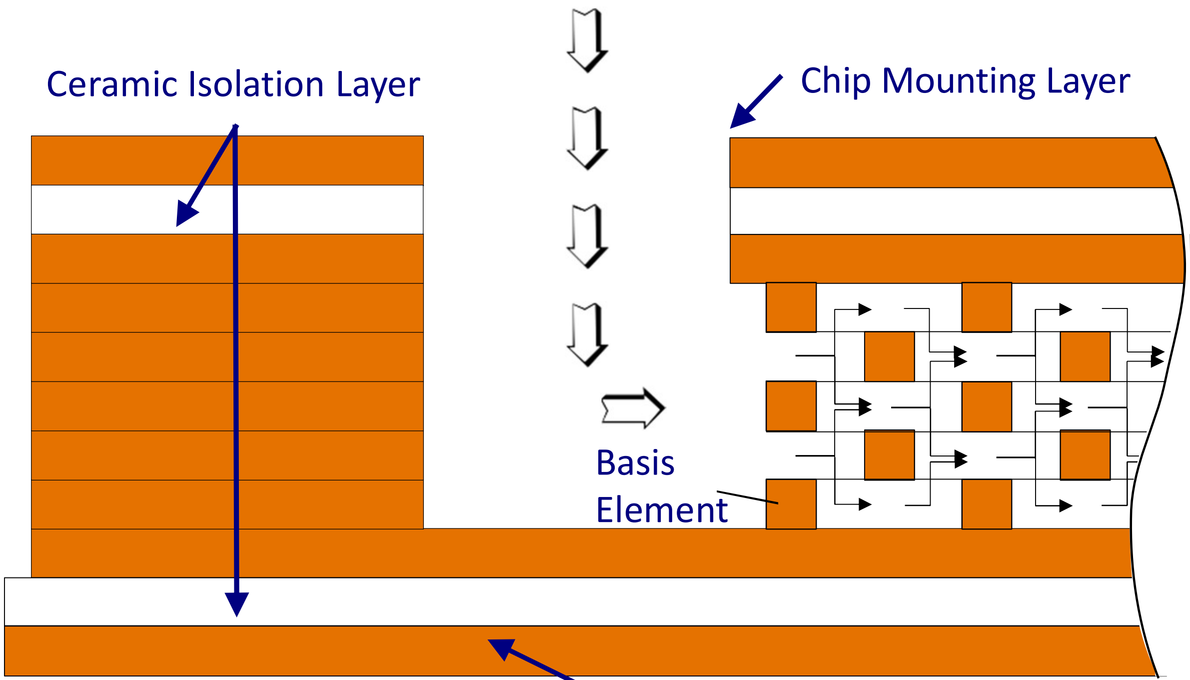
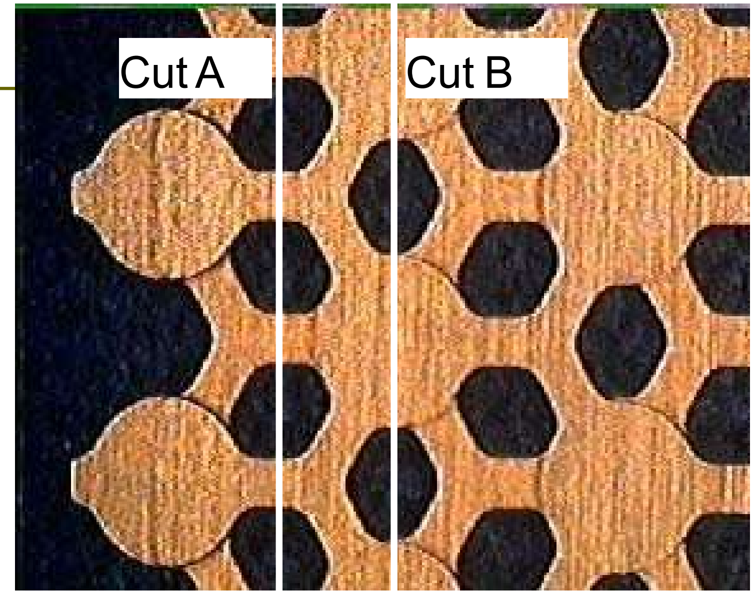
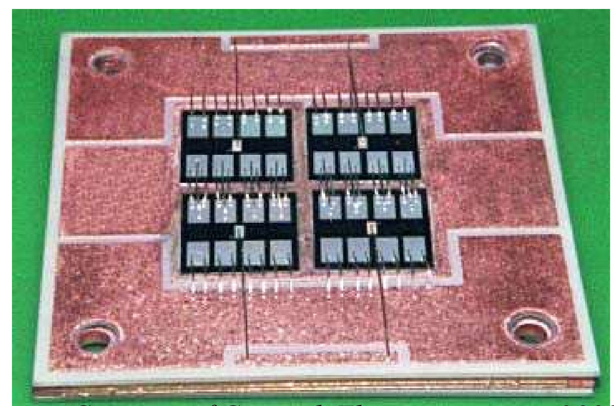
Liquid flow-through Micro-Channels







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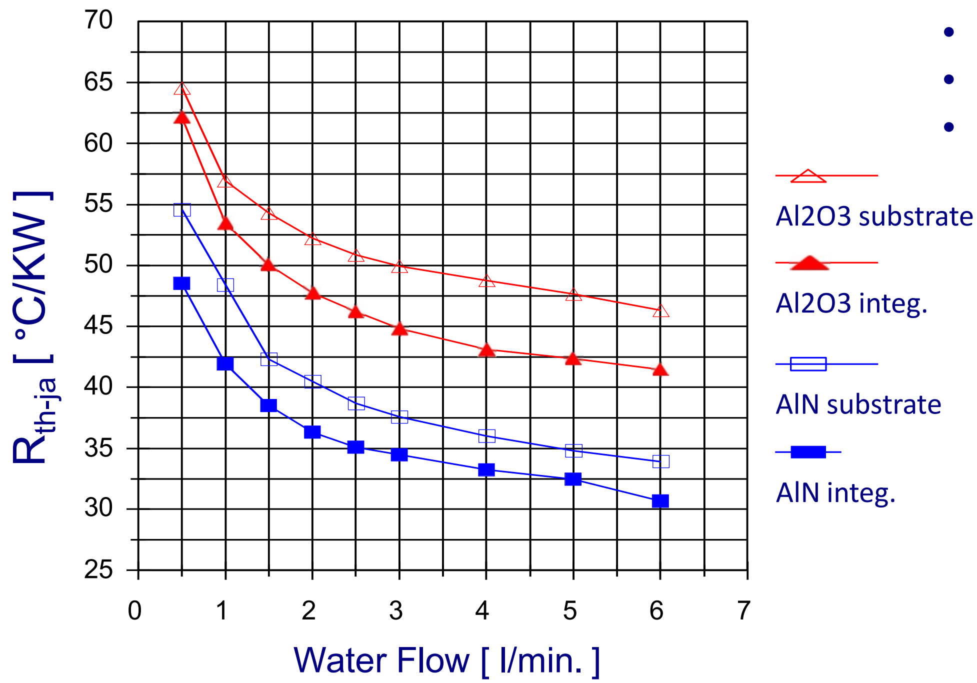
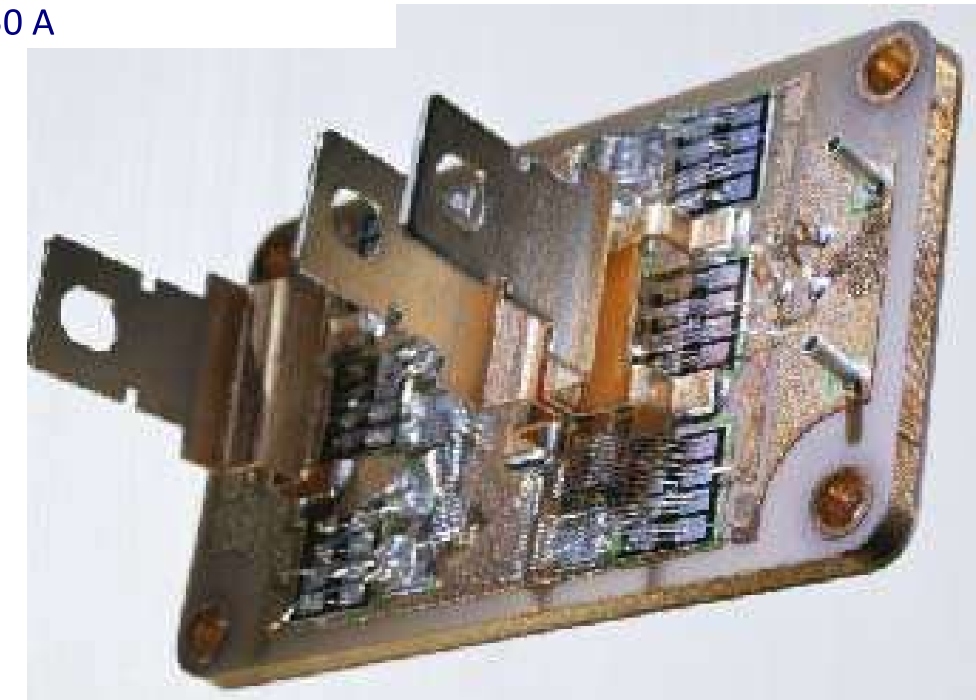
Micro Channel Water Cooled Module



Half bridge

- Cooling water up to 80°C
- 6 IGBTs, 12 Diodes
- 62 mm St'd module size
- 450 A



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2. Review characteristics of Epoxy Resin Composite Dielectric (ERCD)

Epoxy Resin Composite Dielectrics – ERCDs
These provide and opportunity to look at very low-cost modules with embedded components.

“Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module,”
Xin Zhao1, Yifan Jiang1, Bo Gao1, Kenji Nishiguchi2, Yoshi Fukawa3, D. C. Hopkins1
1North Carolina State University, 2Risho Kogyo Co., LTD, 3TOYOTech LLC

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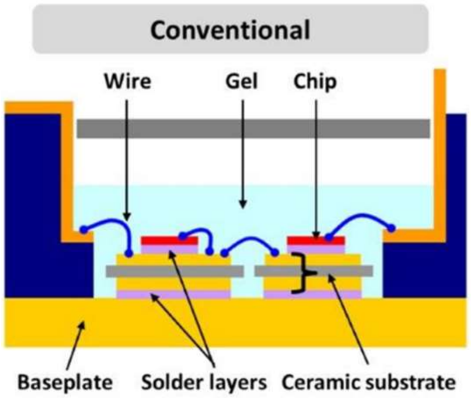
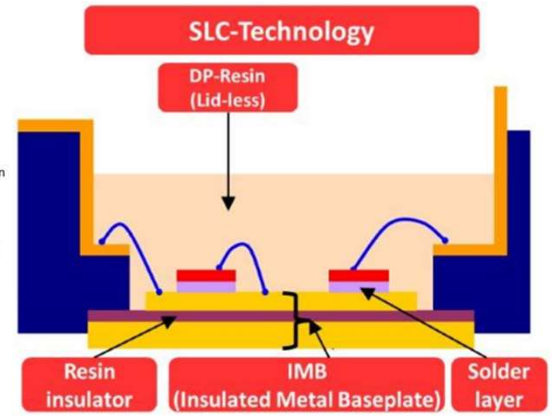
State-of-art development of WBG power module





Insulated-Metal-Baseplate based IPM by Mitsubishi [4, 5]

- CTE of insulating resin layer ~17ppm, close to Copper, with better mechanical stress management
- 35% thermal impedance reduction from development of resin
- Less interconnection layers for lower profile, up to 55% size reduction from traditional DBC based module
- Better thermal cycling reliability with less cracks during cycling
- Depends on the resin interface material heavily

[4] Y. Kaji, et al. Novel IGBT Modules with Epoxy Resin Encapsulation and Insulating Metal Baseplate. ISPSD 2016.
[5] T. Takahashi, et al. A 1700V-IGBT module and IPM with new insulated metal baseplate (IMB) featuring enhanced isolation properties and thermal conductivity. PCIM Europe 2016.

High Thermal Conductivity Materials

[1] Low modulus
CC: Cu Clad
CCL: Cu Clad Laminate
AC: Aluminum Clad
ACL: Aluminum Clad Laminate
CS: Woven Glass cloth
ES: B-Stage w/ Woven Glass cloth

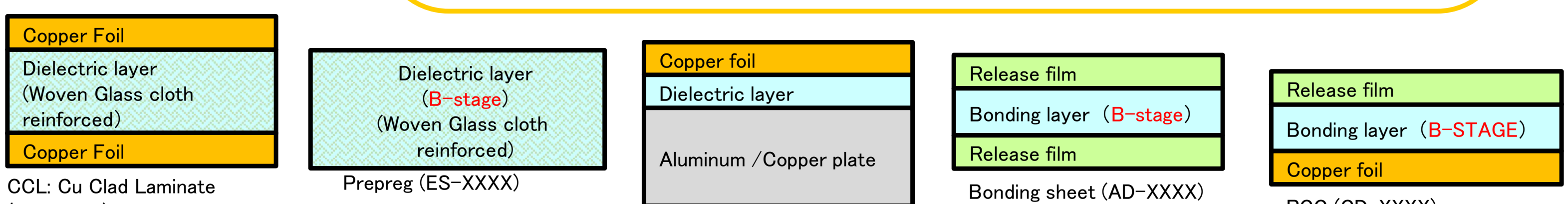
Low resin flow Bonding sheet
- AD-7006, 0.3W/mK

Glass epoxy laminate, Prepreg
- CS-3945, 1.3W/mK — CCL
- CS-3295, ES-3245, 3W/mK — CCL, Prepreg

Liquid Molding Compound (One-pack type) (1～4W/mK)

Liquid Molding Compound (Two-pack type) (1～7W/mK)

Bonding sheet, RCC, Copper-base CCL without glass fabric
- AC-7900, 1W/mK — Al base CCL
- [1] AC-7303, 3W/mK — Al base CCL
- AC-7200TY, 5W/mK — Al base CCL
- AC-7208, 8W/mK — Al base CCL
- AC-7210, 10W/mK
- [1] CC-7303, AD-7303, CD-7303, 3W/mK
- CC-7200TY, AD-7200TY, CD-7200TY, 5W/mK
- AD-7208, CD-7208, 8W/mK
- AD-7210, CD-7210, CC-7210, 10W/mK



CCL: Cu Clad Laminate (CS-XXXX) Woven Cloth
Prepreg (ES-XXXX)
CCL: Cu Clad Laminate with metal base (AC-XXXX)
Bonding sheet (AD-XXXX)
RCC (CD-XXXX)

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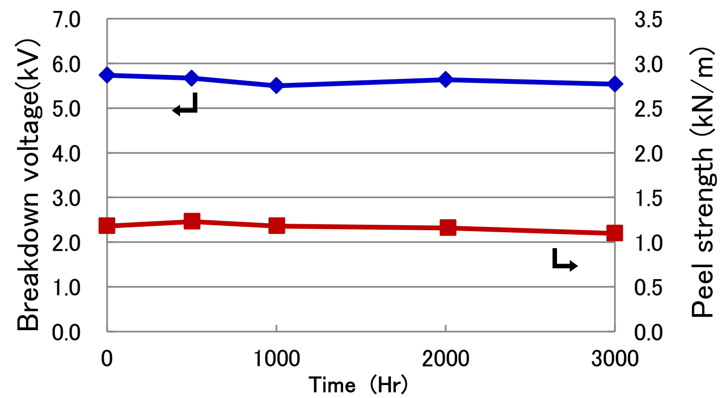
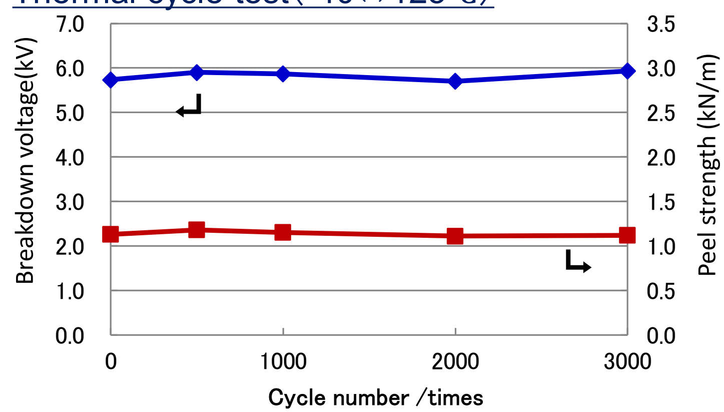
High thermal conductivity mat'ls: AC-7208 (8W/mK)

Product number	AC-7208	
Dielectric layer thickness	120µm	
Thermal conductivity（W/mK）	**8**	Laser flash
Tg（℃）	**270**	DMA method
Peel strength（kN/m）	1.2	1 oz copper
Solder limit（sec）	Over60	260℃
CTE（ppm/℃）	9/22	α_1/α_2
Breakdown V（kV）	**> 5**	JIS C2110
CTI	over600	IEC method
Flammability	V-0equiv.	UL94

High temperature long term test（@175℃）



Thermal cycle test（-40⇔125℃）



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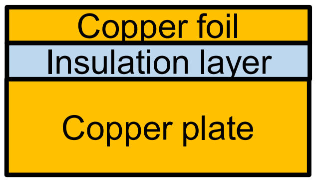
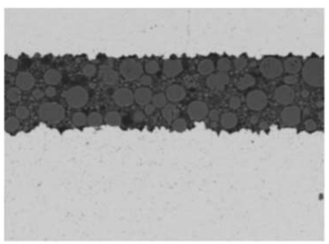
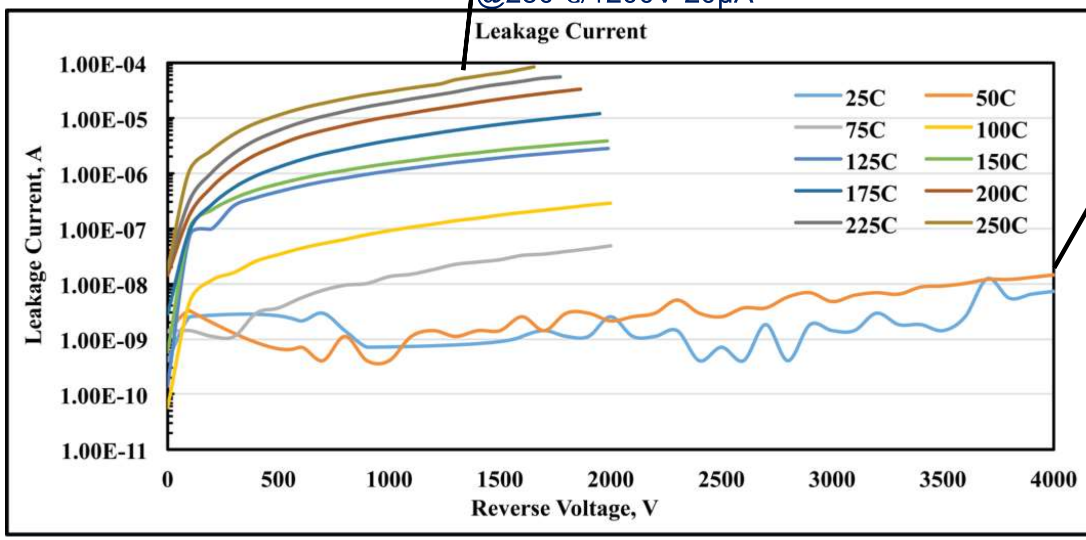
High voltage capability: CC-7208 (8W/mK)

"Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, et.al., IEEE 67th ECTC –Orlando, FL, USA

Characterization of Leakage Current v. Temperature







Limited leakage current is measured on the 80 μm sample with copper bonded on both sides

- 20 μA leakage even at 250℃ with 1200 V voltage applied
- 1 nA leakage at room temperature with > 4kV voltage applied

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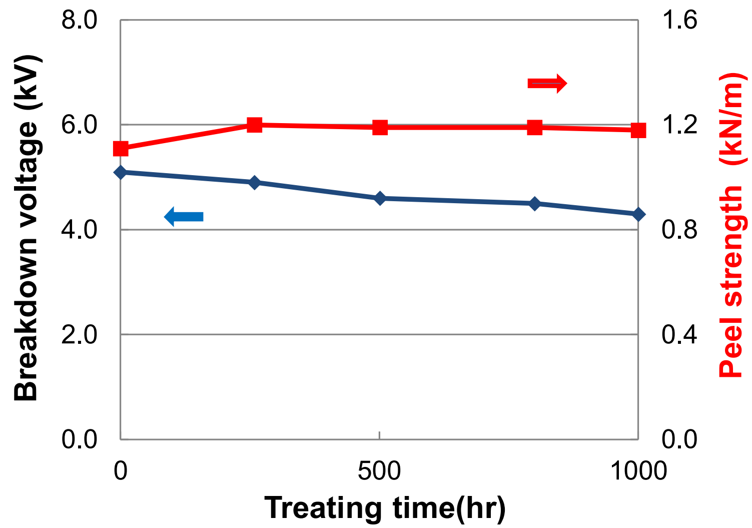
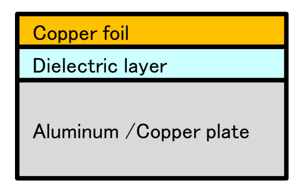
High thermal conductivity mat'ls: AC-7210 (10W/mK)

PROPERTIES

Product number	AC−7210	
Dielectric layer thickness	120 μ m	
Thermal conductivity (W/mK)	10	Laser flush method
Tg (℃)	270	DMA method
Peel strength (kN/m)	1.2	1 oz copper
Solder limit (sec)	60<	260℃
CTE (ppm/℃) α 1	14/14/14	X/Y/Z
Breakdown V (kV)	>5	JIS C2110
CTI	>600	IEC method
Flammability	V−0 equivalent	UL94

High temperature long term reliability(175℃)





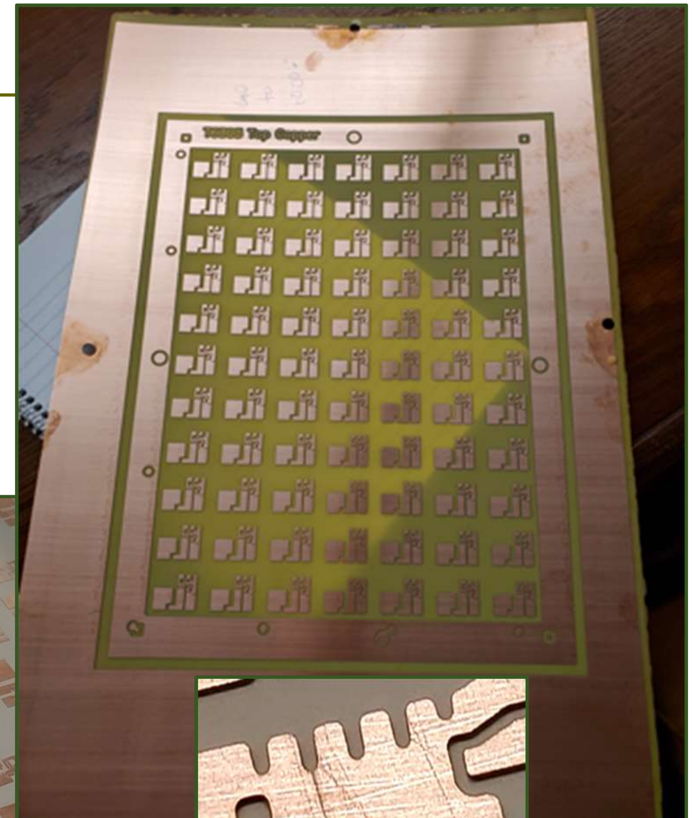
CCL: Cu Clad Laminate
with metal base (AC-XXXX)

A SIMPLER HIGHER POWER PCB

Ordered **1.5’x2’** ERCD B-Stage sheets from RISHO (120µm AD-7210N)

- Trimmed to 0.75’x12’ for top-, 1’x1.5’ for bottom-eIMS plates
- 4oz. Cu on 120µm ERCD laminated onto 2mm Cu baseplates

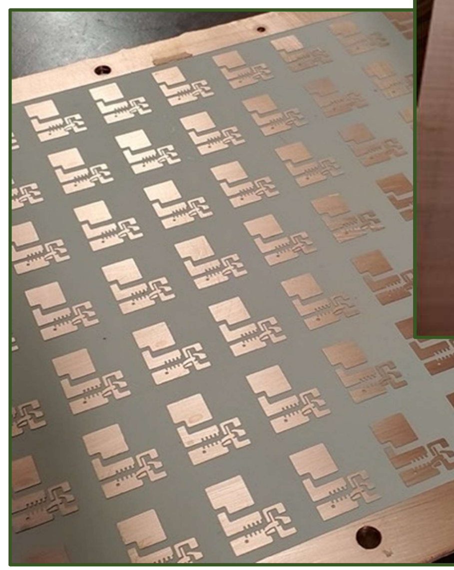
Panel Size eIMS Manufacturing

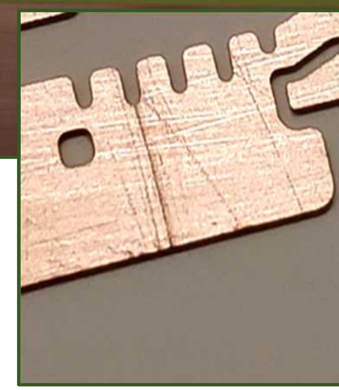


RISHO KOGYO CO.,LTD
TOKYO OFFICE

LIST of TEST Samples

Product No.	AD-7210N
Material	High Thermal Bonding Sheet (10W/mk)
Production Lot No.	AK6-X419-4
Quantity(sheets)	15
Dielectric nominal thickness(mm)/(mil)	0.12/(5mil)
Panel size(mm) /(inch)	458×610/(18×24)
Releasing film	PET film double sided
Appearance	No problem
HS Code	3919.90.5060
Gross Weight (Kg)	3





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Other Suppliers

清晰科技股份有限公司 sem Chin-Shi Electronic materials Ltd.

Hsinchu, Taiwan (HQ)
124 Zhonghua Rd, Hukou Township,
Hsinchu County 303, Taiwan R.O.C.

CS-5100M9 (Super-High Thermal Conductivity) 9W/m°C)

Technology cooperate with HITACHI CHEMICAL CO., LTD

CHIN-SHI ELECTRONIC MATERIALS LTD.

Specification of Aluminum Based Copper-clad Laminate

Item	Unit		Specification	CS-AL-88/89 AD8 Specification
Insulation thickness	μm	Max Min	150 95	200 75
Solder resistance (288°C)	Sec.	Min	600	600
Thermal shock	288°C*10"/cycle	Min	6 Times	6 Times
Peel strength (Normal status)	lb/in	Min	7.5	9
Breakdown Voltage	V/mil		750	750
Volume resistivity (Normal status >E+14)	Ω•cm		10^{13}	$3.5x10^{15}$
Surface resistivity (Normal status >E+12)	Ω	—	10^{11}	$4.7x10^{14}$
Dielectric constant				
1 MHz Normal status	—		8.0	5.8
1 GHz Normal status			7.6	5.7
Dissipation Factor				
1 MHz Normal status			0.005	0.015
1 GHz Normal status			0.003	0.008
Water absorption	%		0.2	0.2
Thermal conductivity (measured on insulation layer only)	W/m°C		9.0	8.0
Flammability	94V-0		Pass	Pass
Tg	°C		160	100
Td	°C		350	450

3. Compare Ceramic to Organic ERCD

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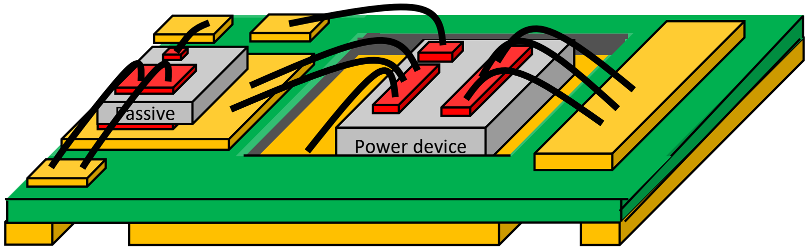
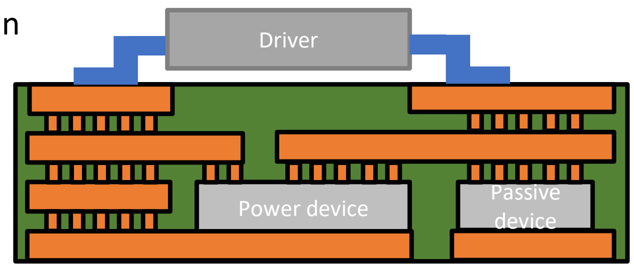
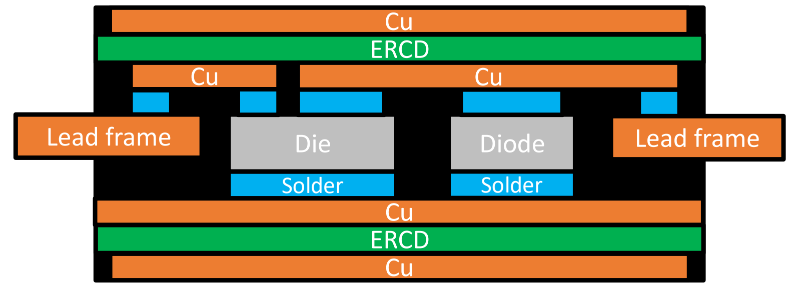
Advanced Concept for Double Sided Cooling



Traditional wire bond version



Wire bond-less version



Double sided power module
for investigation

Infineon FF400R07A01E3 Double Side Cooled IGBT Module

Ref: https://www.autonomousvehicletech.com/articles/1497-infineons-dual-sided-power-module-for-electric-vehicle-systems

Ref: https://www.systemplus.fr/wpcontent/uploads/2018/01/SP18375_Infineon_double_side_cooling_IGBT_flyer.pdf

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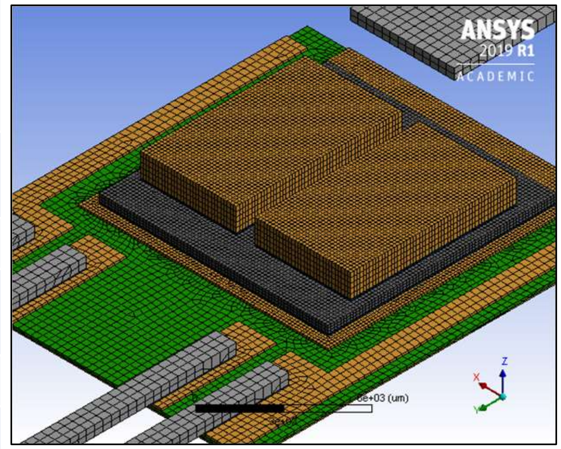
Material Properties for Finite Element Modeling

Compon-ents	Materials	Thickness (mm)	Modulus (GPa)	CTE (ppm/˚C)	Thermal cond'vity (W/mK)
BiDFET	4H-SiC	0.36	347	4.5	380
Spacer	Cu	1	110	17.6	398
Conductor layer on dielectric		ERCD: 0.07 DBC: 0.2			
Solder	Sn5/Pb92.5/Ag2.5	0.1	13.8	28.9	36
	Sn95/Sb5	0.1	50	22.8	46
	Sn96.5/Ag3/Cu0.5	0.1	38.7	21	60
Dielectric	ERCD	0.12	30	14	10
	Al2O3	0.32	310	6	24
Molding	2-Pack type (Epoxy + Hardener)	Dual ERCD:2.18 Dual DBC: 3.1	15	16	3



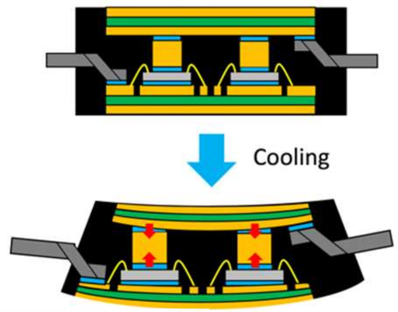
Thermal-Mechanical Analysis – WHAT IS NEEDED

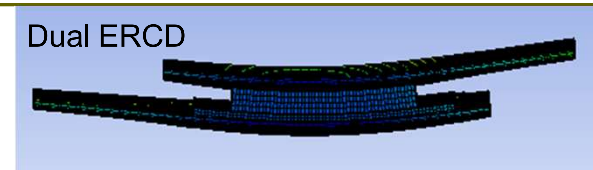
- **Thermal cycling test:**
  - ✓ Temperature range: -40 – 150˚C
  - ✓ Ramp rate of temperature: 19˚C/min
  - ✓ Dwell time : 10 mins
- **Fatigue life prediction:**
  - ✓ Coffin-Manson fatigue life relationship

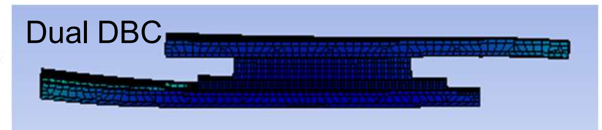
$$N_f = C(\Delta\varepsilon_{eq}^{pl})^{-\eta} \quad \text{where}$$

$$\Delta\varepsilon_{eq}^{pl} = \frac{\sqrt{2}}{3}\sqrt{(\Delta\varepsilon_x^{pl}-\Delta\varepsilon_y^{pl})^2+(\Delta\varepsilon_y^{pl}-\Delta\varepsilon_z^{pl})^2+(\Delta\varepsilon_z^{pl}-\Delta\varepsilon_x^{pl})^2+\frac{3}{2}(\Delta\gamma^{pl})}$$

$$\Delta\gamma^{pl} = \Delta\gamma_{xy}^{pl2}+\Delta\gamma_{yz}^{pl2}+\Delta\gamma_{zx}^{pl2}$$







- **Anand Viscoplastic Constitutive Model**
  - ✓ Considered rate-dependent plastic behavior and creep behavior
    - Flow Equation

$$\dot{\varepsilon}_p = A\exp\left(-\frac{Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m}$$

    - Evolution Equations

$$\dot{s} = \{h_0(|B|)^a\frac{B}{|B|}\}\dot{\varepsilon}_p;(a>1) \qquad s^* = \hat{s}\left(\frac{\dot{\varepsilon}_p}{A}\exp\left(\frac{Q}{RT}\right)\right)^n \qquad B = 1-\frac{S}{S^*}$$

- **Criteria:**
  - ✓ Fatigue life of SAC305 solder > 1000 cycles
  - ✓ Max. principal stress of SiC die < 250 MPa

- **Thermal-mechanical reliability assessment:**
  - ✓ **Since the failure mode is unknown in the simulation, two common failure criteria are assumed in this study as below.**
  - ✓ The solder layer (SAC305) between spacer and device would experience cyclic tensile and compressive stress due to the CTE mismatch and it can induce fatigue failure. According to the Coffin-Manson empirical equation, the fatigue life can be estimated by the equivalent plastic strain (ε_{eq}^{pl}).
  - ✓ Chip crack is also a common failure mode in TCT. Based on the tensile strength of the SiC material, the maximum principal stress can't exceed 250 MPa.

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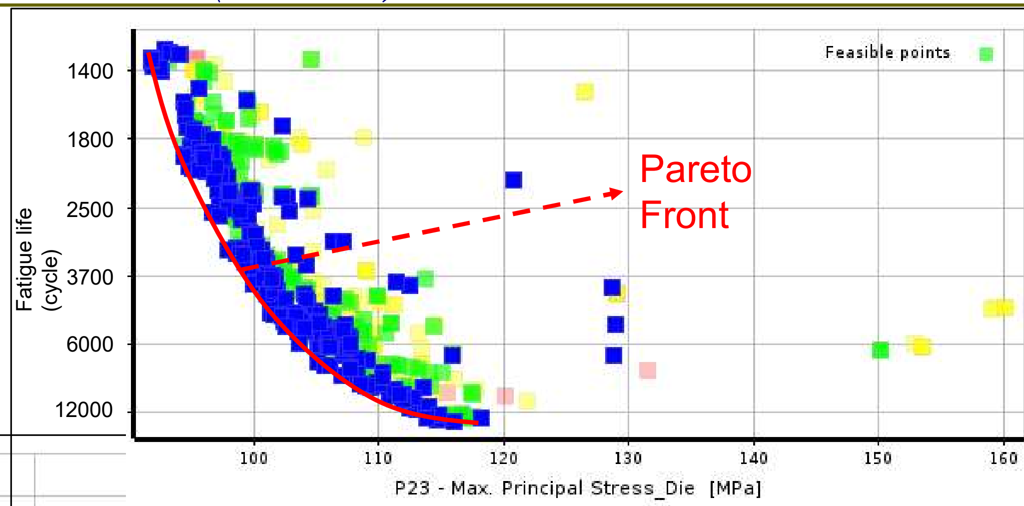
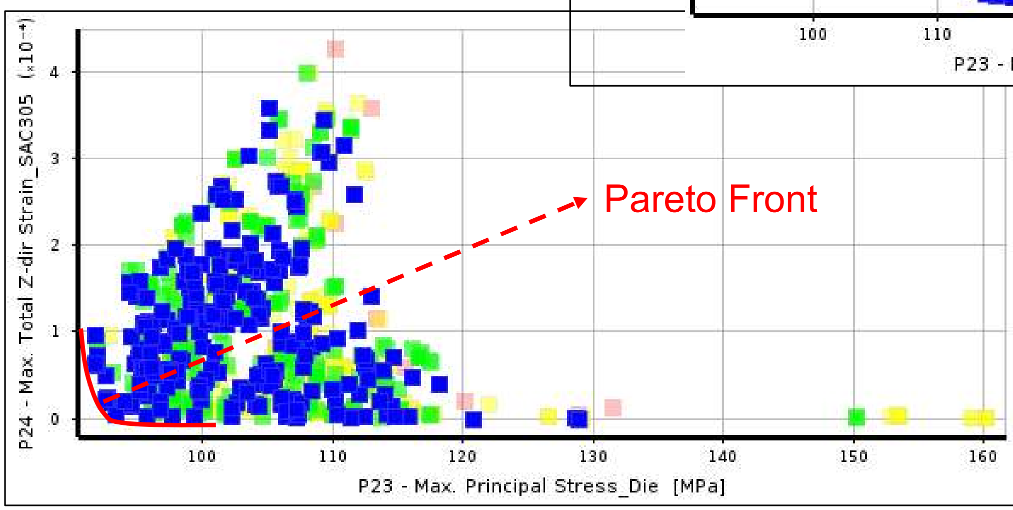
Optimization of Material Selection (con'd)





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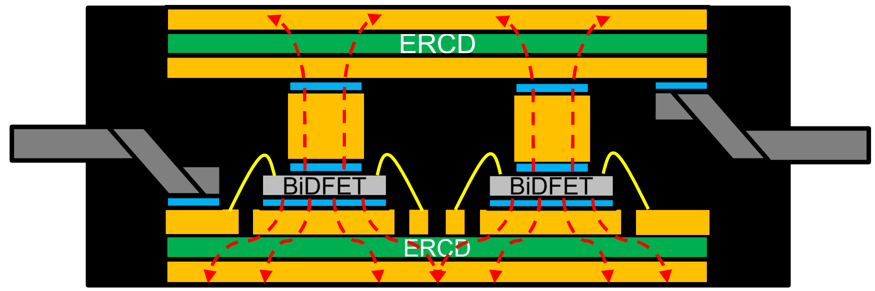
Steady-state thermal analysis

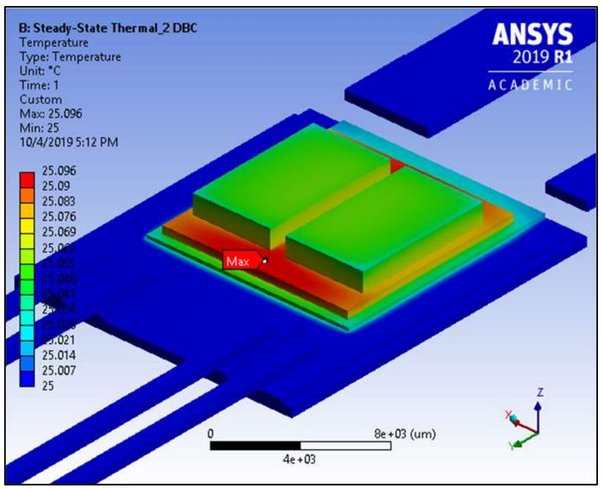
Boundary conditions:

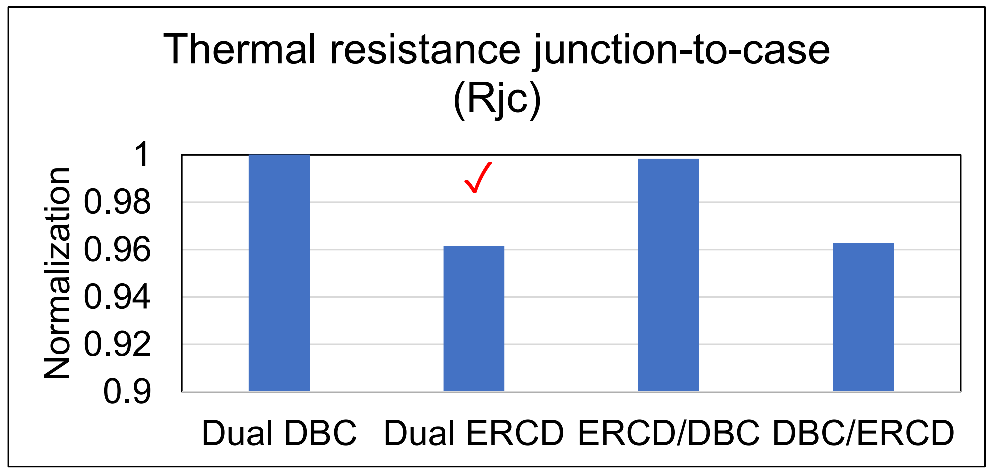
- Infinite heat transfer on top and bottom exposed Cu pads
- Heat sources on die top surface

Thermal resistance:

$$R_{jc} = \frac{T_{j,max} - T_c}{P}$$







The advantage of ERCD material not only provides a competitive thermal and mechanical performance but also a cost effective solution for the advanced power module.

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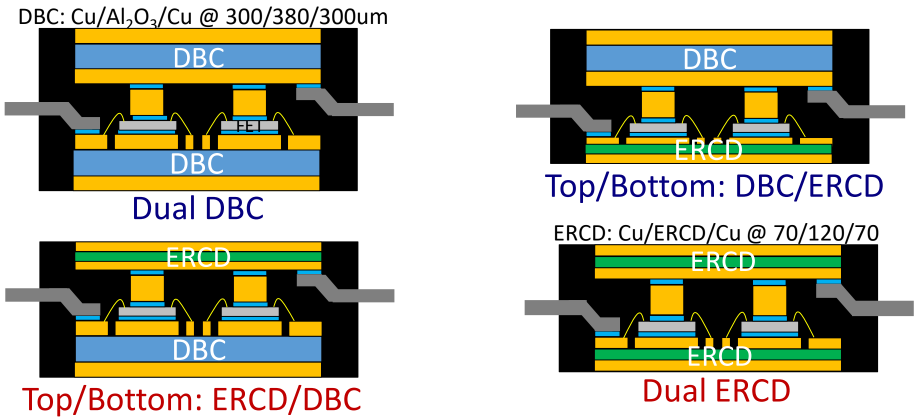
The "Trigger" ERCD vs DBC Performance

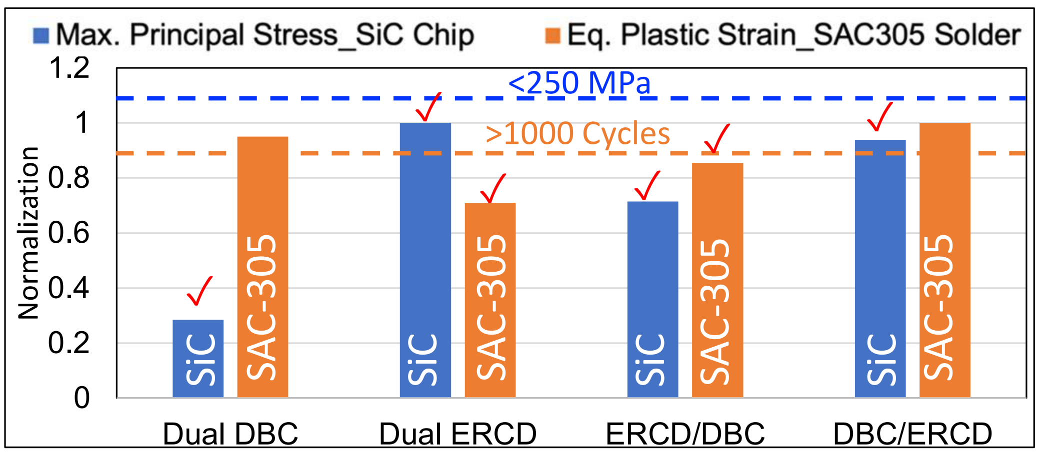
ERCD (Epoxy Resin Composite Dielectric)
by www.risho.co.jp

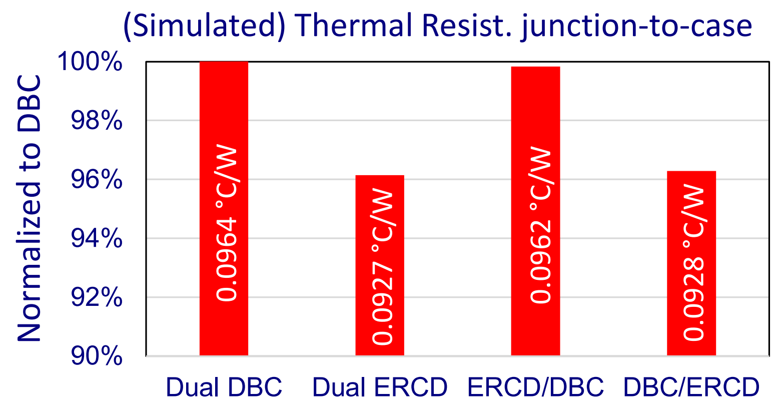
Thermal-mechanical reliability comparison: Only "dual ERCD" and "ERCD/DBC" pass failure criteria for SAC305 and SiC device.



The "trigger" is Organic Dielectric with ≥8W/mK @ 120µm thick. This is better than 380µm (15mil) Al_2O_3 in thermal performance.

[Al_2O_3 Ribbon ceramic at 36W/mK @ 120µm thickness is better that AlN]





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4. Introduce a double-side cooled GaN ½-bridge power module using an Epoxy Insulated Metal Substrate (eIMS)

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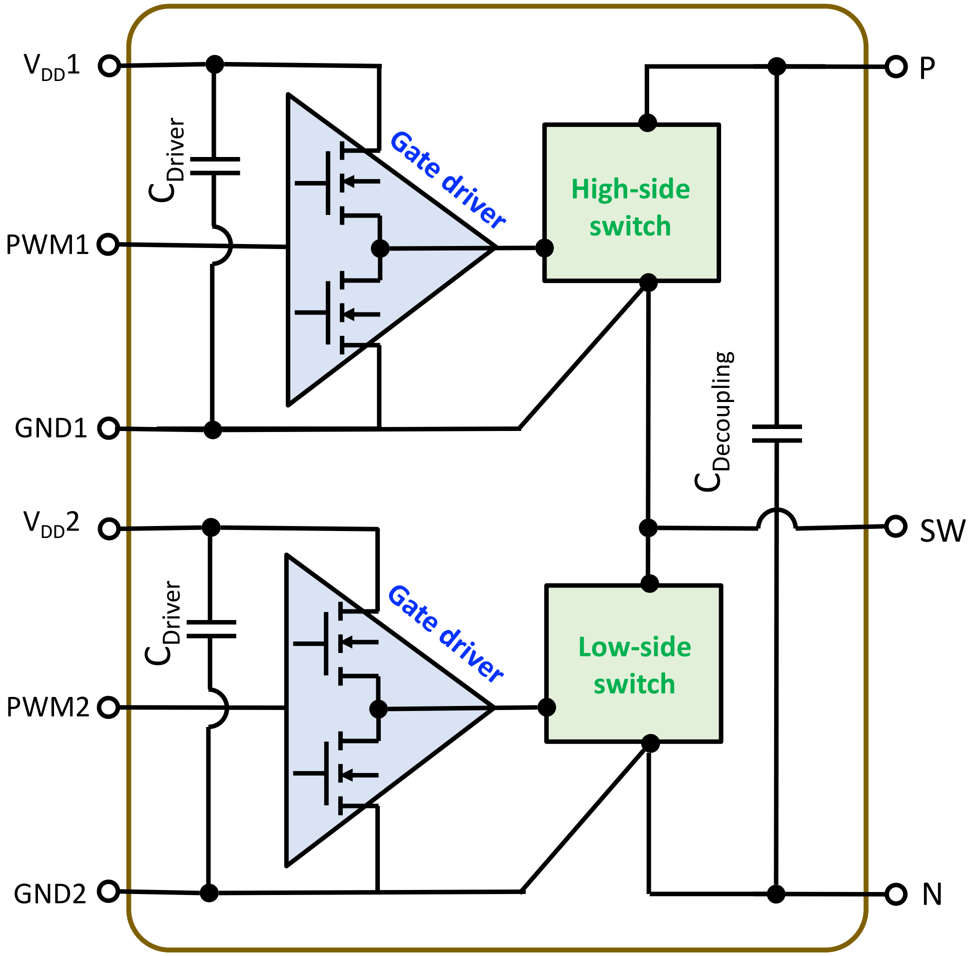
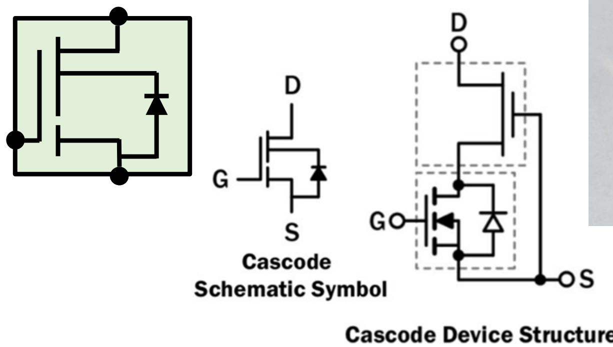
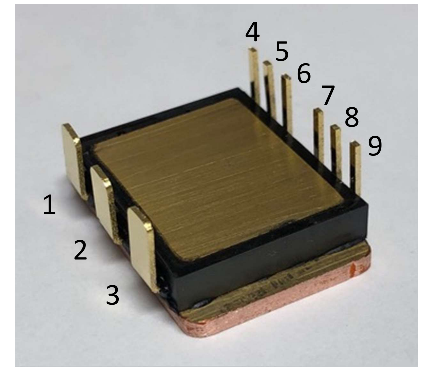
Integrated Power Module Circuit



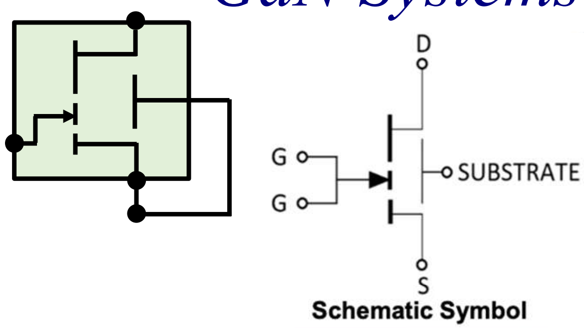
Transphorm





Pin No.	Symbol
1	SW
2	P
3	N
4,9	GND1,2
5,8	PWM1,2
6,7	$V_{DD}1,2$

GaN Systems



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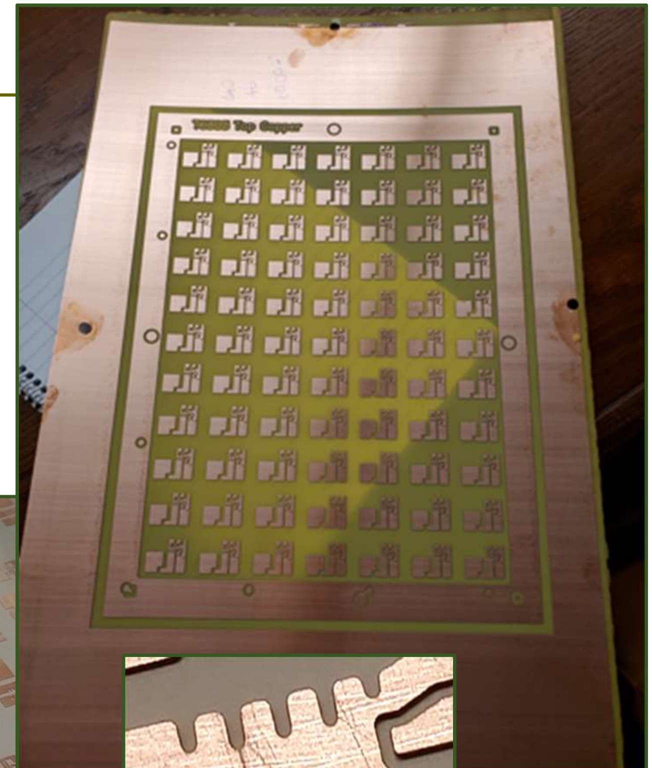
A SIMPLER HIGHER POWER PCB



Brigitflex ordered **1.5’x2’** ERCD B-Stage sheets from RISHO (120µm AD-7210N)

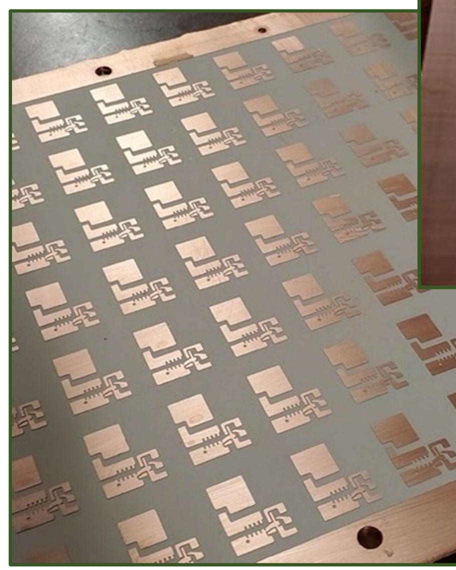
- Trimmed to 0.75’x12’ for top-, 1’x1.5’ for bottom-eIMS plates
- 4oz. Cu on 120µm ERCD laminated onto 2mm Cu baseplates

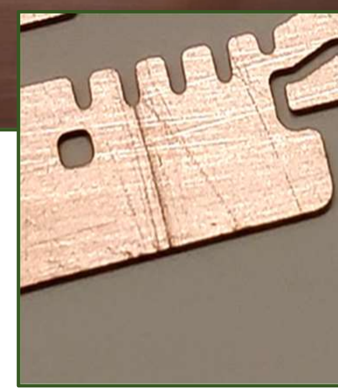
Panel Size eIMS Manufacturing

RISHO KOGYO CO.,LTD
TOKYO OFFICE

LIST of TEST Samples

Product No.	AD-7210N
Material	High Thermal Bonding Sheet (10W/mk)
Production Lot No.	AK6-X419-4
Quantity(sheets)	15
Dielectric nominal thickness(mm)/(mil)	0.12/(5mil)
Panel size(mm) /(inch)	458×610/(18×24)
Releasing film	PET film double sided
Appearance	No problem
HS Code	3919.90.5060
Gross Weight (Kg)	3





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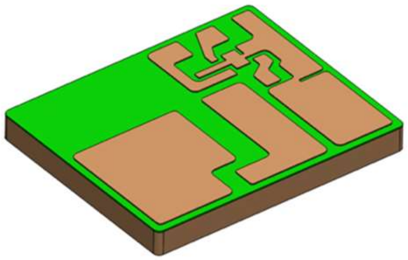
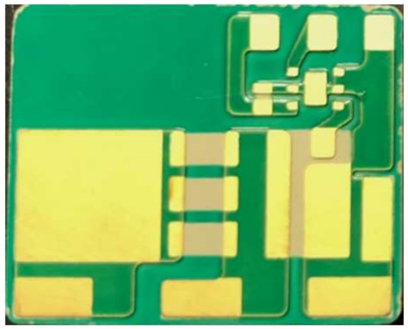
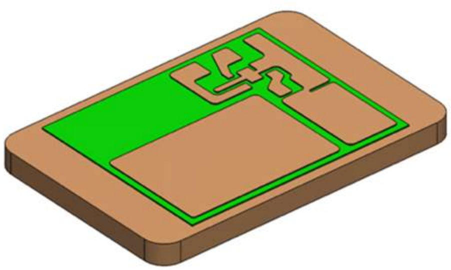
IPM Substrates for Assembly

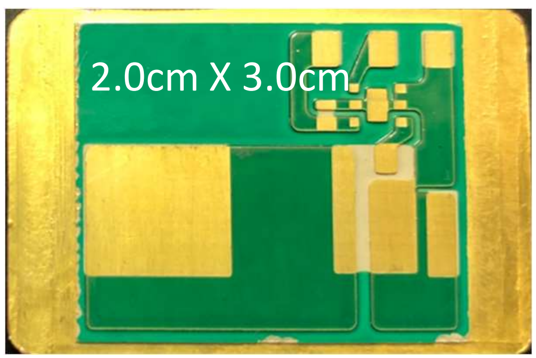
Transphorm on eIMS Substrates





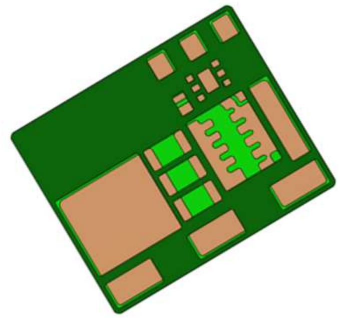
Top (T1-smaller)
Substrate

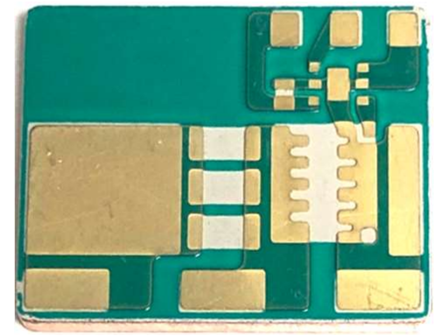




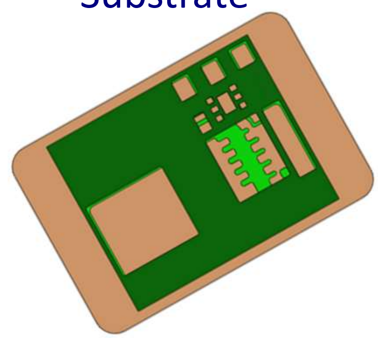
Bottom (T2-longer)
Substrate

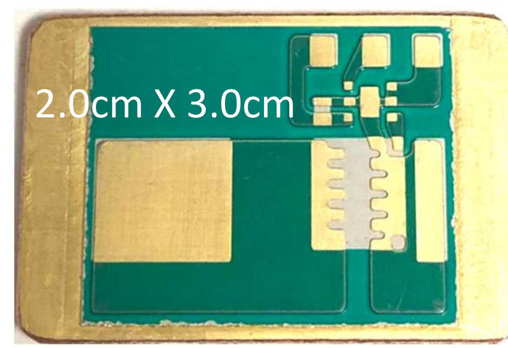
GaN System on eIMS Substrates





Top (T1-smaller)
Substrate





Bottom (T2-longer)
Substrate

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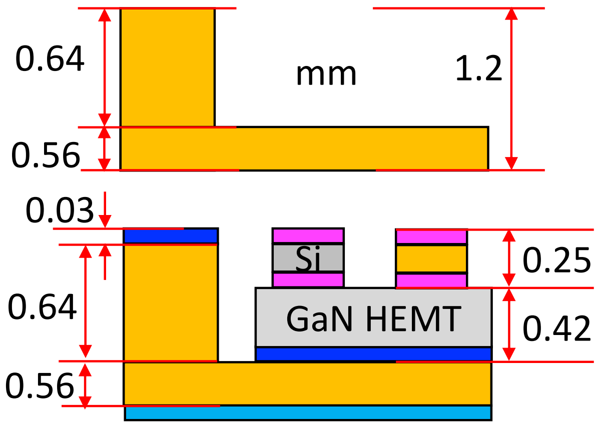
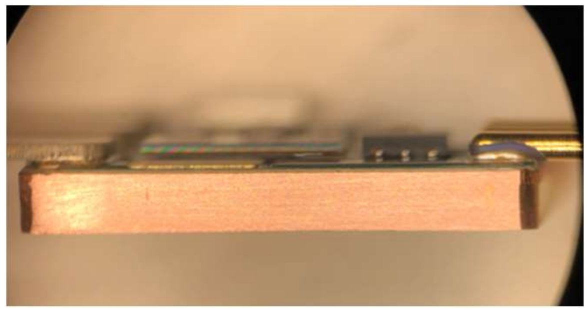
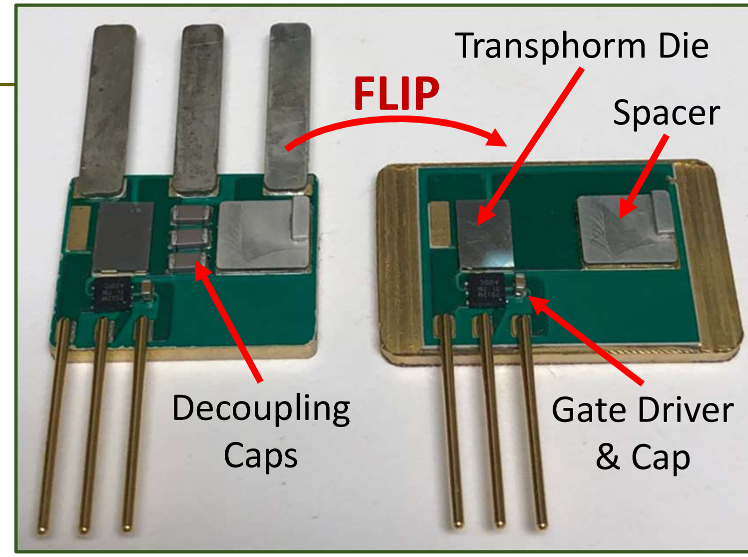
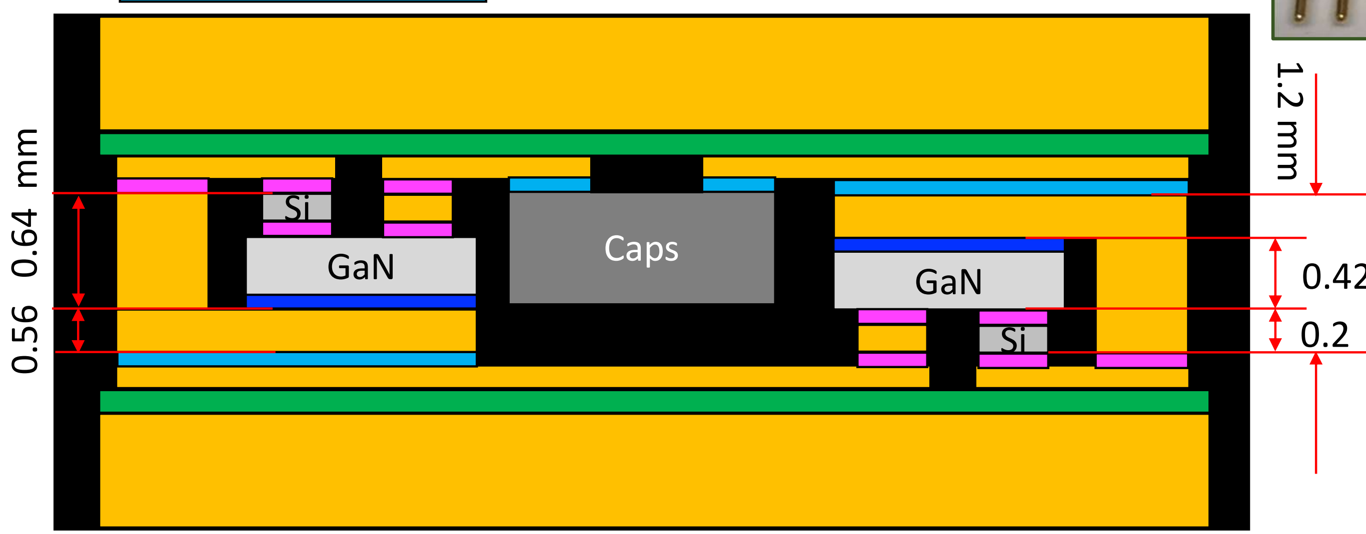
Transphorm IPM Structure









Thickness of each component:

- Decouple C (1206): 0.85mm
- Cu Trace/ERCD: 4oz Cu/120um
- IMS Cu baseplate:2mm
- GaN die: 0.39 mm
- SiFET: 0.17 mm
- Driver: 0.75 mm
- Driver Cap: 0.8 mm
- Cu Spacer: 1.2 mm
- Pin terminal: 0.6 mm

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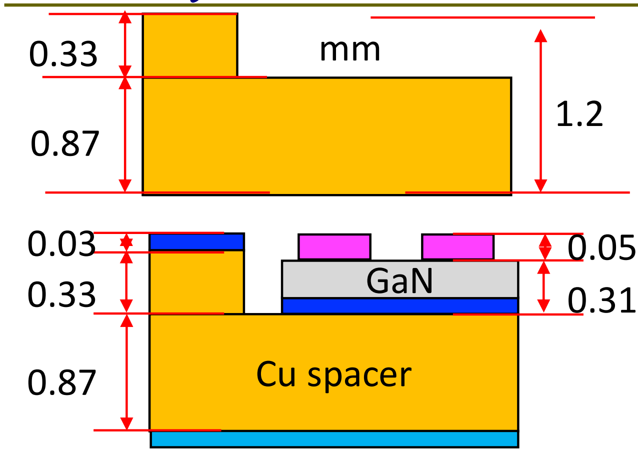
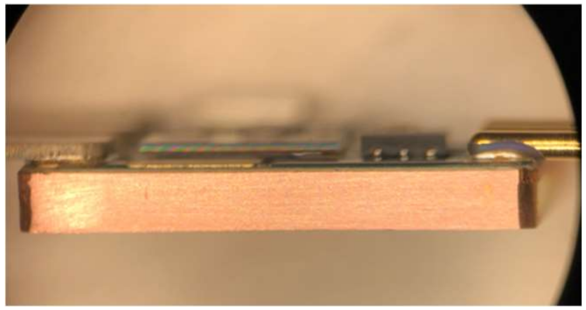
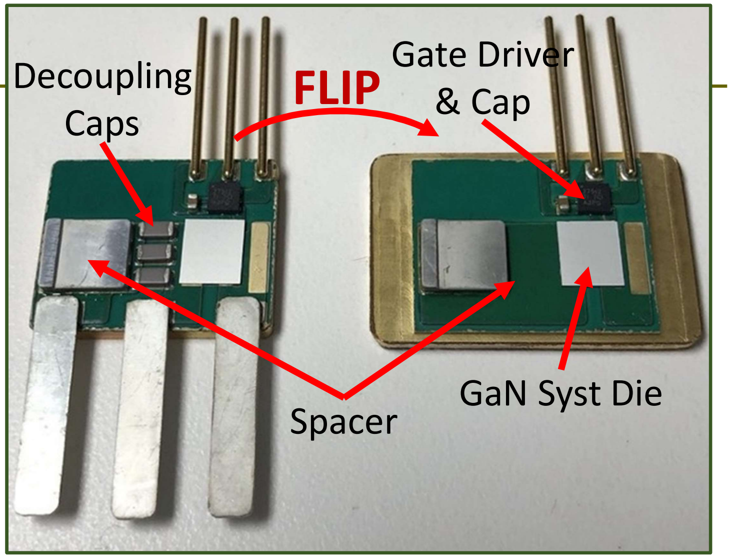
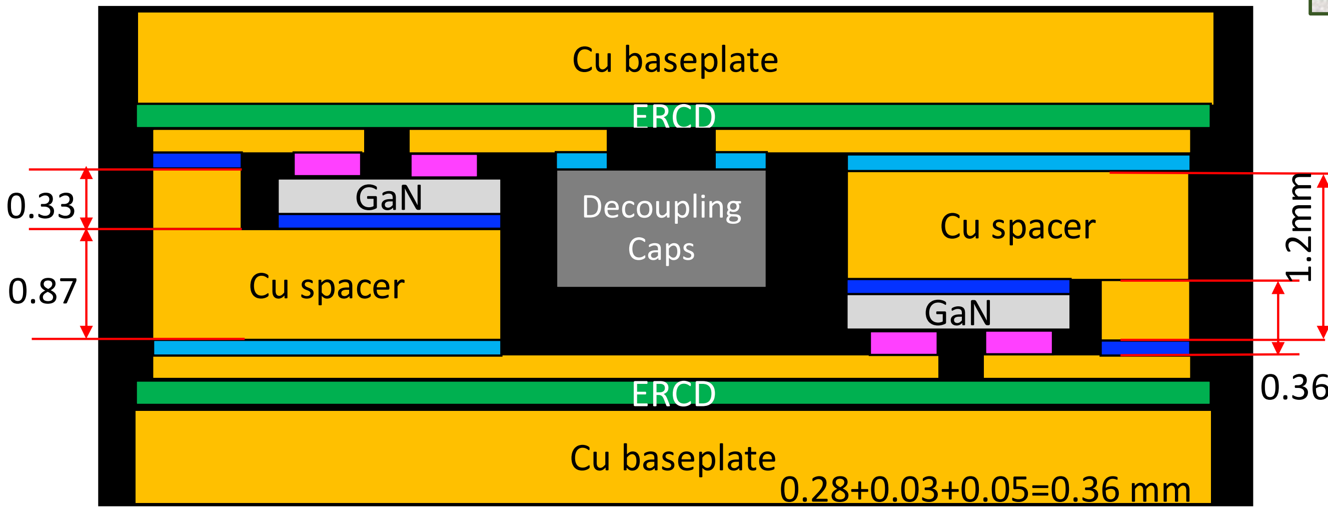
GaN Systems IPM Structure









Thickness of each component:

- GaN die: 0.28 mm
- Driver: 0.75 mm
- Driver C: 0.8 mm
- Cu Spacer: 1.2 mm
- Pin terminal: 0.6 mm
- Decoupling C (1206): 0.85 mm
- IMS: 4oz Cu/120um ERCD/2mm Cu baseplate

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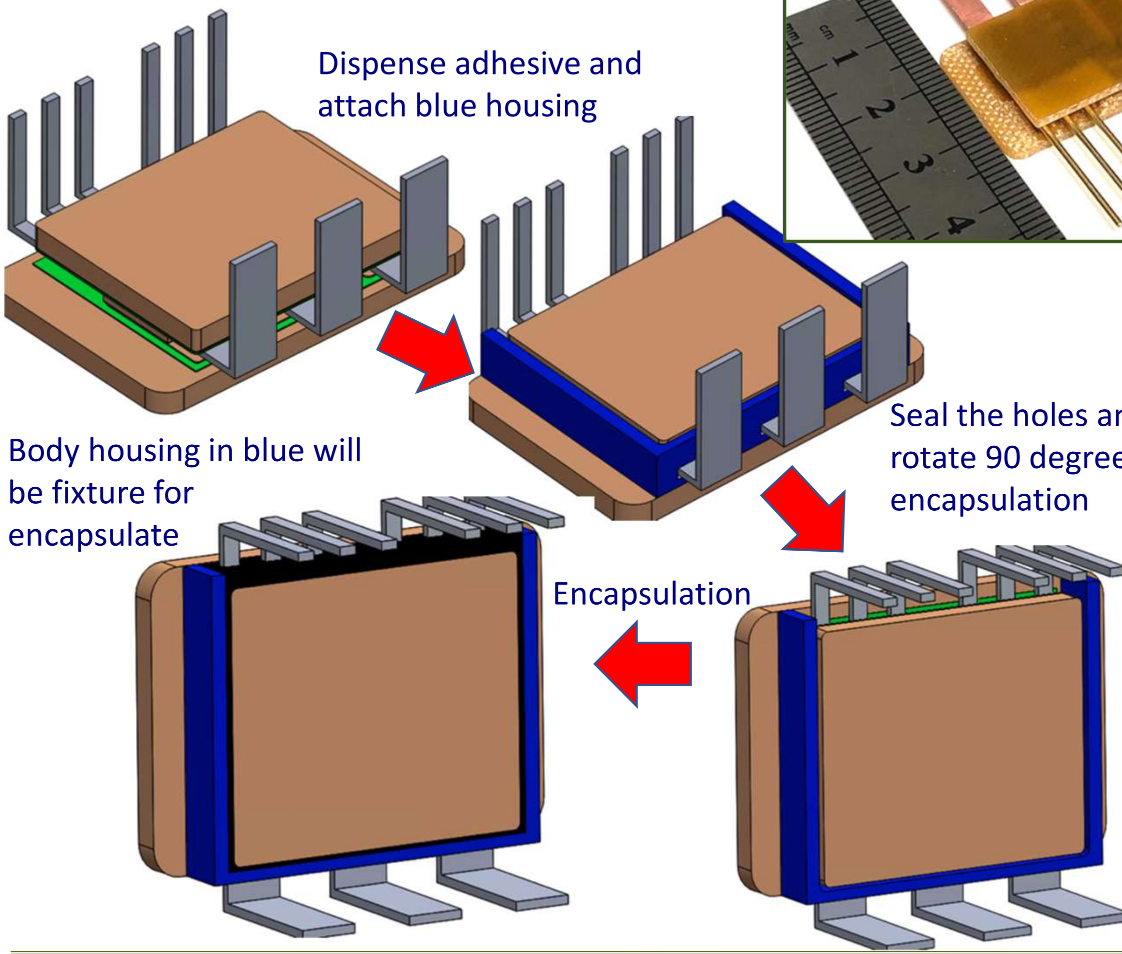
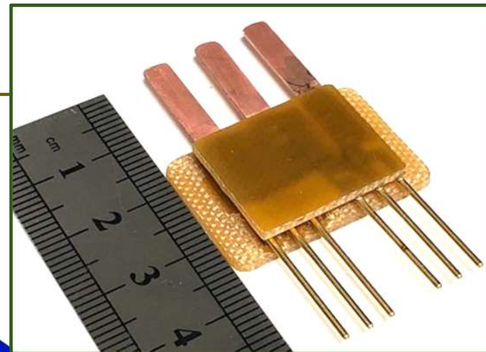
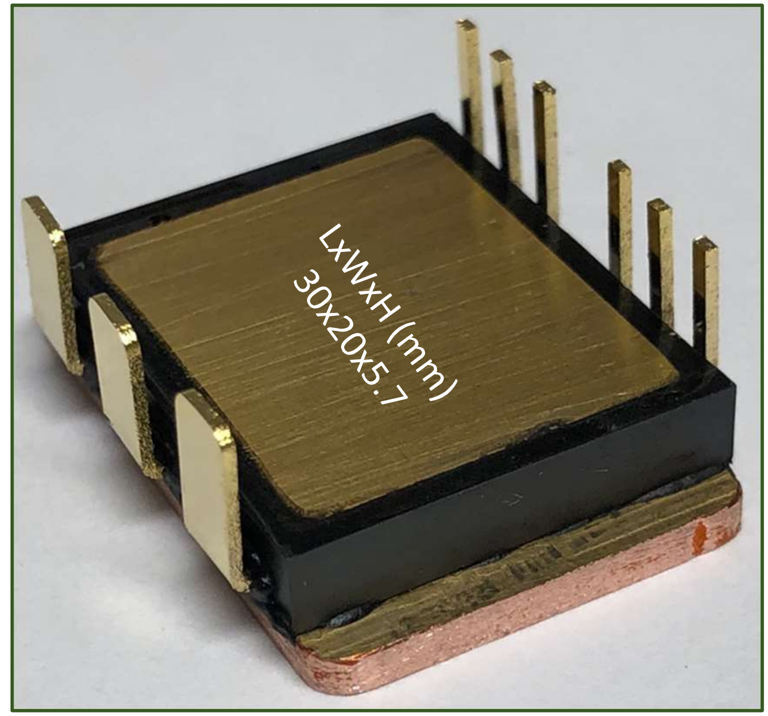
IPM Assembly Steps







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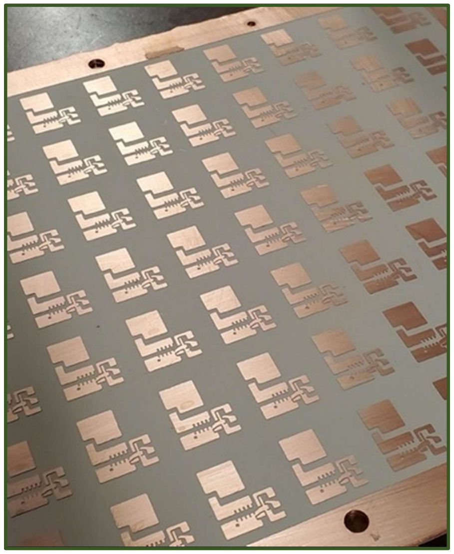
IPM BOM & ERCD Patterned Panel

Component	Specification	Pcs.	Supplier/Mfg	Link/Note
Cascode GaN	650V/15mΩ	2 pcs	Transphorm	https://www.transphormusa.com/en/
GaN E-HEMT	650V/18mΩ	2 pcs	GaN Systems	https://gansystems.com/
Gate driver	Part number: UCC27512DRSR WSON PKG 3x3x0.8 mm	2 pcs	Texas Instr.	https://www.digikey.lu/product-detail/en/texas-instruments/UCC27512DRSR/296-34812-1-ND/3523717
Gate driver capacitor	Part number: CGA3E1X7R1E105K080AC 25V/1uF/0603	2 pcs	TDK	https://www.mouser.com/ProductDetail/TDK/CGA3E1X7R1E105K080AC?qs=NRhsANhppD9VxGl2AsmRpw%3D%3D&countrycode=US&currencycode=USD
DC link capacitor	Part number: CGA5F4NP02J472J085AA 630V/4.7nF/1206	3 pcs	TDK	https://www.mouser.com/ProductDetail/TDK/CGA5F4NP02J472J085AA?qs=sGAEpiMZZMvsSlwiRhF8qtYrDJZp5VWMvuhc8o6DvzFff%252B36HvyUUw%3D%3D
eIMS	4oz Cu/120um dielectric/2mm Cu	2 pcs	Risho/ Brigitflex	Material Supplier: https://www.risho.co.jp/english/ Manufacturer: http://www.brigitflex.com/
Spacer	7.1x7.9x1.2mm Cu	2 pcs	Hanz Mfg	https://hanzmanufacturing.com/
Power termn'l	4x12x0.6mm Cu	3 pcs	Hanz Mfg	https://hanzmanufacturing.com/
Signal termn'l	1x12x0.6mm Cu	6 pcs	Hanz Mfg	https://hanzmanufacturing.com/
Epoxy Encapsulant	Tg=219˚C	966 mm^3	Risho	https://www.risho.co.jp/english/



Patterned ERCD from Brigitflex processed 9x12" and 12x18" panels for T1/T3 (Top) and T2/T4 (Bottom) for Transphorm/GaN Syst, respectively.

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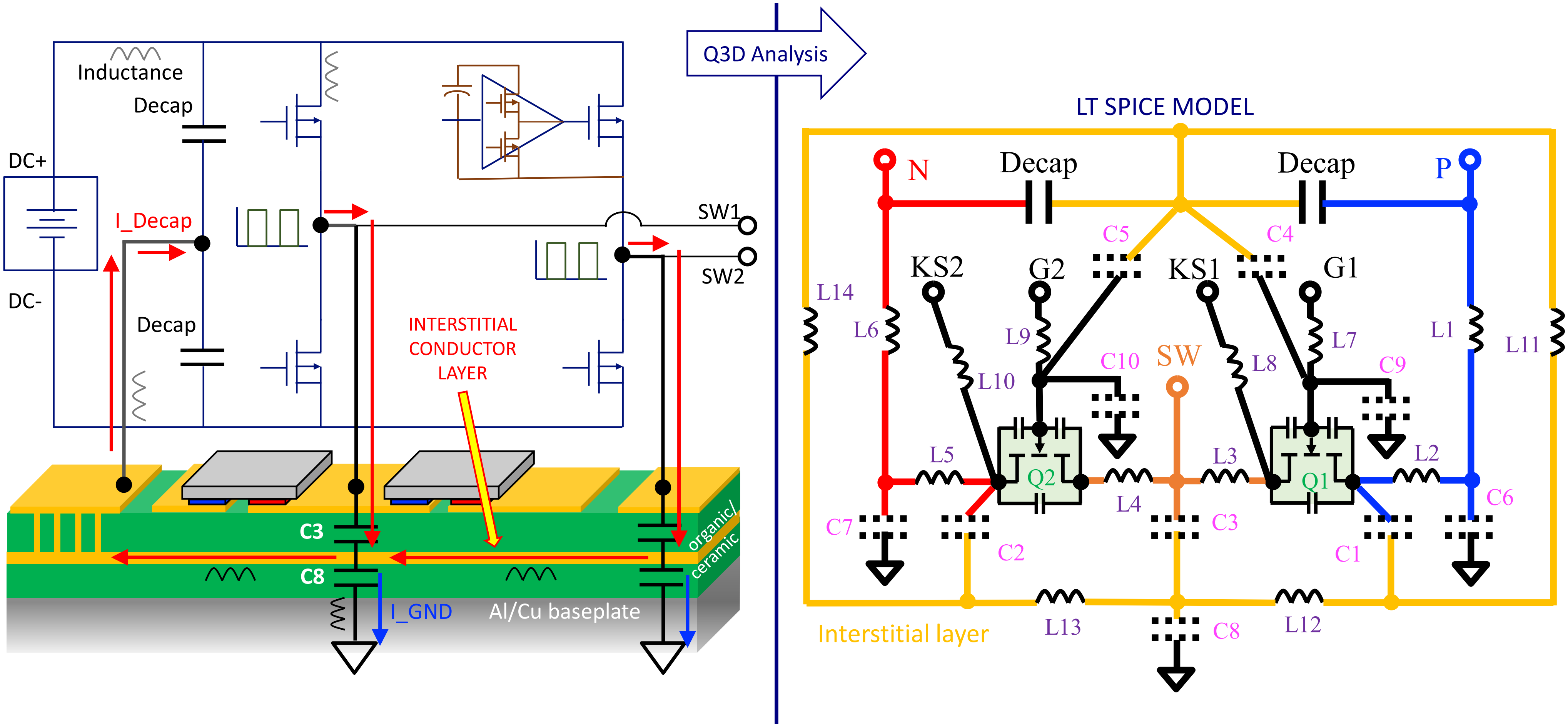
Use of Muti-Conductor Planes (Interstitial Layers, e.g. in PCBs)



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4a. Supply Chain

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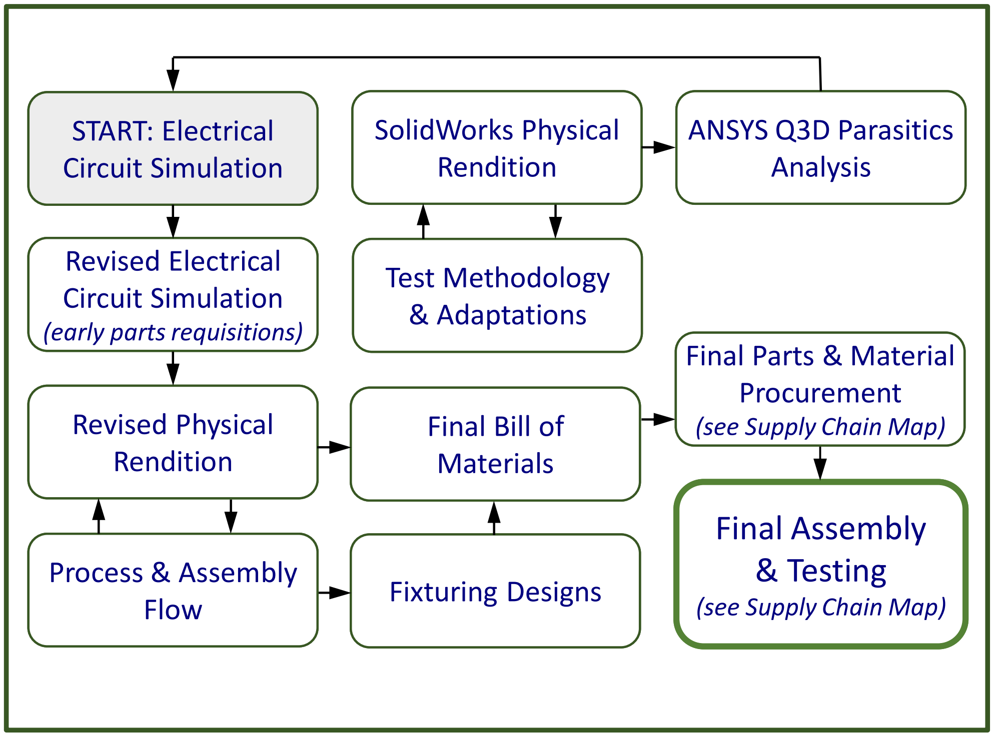
Design Flow & Supply Chain



N. Mescia
6/4/2022

ERCD PCB Mfgrs & Assemblers

PCB MFGR’	ADDRESS	PANEL SIZE
Amitron	2001 Landmeier Road | Elk Grove Village, IL 60007	18"x24"
Aurora	2250 White Oak Circle, Aurora, IL 60502	
Brigitflex	1725 Fleetwood Drive, Elgin IL 60123	21"x41"
Electronic Interconnect	2375 Estes Avenue, Elk Grove Village, IL 60007	
TCI (Taihong Circuit Ind. Co., Ltd.)	No.81, Guangfu Rd., Hukou Township, Hsinchu County 303, Taiwan (R.O.C.)	20"x24" (510x610 mm)

MODULE ASSEMBLY	ADDRESS	WEBSITE
NCSU-PREES	N. C. State University Raleigh, NC 27606 USA	www.prees.org
IMI	North Science Avenue Special Export Processing Zone Laguna Technopark, Binan, 4024, Laguna, Philippines	https://www.global-imi.com/markets/automotive
Starpower	Ai Ciòss, CH-6593 Cadenazzo, Switzerland	https://www.starpowereurope.com/en
ASE	No.550, Chung-Hwa Rd. Sec. 1, Chung-Li, Taiwan (ROC)	https://ase.aseglobal.com/en

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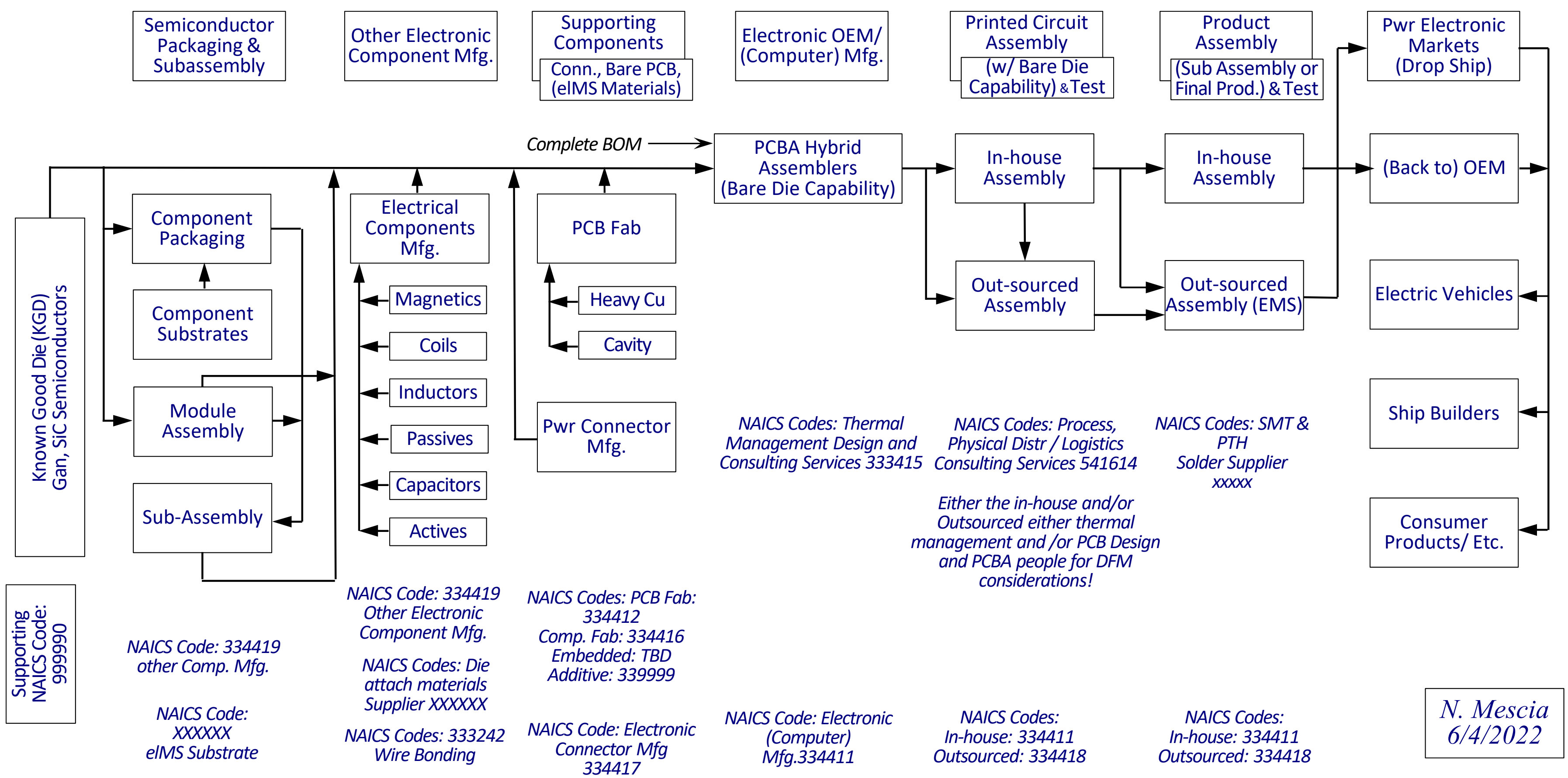
Typical IPM/Converter Supply Chain (including eIMS)



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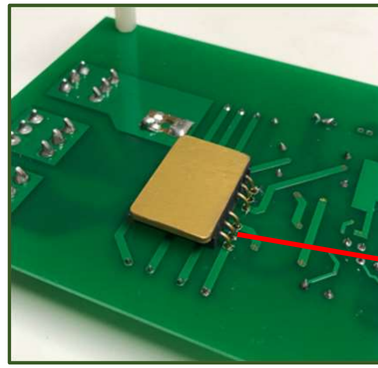
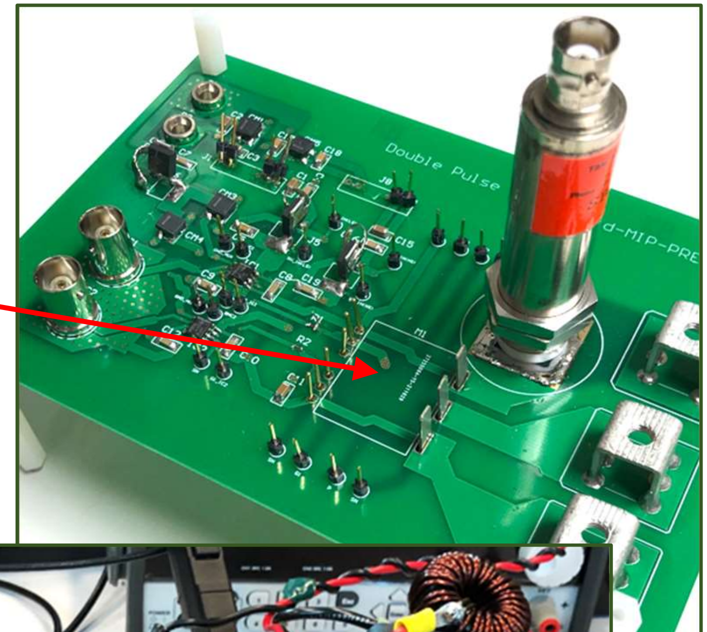
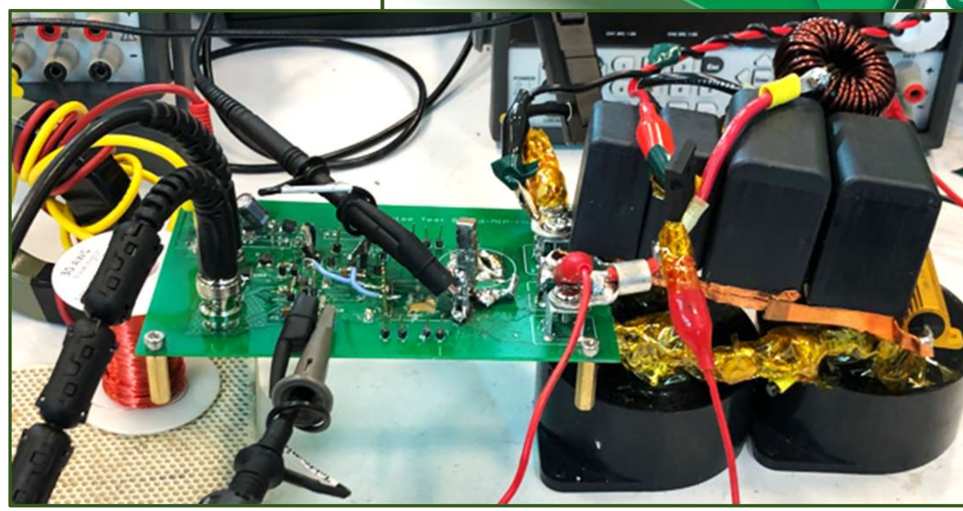




Ultra High Frequency Double Pule Testing

(Continued with revisions underway-Aug'22)



By Sourish Sinha, PhD student

- Developed Double Pulse Tester (DPT)
- Initial tests:
  - GaN Sys IPM is more sensitive to CM
  - Transphorm fast, but with high Ciss
  - Module revisions underway
- Refined Q3D model.

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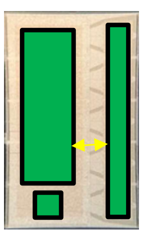
Q3D & Thermal Comparison for Transphorm & GaN Systems IPMs

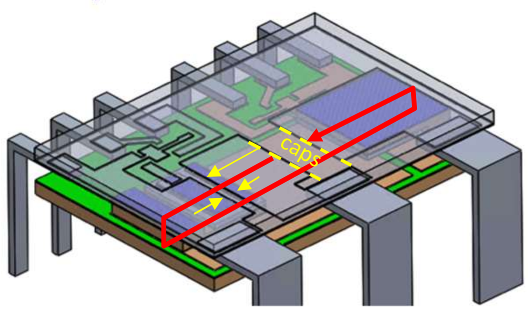
Commutation Loop Inductance	Value (nH)			
	DC	1 MHz	10 MHz	100 MHz
Transphorm IPM	2.99	1.51	1.50	1.50
GaN Systems IPM	2.51	1.18	1.18	1.18

T_a = 50˚C, $T_{c,max}$ = 90˚C P_1/P_2=12.5W (>98% eff)	Transphorm Baseplate		GaN Systems Baseplate	
IMS type	Cu	Al	Cu	Al
h coefficient (W/m²K)	1450	1585	1450	1570
Tj,1 (˚C)	97.2	96.6	97.2	96.8
Tj,2 (˚C)	99.1	98.5	101.3	101.3
Rjc,eq (˚C/W)	0.36	0.34	0.45	0.45
Rja,eq (˚C/W)	1.96	1.94	2.1	2.1
Pd,max (W)	51.0	51.5	48.7	48.7

Transphorm

4.7x7.1 mm

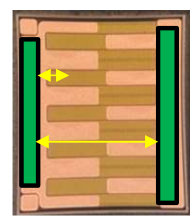


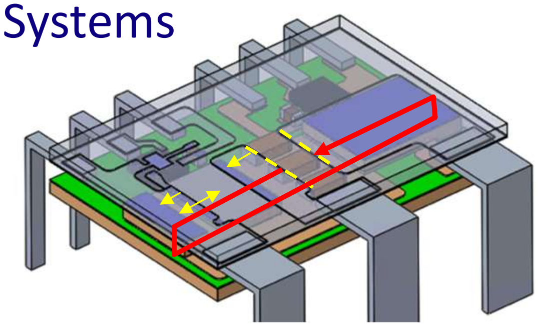


Size: 20 x 30 x 4.24 mm
(excludes terminals)

GaN Systems

5.6x6.6 mm





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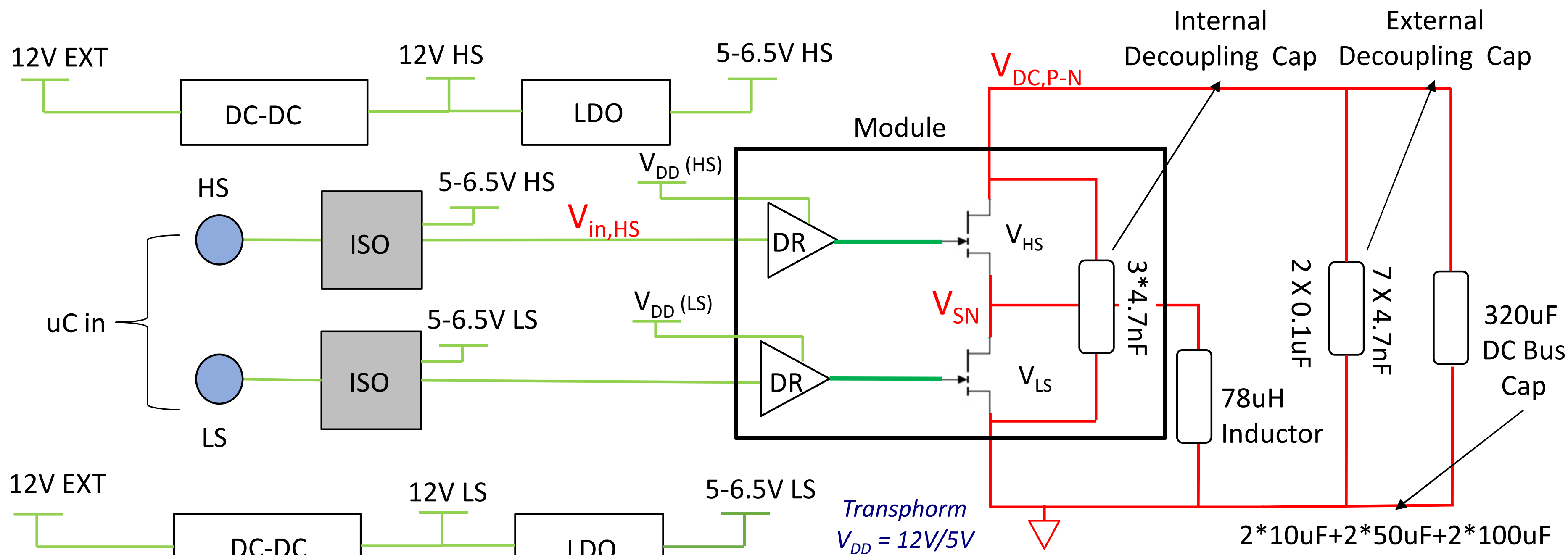
DPT Circuit for Transphorm & GaN Systems



I_{avg} = 6.6kW/210V @50%$_{dcy}$ ➔ ~15.7A per sw.

- Voltage probes are 1GHz BW, probe capacitance 3.9pF; current probes 120MHz.
- "P"=+DC, "N"=-DC, "SN"=Switch Node, "in,HS"= PWM input to High Side driver
- The "V_{DD}" is power supply to internal gate driver
- Test results are for High Side (HS) switch, Low Side (LS) switch is similar.
- In contrast to Transphorm recommendation: No Bus snubber, device snubber, gate ferrite beads or gate resistance.

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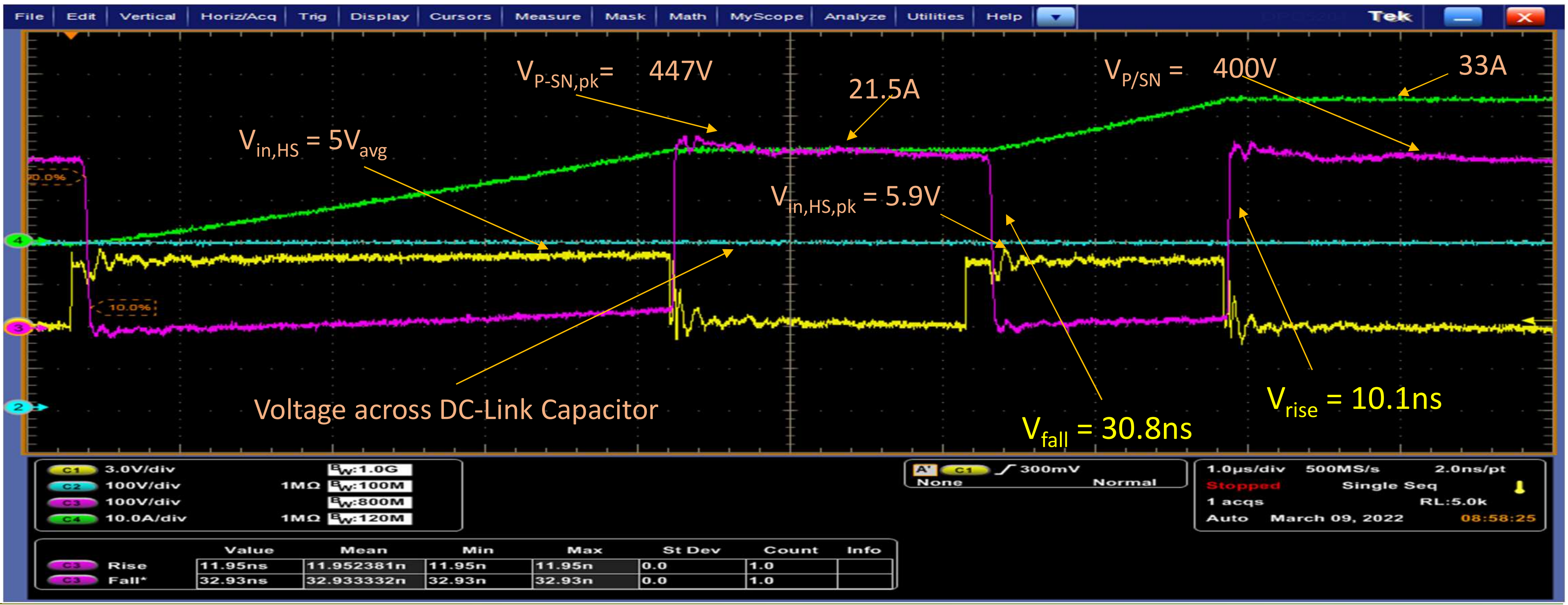
Transphorm: 400$V_{P\text{-}N}$ /33A (5V V_{DD})

V_{rise} = 10.1 ns
V_{fall} = 30.8 ns

When inductor current increased, the $V_{P\text{-}SN}$ increased in voltage magnitude during the device ON state possibly due to the long on time, which would not occur during high frequency switching converter operation.
With higher inductor current the voltage rise time starts reaching datasheet values and fall time stays constant.



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Conclusion for Transphorm IPM Performance

- Without gate resistance, ferrite bead and bus snubber, as mentioned by Transphorm for their packaged device, it is difficult to run the device beyond 300V/18A without false tripping with V_{gs} *= 12V* in the present PREES-FREEDM DPT circuit
- However, devices were run successfully at *400V/18A* and *400V/33A* with V_{gs} *= 5V* (matching end application of 6.6kW EV charger). The V_{tr} *was* close to the datasheet value and V_{tf} *= 12ns* a bit more.

t_R	Rise time	–	18	–	ns	V_{DS}=400V, V_{GS}=0V to 12V, R_G=15Ω, Z_{FB}=120Ω at 100MHz, I_D=60A
$t_{D(off)}$	Turn-off delay	–	123	–		
t_F	Fall time	–	9.4	–		

- With a V_{gs} *= 9-10V*, no gate resistance, ferrite bead, or bus snubber it might be possible to test the devices at *400V/18A* and higher without false tripping. A new DPT tester is in fabrication (July'22)

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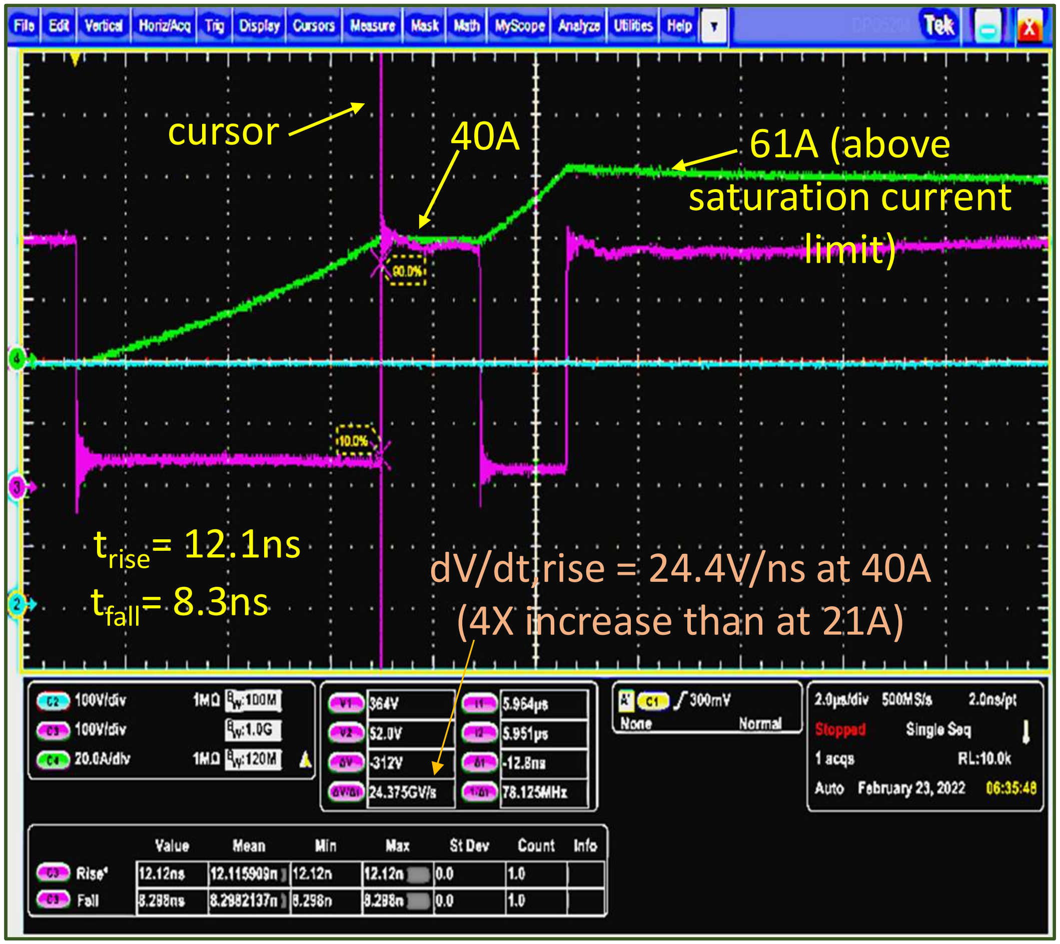
GaN Syst IPM: 400V/40A (650V/30A datasheet comparison)

V_{rise} = 12.1 ns
V_{fall} = 8.3 ns



Impact: PCB Board, integrated gate driver & parasitics

Parameter	Impact	650V/30A/50μΩ GS66508B
Qg (nC)	Switching speed & Switching frequency	5.8
Coss (pF)		65
tdelay(on) / tdelay(off) (ns)		4.1 / 8.0
t_rise / t_fall (ns)		4.9 / 3.4
Eon / Eoff (μJ)	Efficiency	47.5 / 7.5 (Vds 400V/Ids 15A)
Eoss (μJ)		7
Qrr (μC)		0
trr (ns)		0

SUMMARY DPT TEST RESULTS *dt* vs I_D

I_D	t_{rise}	t_{fall}
10.5 (A)	44.5 (ns)	8.9 (ns)
28 (A)	35.0 (ns)	8.5 (ns)
33 (A)	15.7 (ns)	8.0 (ns)
40 (A)	12.1 (ns)	8.3 (ns)

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Leakage Currents of IPMs

GaN Systems: 21mΩ(typ.) @ Vgs=6V
Transphorm: 15mΩ(typ.) @ Vgs=10V
18mΩ(max.) @ Vgs=10V

GaN Systems

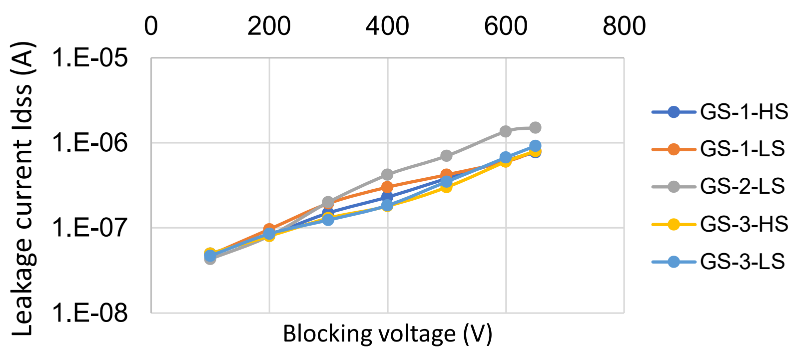
Drain to Source Leakage Current	I_{DSS}		6		µA	V_{DS}= 650 V, V_{GS}= 0 V
Gate to Source Current	I_{GSS}		732		µA	V_{GS} = 6 V, V_{DS} = 0 V

Transphorm

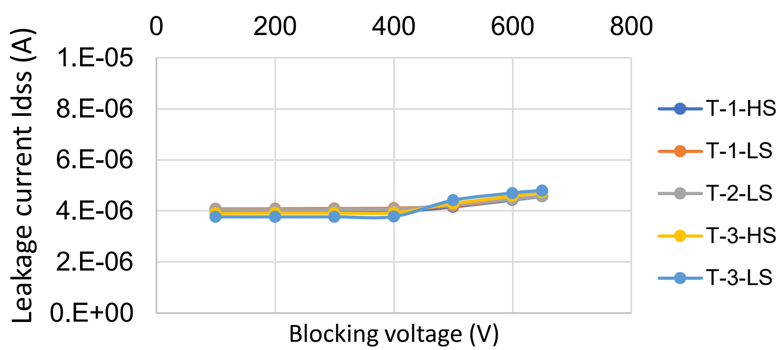
I_{DSS}	Drain-to-source leakage current	–	7	70	µA	V_{DS}=650V, V_{GS}=0V
		–	50	–		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	–	–	400	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	–	–	-400		V_{GS}=-20V

Sample	Rdson (mΩ)	Blocking Voltage Vds @ Vgs=0 (V)	Leakage current Idss (uA)
GS-1-HS	14.97 (Vgs=6V)	650	0.77
GS-1-LS	15.30 (Vgs=6V)	650	0.80
GS-2-HS	NA (one pin broken)	NA (one pin broken)	NA (one pin broken)
GS-2-LS	15.22 (Vgs=6V)	650	1.50
GS-3-HS	15.48 (Vgs=6V)	650	0.80
GS-3-LS	15.32 (Vgs=6V)	650	0.92
T-1-HS	9.72 (Vgs=10V)	650	4.57
T-1-LS	10.03 (Vgs=10V)	650	4.58
T-2-HS	NA (Gate leaky)	NA (Gate leaky)	NA (Gate leaky)
T-2-LS	9.85 (Vgs=10V)	650	4.37
T-3-HS	10.13 (Vgs=10V)	650	4.73
T-3-LS	10.21 (Vgs=10V)	650	4.8

GaN Systems Module



Transphorm Cascode Module



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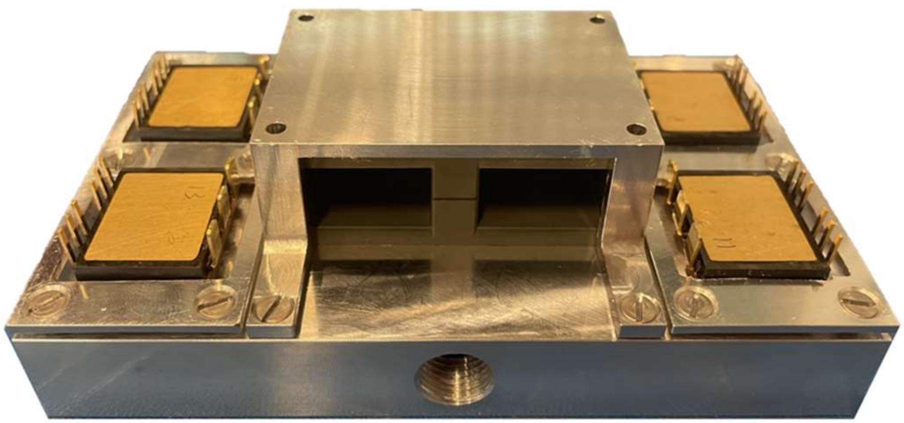
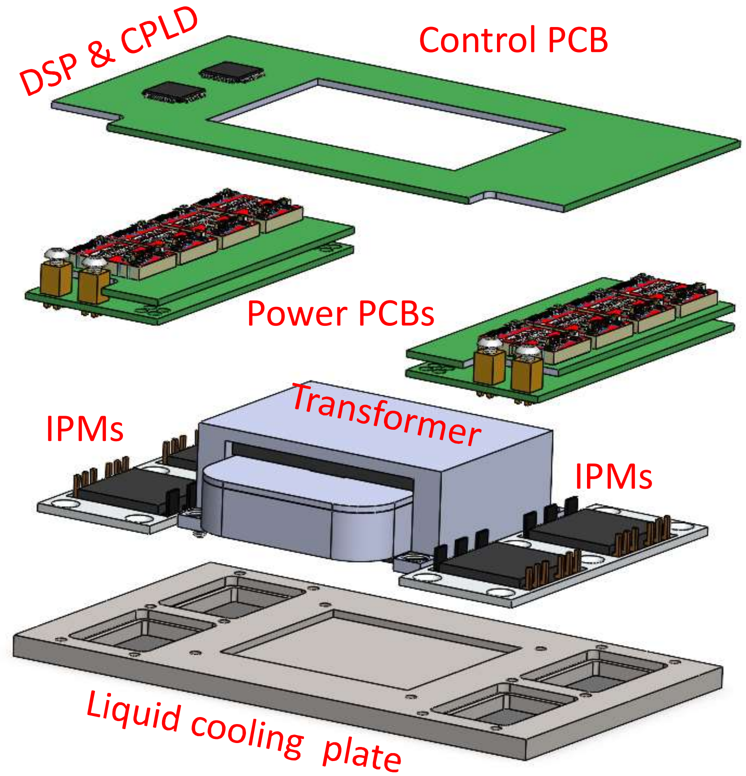
Demo GaN Modules in 400V/6.6kW/ 1MHz Charger

Co-PI: Prof. Wensong Yu

Dakai Wang, PhD Student
Xiang Li, Master Student



Vertical integration of GaN IPMs with 1MHz transformer, 6.6 kW resonant power stage, and DSP+ CPLD digital controller



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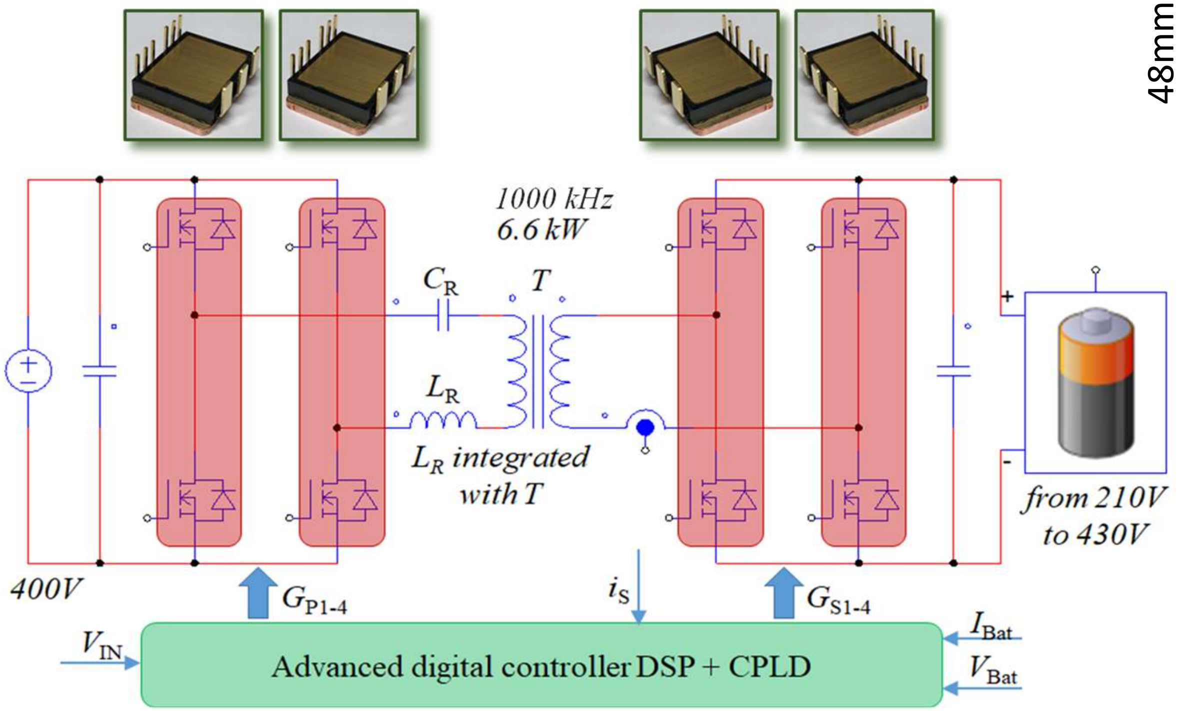
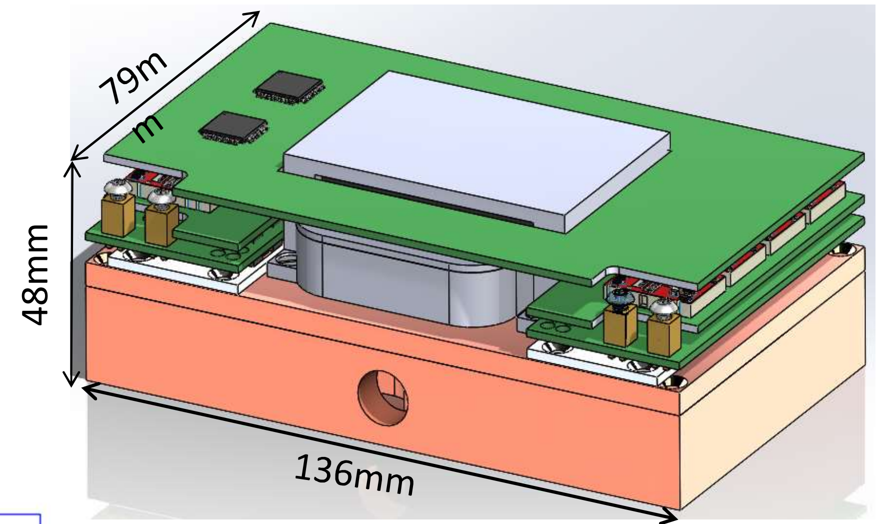
Complete 400V/6.6kW/1MHz/12.7kW/L Charger Using GaN IPMs

- Compact design of 400V/6.6kW, 1MHz charger demonstrator
  - 12.7kW/L (209 W/in3) power density including cooling plate
- Efficient liquid cooling design for both IPMs and transformer
  - Optimized cooling pattern for IPMs and transformer





- Power topology: LLC converter + digital control, using four half-bridge GaN IPMs
- Prototype modules used in final physical layout

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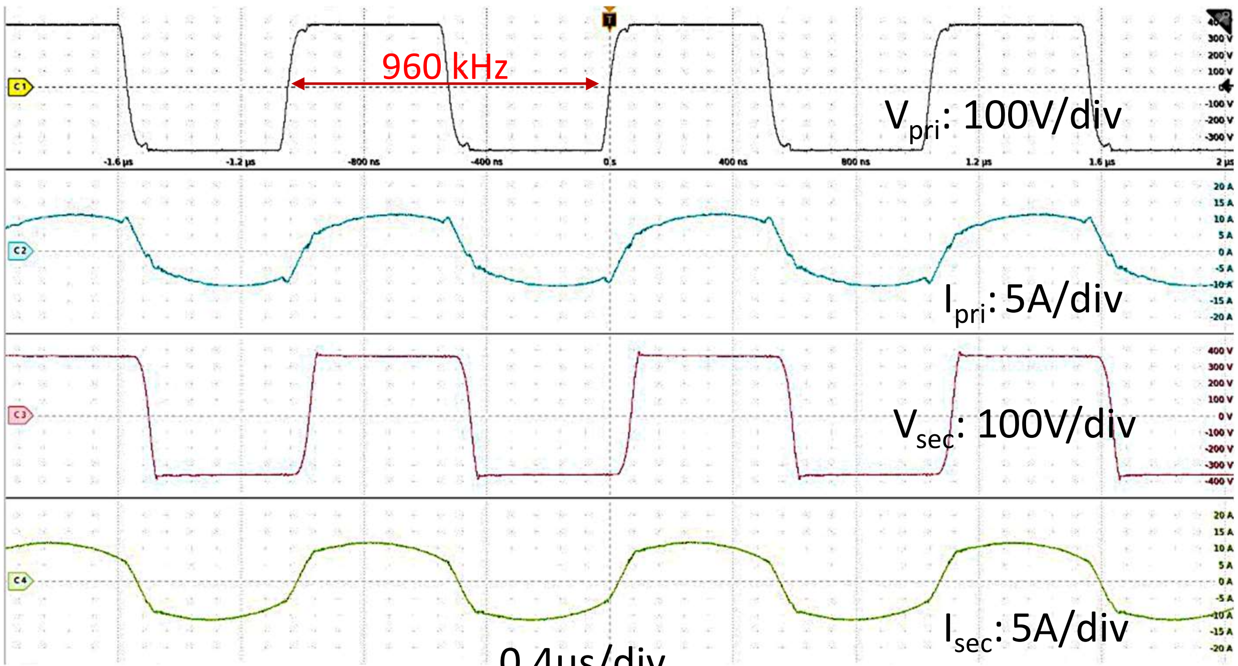
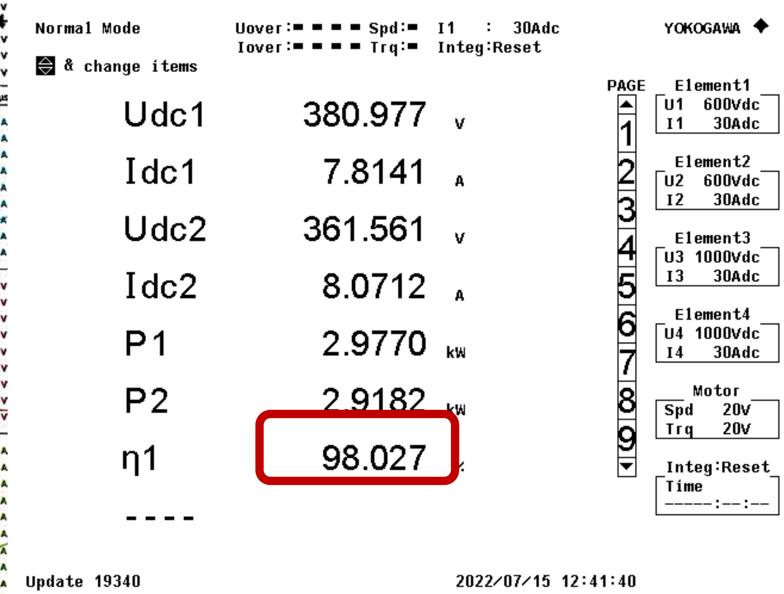
Experimental Results at 960 kHz with 98.02% Efficiency

- The developed GaN IPMs are demonstrated using an isolated DC-DC converter, which is capable of operating at 960 kHz switching frequency.
- The <u>isolated</u> dc-dc converter efficiency is tested to 98.03% at 960 kHz and 2918 W out using high accuracy (± 0.02%) power analyzer Yokogawa WT3000





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PowerAmerica

PREES Laboratory
NC STATE UNIVERSITY

THANK YOU

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