

Understanding Semiconductor Lead Times

PCB Carolinas 2022

Note regarding material

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Goal

 To provide insight into the market dynamics that impact the availability and Lead times of semiconductor products. Additionally, to explore the global nature of how Semiconductor devices are fabricated Packaged and Tested.



Agenda

- 1) Understanding How Semiconductors are made
- 2) The impact of surging demand on a constrained Fab resources



Where are Semiconductors made?

In Facilities known as Fabrication Facilities most often called <u>FABs</u>





-A Modern FAB costs approximately \$3-12B US to build. Also 24+ Months to construct -Inside the process areas the air is 1000 times cleaner than most operating rooms

What do we mean a "Wafer Fabrication"

Raw unprocessed wafers go in

 Finished wafers come out ready to be cut or "Diced".



- Determines Lead-time

Raw unprocessed Wafers

Wafers are Processed in the FAB

8-16 Weeks

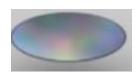


ICs are Placed in Package and Wire Bonded

Final Test of packaged ICs

Chips in warehouse

0-2 Weeks



16-52 Weeks









Determines Lead-time



Recent spikes in Demand have pushed out Lead times to unprecedented lengths



- Determines Lead-time

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16-52 Weeks







6-8 Weeks 4-6 Weeks 2-4 Weeks



0-2 Weeks

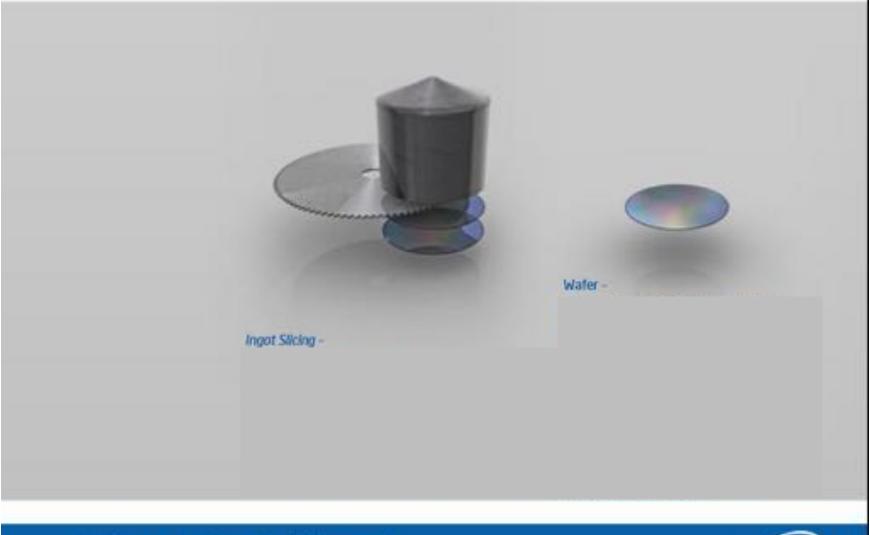
Sand / Ingot







Ingot / Wafer



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- Determines Lead-time

Raw unprocessed Wafers



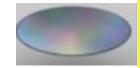
8-16 Weeks

Finished Wafers are Sawn into Die

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Final Test of packaged ICs

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16-52 Weeks





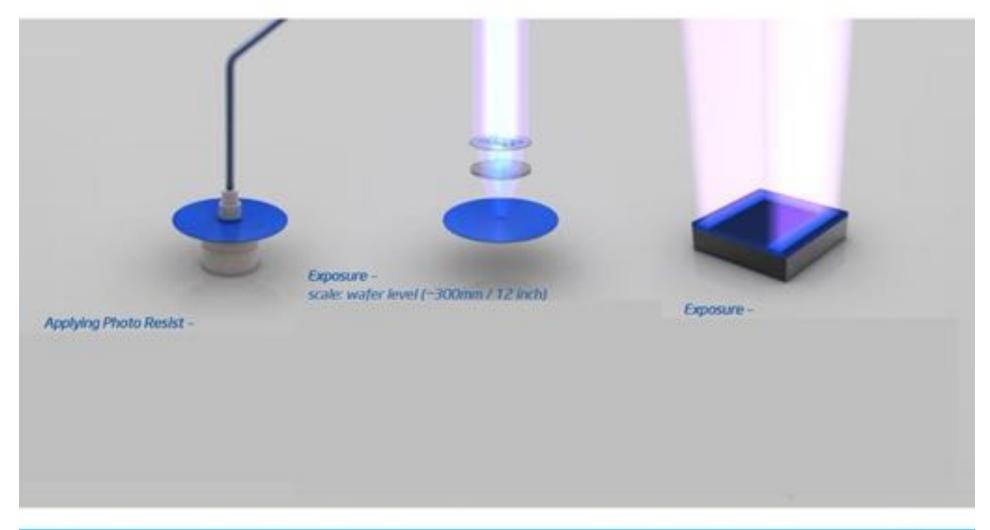
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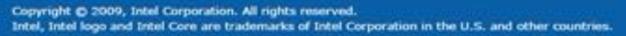


0-2 Weeks



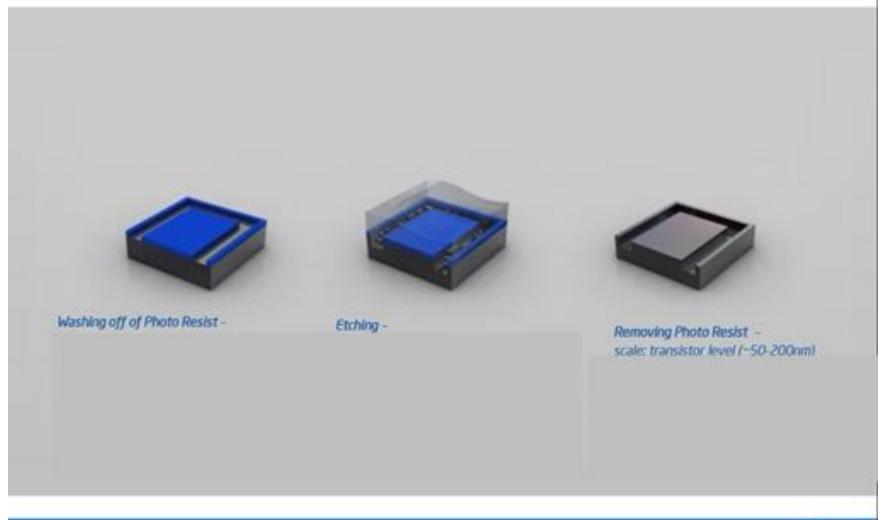
Photo Lithography







Etching

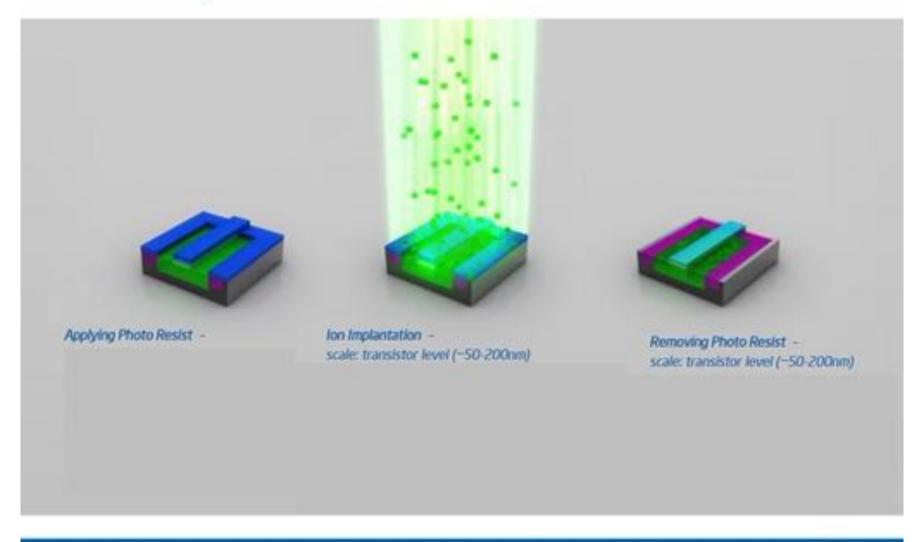


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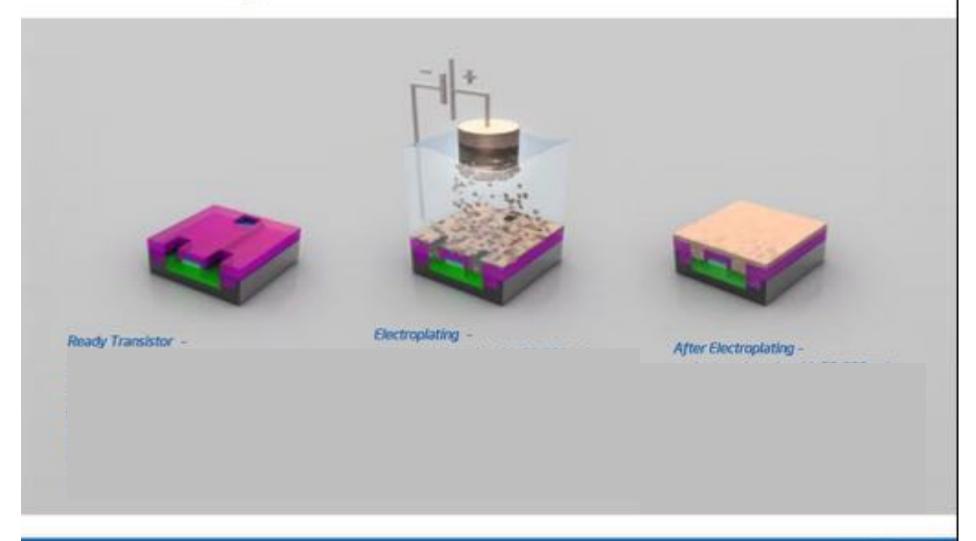
Ion Implantation







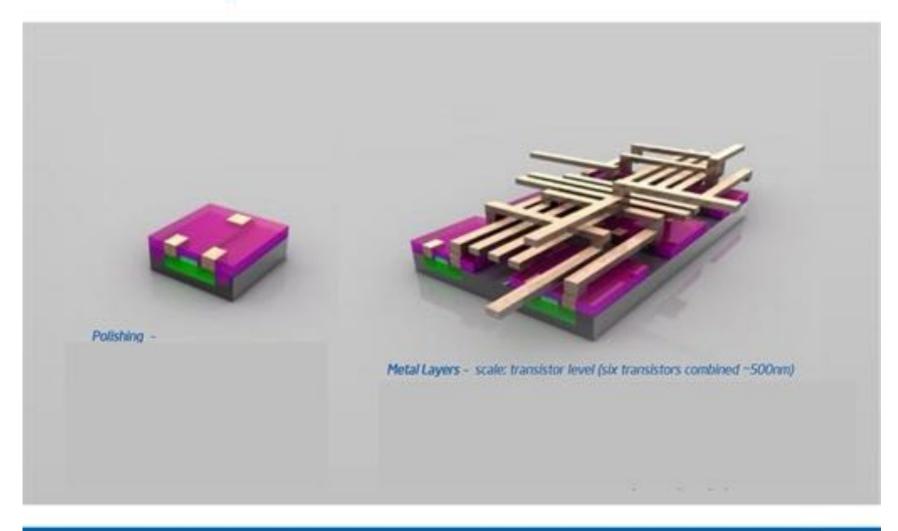
Metal Deposition







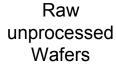
Metal Layers







- Determines Lead-time



Wafers are Processed in the FAB



16-52 Weeks

8-16 Weeks

Finished Wafers are Sawn into Die

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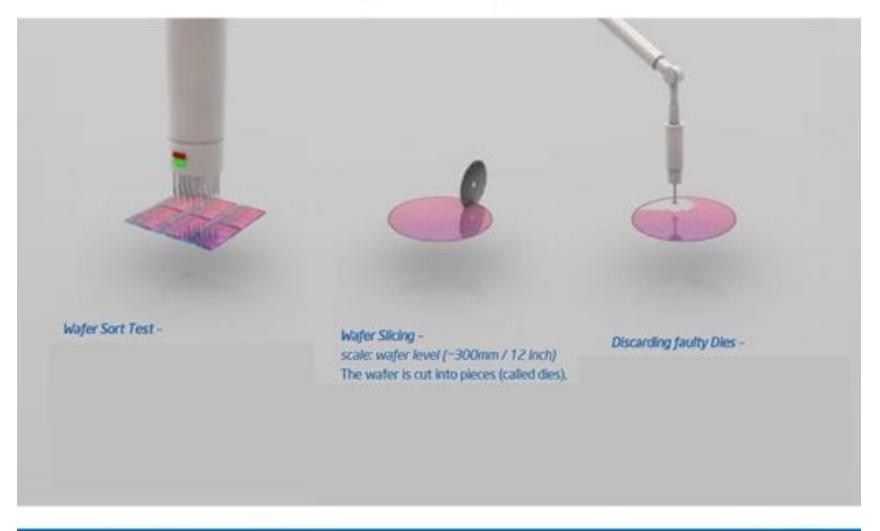
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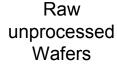
Wafer Sort Test / Slicing







- Determines Lead-time



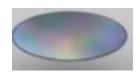
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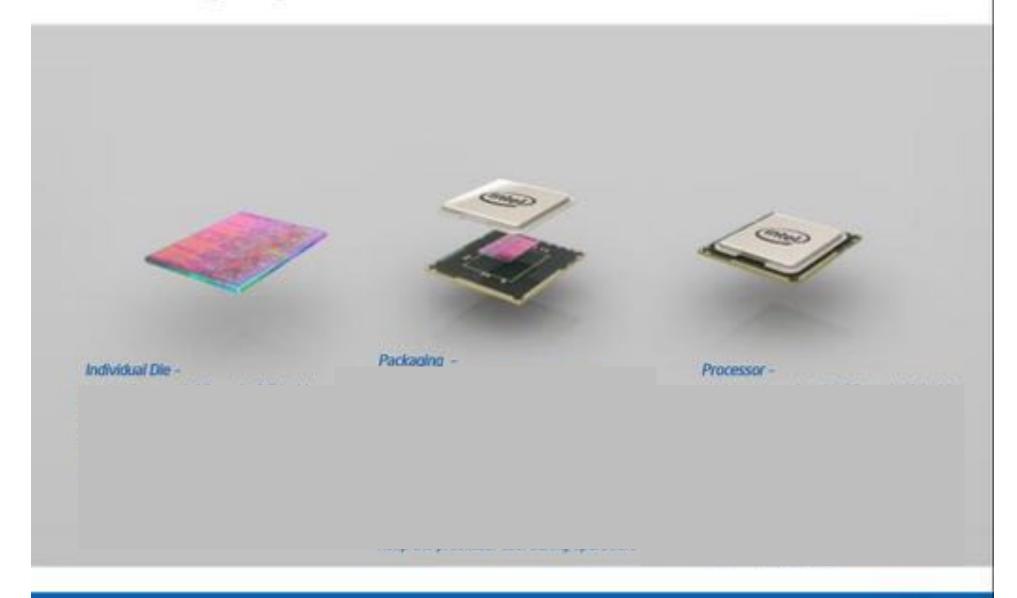
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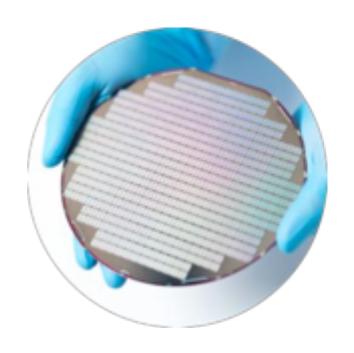


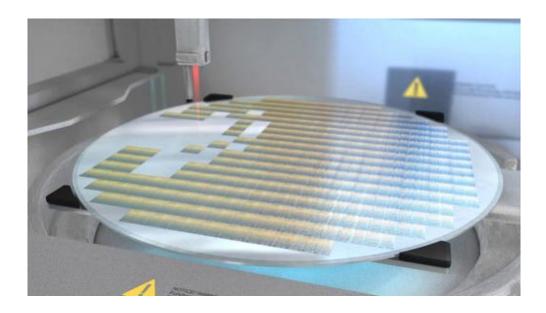
Packaging





Semiconductor Packaging







Individual wafers are then 'Diced" into individual "Die" that are then placed on a metal "leadframe" and then hermetically sealed into a Plastic (or similar) "Package"

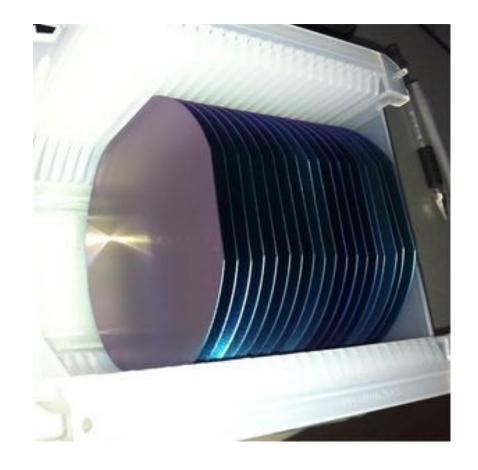
Wire Bonding the die to a package

ASM Eagle 60 video 1 OK - YouTube



What is a "Boat" of wafers

- Typically, 10-25 wafers of identical die processed at the same time with the same mask set*
- So say we get 5000 die per wafer x 20 wafers = 100K units
- Although the die may be the same it is possible, even likely, they will be used across dozens of different final part numbers.



 * A Mask Set is a series of Stencils that allow the specific patterns of transistors to be etched into the Silicon Substrate through a process called photo-lithography.



What are Masks

- A Mask defines the pattern of Light that is allowed to fall upon the silicon substrate that has been coated with Photoresist.
- Allows multiple exact copies of the die to be produced on a single wafer.



https://www.researchgate.net/figure/Two-photomasks-with-pellicles-The-upper-mask-is-a-conventional-binary-intensity-mask_fig1_234146446

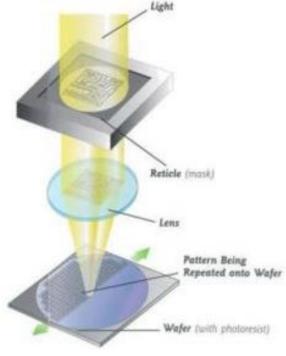


Figure 1 from THE USE OF EUV
LITHOGRAPHY IN CONSUMER MICROCHIP
MANUFACTURING | Semantic Scholar



Example of Multiple different parts using the same "Mask Set"

FINISHED_GOODS_				CPU Speed						
PLANNER	CPN 🔻	MASK 🚅	DCLASS 🚚	TIME_STAMP 🔽	Core 🔽	(MHz)	Flash (Kl	Package -	Temp Grade	T&R 🔽
KM	ATSAMD21E15C-UUT	661A7	30,000	1/16/2022	Cortex-M0+	48	32	45 WLCSP	Industrial (85°C)	T&R
KM	ATSAMDA1G16B-MBT	661A7	12,549	1/16/2022	Cortex-M0+	48	64	48 QFN (7x7)	Automotive Grade 2 (105°C)	T&R
KM	ATSAMDA1E14B-MBT	661A7	11,092	1/16/2022	Cortex-M0+	48	16	32 VQFN (5x5)	Automotive Grade 2 (105°C)	T&R
KM	ATSAMD21J16B-AFT	661A7	10,500	1/16/2022	Cortex-M0+	48	64	64 TQFP (10x10)	Extended (125°C)	T&R
	-		/							



So, What is the "Hold up"?

- There are hundreds of steps involved in making silicon wafers.
- Boats of Wafers can only be done sequentially
- Meaning if a lot of "Boats" are waiting to move through the fab, they can't start until an available spot is open.



- It is analogous to moving a ship through a canal with dozens of locks.
- The next "Boat" can't move into the next lock (or fab station) until the last Boat has cleared that same lock.

Unfortunately, today, We have dozens of suppliers waiting on their fab starts





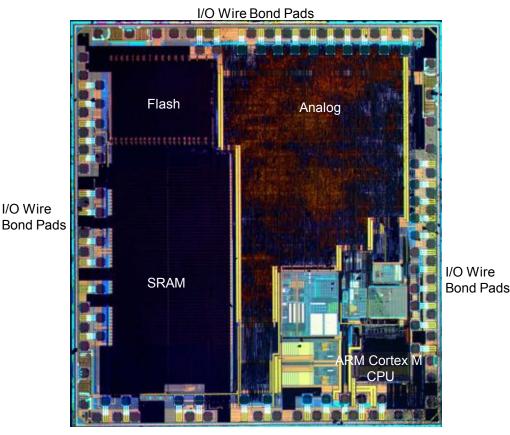
Global footprint of World Semiconductor manufacturing



Ongoing Covid response regulations differ by nation so add uncertainty to supply chain

Why have Microcontrollers been so Hard Hit

- Microcontrollers use various building blocks of mixed technology types including Digital Processors,
 Analog Static RAM memory and Flash Memory
- Common Building Blocks of IP (intellectual Property)
- Can only be built on their designated geometry process (i.e. 90 nm, 60nm, etc)
- The past decade has concentrated the "Fabrication" of these devices into a few common fabs, namely TSMC, Global Foundries and a few others



I/O Wire Bond Pads

https://en.wikipedia.org/wiki/STM32#/media/File:STM32F100C4T6B-HD.jpg

The impact of Geometry –90nm vs 60nm vs 40nm

- Semiconductor wafers are processed at a particular fixed geometry
- Although a Fab may support various geometries, they must run the wafer on the line of the designed geometry
- A fab may have more availability on a smaller (newer) geometry while larger lines are more tightly constrained.



As a reference the diameter of a Human hair is approximately 75,000 nm

What is Global Wafer Start Capacity = ~250 Million Wafers annually

Worldwide Wafer Capacity Leaders

(Monthly Installed Capacity in Dec 2020, 200mm-equivalents)

2020 Rank	2019 Rank	Company	Headquarters Region	Dec 2019 Capacity (K w/m)	Dec 2020 Capacity (K w/m)	Yr/Yr Change	Share of Worldwide Total	of Capacity Shares from JV Fabs
1	1	Samsung*	South Korea	2,935	3,060	4%	14.7%	
2	2	TSMC	Taiwan	2,505	2,719	9%	13.1%	+ shares of SSMC & VIS
3	3	Micron	North America	1,841	1,931	5%	9.3%	
4	4	SK Hynix	South Korea	1,743	1,878	8%	9.0%	
5	5	Kioxia/WD	Japan	1,406	1,598	14%	7.7%	

^{*}Line 13 partially excluded in 2020 due to conversion to image sensors.

Source: Companies, IC Insights' Global Wafer Capacity 2021-2025 Report

The top 5 Semiconductor Fab companies supply about 54% of the world's wafer starts

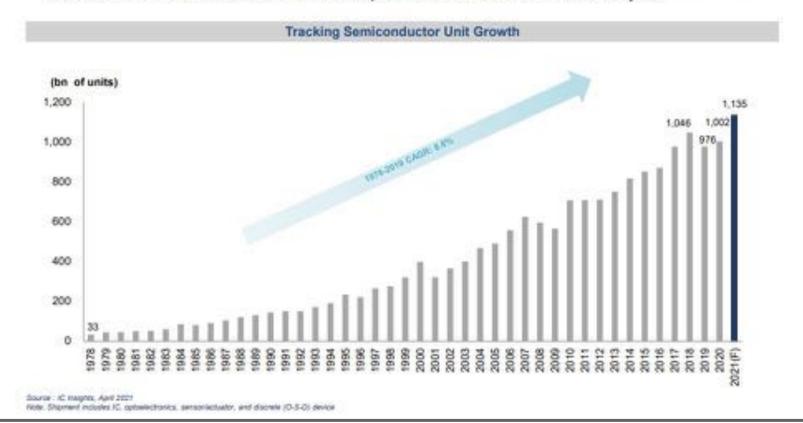


What is Global Wafer Start Capacity



Semiconductor Unit Shipment

Total semiconductor unit shipments are forecast to rise 13% in 2021, to 1,135 bn, setting a new all-time annual record and marks the third time that surpassed one trillion units in a calendar year.





Understanding Global Wafer Capacity

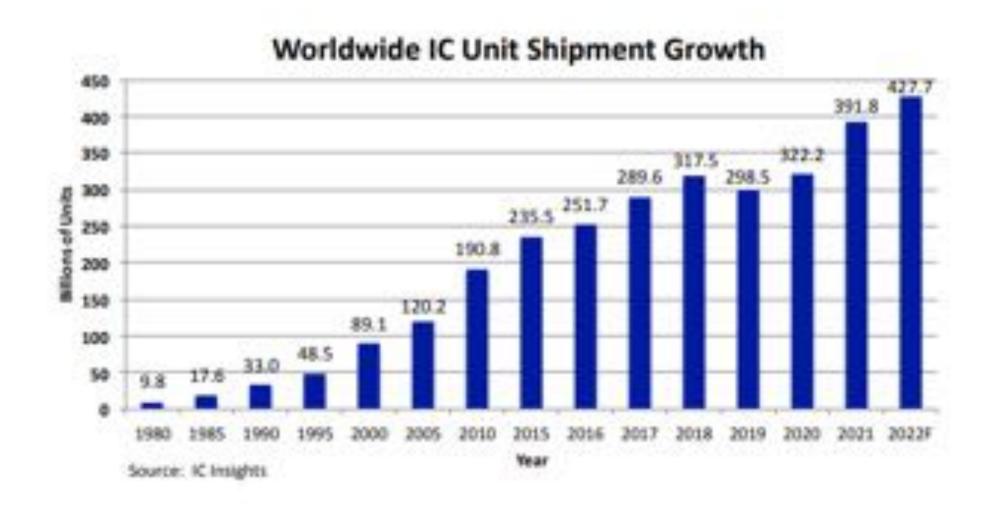
2016-2022F IC Industry Capacity Trends (200mm Equivalents)

Year	Total IC Wafer Capacity (M)	IC Wafer Capacity % Chg	Total IC Wafer Starts (M)	IC Wafer Starts % Chg	Total IC Capacity Utilization
2016	178.9	4.0%	161.5	4.9%	90.3%
2017	190.5	6.5%	175.8	8.9%	92.3%
2018	201.6	5.8%	188.9	7.5%	93.7%
2019	209.8	4.1%	180.0	-4.7%	85.8%
2020	223.5	6.5%	191.1	6.2%	85.5%
2021	242.5	8.5%	227.5	19.0%	93.8%
2022F	263.6	8.7%	245.1	7.7%	93.0%

Source: IC Insights, Knometa Research, WSTS, SIA

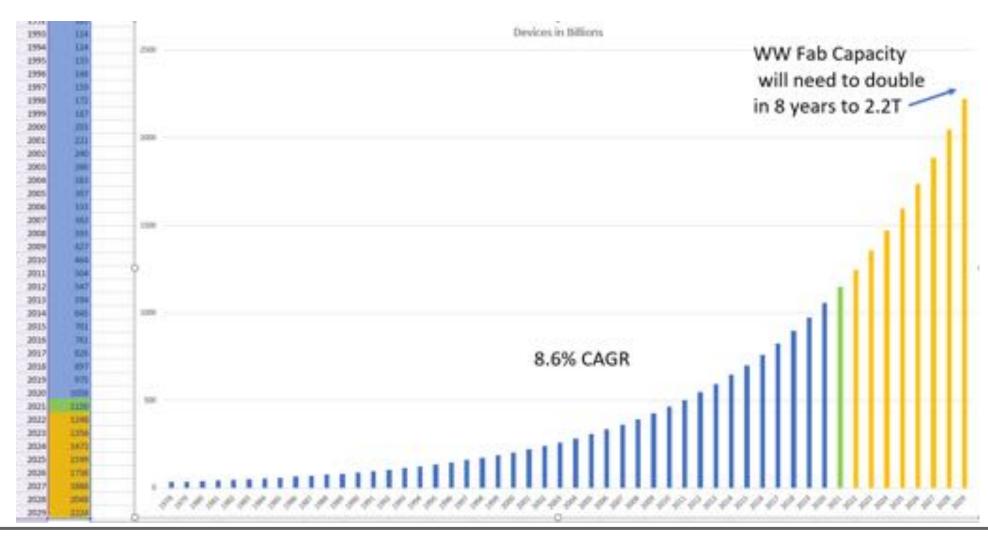


2022 IC (minus Discrete Semiconductor)





Our Dilemma – Doubling Fab capacity in 8 years.

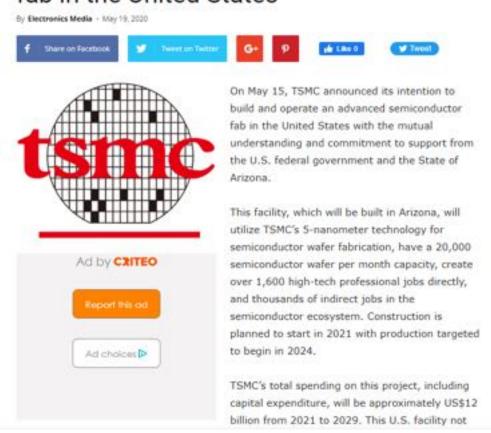




We will see more announcements like these



TSMC to Open advanced semiconductor fab in the United States





We will see more announcements like these



by Rick Smith and Juson Parker, WRAL TechWire - January 5, 2022 .



RALEIGH - At least two major semiconductor manufacturers are considering a site south of the Triangle in Chatham



County for the construction of a mammoth semiconductor manufacturing plant, an industry source tells WRAL



TechWire. And a corporate real estate executive confirms that there is "lots of interest" in the location from multiple

companies.

While not identifying the firms, a source in the semiconductor industry who requested anonymity said North Carolina is "well positioned" to land a project that could be worth as much as \$30 billion and create as many as 10,000 jobs.



We will see more announcements like these



TSMC to Open advanced semiconductor fab in the United States

By Electronics Media - May 19, 2020















On May 15, TSMC announced its intention to build and operate an advanced semiconductor fab in the United States with the mutual understanding and commitment to support from the U.S. federal government and the State of Arizona.

This facility, which will be built in Arizona, will utilize TSMC's 5-nanometer technology for semiconductor wafer fabrication, have a 20,000 semiconductor wafer per month capacity, create over 1,600 high-tech professional jobs directly, and thousands of indirect jobs in the semiconductor ecosystem. Construction is planned to start in 2021 with production targeted to begin in 2024.

TSMC's total spending on this project, including capital expenditure, will be approximately US\$12 billion from 2021 to 2029. This U.S. facility not

by Rick Smith and Jason Parker, WRAL TechWire — January 5, 2022.



RALEIGH - At least two major semiconductor manufacturers are considering a site south of the Triangle in Chatham County for the construction of a mammoth semiconductor manufacturing plant, an industry source tells WRAL. TechWire. And a corporate real estate executive confirms that there is "lots of interest" in the location from multiple



companies.

While not identifying the firms, a source in the semiconductor industry who requested anonymity said North Carolina is "well positioned" to land a project that could be worth as much as \$30 billion and create as many as 10,000 jobs.



Fab Expansion over the next few years





Thank You!

- Determines Lead-time

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