Place and Route
"It's So Much More…"

Wednesday Nov 9th, 2022

Mike Creeden CID+
Background

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- ❑ Insulectro – Technical Director Design Education
- ❑ PCEA - Printed Circuit Engineering Association - Vice Chair
- ❑ PCE-EDU, Inc. - Certified Curriculum Author & Instructor
- ❑ IPC-CID+ Curriculum - Primary Contributor & Instructor
- ❑ Chairman IPC-2221/2222 Standards Committee
- ❑ Founder of San Diego PCB, Design, LLC
- ❑ PCB Designer 45 Years - "*I Love PCB Design*"

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INSULECTRO

PCEA
Printed Circuit Engineering Association

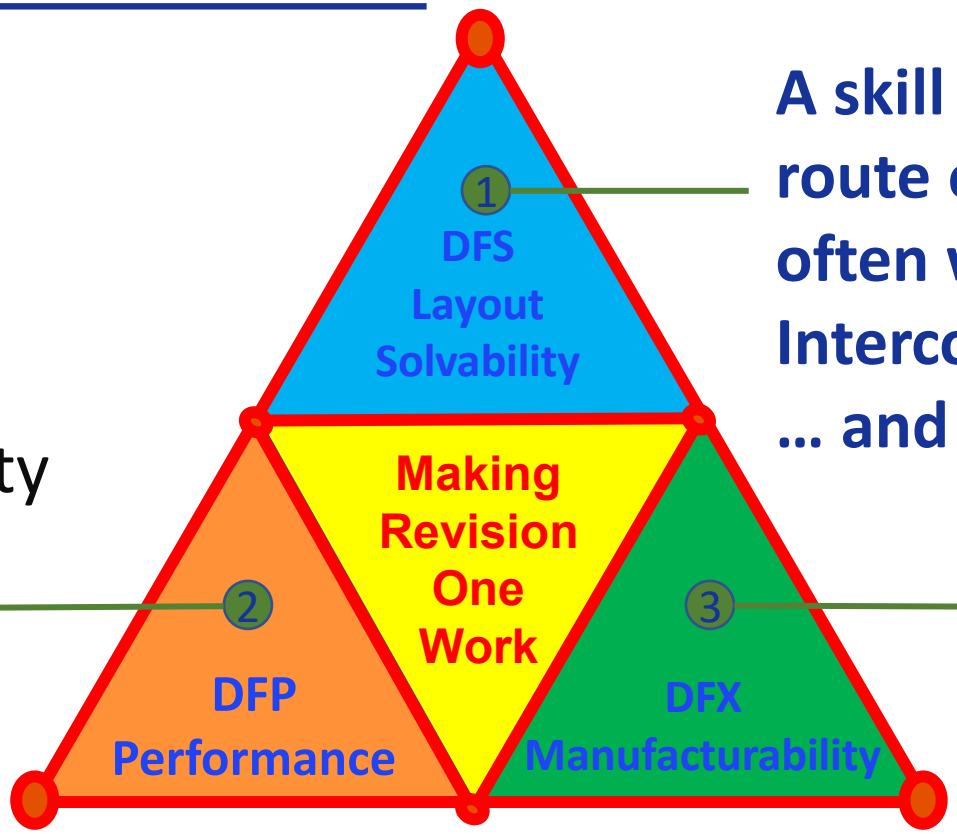
PCE-EDU, Inc.
Printed Circuits Engineering Education

MOST IMPORTANT SLIDE

Today's Circuit Engineer must meet 3 Competing Perspectives for Success

Design For:

- **DFS**olvability
- **DFP**erformance
- **DFM**anufacturability



A skill set to solve the place and route of all parts and connections often with complex High Density Interconnect (HDI)
… and master this on your CAD Tool

Signal Integrity/EMC
Power Delivery
Thermal

DFX all considerations producing high yield and lower cost

THE RESULT

Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing

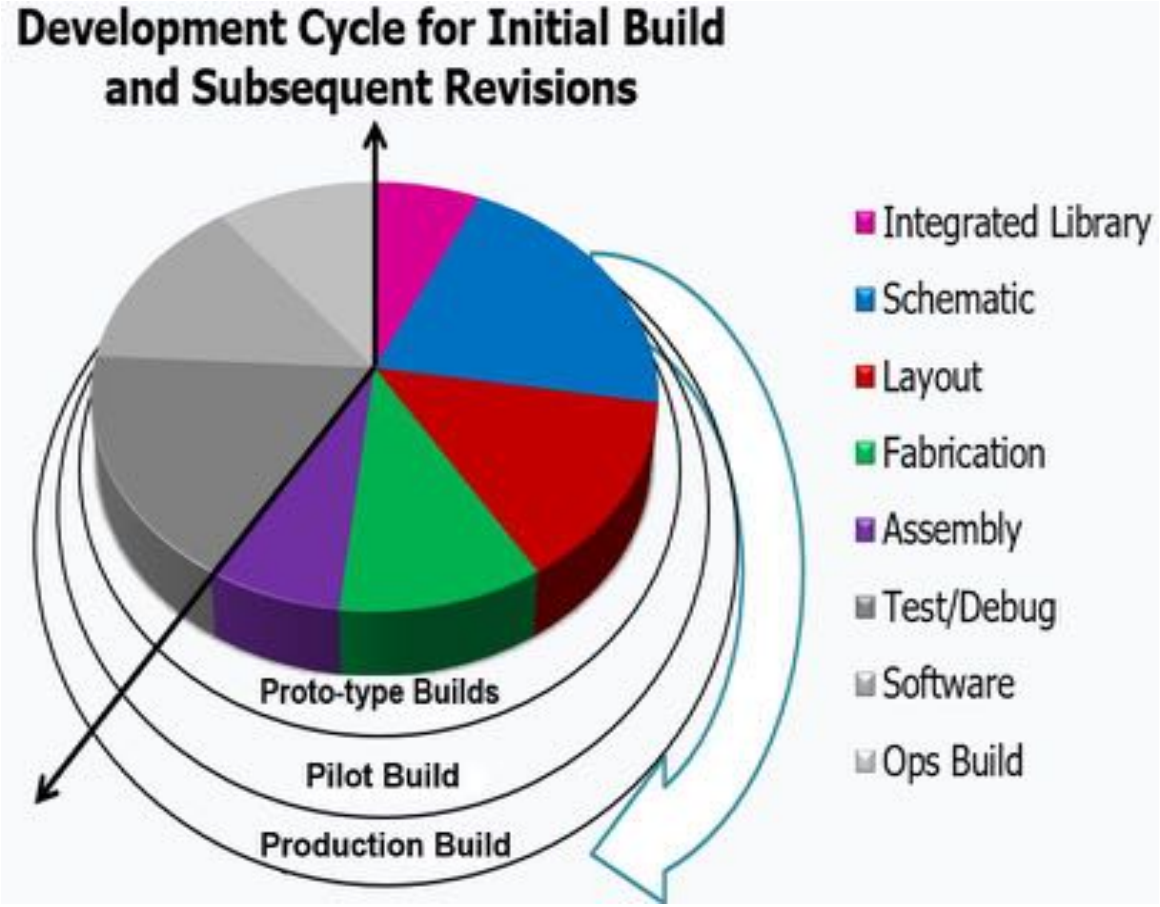
Understanding the End Goals at the Start of CAD

Designing to the End Production Goals

- Yearly Quantities
- Life Expectancies
- Environmental-Usage Requirements

Proto – Pilot - Production

- Proto - Data Feature Size vs Mfg. Capability
- Pilot – Shop Floor Implementation
- Production – Long Term Reliability Issues from Usage, Operation or Environment



Images courtesy of San Diego PCB Designs, LLC.

Printed Circuit Engineering - Overview

Company procedures, conventions and best practices support consistent methods with consistent high yield results.

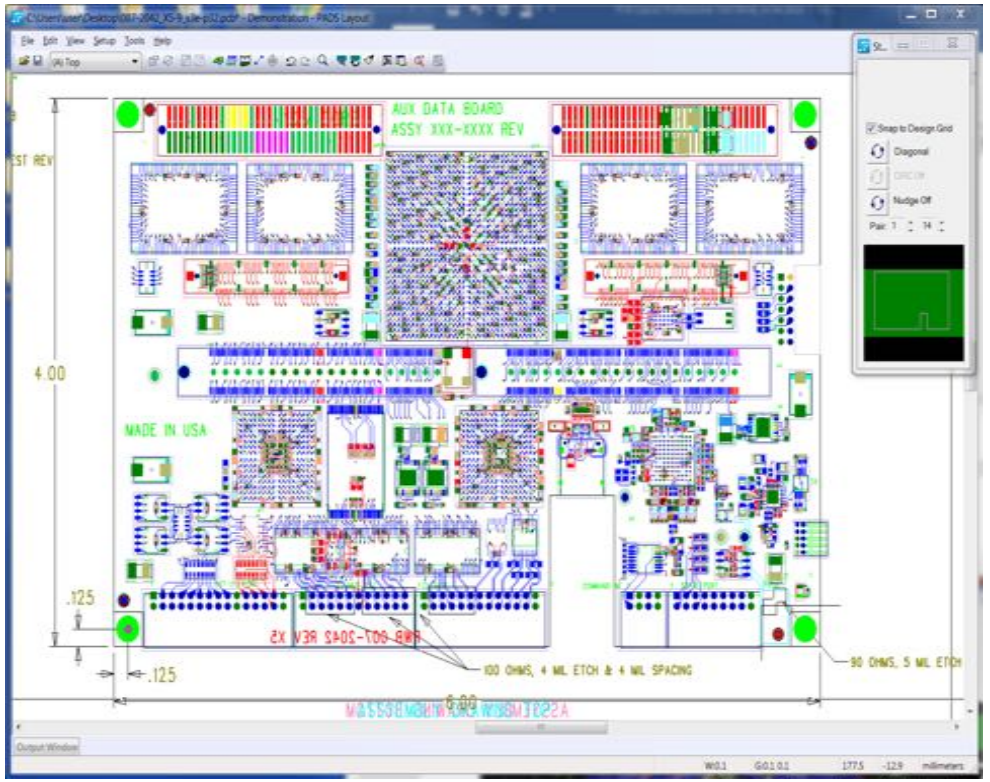
File Naming Convention

All iterative modification while in development between the tools and the engineer and the layout team are tracked with a temporary-iteration schema to ensure utmost accuracy.

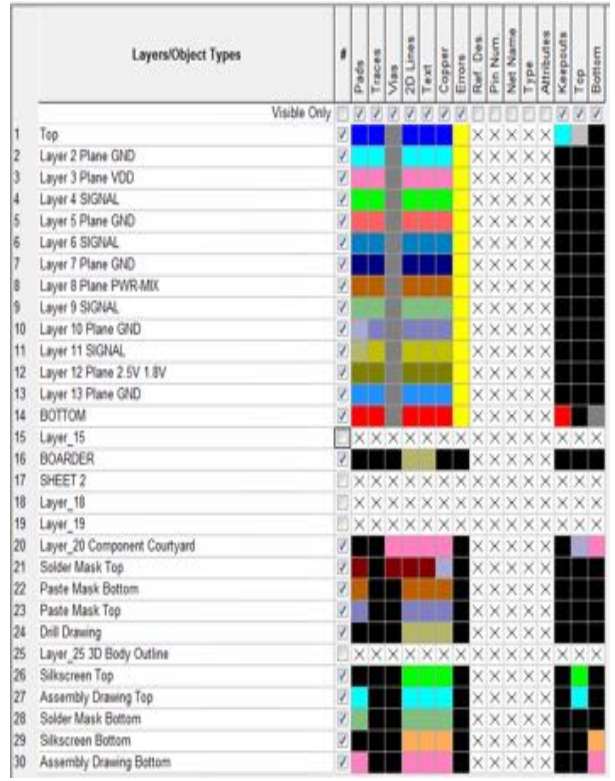
i.e.

Filename-number _S3-P15.ext

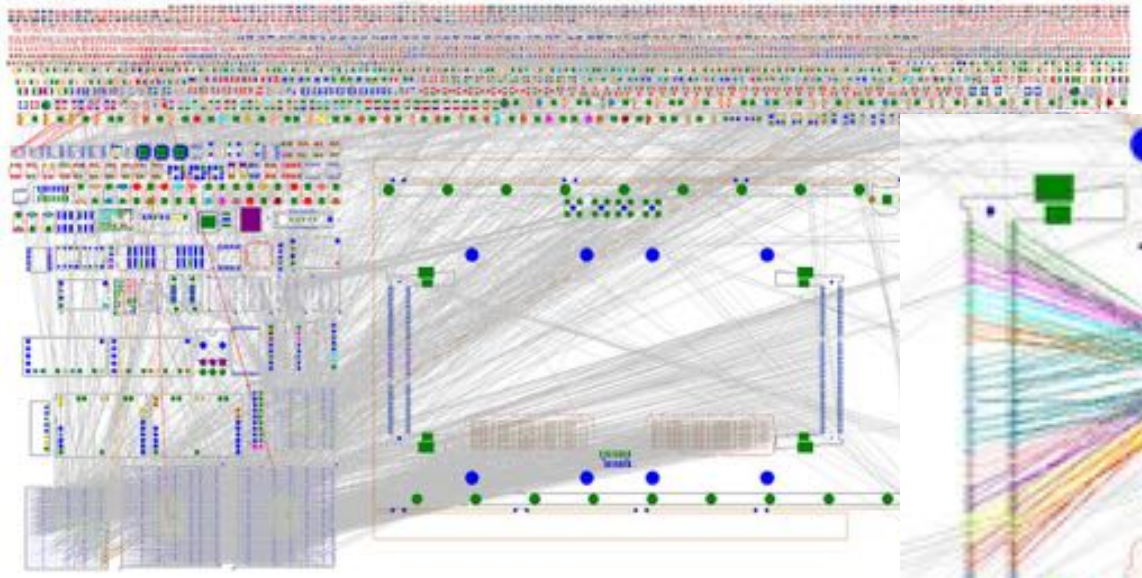
Color Conventions



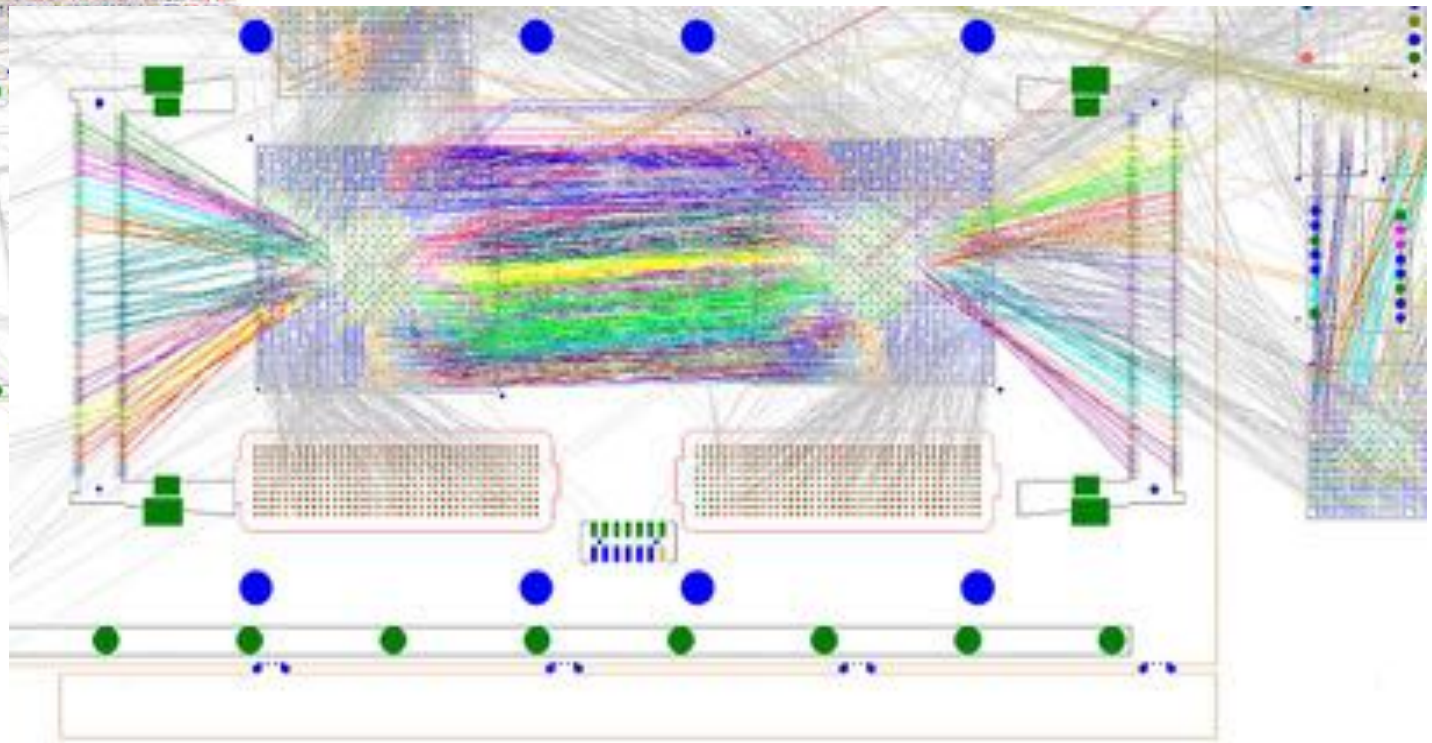
Layer Naming Conventions



Color Code Netlist



Unrouted Connections,
No Color Code



Unrouted Connections, Color Coded Net-Classes - Placement Aid

Printed Circuit Engineering – Start Data

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SMT Device Packaging: Discrete and Active

Common Discrete SMT Case

Common Active SMT Case

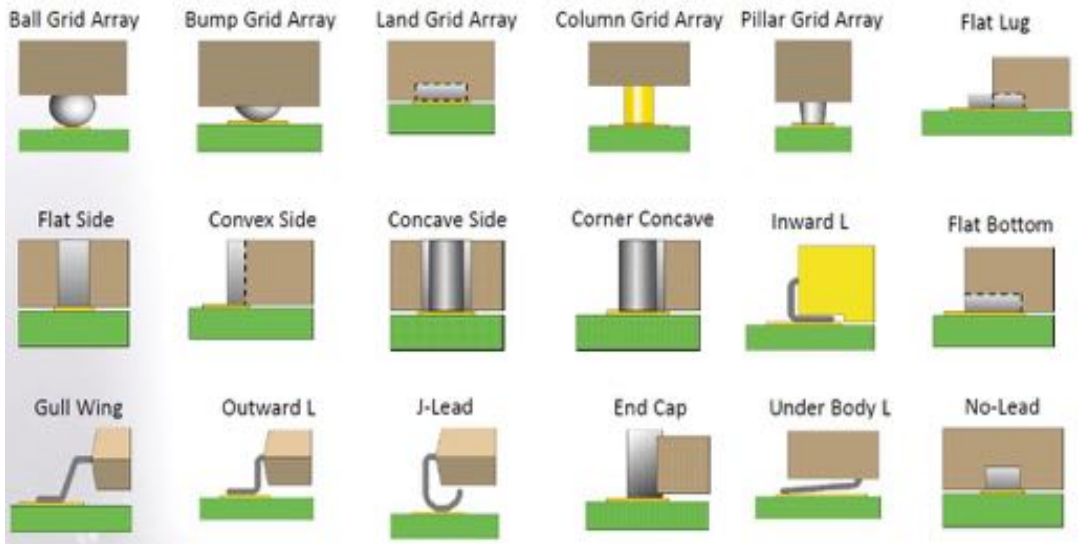
Images courtesy of PCB Libraries, Inc.

Printed Circuit Engineering – Start Data

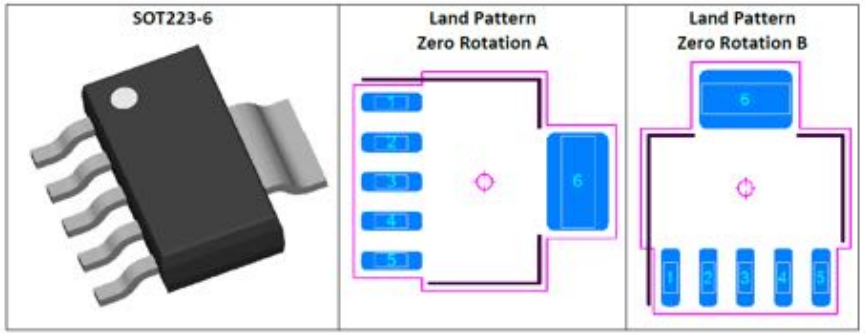
Libraries –

Land Patterns for Layout

A Land pattern is the best name to describe the library entry for PCB CAD. A footprint is the impression a part would make if you pushed it into clay. There are several purposes for the PCB land pattern. First and foremost, the land pattern purpose is to provide the parameters for the component to be joined to the board using solder as the joining agent. Each type of terminal must have a specific terminal land to ensure a robust solder attachment.



Small Outline Transistor SOT223 (SOT)

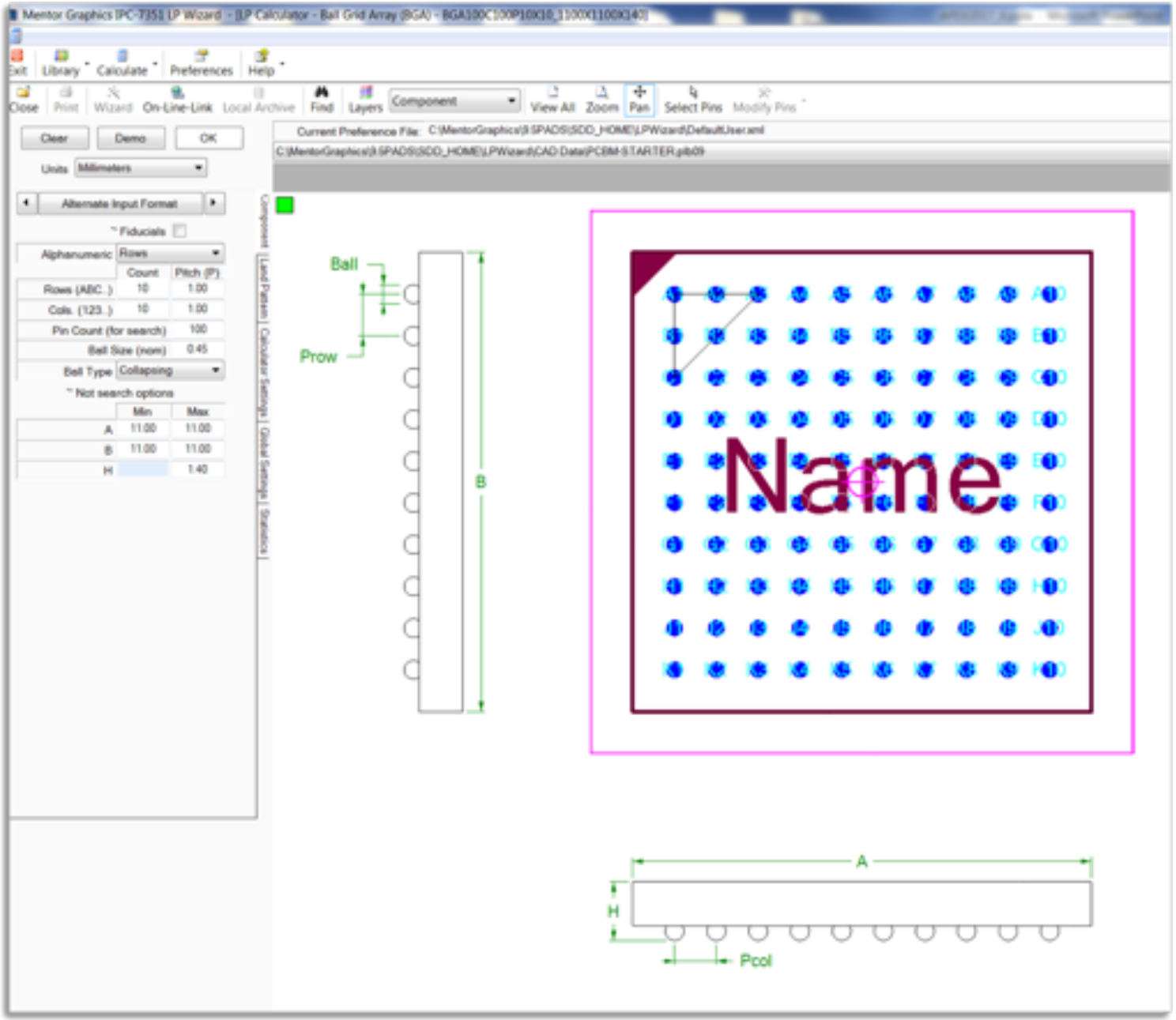


Flat Ribbon Land Gull-Wing Leads (unit: mm)

Lead Part	Most Density Level A	Nominal Density Level B	Least Density Level C
Toe (J_T)	0.55	0.35	0.15
Heel (J_H)[1]	0.45	0.35	0.25
Side (J_S)	0.05	0.03	0.01
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.01, 1.02, 1.03		
Courtyard excess	0.50	0.25	0.12

Images courtesy of PCB Libraries, Inc.

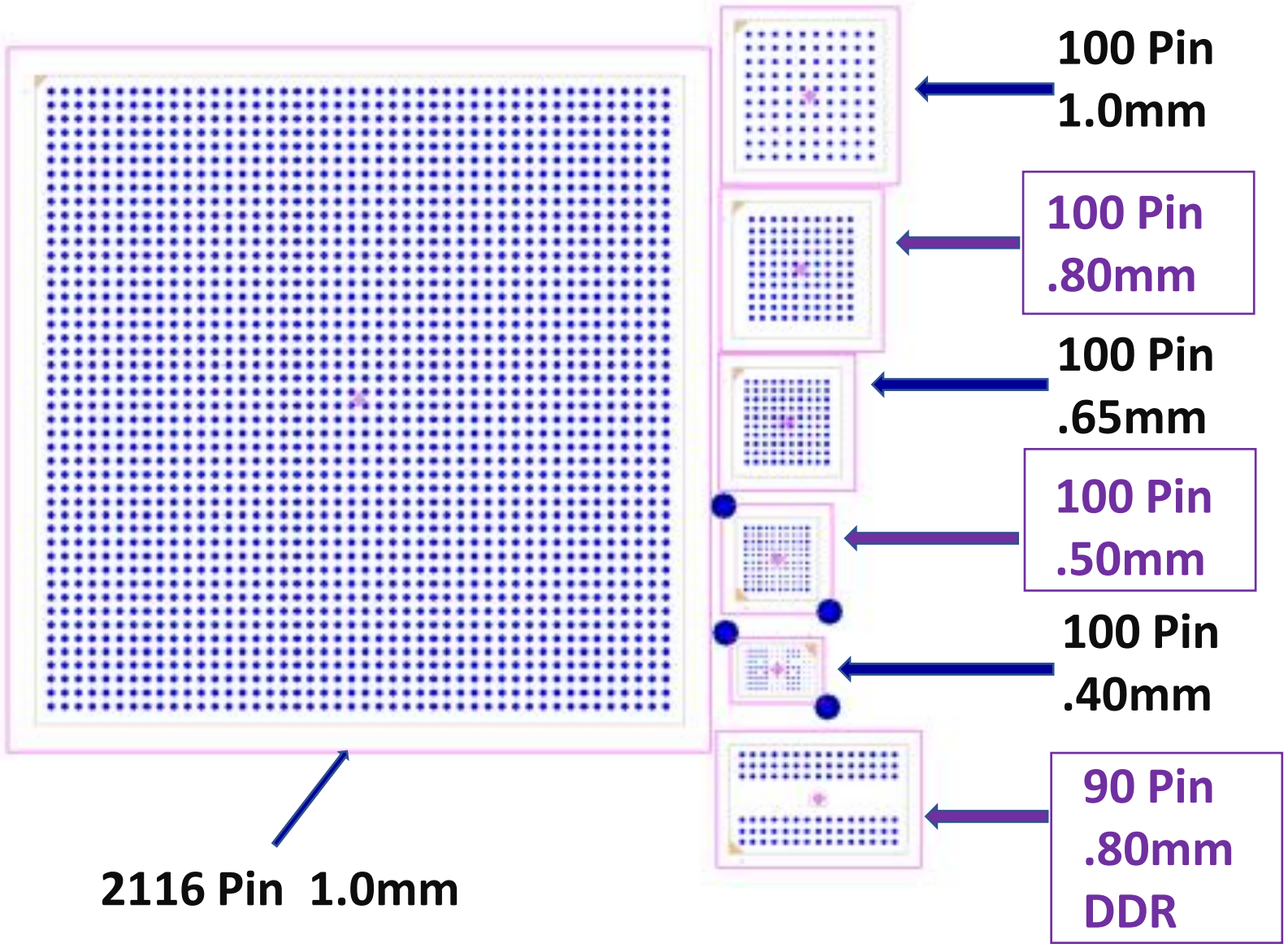
Printed Circuit Engineering – Start Data



IPC-7351
Land Pattern Calculator

- PCB Layout in it's most simplistic form is parts interconnected.
- 50% of that sentence is parts", meaning it's important.
- Do you want accuracy or tribal knowledge in your parts libraries?
- Don't accept libraries from any unknown source, create them from known formulas!

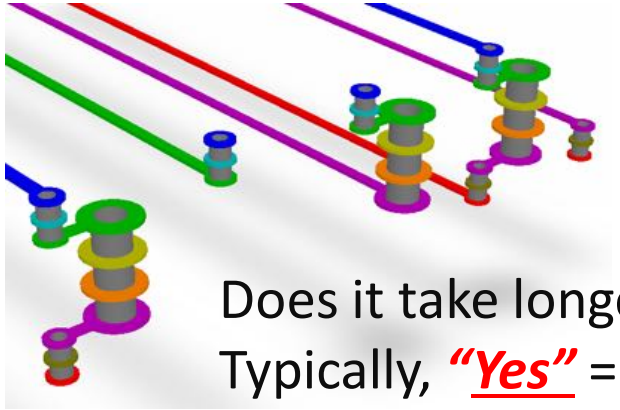
Printed Circuit Engineering – Start Data



IC Packaging Miniaturization

- Area comparison of (100 pin) BGA's with varied Pin Pitch's

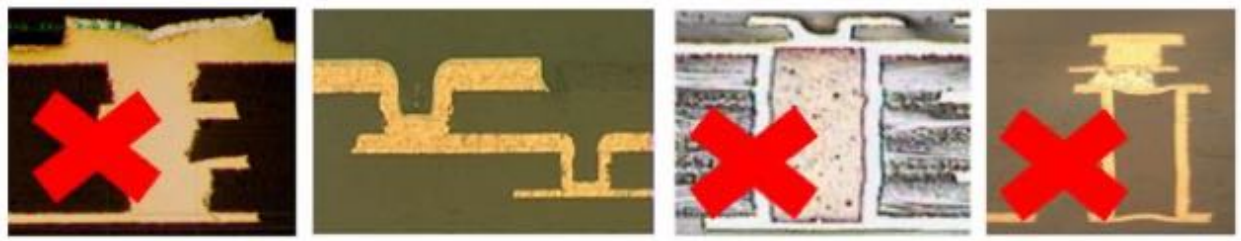
Routing HDI

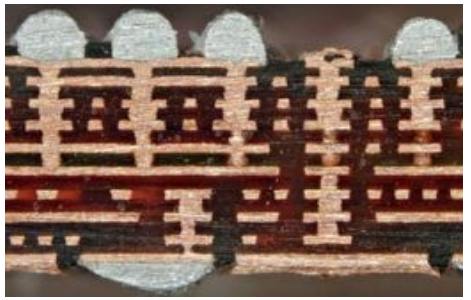


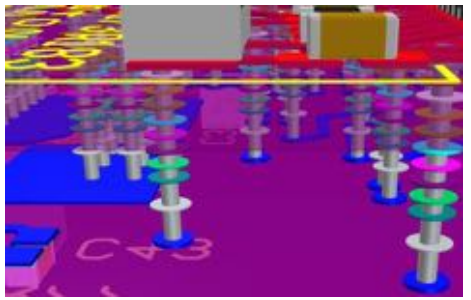
Does it take longer to complete an HDI design?
Typically, ***"Yes"*** = You're routing 3D, Z-Axis

HDI and Via Fanouts – Fine Pitch BGAs

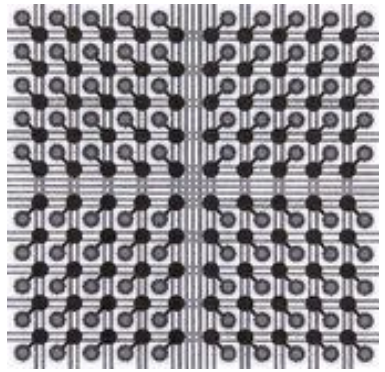
- Fine pitch BGA – <.65mm, .5mm (must be used)
- Sequential lamination - multiple stacking options
- Thin materials - down to 50um [0.002 inch] dielectric
- 3D Routing is more challenging from a layout perspective.
- Improved signal and power integrity performance
- Don't Stack Vias low reliability

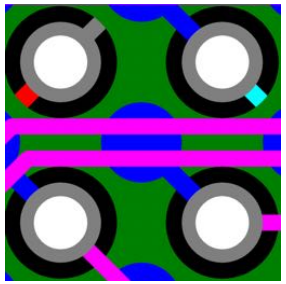






Printed Circuit Engineering – Start Data





Metric vs. Inches

As shown on a 1.0mm pitch BGA

- ***Do you value accuracy?***
- **Use Metric because the parts are metric in their pitch, pad size and body dimensions**.
- Don't us round offs because they're inaccurate! **You're not solving for one**, rather you're solving for many rows and columns. Tolerance errors accumulate…
- The **imperial measurement system** is based on England's King George IV in 1825 and his rule of thumb.

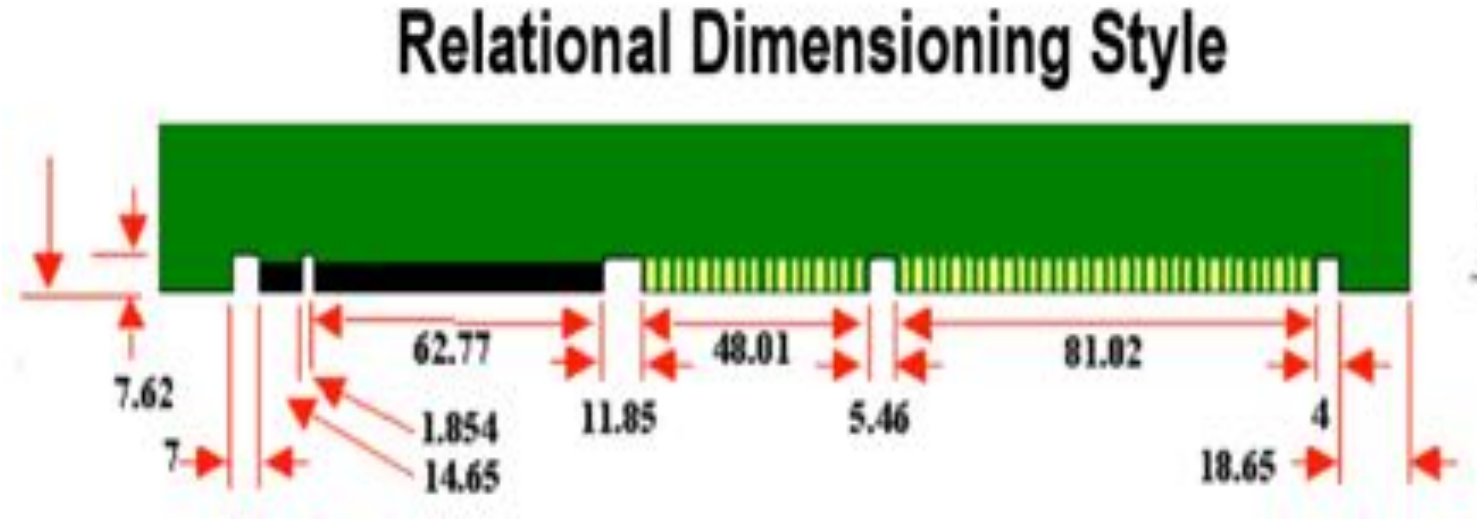
Metric	vs.	**(Inches)**
Via Data		
Pad: 0.50		**(0.01968498)**
Hole: 0.25		**(0.00984249)**
Anti-Pad: 0.70		**(0.02755897)**
BGA Pad Size: 0.5		**(0.01968498)**
Trace/Space Data		
Trace Width: 0.1		**(0.003936996)**
Trace/Trace Space: 0.1		**(0.003936996)**
Trace/Via Space: 0.1		**(0.003936996)**
Routing Grid: 0.1		**(0.003936996)**
Via Grid: 1		**(0.03936996)**
Part Place Grid: 0.5		**(0.01968498)**

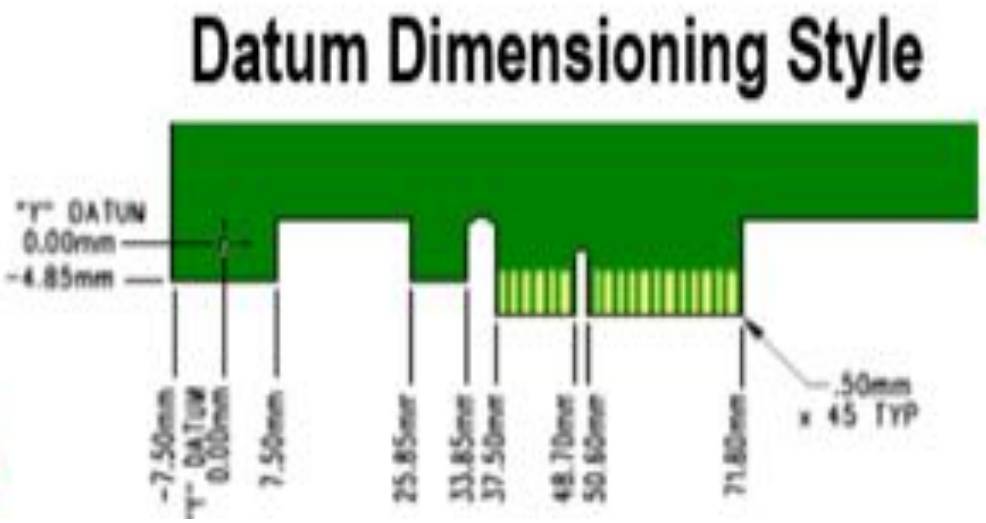
Printed Circuit Engineering – Start Data

Mechanical Dimension Styles

Our Fab-Drawing should have no accumulation of tolerances (Relational style - accumulates tolerances).

Positioning may be relative, but they are entered in an absolute format. Then manufactured in absolute format known as NC (Numerical Control) referenced from 0/0 on a Cartesians Plane.



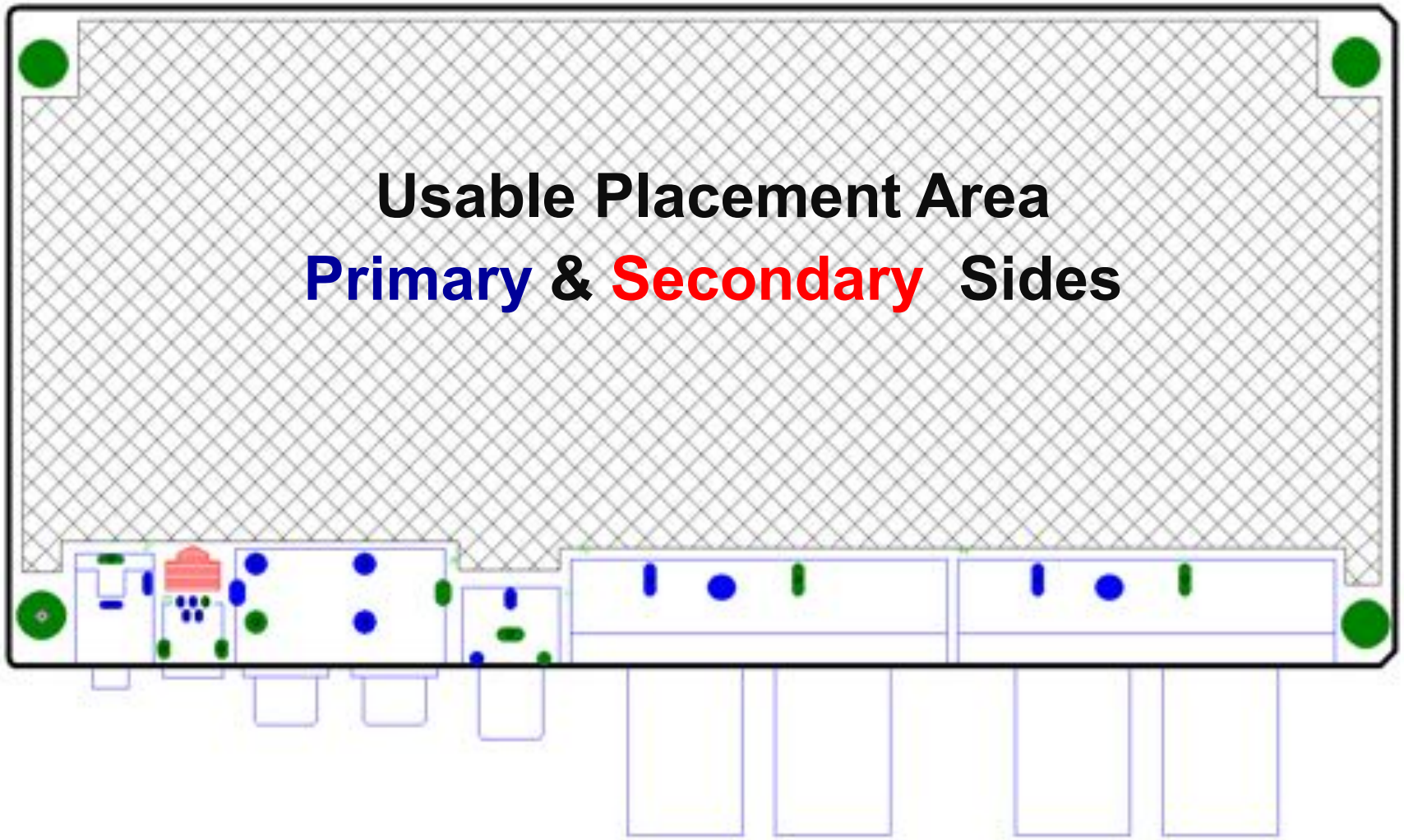


Relational style dimensions = Bad

Datum style dimensions = Good

Printed Circuit Engineering – Start Data

Mechanical Constraints Data Base or Drawing



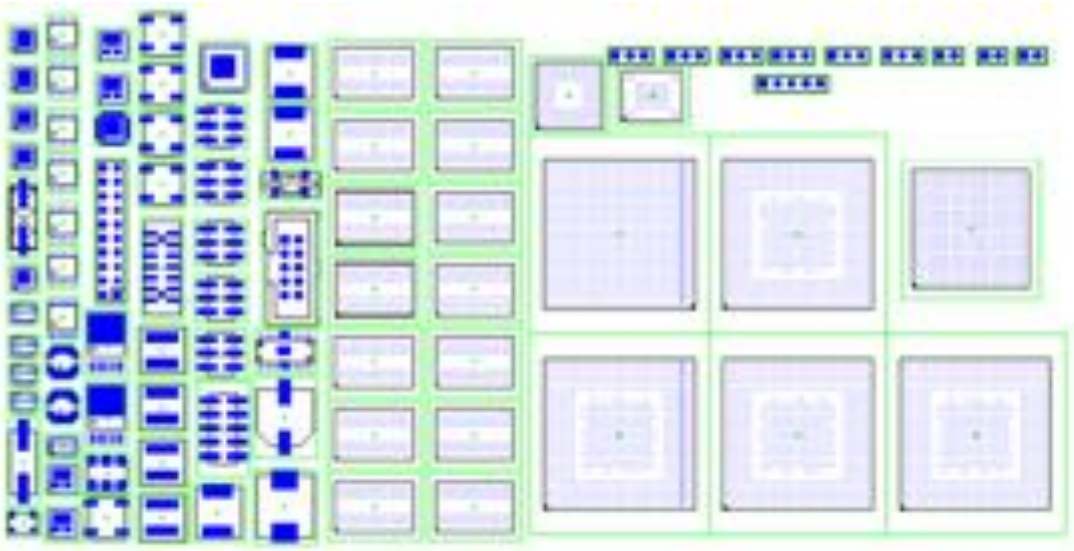
Mechanical Constraint as received by DXF, Step-file or pdf:

Usable Board Placement Area

Feasibility Study is often done prior to official CAD-start

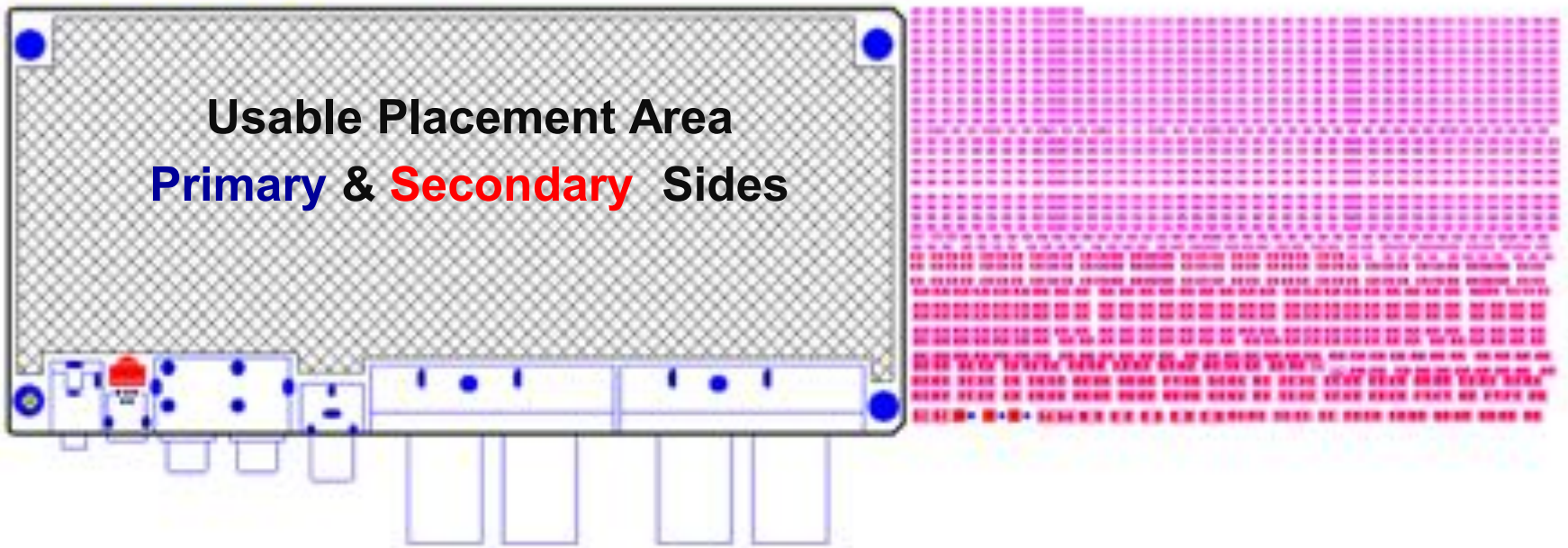
Printed Circuit Engineering – Start Data First Effort…

Feasibility Placement Study



Primary Side: Active Devices Shown in Blue

Secondary Side: Passive Devices Shown in Red



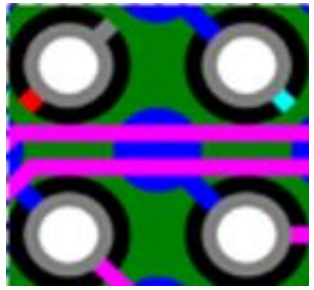
Quick Rooms component dispersement shows some feasibility, thus DFM/DFA ready.

Quickly observed, this is probably "Not Feasible"

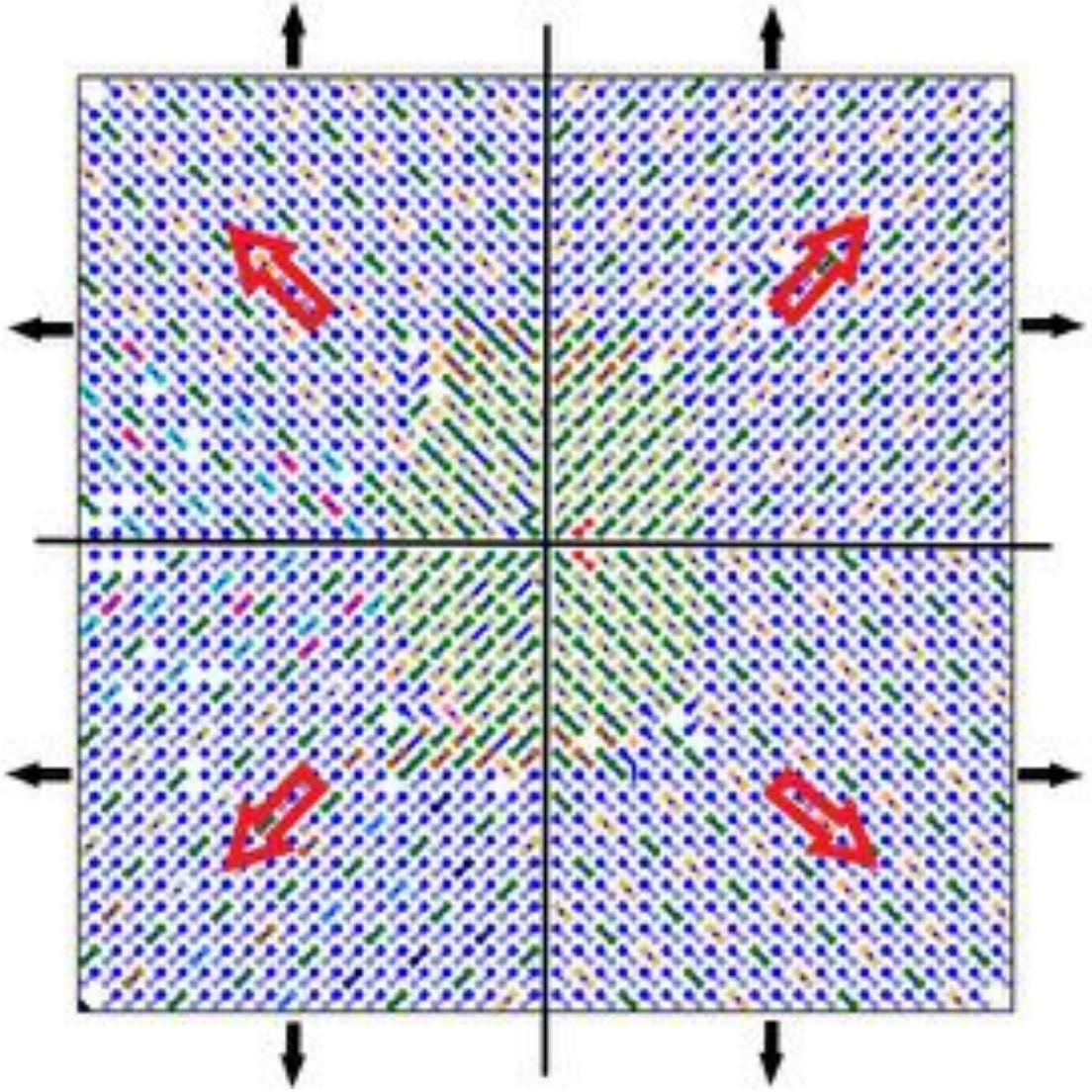
To many components to fit in circuit board area.

DFS – Solvability
Estimating the Number of Signal Layers

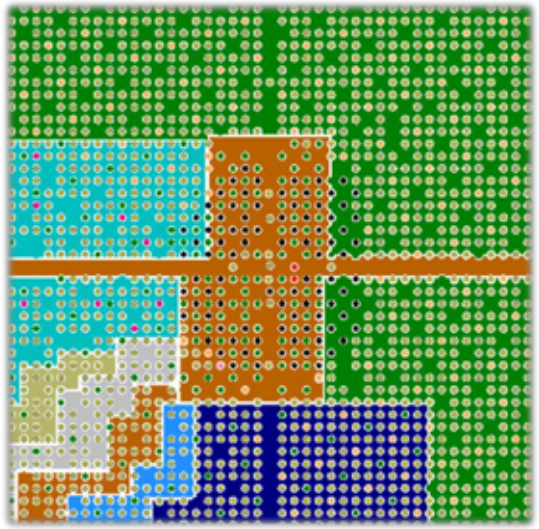
The number of routing layers is determined by number of signals exiting the Via field (shown in blue) in a *wagon wheel* fashion of the largest BGA.



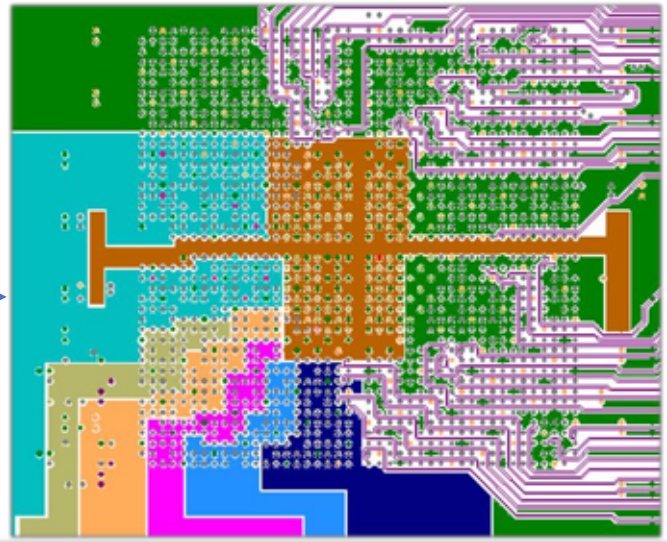
Class 2 - 1.0mm pitch BGA with 2 traces in-between Via columns = Approx. 6 layers



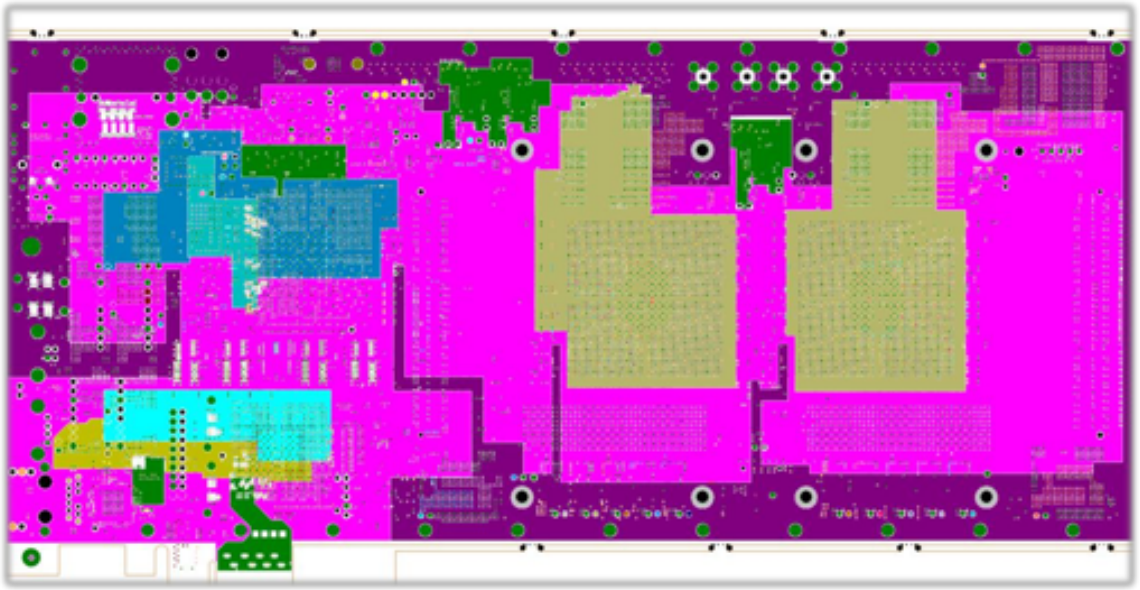
Split PWR Planes & Uninterrupted GND Return Planes



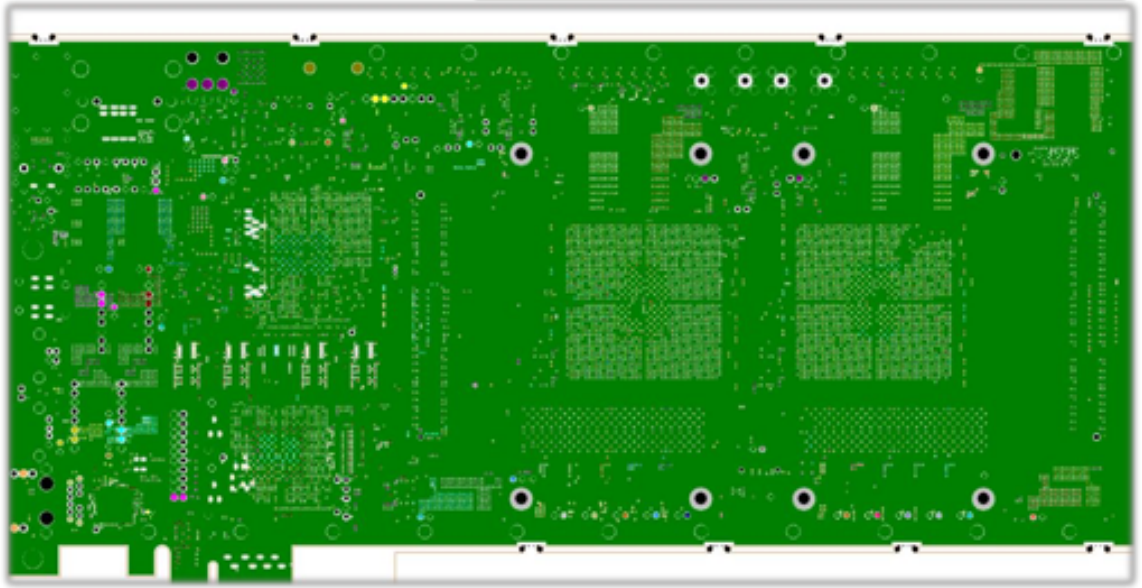
All Split PWR Planes can have dual usage; PWRs & Traces



Split PWR Planes Under a BGA Help to Balanced Copper

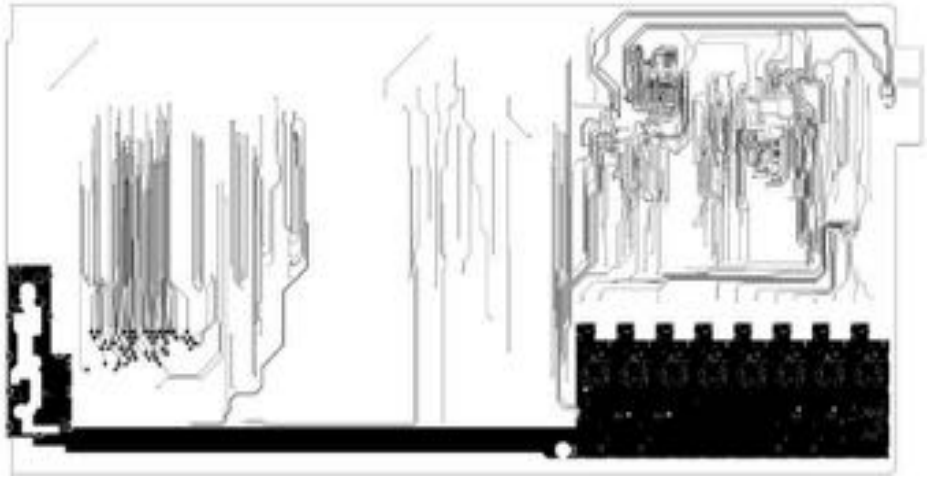


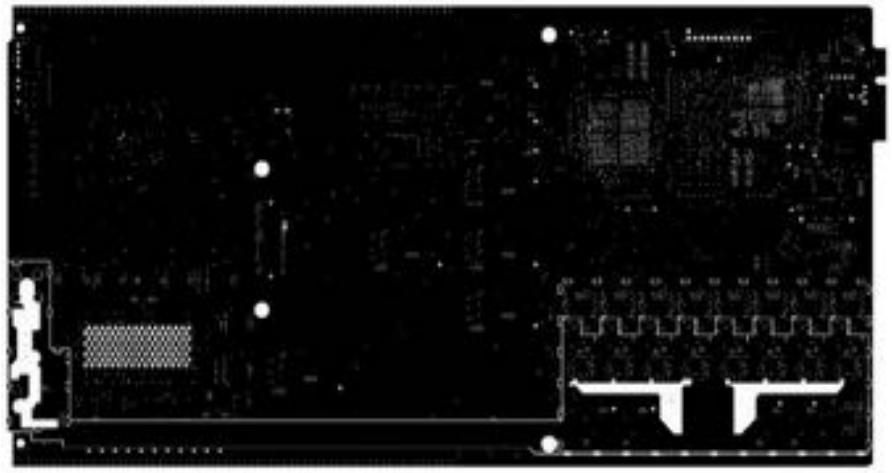
Split PWR Plane



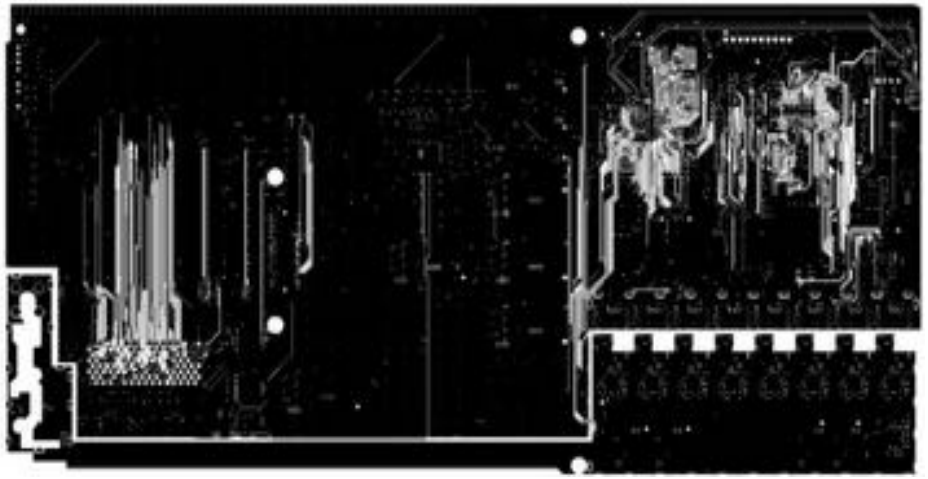
Uninterrupted GND Return Plane

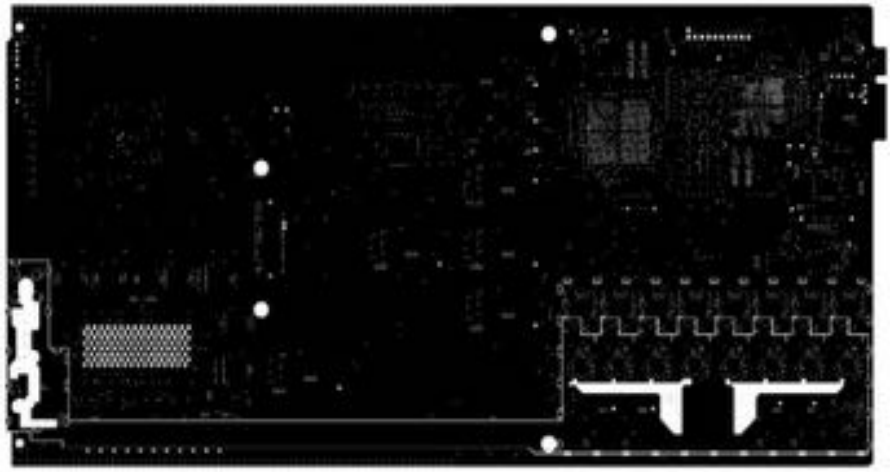
Balanced Copper Core - Split Planes & Uninterrupted Planes





Unbalanced Core Pair of Layers – Signal (Left) with GND Return (Right)





Balanced Core Pair of Layers – Signal with Back-filled PWR Flood (Left) and GND Return (Right)

Split Power Planes

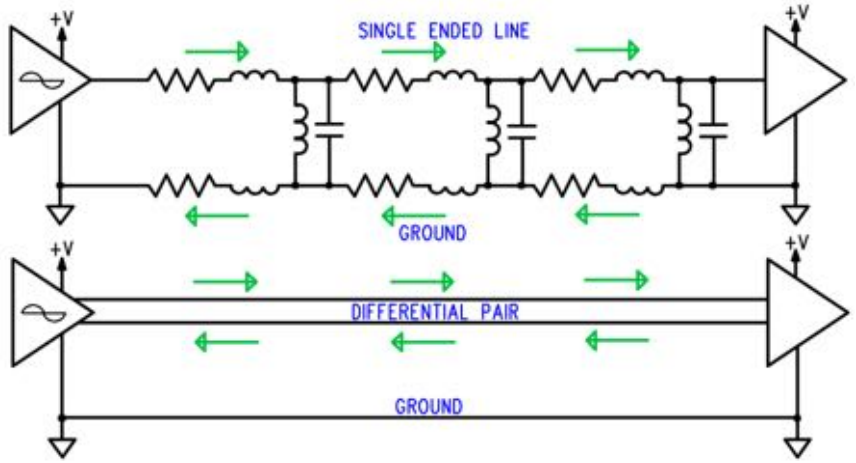
Uninterrupted GND Return Plane

Signal Energy in the Dielectric

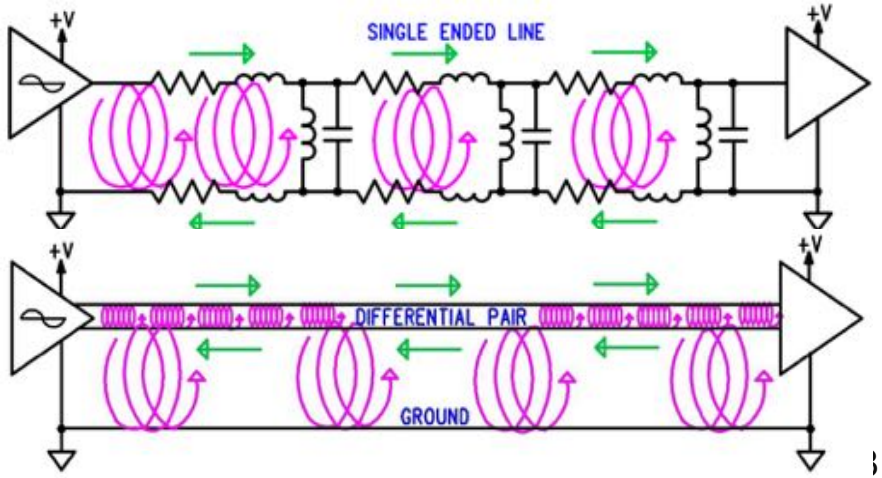
Signal Propagation and Return (energy moving forward & back)
However, it is not forward and back, rather, the energy field is
immediate between trace and plane in the dielectric material

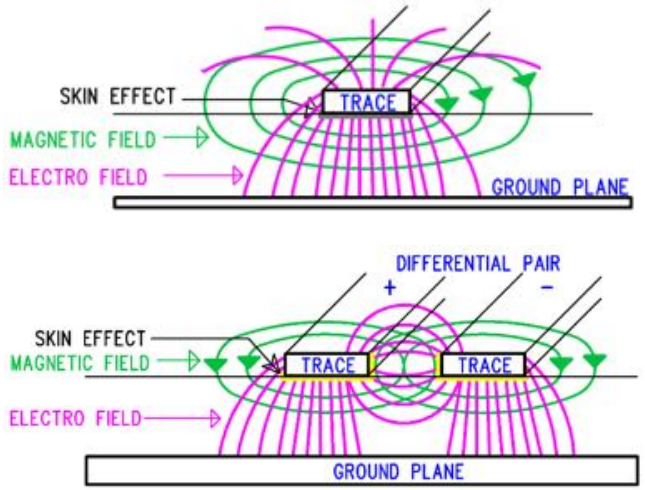
"Materials are part of the circuit"

Not forward and back



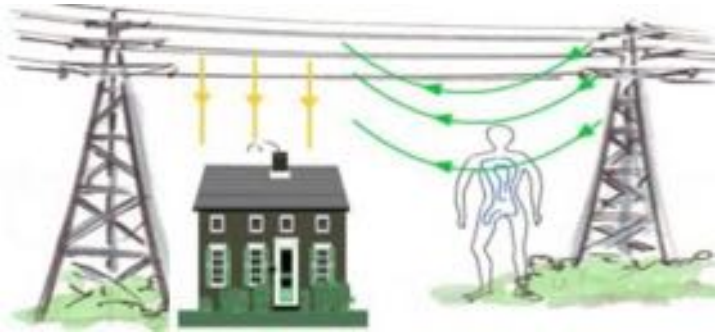
Fields exist in the dielectric

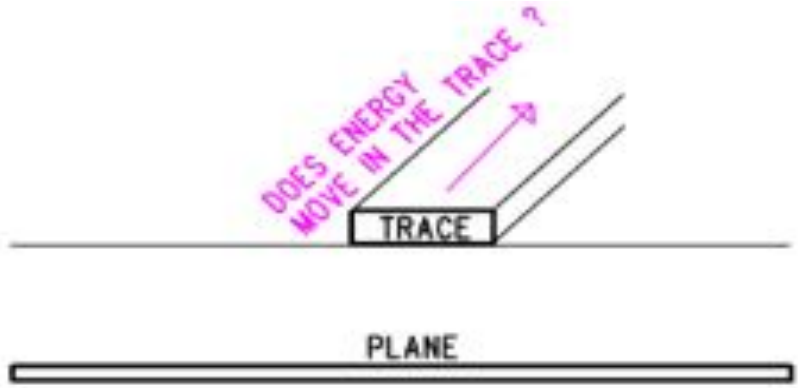




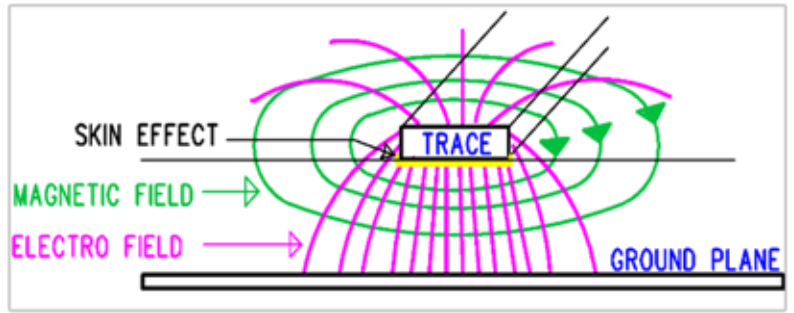
Understanding EM Theory

- **Electro and magnetic fields**, Where does the energy exist, in the trace? NOOOOO! ---------→

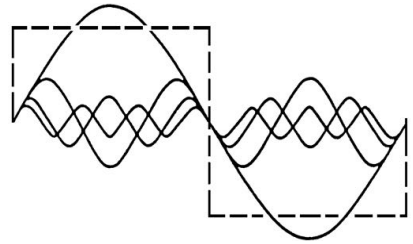




- Energy fields exists between the trace and the plane (return path) **within the dielectric material.**
- Why this is important – you're not just connecting a route, rather you are managing an EM field.



Signal Integrity Issues



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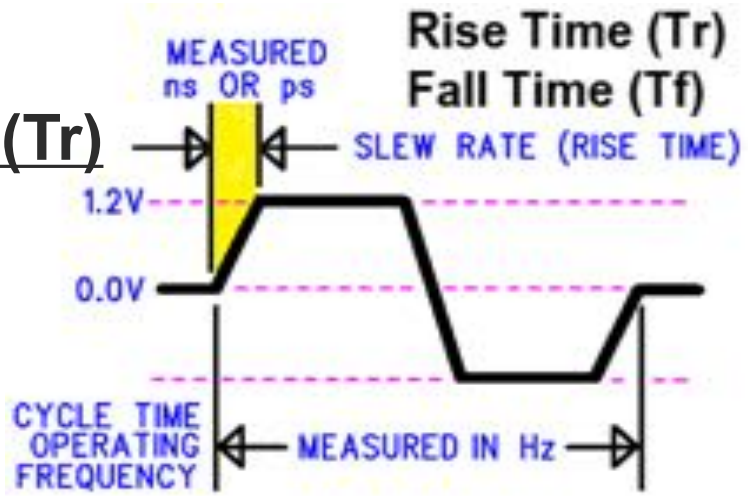
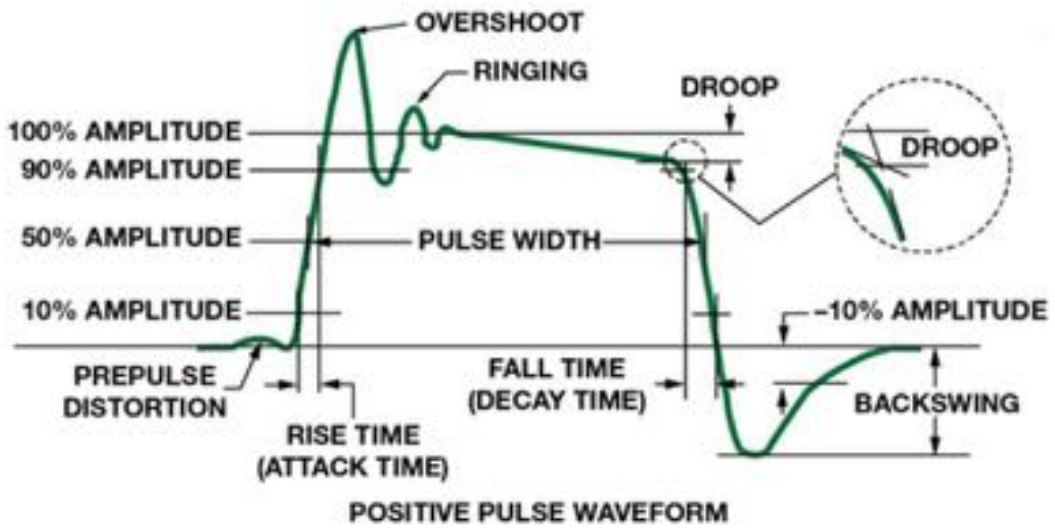
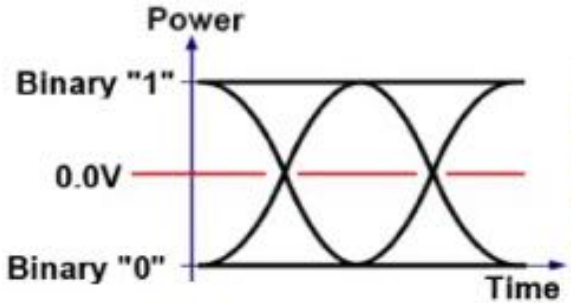
Rise Time (Tr)

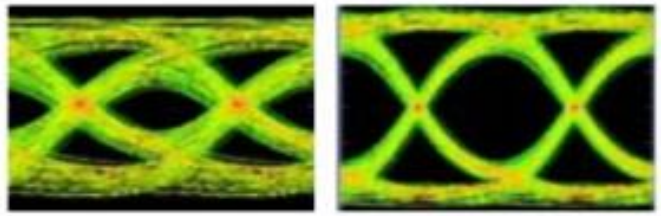


Trace length equal to ¼ of the Rise Time (Tr) signal integrity issues such as reflections start to occur with any impedance discontinuities

Ideal vs. Actual





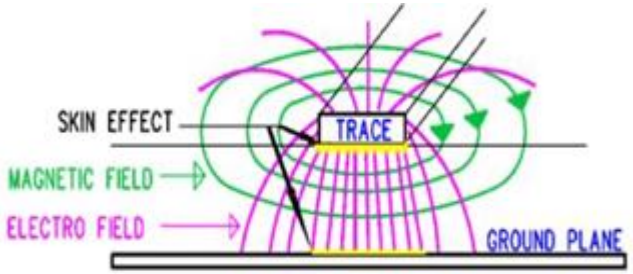


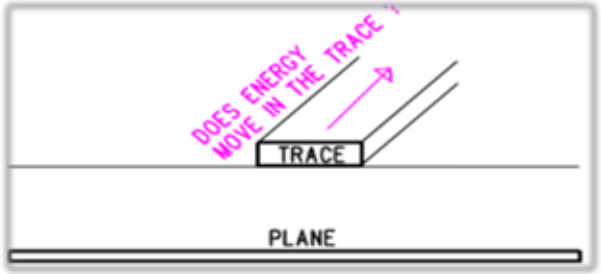
Eye Diagram

- One pulse - left image
- Billions of pulses per sec. - right image

GND (0.0V) Most Important Net

- Copper Sheets have Two Sides (Skin deep)
- Signal Energy is in the material

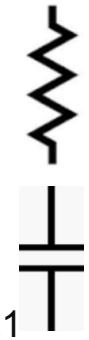




No BLACK MAGIC Secret for Stack-ups

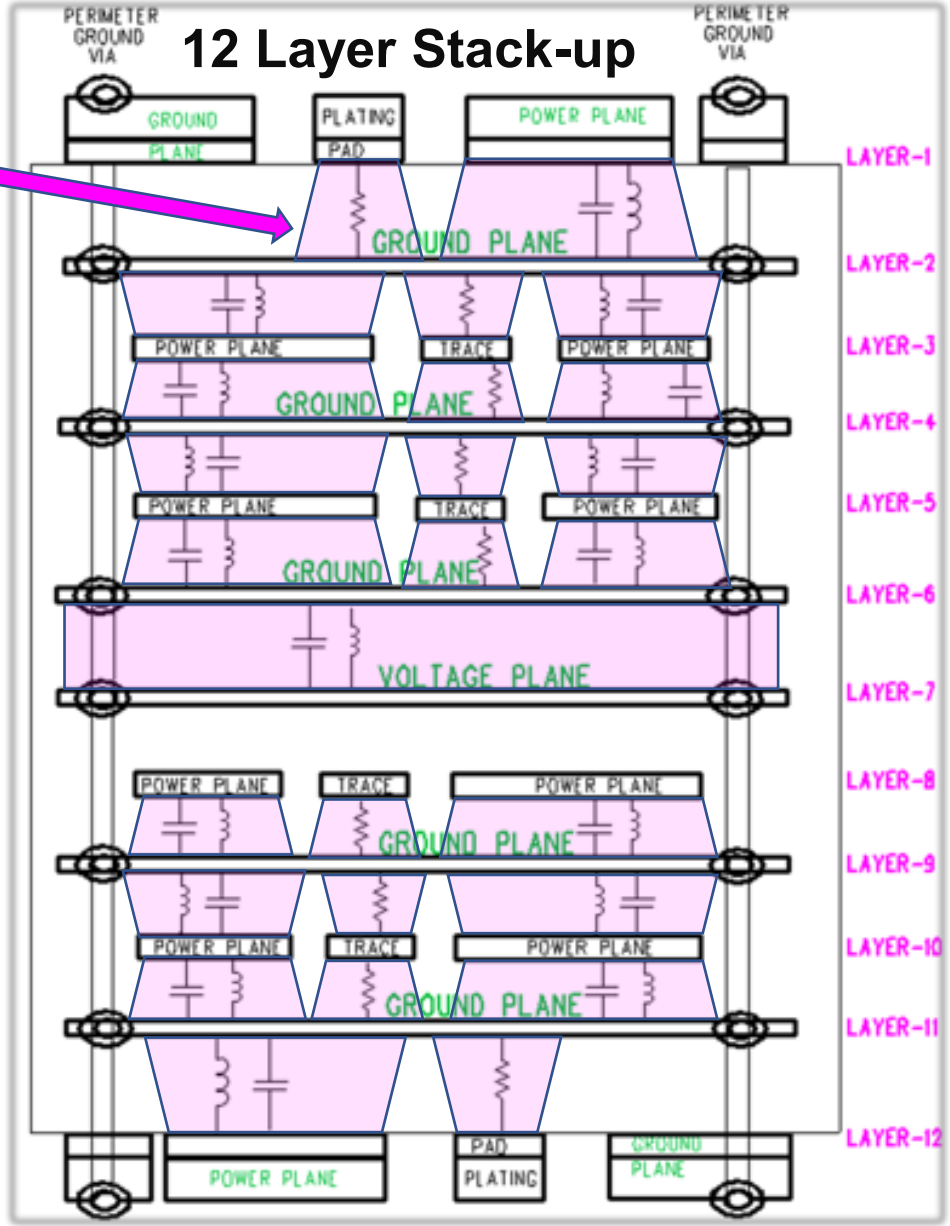
- GND (0.0V) reference every signal
- GND (0.0V) reference every PWR

When defining a Stack-up:



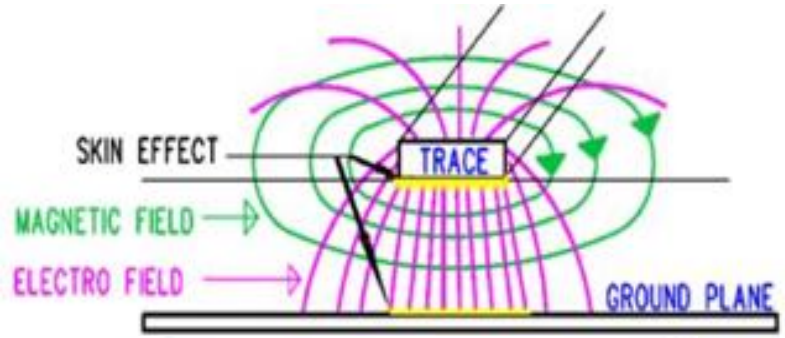
- Sketch a resistor symbol from your signal layer to an adjacent uninterrupted GND plane
- Sketch a capacitor symbol from your voltage layer to an adjacent uninterrupted GND plane

Determining a Stack-up



Reversed Treated Copper Clad Cores

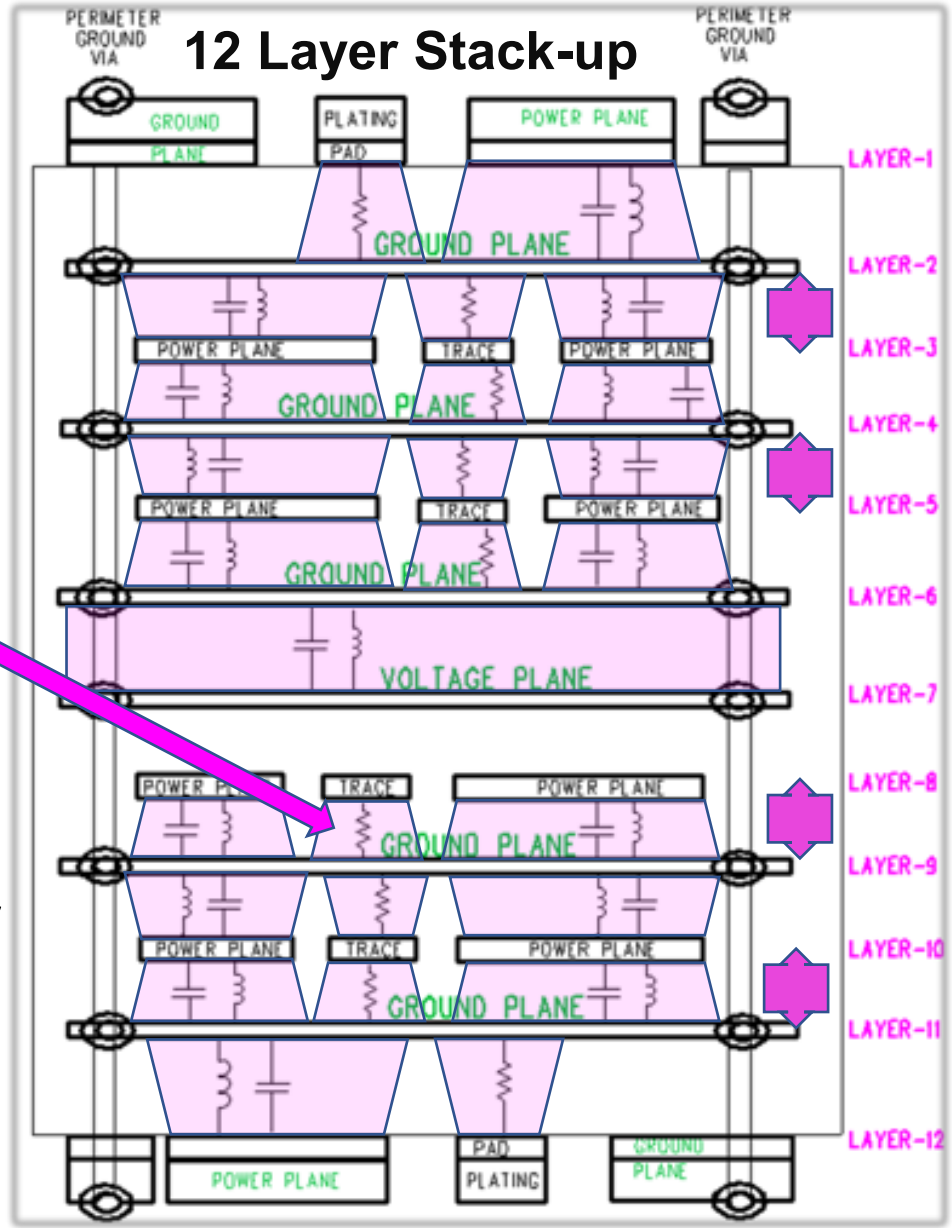
Signal Energy is in the Material, **Plan EM Field Locations** using Low Tooth Profile, Reversed Treated, Copper Clad Cores i.e.; L2-3, L4-5, L8-9, L10-11 (As shown)



Reversed Treated Copper Clad Core

EM Field is Better Suited Between Reverse Treated Core

Determining a Stack-up



Printed Circuit Engineering – Start Data

Stackup Design

Design-Request vs. Fabricator Stack-up with Manufacturing Tolerance Allowances

CAD Design by: _____.
12layer Class 2
FR370HR RoHS

Overall board thickness to be 1.57mm (.062) as required.
Surface finish NI/AU
½ oz CU on all layers, plate outers 1.4mils, and plate drill layers as required

Mech. Thru via L1-L12 .020pad/.010drill
Via in Pad, non-conductive fill, coplanar finish

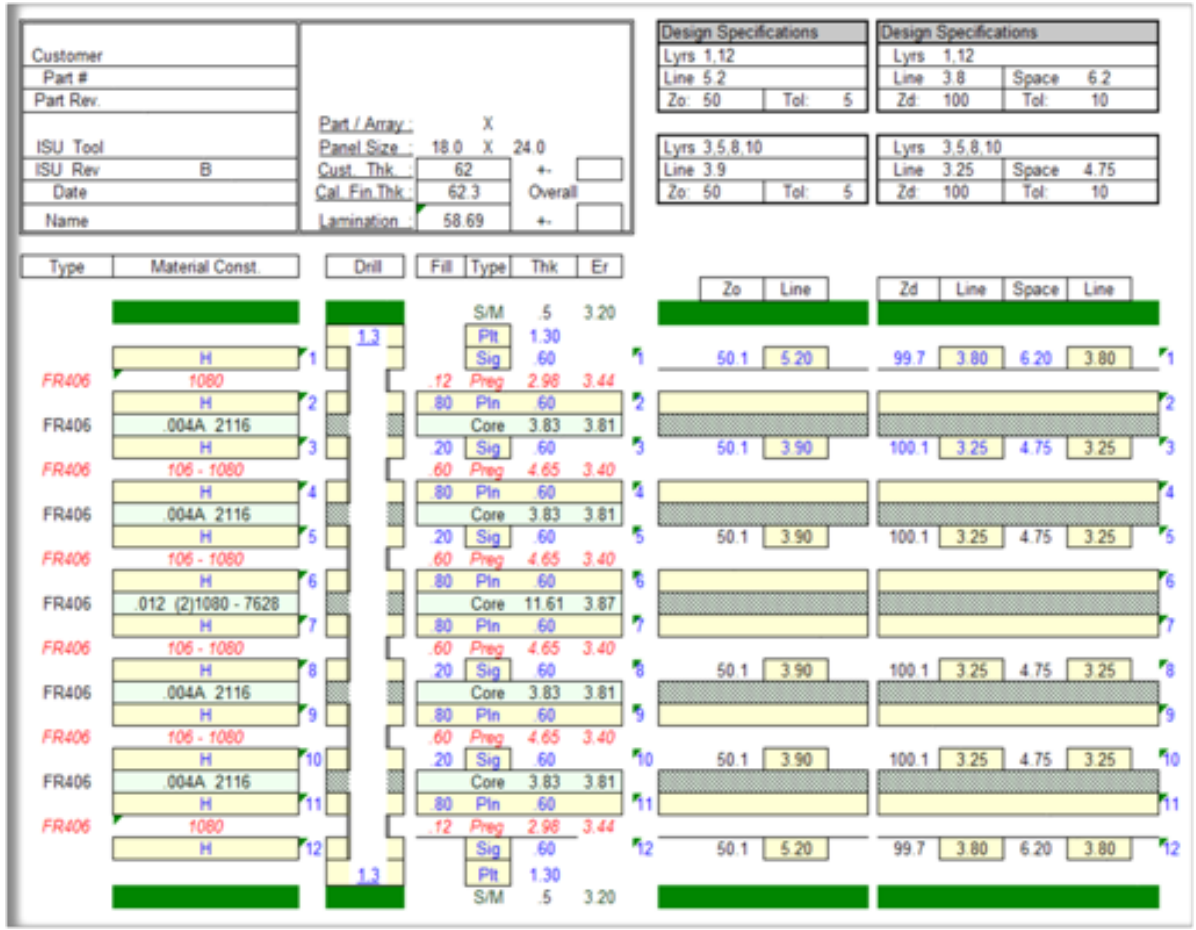
Impedance designed features: routed on .1mm grid

- **50 ohm +/- 10% .00394 Trace & space Layers 3, 5, 8, 10**
- **50 ohm +/- 10% .005 Trace & space Layers 1, 12**
  Differential pairs routed on .1mm grid with a .2mm differential pitch
- **100 ohm +/- 10% Differential Pairs - approximately .0033 Trace & .0046 space**
  - **Used on Layers 3, 5, 8, 10**
- **100 ohm +/- 10% Differential Pairs - approximately .0045 Trace & xxxx space**
  - **Used on Layers 1, 12**

12 Layer Stack-up Single-Stripline

Layer 1 Top GND/PWR & -.00_ trace-via fanout, a few diff-pairs
Layer 2 GND
Layer 3 Signal/PWR
Layer 4 GND
Layer 5 Signal/PWR
Layer 6 GND
Layer 7 PWR
Layer 8 Signal/PWR
Layer 9 GND
Layer 10 Signal/PWR
Layer 11 GND
Layer 12 Bottom PWR/GND & .00_via fanout, a few diff-pairs

Sample Stack-up Request to be Submitted to Production Fabricator



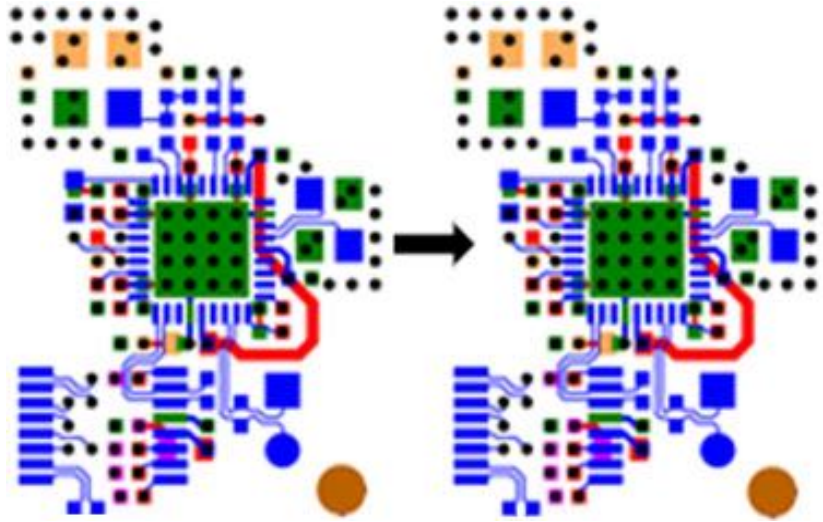
Sample Stack-up provided by Production Fabricator

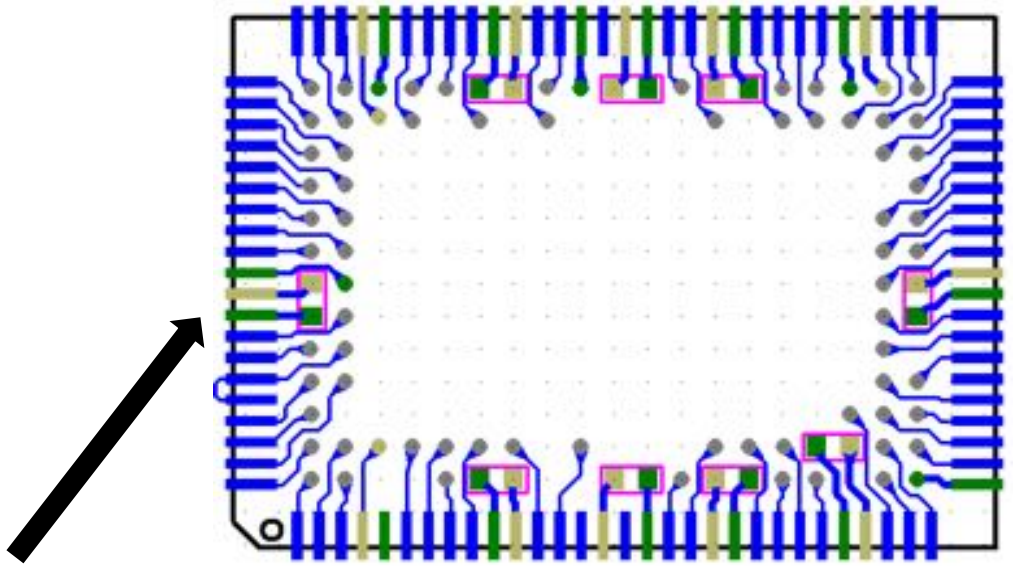
Parts Placement - Review & Approval

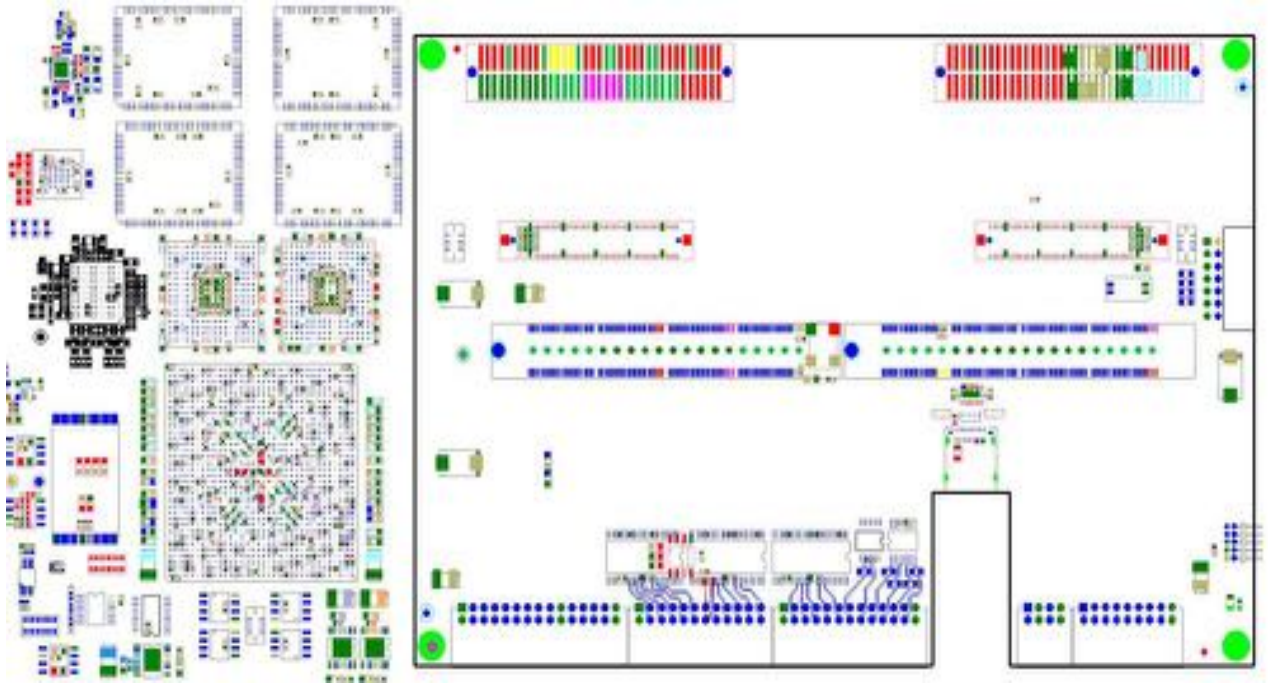
Unions build up as a **placement grouping** from the schematic or application note. Shown on right

All relative components should be included in these groupings. Replicated with Multichannel Placement functionality.

Build about a **Metric VIA GRID** Routing usage with consistent **characterization** and **repeatability**. As shown below

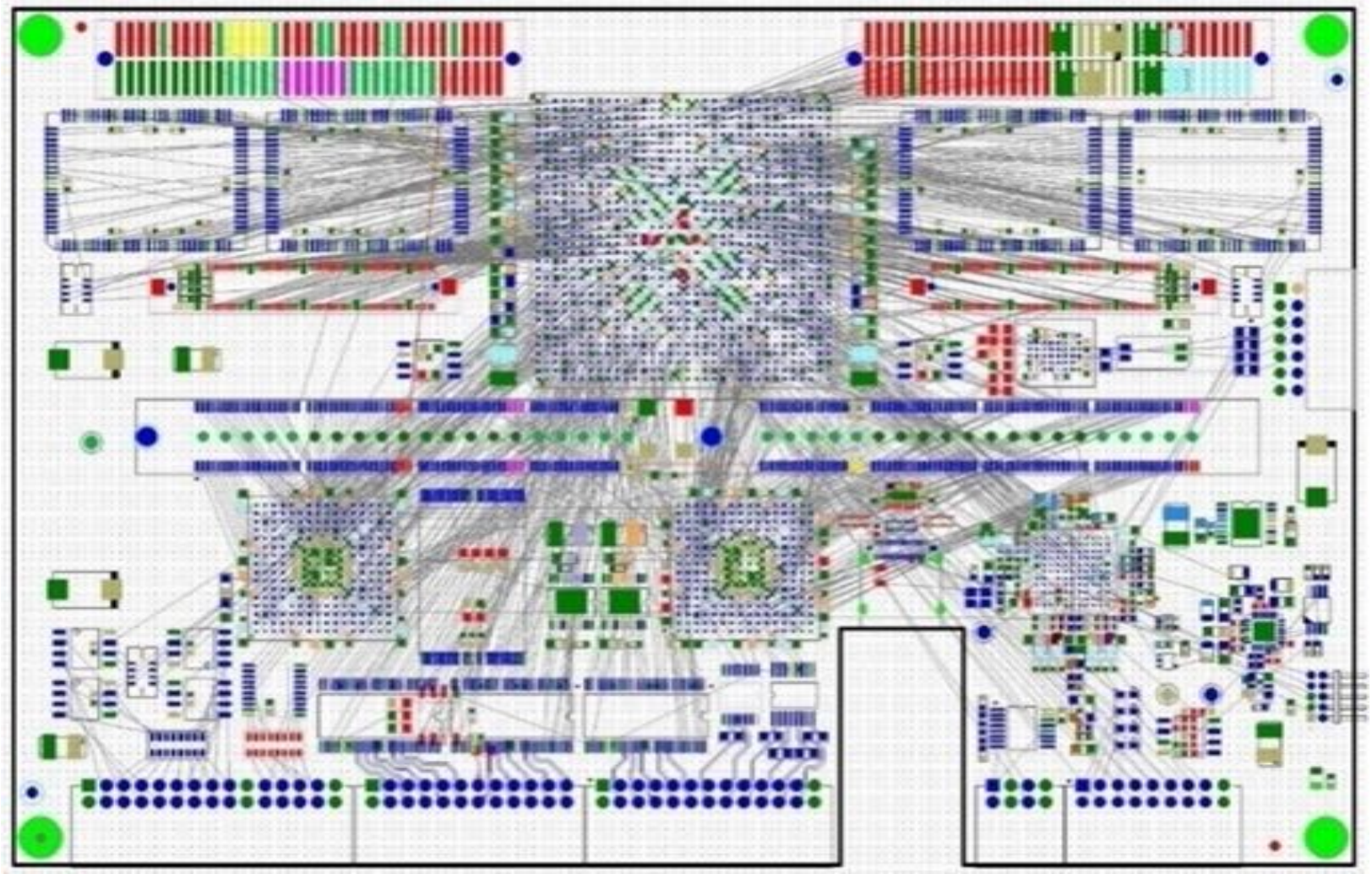




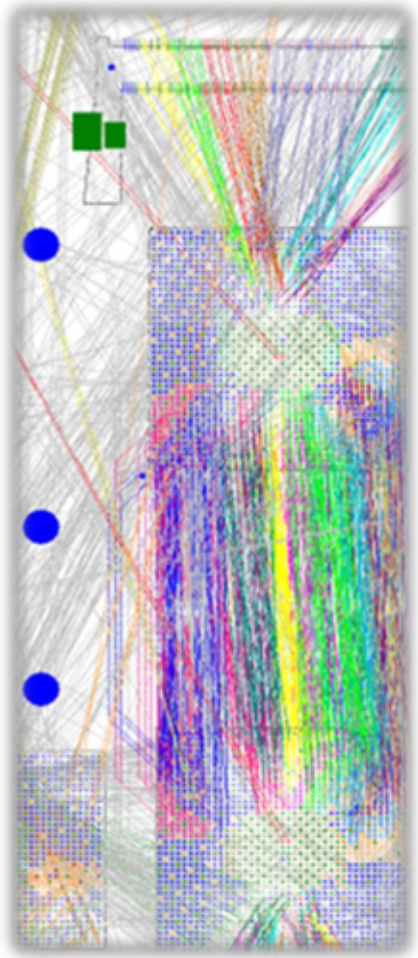


Unions Created Outside Board Outline, Floorplanning

Parts Placement - Review & Approval

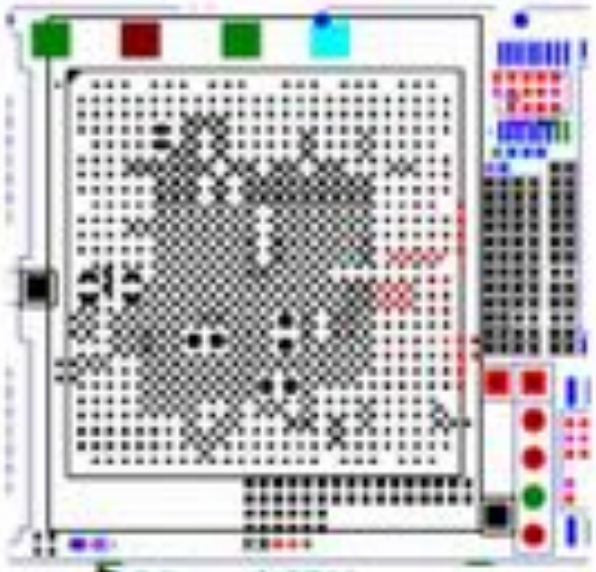


Floorplan Placement of Union Groupings



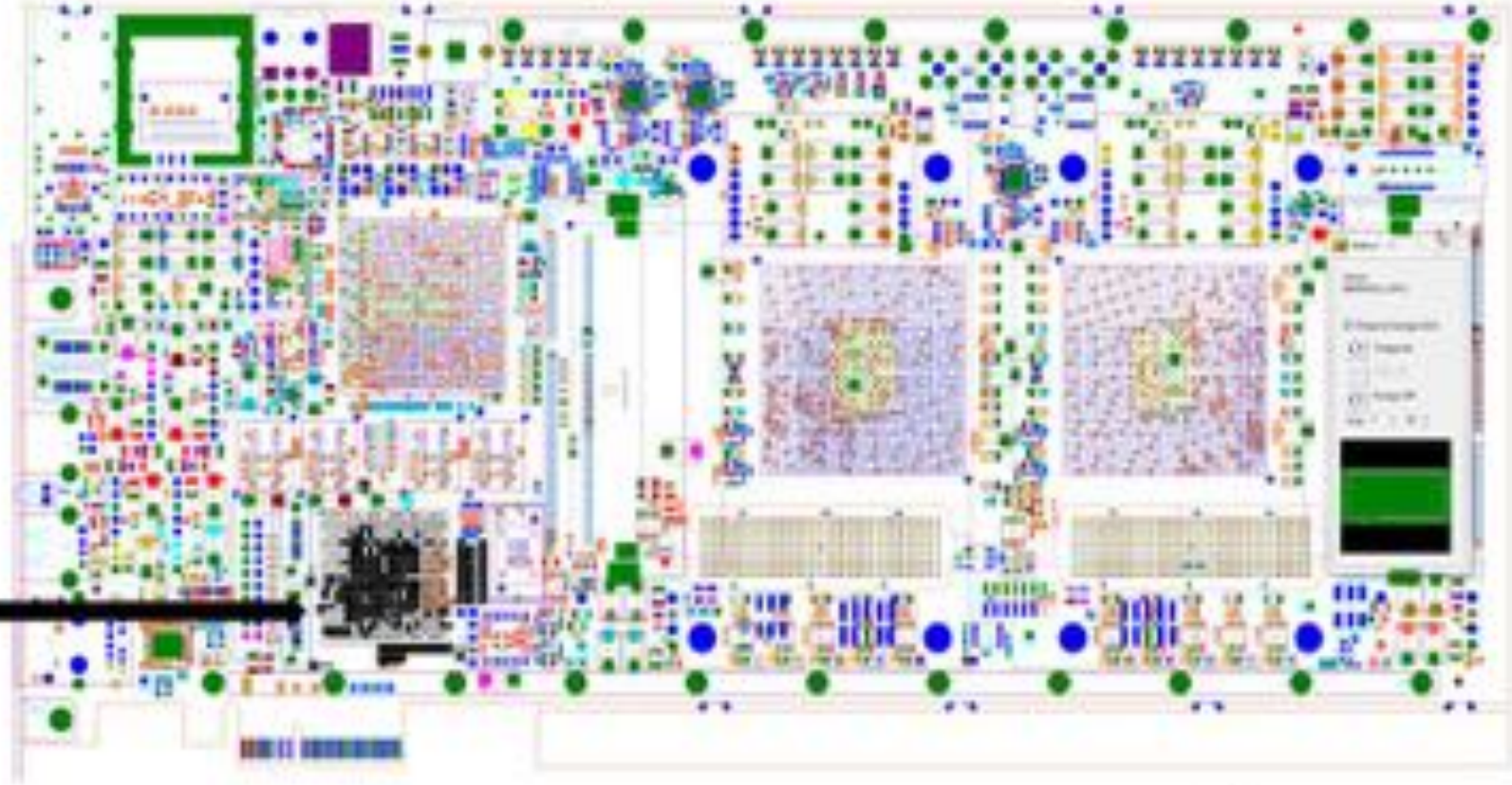
Color Coded Net-Classes
- Placement Aid

Parts Placement - Review & Approval



Marvel CPU

Create UNIONs (Groups of associated Parts)



One component grouping called by its functional name Marvel CPU

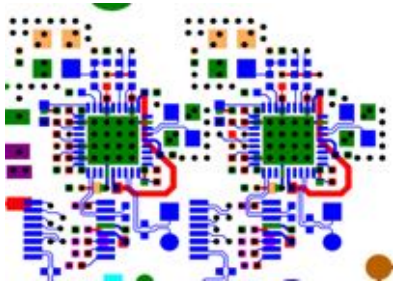
114 Unions placed as functional blocks

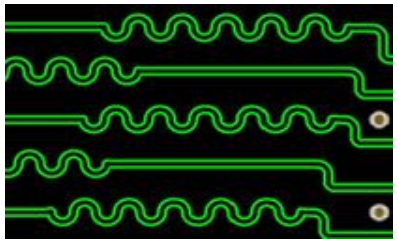
Which would you prefer to do, sit with your engineer and place 114 Unions or 2,629 individual components ?

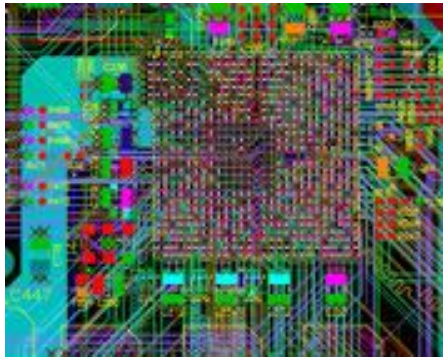
2,629 Individual Components

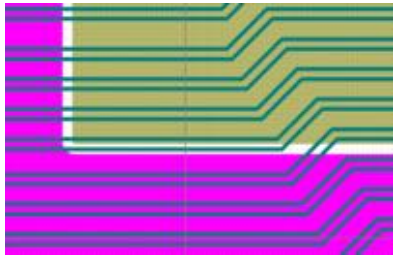
Routing – Planning & Overview

- Stack-up
- Constraint rules (**DFS** – **DFP** – **DFM**)
- Planning and feasibility during placement
- Solving the surface with SMT:
  - Pin escape
  - Short pin to pin
  - Power source
  - Testability
- Power (Source –Distribution – Usage)
- Route critical (constraints driven)
- Route bulk (is auto-routing acceptable?)
- Route clean-up (**DFS** – **DFP** – **DFM**)
- Route review (**DFS** – **DFP** – **DFM**)









Routing HSD/RF - Review & Approval

Via Fanouts – BGAs

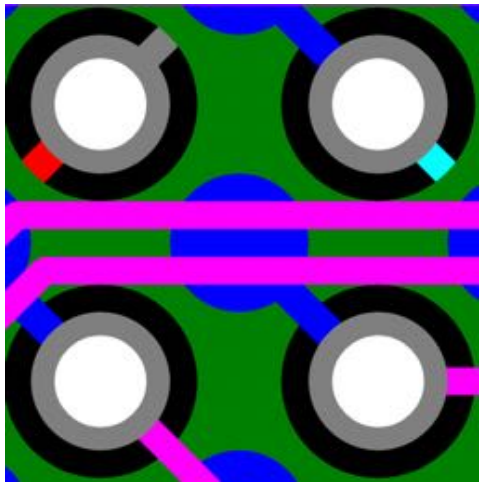
Number of I/O signals on a BGA can determine the layer count

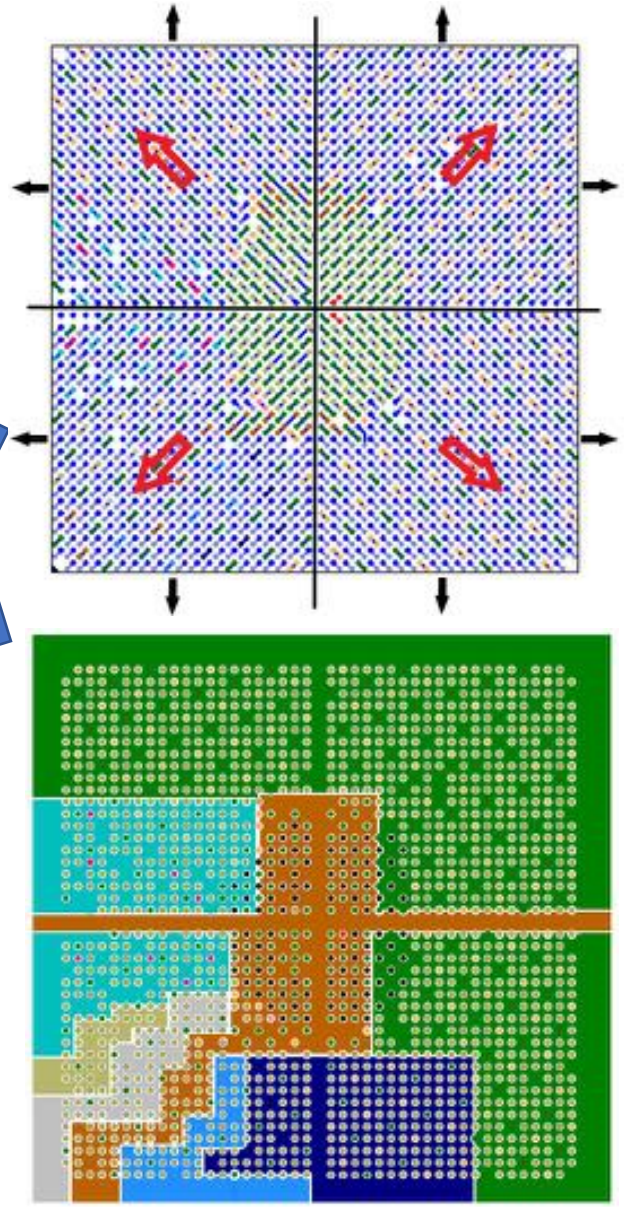
Fanout

- Use a **via-grid** with factor of pin-pitch that matches each BGA, reset origin to pin.
- Simplifies fanouts, makes them consistent.
- Wagon wheel fanout from BGA center - Allows power rails more robust entry to core power, as shown on bottom image.
- Wagon wheel route-away from BGA center in a quadrant manner to minimize cross over and layer usage.

Pin Swap

- Make routing more direct, fewer layers

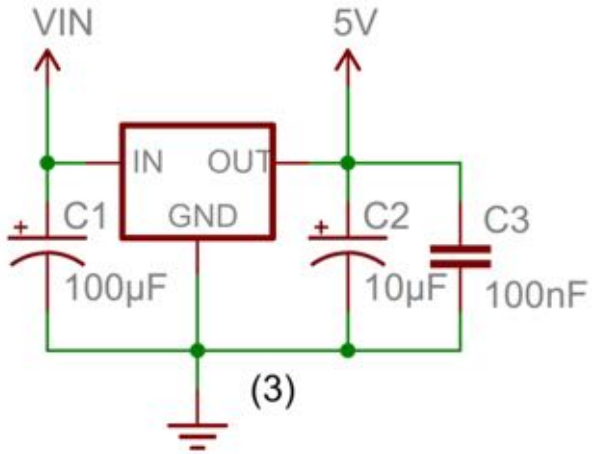




"No Micron Left Behind"
optimal 1mm pitch BGA
two track routing

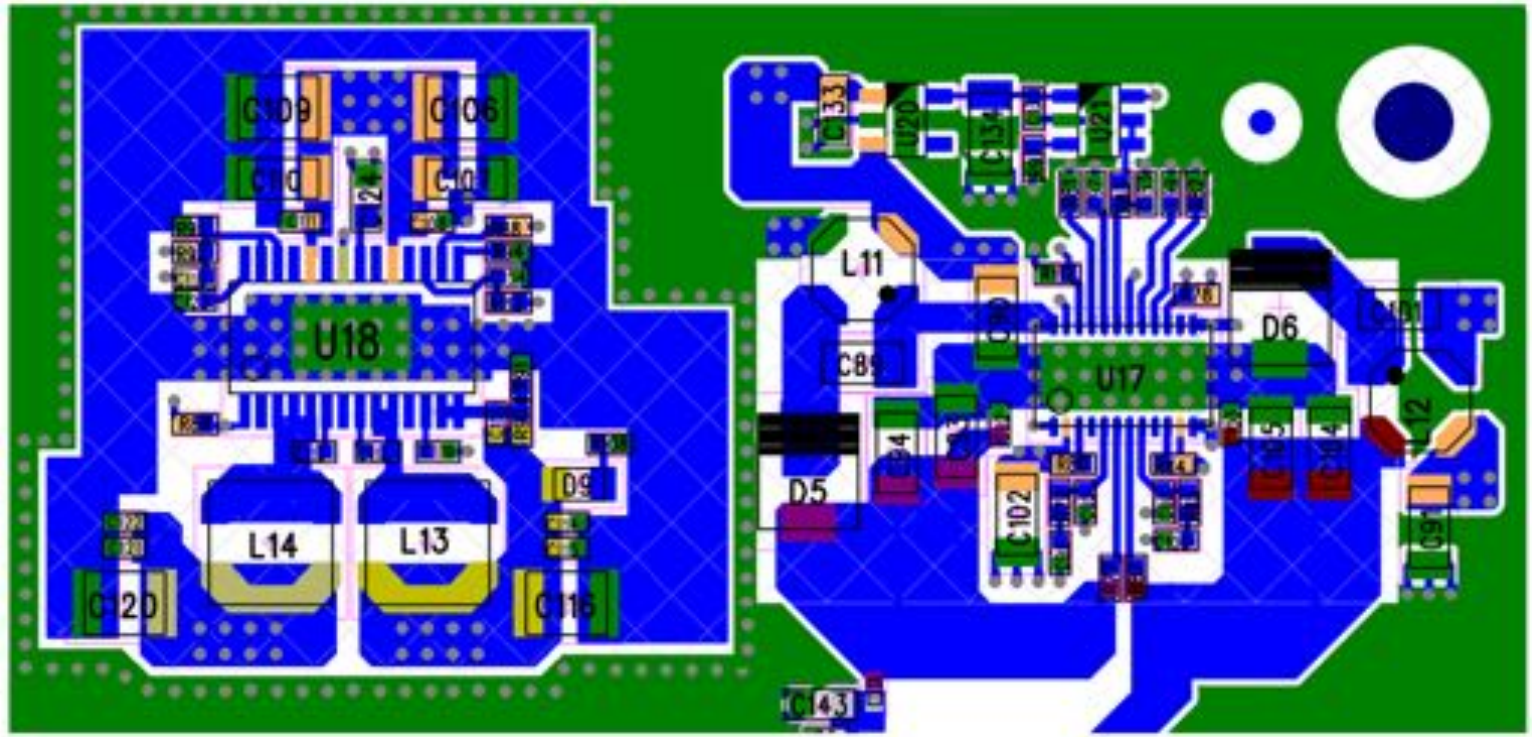
Via Fan-out, Power Dist., Completion, & Clean-up

Power Delivery – The Source



(Follow the app note)

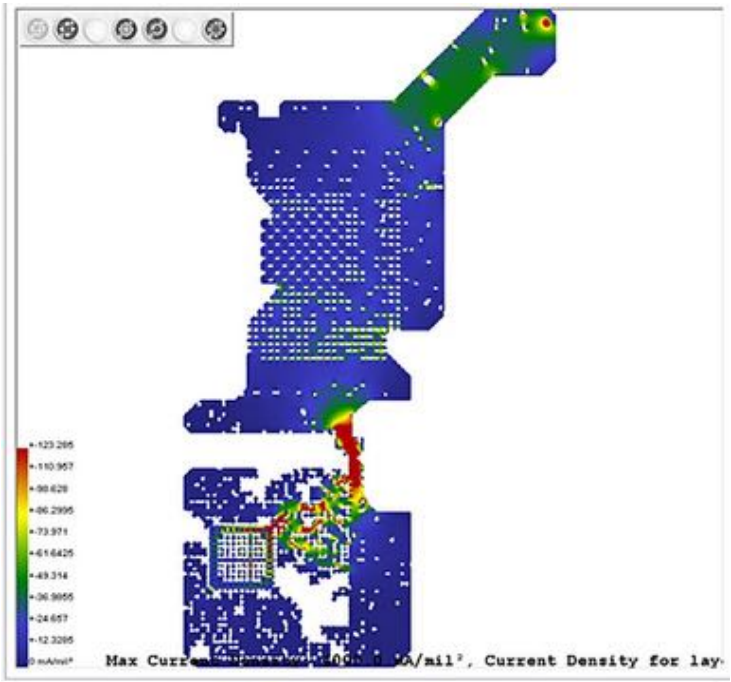
- Isolate **GND Return** to the main device, to best localize and filter noise
- Ensure **sufficient current carrying capacity** in all traces, surface planes & vias
- Any High-speed or **sensitive circuity should avoid** this area
- Use **Shields and Via Fencing** to isolate all directions XY & Z

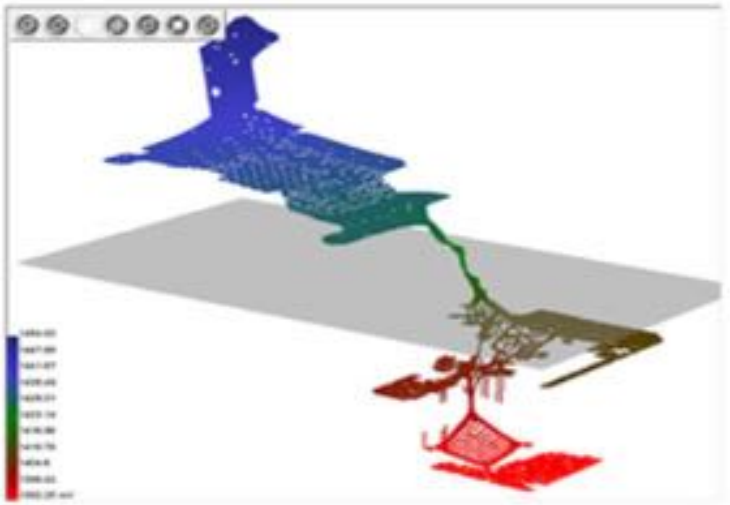


Via Fan-out, Power Dist., Completion, & Clean-up

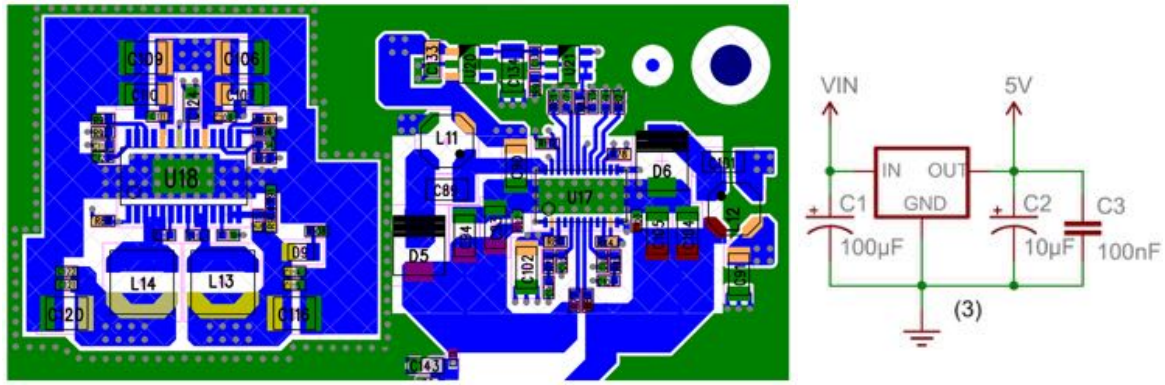
Power Delivery Challenges

- When you talk about routing you should consider your power delivery early.
- Don’t reduce plane areas with **choke points,** **same layer or layer to layer.** On each layer consider the anti-pads that will add openings, making it look like Swiss cheese. Consider the amount of vias required from layer to layer.
- ***Always*** associate **voltage planes** with **ground planes** in a multilayer stack-up for capacitive/inductive coupling.

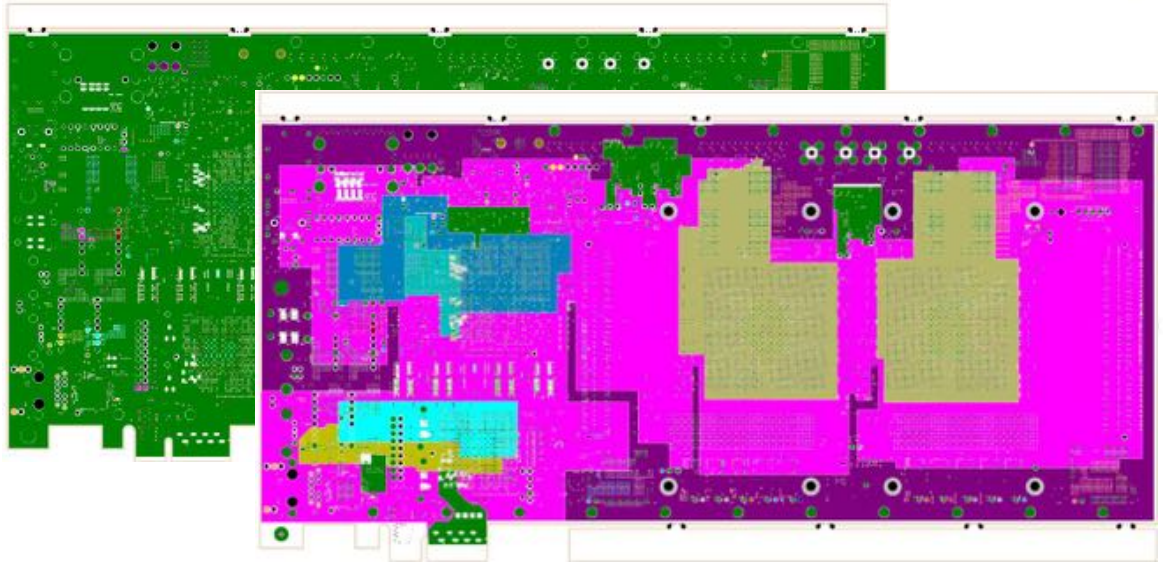




Power Delivery: Source – Distribution & Usage

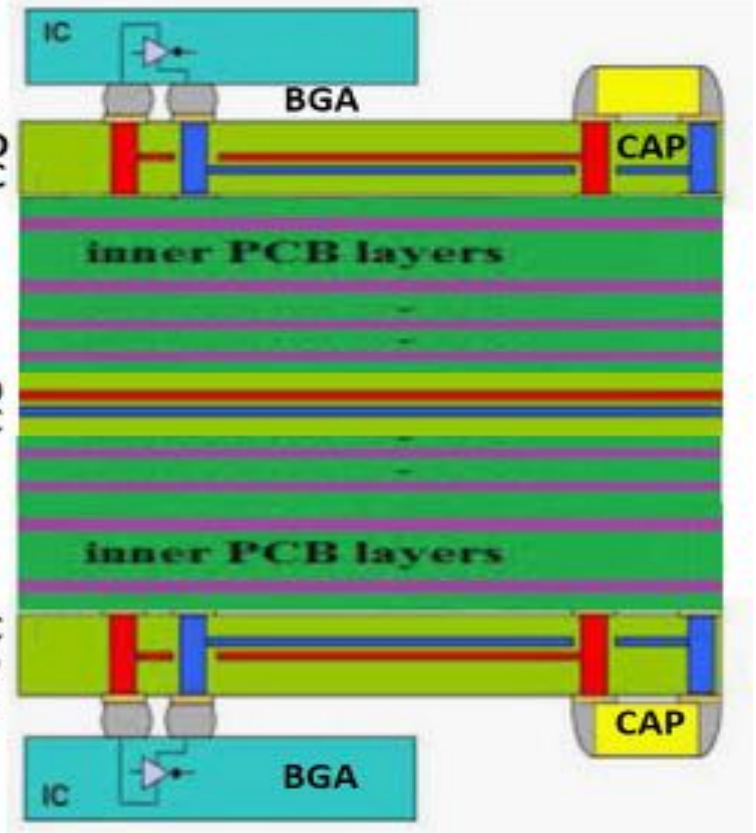


PWR Supply Layout and Schematic - Source



Uninterrupted GND Return Plane - Split PWR Planes

Distribution



Distribution and Usage Pairs

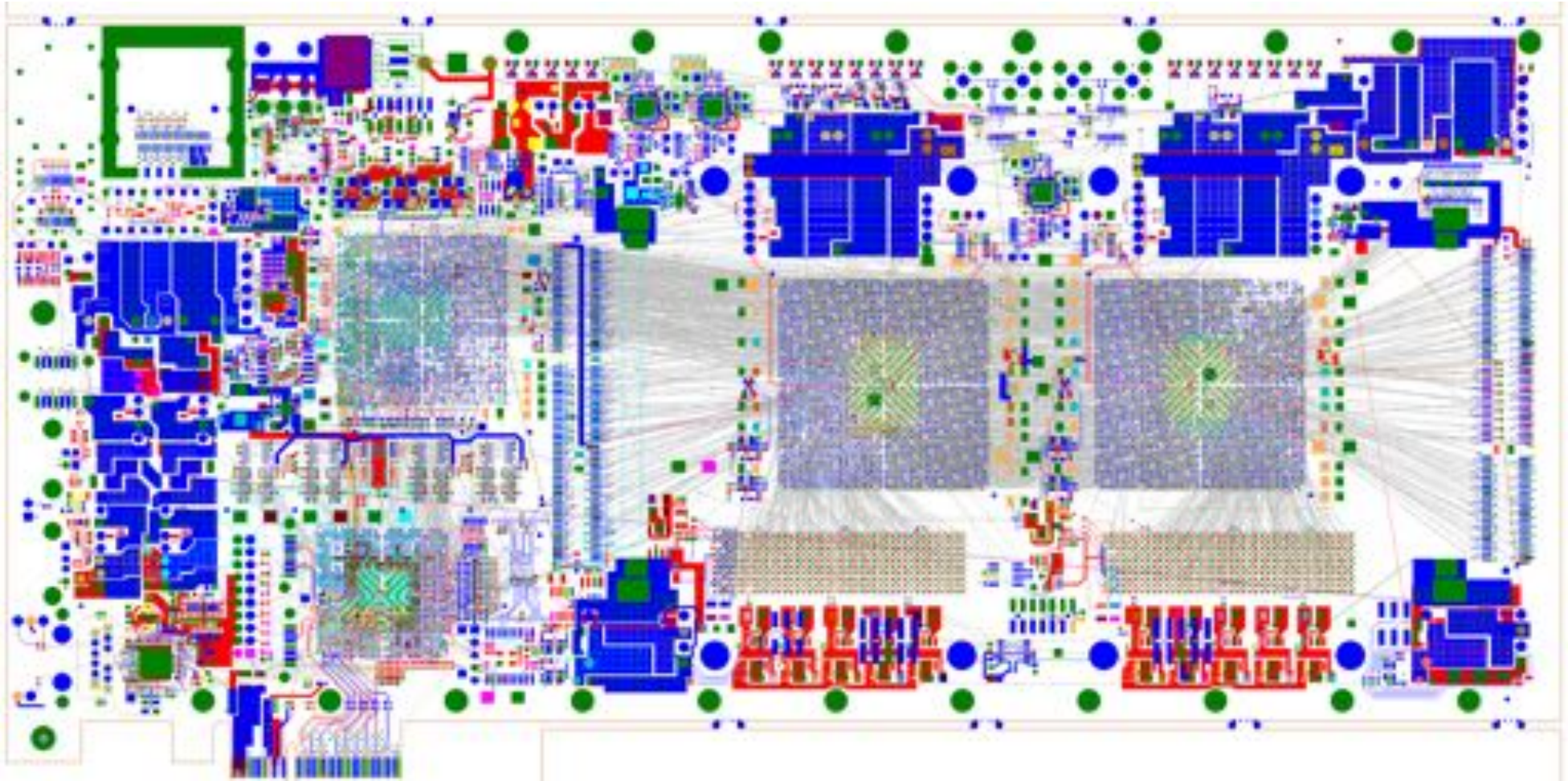
Via Fan-out, Power Dist., Completion, & Clean-up

Solving the outer Layers first

Route the outer layers: SMT pins to **via-fanout using a via grid**. Then route surface only connections. Once completed the **outer layers should be DRC'd and locked down as unmovable**.

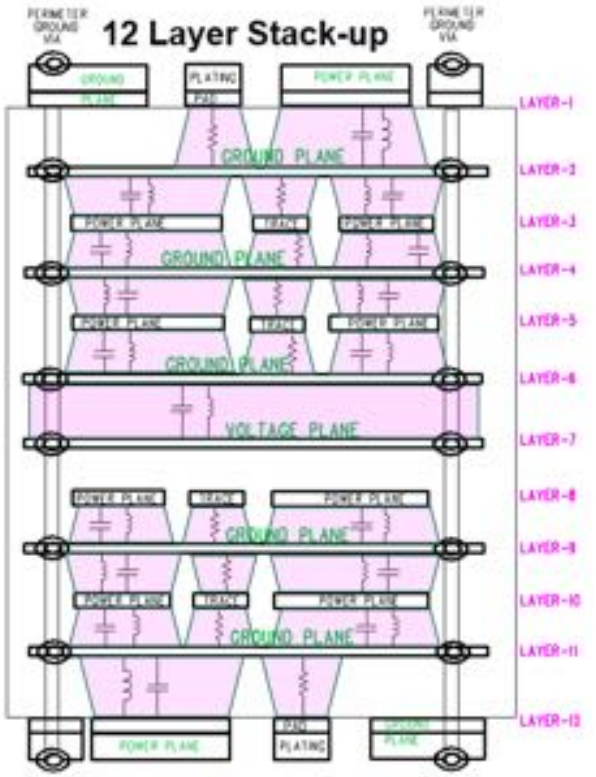
The outer layers now may be used for **power flooding** areas, assuming next layer down (Layer 2) GND plane

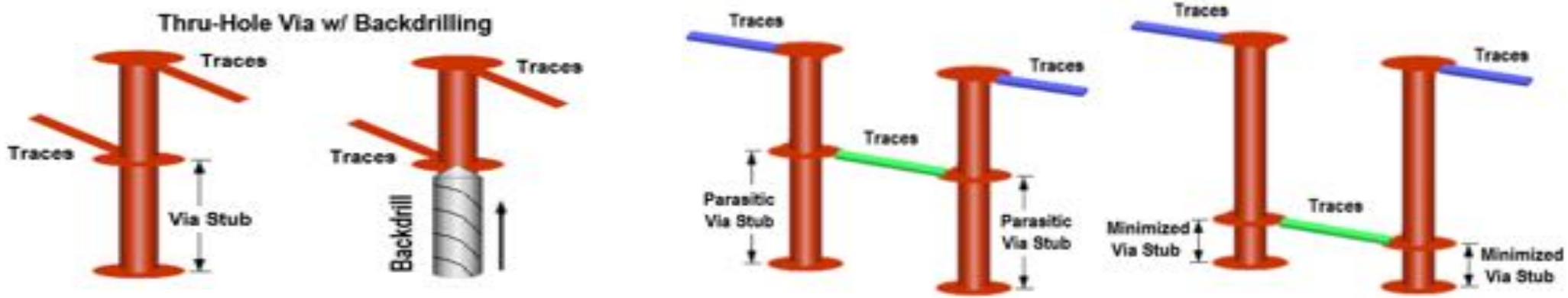
(Un-routes shown)



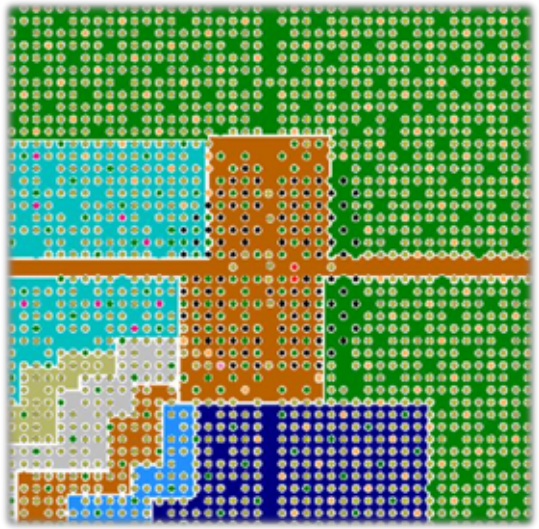
Signal Layer Usage:

- Once outer layers are solved and DRC'd – **Which internal layer should I start routing on?** Most people conclude a top-down approach **and that is wrong**. It leaves the most via stubs.
- Therefore, maximize lower layers first when routing. This will allow for **Power Distribution layer-pairs positioned higher in the stack-up and closer to the device of use (Reduced Inductance).**
- Fabrication allowances should be made for plating, if routed on outer layers. Digital signals when routed stripline **(inside of GND planes) will better contain emissions.**
- Digital signals perform best when they use the maximum depth of every via, leaving a **short stub on the via**.

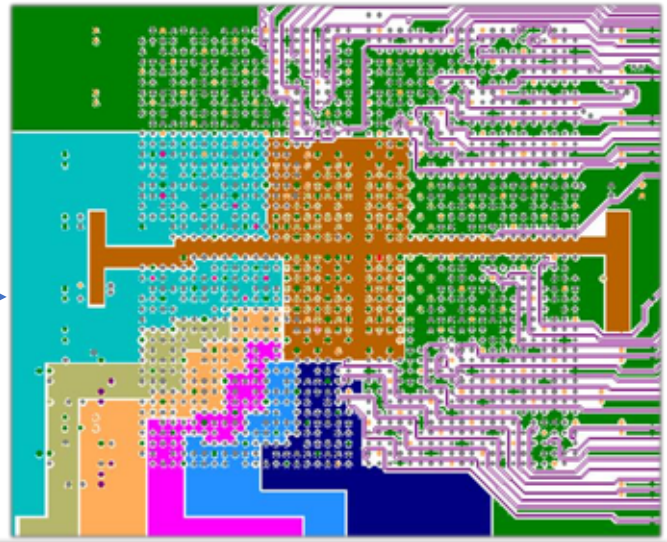




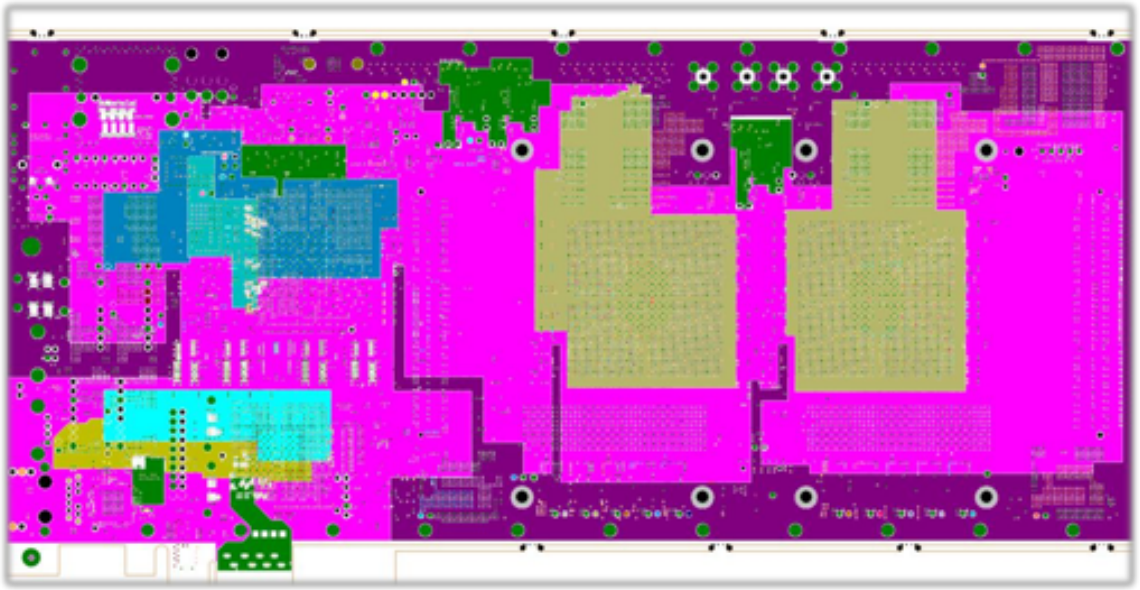
Split PWR Planes & Uninterrupted GND Return Planes



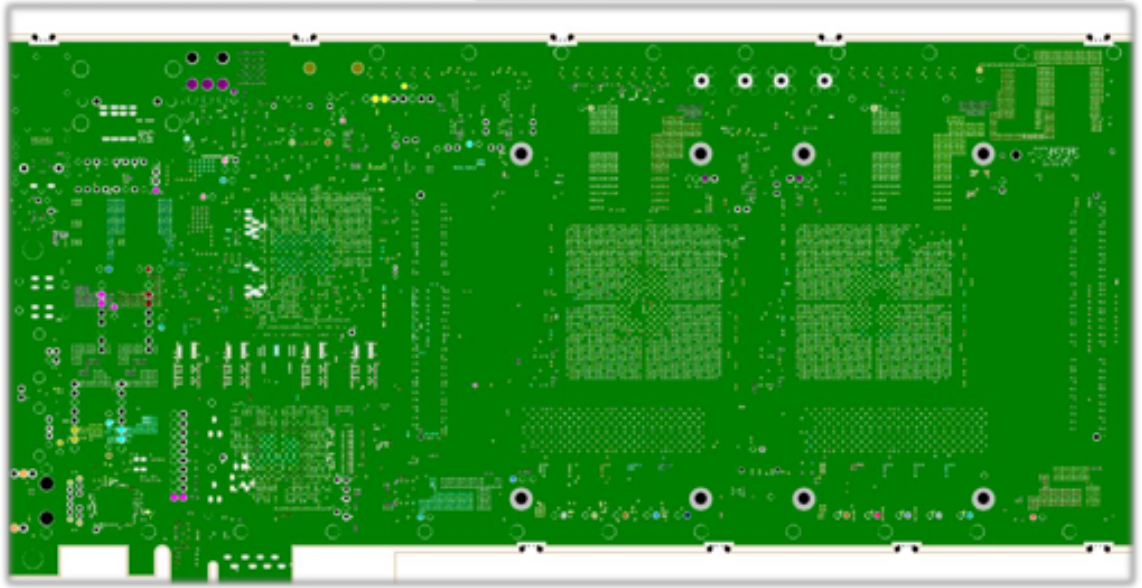
All Split PWR Planes can have dual usage; PWRs & Traces



Split PWR Planes Under a BGA Help to Balanced Copper



Split PWR Plane



Uninterrupted GND Return Plane

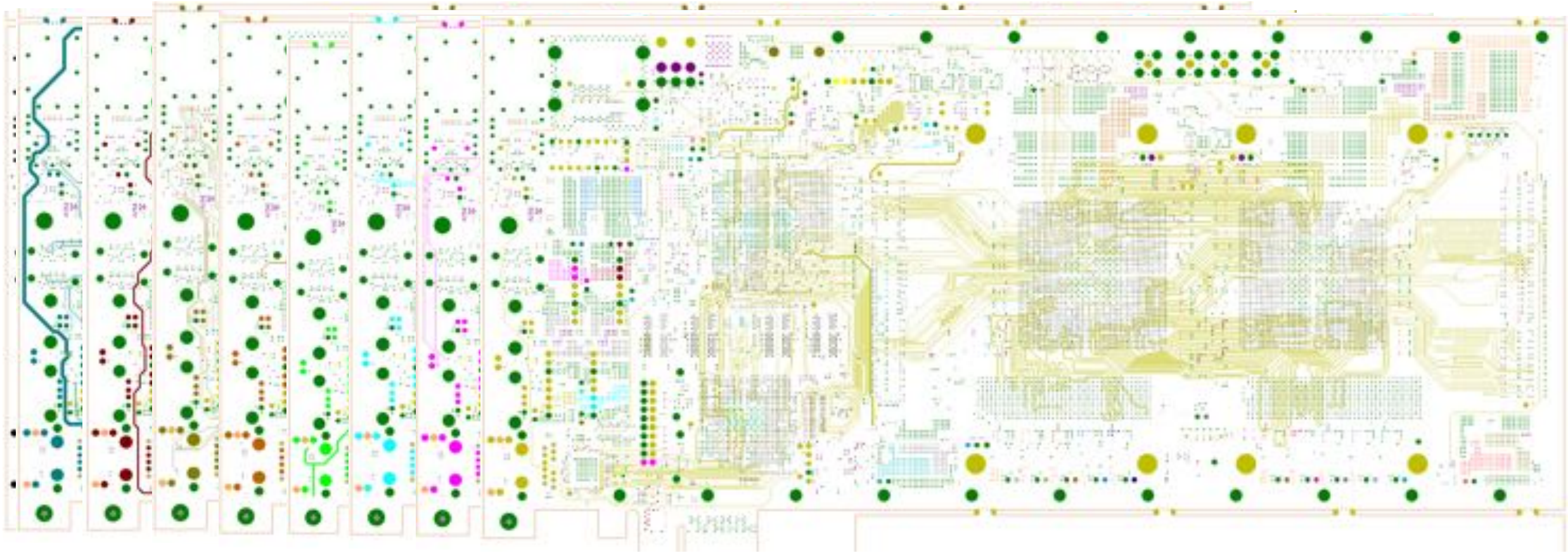
Via Fan-out, Power Dist., Completion, & Clean-up

Solving the Inner Layers next…

Prior to routing the inner layers, the outer layers and all vias are locked down.

The inner layers are a resource to solve all remaining signal and power connections.

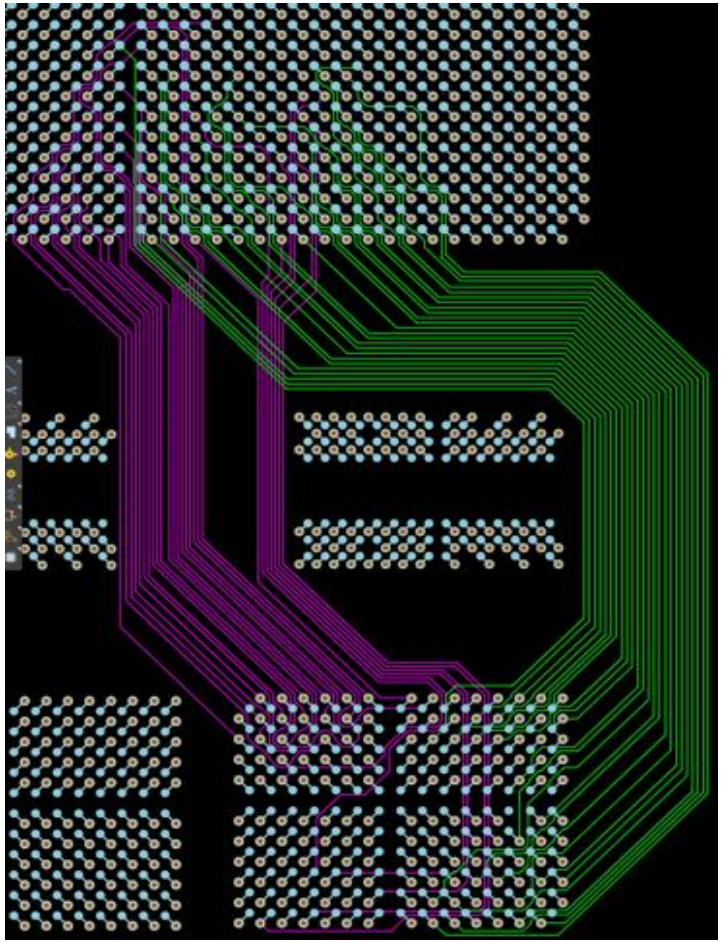
Insure a GND return path is adjacent to every signal layer on at least one side.



Electrical Performance of Advanced Routing

Improved Routing Software Enables Productivity

- **Take advantage of automation**
  - **Auto-interactive**
  - Does it allow designer control?
  - Does it produce manual quality?
- **After careful via fanout**
  - **Quickly solve large amounts of rules-controlled busses**
- **Gloss & Retrace**
  - **Better diff. pair quality and implemented faster**
  - Pad entry, change width gap, etc.
- **Routing Cleanup**
  - **Every layer, every trace**

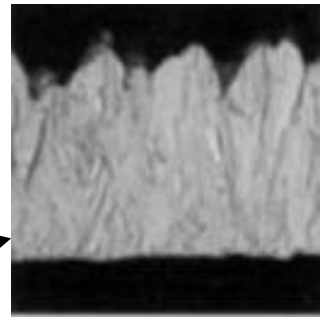


Never Auto-Route the Entire Board Inner & Outer Layers

Routing HSD/RF - Review & Approval

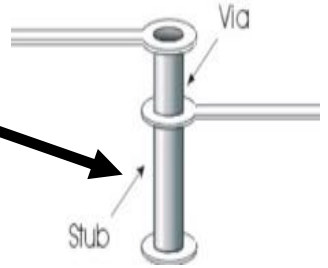
Routing – RF style

The **RF circuit** is often lower in volume of routing, but it is extremely more sensitive to every feature in its routing topology.



Wider traces provide a less lossy transmission and require increased dielectric thickness to maintain 50-ohm impedance. "Welling down" to a lower layer may be required.

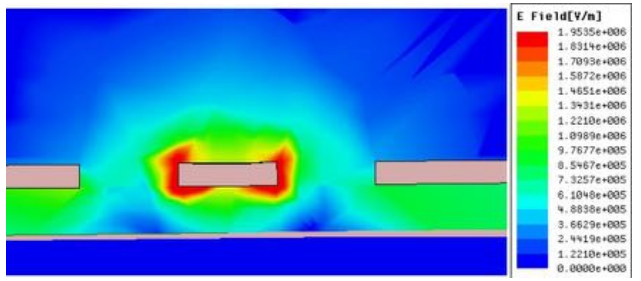
Reduce Signal Loss (Df): **wide traces, low loss material, low profile copper.**

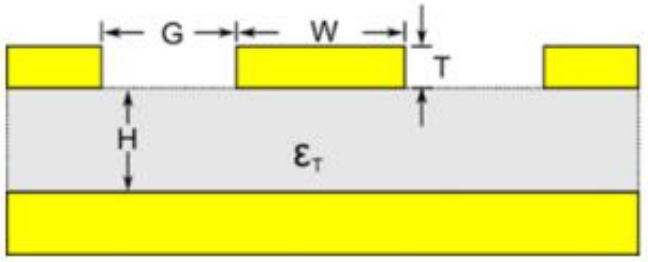


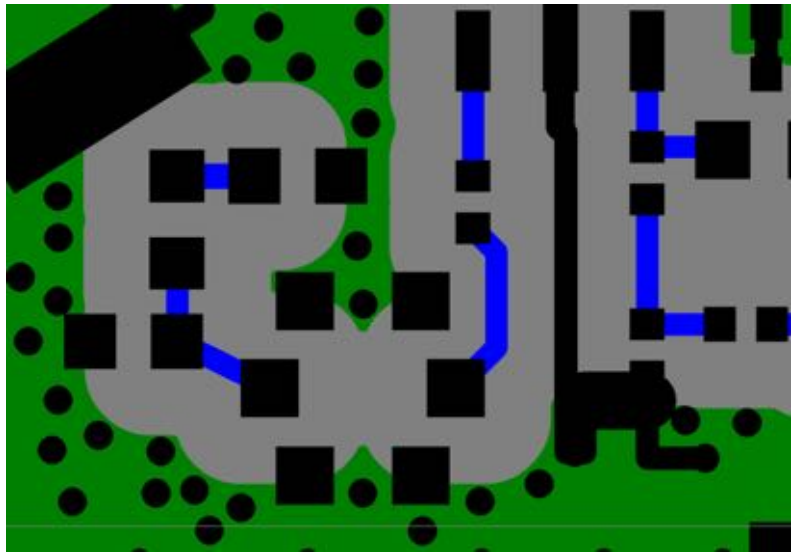
Vias on transmission lines are problematic because they often leave **radiating stubs**.

Coplanar waveguides are often utilized to control EM (Electro-Magnetic) signature with shield GND vias along the way.

(3 Images)







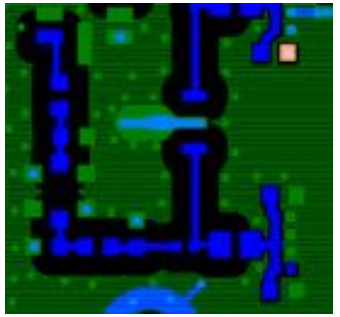
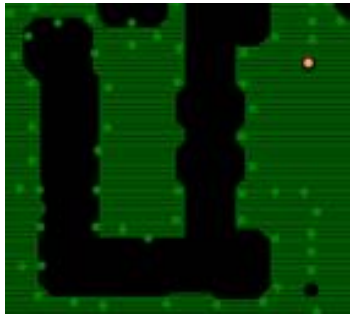
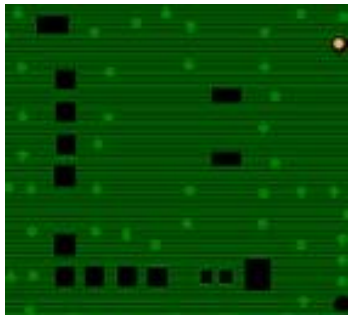
Isola's ASTRA®MT77

Is a great RF laminate with low loss performance points similar to PTFE material but it's not dissimilar to other epoxy materials in the stack-up, will improve long term product reliability.

(Mostly neat resin w/ a thin weave)

Routing – RF Circuits

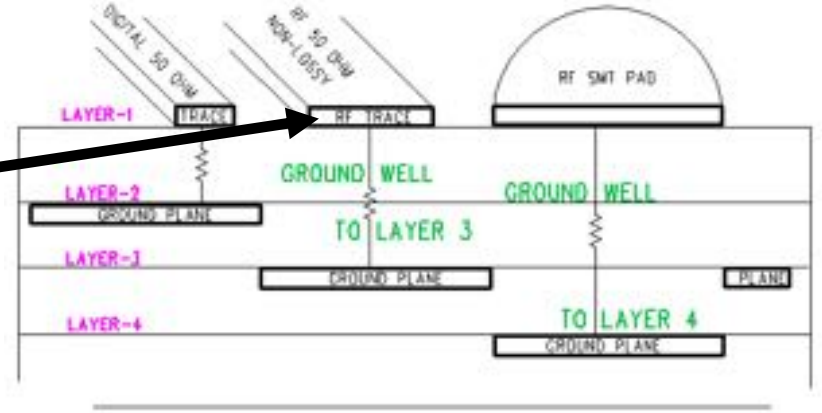
Design Practices to Reducing Loss

RF Keep-outs & Ground-wells on: **L1** **L2** **L3**

<u>3 Factors Contribute to Insertion Loss (Df):</u>

1. **Wide Traces** = with matching dielectric thickness
2. **Copper Profile** = Rz .7um - 18um (.1-.2 dB loss/cm)
3. **Material Dissipation Factor** = Df .0009 to .020



At 10Ghz - 80% of all loss, dominated by trace width and copper roughness, measured (dB/cm)

Layout – Summary

PCB Carolina 2022

Technically Appropriate Materials

- **Don't Let someone select your component values, don't let them select your Material Values**

Solvability:

- Capture Circuit & Mechanical, w/ Appropriate Rules
- Co-Engineer with Fabrication & Assembly Supply Chain
- Place & Route with correct by construction DRC's

Performance:

- High-Speed, RF and Antenna - Signal Integrity, Thermal, EMI/EMC, & Power Delivery

Manufacturability:

- High Yield = Low Cost
- High Process Producibility
- High Quality and Reliability

Thank You!

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