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Flash Memory Technologies and Costs Through 2025 (C-9)

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NAND Companies and Current Status



- The 96L generation (92-96 active layers) is the dominate technology today
 - Ideal for 512Gbit, works for 256Gbit, Capable of 1Tbit+
 - >50% of bits shipped
- 128L Generation (112-144L Active) is being introduced.
 - Less than 15% of bits in Q4 2020.
- 176L Generation (~160-192L) is being announced and developed
- 256L Generation is possible by all companies with no limit
- Note: We are doing new technologies for lower cost, not capacity



Company Updates



- Samsung: Moving to 128L, Still one string stack, no CUA (CMOS Under Array) yet. Shipping Today
- Hynix: Moving to 128L, 2 string stack, CUA (PUC).
- WDC/Kioxia: 112L, 2 String Stack, CUA expected
- Micron: Limited ramp on 128L 2 string stack, CUA on 1st gen RG (replacement gate=Charge trap) technology.
 - Micron is moving from floating gate to CTF
 - Minimal cost reduction expected over 96L in 2020-2021
- Intel: moving to 144L, Floating gate, CUA, 3 string stack?



Status YMTC



- YMTC: shipping 64L wafer bonded Xstacking technology.
- Moving to 128L, but 64L is just ramping so it is unclear when this would ramp. It won't be ramping in 2020. Maybe in 2021
- 64L product has excellent die size due to CUA provided by wafer stacking.
- This technology is <u>very expensive and complex</u>. It is seen as a way to allow periphery to be optimized but it is not cost competitive yet
 - Costs are 50% higher than competition IF they hit target yields
- YMTC is still less than 2% of the Industry bits shipped annually.
- If they execute to plan, they could grow to over 5% market share by 2025



Future Technologies



- All Companies have announced moves to 1yy technology in late 2021. 2xx (256L) technologies are possible.
- With Intel announcements of Hynix selloff, we would expect floating gate to end although Hynix announce continuation for 2-3 Generations
 - FYI: many companies have experimented with floating gate for alternative architectures (See IEDM papers)
- The 176L Nomenclature is being used for next generation. We expect companies to make pragmatic decision on number of layers based on yields and costs.
- With a 1-2 year cadence (18mo nominal), we expect companies to convert some but not all NAND products on each new generation.



QLC Models



- We were not originally a fan of QLC back in 2017. But is appears MLC/TLC history will repeat on QLC.
 - It will start as a little cheaper, with worse performance and endurance. Few adoptions, lots of complaints
 - Performance, caching, controllers will improve product.
 - Customers will become tolerant of issues
 - It will become dominant in bits over a 7-8 year timeframe.
- We model QLC percentage of bits around 15% in 2021, 50% after 2025.
 - Theoretically 25% cheaper, Actually 20-23% cheaper after accounting for some design and test overhead
- PLC is possible and we could expect the same timeline



MKW Ventures Model For NAND Cost Reductions

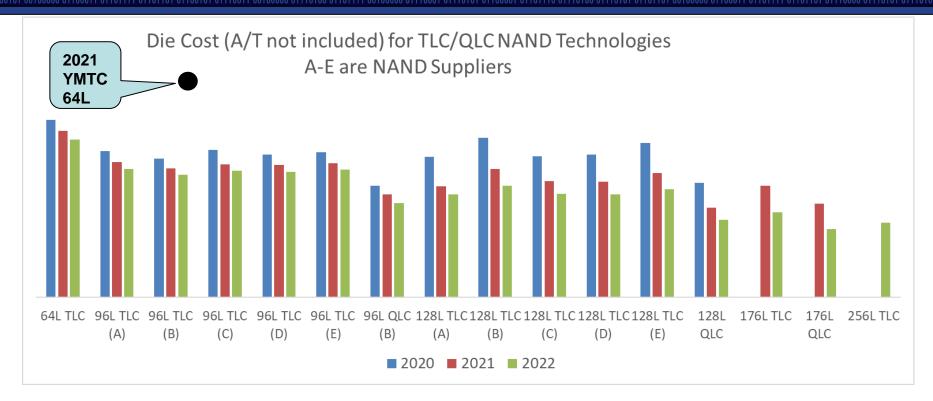


- Each generation we add 30-50% more layers.
- The <u>goal</u> is to improve manufacturing so that the output per tool is the same. Fabs and Tool vendors partner on this. No cost adder is <u>goal</u>
- In reality, we have typically added 10-15% to wafer cost for each new generation depending on inputs from tool vendors.
- String stacking adds to wafer cost. CUA adds to wafer cost.
- On mature technologies, we assume ~5-10% wafer cost improvement/year
- Based on inputs from tool and NAND companies, <u>we significantly</u> increased wafer cost improvement rate on 3D NAND technologies
 - 3D NAND is becoming more efficient at a faster rate than previously estimated



NAND Die Costs







Key Takeaways from Cost Slide

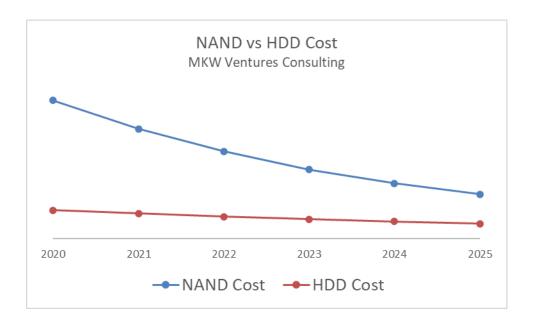


- Costs are being reduced every year and with every new technology
- We have exact numbers, company names, and reasons for numbers available in follow up discussions
- Each company has a slightly different cost reduction path
- The Cost leader at 96L is not the cost leader at 128L
 (They are modeled as highest cost for 128L)
- We have line of sight to at least 256L



Overall Average Cost Trends





- NAND Average Costs Below 2c/GB after 2025
- Cost reduction for NAND is 20% per year on average
 - New technology+ Cost learning +QLC percentage
- NAND and HDD costs crossover sometime after 2033
- UPDATE: If we had 100% Penta-Level Cell, crossover is 2031
- Nearline HDDs will be around for a long time
- Numbers and Log plot available



NAND Market and ASPs



- The NAND pricing market recovered some in early 2020 but has since struggled
- NAND Operating margins are minimal
- Bit growth is unclear but probably around 30% CAGR
- Bit costs will drop 20% per year on average
- All of these numbers add up to a challenging financial model if prices drop >20% per year (20-25% is model)
 - Result would be a slow down in new technologies and capex



Summary



- No end in sight for NAND technology progression and cost reduction
 - There are no major limiters
- QLC improves costs and will grow to 50% of bits after
 2025
- NAND Costs will reach 2c/GB after 2025.
- Cost leaders change over the next 5 years
- Costs are modeled to cross HDD cost after 2033





- All of the numbers, back up charts, company names and reasons for numbers are available. Call us to discuss
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