SEMI CONDUCTOR

1. ENERGY BANDS IN SOLIDS

In case of a single isolated atom, there are single energy levels in case of solids, the atoms is arranged in a systematic space lattice and hence the atom is greatly influenced by neighbouring atoms. The closeness of atoms results in the intermixing of electrons of neighbouring atoms of course, for the valence electrons in the outermost shells which are not strongly bounded by nucleus. Due to intermixing the number of permissible energy levels increases or there are significant changes in the energy levels. Hence in case of a solid, instead of single energy levels associated with the single atom, there will be bands of energy levels.

1.1 Valence Band, Conduction Band & Forbidden Energy Gap

The band formed by a series of energy levels containing the valence electrons is known as valence band. The valency band may be defined as a band which is occupied by the valence electrons or a band having highest occupied band energy.

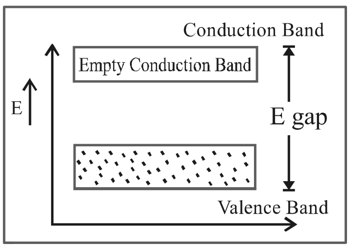
The conduction band may also be defined as the lowest unfilled energy band. The separation between conduction band and valence band is known as forbidden energy gap. There is no allowed energy state in this gap and hence no electron can stay in the forbidden energy gap.

1.2 Insulators, Semiconductors and Conductors

On the basis of forbidden band, the insulators, semiconductors and conductors are described as follows:

1.2.1 Insulators

In case of insulators, the forbidden energy band is very wide. Due to this fact electrons cannot jump from valence band to conduction band. In insulators the valence electrons are bond very tightly to their parent atoms. Increase in temperature enables some electrons to go to the conduction band.



1.2.2 Semiconductors

In semiconductors, the forbidden band is very small. Germanium and silicon are the examples of semiconductors. A semiconductor material is one whose electrical properties lies between insulators and good conductors. When a small amount of energy is supplied, the electrons can easily jump from valence band to conduction band. For example when the temperature is increased the forbidden band is decreased so that some electrons are liberated into the conduction band.

12..3 Conductors

In case of conductors, there is no forbidden band and the valence band and conduction band overlap each other. Here plenty of free electrons are available for electric conduction. A slight potential difference across the conductor cause the free electrons to constitute electric current. The most important point in conductors is that due to the absence of forbidden band, there is no structure to establish holes. The total current in conductors is simply a flow of electrons.

2. SEMICONDUCTORS

Thus a substance which has resistively in between conductors and insulators is known as semiconductor.

Semiconductors have the following properties.

(i) They have resistively less than insulators and more than conductors.

(ii) The resistance of semiconductor decreases with the increase in temperature and vice versa.

(iii) When suitable metallic impurity like arsenic, gallium etc. is added to a semiconductors, its current conducting properties change appreciably.

2.1 Effect of temperatue of Semiconductors

At very low temperature (say 0 K) the semiconductor crystal behaves as a perfect insulator since the covalent bonds are very strong and no free electrons are available. At room temperature some of the covalent bonds are broken due to the thermal energy supplied to the crystal. Due to the breaking of the bonds, some electrons become free which were engaged in the formation of these bonds.

The absence of the electron in the covalent bond is represented by a small circle. This empty place or vacancy left behind in the crystal structure is called a hole. Since an electron unit negative charge, the hole carries a unit positive charge.

2.2 Mechanism of conduction of Electrons and Holes

When the electrons are liberated on breaking the covalent bonds, they move randomly through the crystal lattice.

When an electric field is applied, these free electrons have a steady drift opposite to the direction of applied field. This constitute the electric current. When a covalent bond is broken, a hole is created. For one electron set free, one hole is created. This thermal energy creates electron-hole pairs-there being as many holes as free electrons. These holes move through the crystal lattice in a random fashion like liberated electrons. When an external electric field is applied, the holes drift in the direction of applied field. Thus they constitute electric current.

There is a strong tendency of semiconductor crystal to form a covalent bonds. Therefore, a hole attracts an electron from the neighbouring atom. Now a valence electron from nearby covalent bond comes to fill in the hole at A. This results in a creation of hole at B. The hole has thus effectively shift from A to B. This hole move from B to C from C to D and so on.

This movement of the hole in the absence of an applied field is random. But when an electric field is applied, the hole drifts along the applied field.

2.3 Carrier Generation and Recombination

The electrons and holes are generated in pairs. The free electrons and holes move randomly within the crystal lattice. In such a random motion, there is always a possibility that a free electron may have an encounter with a hole. When a free electron meets a hole, they recombine to re-establish the covalent bond. In the process of recombination, both the free electron and hole are destroyed and results in the release of energy in the form of heat. The energy so released, may in turn be re-absorbed by another electron to break its covalent bond. In this way a new electrol-hole pair is created.

Thus the process of breaking of covalent bonds and recombination of electrons and holes take place simultaneously. When the temperature is increased, the rate of generation of electrons and holes increases. This is turn increases, the densities of electrons and hole increases. As a result, the conductivity of semiconductor increases or resistivity decreases. This is the reason that semiconductors have negative temperature coefficient of resistance.

2.4 Pure or Intrinsic Semiconductor and Impurity or Extrinsic Semiconductors

A semiconductor in an extremely pure from is known as intrinsic semiconductor or a semiconductor in which electrons and holes are solely created by thermal excitation is called a pure or intrinsic semiconductor. In intrinsic semiconductor the number of free electrons is always equal to the number of holes.

2.4.1 Extrinsic Semiconductors

The electrical conductivity of intrinsic semiconductor can be increased by adding some impurity in the process of crystallization. The added impurity is very small of the order of one atom per million atoms of the pure semiconductor. Such semiconductor is called impurity or extrinsic semiconductor. The process of adding impurity to a semiconductor is known as doping. The doping material is either pentavalent atoms (bismuth, antimony, arsenic, phosphorus which have five valence electrons) or trivalent atoms (gallium, indium, aluminium, boron which have three valence electrons). The pentavalent doping atom is known as donor atom because it donates one electron to the conduction band of pure semiconductor.

The doping materials are called impurities because they alter the structure of pure semiconductor crystals.

2.4.2 N–Type Extrinsic Semiconductor

When a small amount of pentavalent impurity is added to a pure semiconductor crystal during the crystal growth, the resulting crystal is called as N-type extrinsic semiconductor.

In case of N-type semiconductor, the following points should be remembered

(i) In N-type semiconductor, the electrons are the majority carriers while positive holes are minority carriers.

(ii) Although N-type semiconductor has excess of electrons but it is electrically neutral. This is due to the fact that electrons are created by the addition of neutral pentavalent impurity atoms to the semiconductor i.e., there is no addition of either negative changes or positive charges.

2.4.3 P–Type Extrinsic Semiconductor

When a small amount of trivalent impurity is added to a pure crystal during the crystal growth, the resulting crystal is called a P-type extrinsic semiconductor.

In case of P-type semiconductor, the following points should be remembered

(i) In P-type semiconductor materials, the majority carriers are positive holes while minority carriers are the electrons.

(ii) The P–type semiconductor remains electrically neutral as the number of mobile holes under all conditions remains equal to the number of acceptors.

2.5 P–N Junction Diode

When a P-type material is intimately joined to N-type, a P-N junction is formed. In fact, merely-joining the two pieces a P-N junction cannot be formed because the surface films and other irregularities produce major discontinuity in the crystal structure. Therefore a P-N junction is formed from a piece of semiconductor (say germanium) by diffusing P-type material to one half side and N-type material to other half side.When P-type crystal is placed in contact with N-type crystal so as to form one piece, the assembly so obtained is called P-N junction diode.

2.5.1 Forward Bias

When external d.c. source is connected to the diode with p–section connected to +ve pole and n–section connected to –e pole, the junction diode is said to be reverse biased.

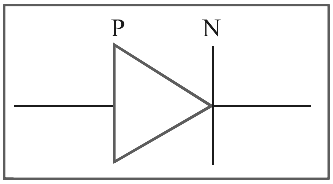
2.5.2 Reverse Bias

When an external d.c. battery is connected to junction diode with P–section connected to –ve pole and n–section connected to +ve pole, the junction diode is said to be reverse biased.

Note..

P–N JUNCTION is such a device (any way) which offers low resistance when forward biased and behaves like an insulator when reverse biased.

Symbol :



2.6 Junction Diode as Rectifier

An electronic device which converts a.c. power into d.c. power is called a rectifier.

2.6.1 Principle

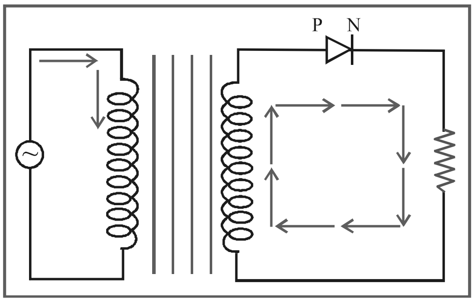
Junction diode offers low resistive path when forward biased and high resistance when reverse biased.

2.6.2 Arrangement

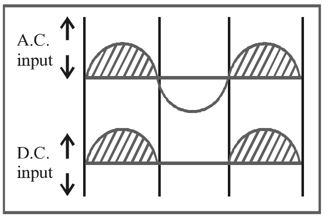
The a.c. supply is fed across the primary coil (P) of step down transformer. The secondary coil 'S' of transformer is connected to the junction diode and load resistance R_L. The output d.c. voltage is obtained across R_L.

2.6.3 Theory

Suppose that during first half of a.c. input cycle the junction diode get forward biased. The conventional current will flow in the direction of arrow heats.



The upper end of R_L will be at +ve potential w.r.t. the lower end. The magnitude of output across R_L during first half at any instant will be proportional to magnitude of current through R_L, which in turn is proportional to magnitude of forward bias and which ultimately depends upon the value of a.c. input at that time.



Thus output across R_L will vary in accordance with a.c. input. During second half, junction diode get reverse biased and hence no–output will be obtained. Thus a discontinuous supply is obtained.

2.7 Full Wave Rectifier

A rectifier which rectifies both halves of a.c. input is called full wave rectifier.

2.7.1 Principle

Junction Diode offers low resistive path when forward biased and high resistive path when reverse biased.

2.7.2 Arrangement

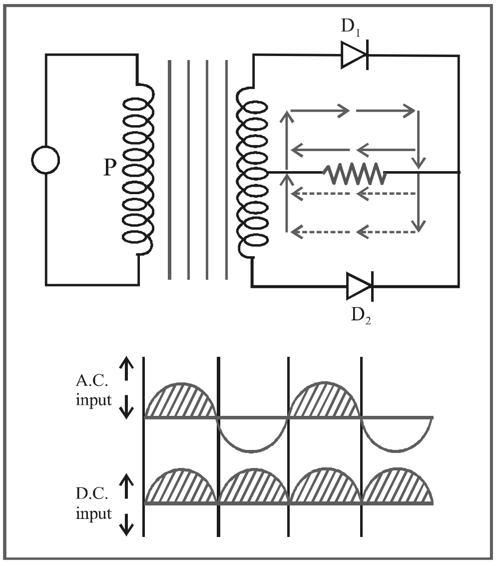
The a.c. supply is fed across the primary coil (P) of step down transformer. The two ends of S–coil (secondary) of transformer are connected to P-section of junction diodes D_1 and D_2. A load resistance R_L is connected across the n–sections of two diodes and central tapping of secondary coil. The d.c. output is obtained across secondary.

2.7.3 Theory

Suppose that during first half of input cycle upper end of s-coil is at +ve potential. The junction diode D_1 gets forward biased, while D_2 gets reverse biased. The conventional current due to D_1 will flow along path of full arrows.

When second half of input cycle comes, the conditions will be exactly reversed. Now the junction diode D_2 will conduct and the convensional current will flow along path of dotted arrows. Since current during both the half cycles flows from right to left through load resistance R_L, the output during both the half cycles will be of same nature.

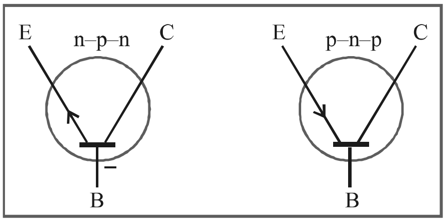
The right end of R_L is at +ve potential w.r.t. left end. Thus in full wave rectifier, the output is continuous.



2.8 Transistor

It is three section semiconductor, in which three sections are combined so that the two at extreme ends have the same type of majority carriers, while the section that separates them has the majority carriers in opposite nature. The three sections of transistor are called emitter (E), Base (B), collector (C).

Symbol :



2.8.1 Action of n-p-n Transistor

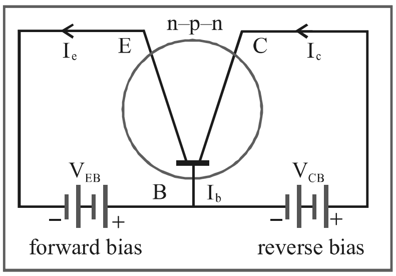


Fig. shows that, the n-type emitter is forward biased by connecting it to -ve pole of V_{EB} (emmitter-base battery) and n-type collector is reverse biased by connected it to +ve pole of V_{CB} (collector-base battery).

The majority carriers (e^-) in emitter are repelled towards base due to forward biase. The base contains holes as majority carriers but their number density is small as it is doper very lightly (5%) as compared to emitter and collector. Due to the probability of e^- and hole combination in base is small. Most of e^- (95%) cross into collector region where they are swept away by +ve terminal of battery V_{CB}.

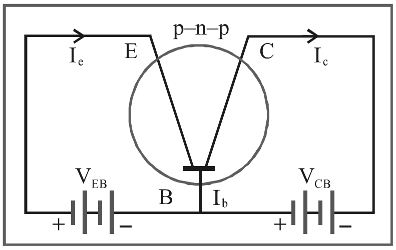
Corresponding to each electron that is swept by collector, an electron enters the emitter from -ve pole of collector – base battery.

If I_e, I_b, I_c be emitter, base and collector current respectively then using Kirchoff first law

$$\boxed{I_e = I_b + I_c}$$

2.8.2 Action p–n–p Transistor

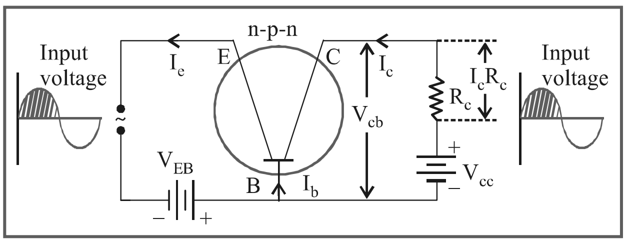
The p–type emitter is forward biased by connecting it to +ve pole of emitter – base battery and p–type collector is reverse biased by connected it to –ve pole of collection - base battery. In this case, majority carriers in emitter i.e. holes are repelled towards base due to forward biase. As base is lightly doped, it has low number density of e^-. When hole enters base region, then only 5% of e^- and hole combination take place. Most of the holes reach the collector and are swept away by –ve pole of V_{CB} battery.



2.9 Common base Amplifier

In this base of the transistor is common to both emitter and collector.

(a) **Amplifier ckt. using n-p-n transistor** : The emitter is forward biased using emitter bias battery (Vcc) & due to this, the resistance of input circuit bias battery (Vcc), due to this, resistance of output circuit is large.



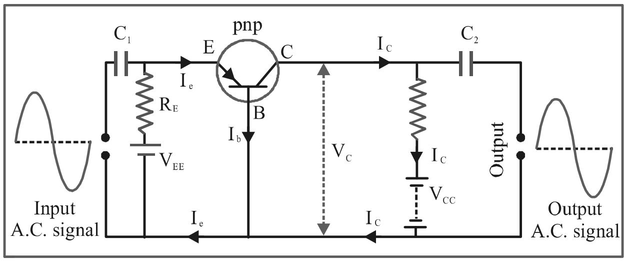
Low input voltage is applied across emitter – base ckt. and amplified circuit is obtained across collector - base circuit. If I_e, I_b, I_c be the emitter, base and collector current than

$$\boxed{I_e = I_b + I_c} \quad \ldots(i)$$

When current I_C flows in collector circuit, a potential drop I_cR_c occurs across the resistance connected in collector - base circuit and base collector voltage will be

$$\boxed{V_{cb} = V_{cc} - I_cR_c} \quad \ldots(ii)$$

(b) Amplifier circuit using p–n–p Transistor



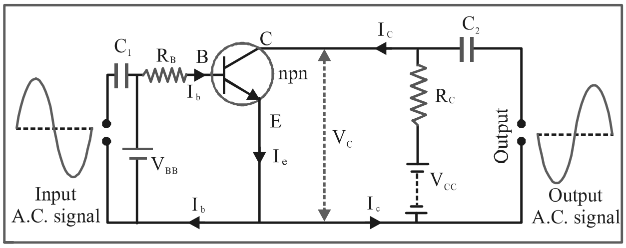
1. When the positive half cycle of input a.c. signal voltage comes, it supports the forward biasing of the emitter–base circuit. Due to this, the emitter current increases and consequently the collector current increases.
2. As I_c increases, the collector voltage V_c decreases.
3. Since the collector is connected to the negative terminal of V_{CC} battery of voltage V_{CB}, therefore, the decrease in collector voltage means the collector will become less negative. This indicates that during positive half cycle of input a.c. signal voltage, the output signal voltage at the collector also varies through the positive half cycle.
4. During negative half cycle of input a.c. signal voltage, the output signal voltage at the collector also varies through the negative half cycle. Thus in common base transitor amplifier circuit the input signal voltage and the output collector voltage are in the same phase.

2.10 Common Emitter Amplifier

Amplifier circuit using n–p-n transitor

1. The input (emitter base) circuit is forward biased with battery V_{BB} of voltage V_{EB}, and the output (collector-emitter) circuit is reversed biased with battery V_{CC} of voltage V_{CE}. Due to this, the resistance of input circuit is low and that of output circuit is high. R_c is a load resistance connected in collector circuit.
2. When no a.c. signal voltage is applied to the input circuit but emitter base circuit is closed let us consider, that I_e, I_b and I_c be the emitter current, base current and collector current respectively. Then according to Kirchhoff's first law

$I_e = I_b + I_c$



3. When the positive half cycle of input a.c. signal voltage comes, it supports the forward biasing of the emitter-base circuit. Due to this, the emitter current increases and consequently the collector current increases. As a result of which, the collector voltage V_c decreases.
4. Since the collector is connected to the positive terminal of V_{CE} battery, therefore decreases in collector voltage means the collector will become less positive, which means negative w.r. to initial value. This indicates that during positive half cycle of input a.c. signal voltage, the output signal voltage at the collector varies through a negative half cycle.
5. When negative half cycle of input a.c. signal voltage comes, it opposes the forward biasing of emitter-base circuit, due to this the emitter current decreases and hence collector current decreases; consequently the collector voltage V_c increases i.e., the collector becomes more positive. This indicate that during the negative half cycle of input a.c. signal voltage, the output signal voltage varies through positive half cycle.

2.11 Common base Amplifier

a.c. current gain : It is defined as the ratio of change in collector current as constant collector voltage. It is denoted by α_{ac}

$$\alpha_{ac} = \left(\frac{\Delta I_c}{\Delta I_e}\right) \qquad [V_{CB} = \text{const.}]$$

Voltage gain : It is defined as the ratio of change in output voltage to the change in input voltage. It is denoted by A.

$$Av = \frac{(\Delta I_c)R_{out}}{(\Delta I_e)R_{in}} = \frac{\Delta I_c}{\Delta I_e} \times \frac{R_{out}}{R_{in}}$$

Or $Av = \alpha_{AC} \times$ resistance gain,

where R_{out}/R_{in} is called resistance gain.

Power gain : It is defined as the ratio of change in output power to the change in input power. Therefore,

$$\text{a.c. power gain} = \frac{\text{change in output power}}{\text{change in input power}} = \frac{(\Delta I_c)R_{out}}{(\Delta I_e)R_{in}}$$

$$= \frac{\Delta I^2 c}{\Delta I^2 e} \times \frac{R_{out}}{R_{in}}$$

Or a.c. power gain = α^2_{ac} × resistance gain.

2.12 Common Emitter Amplifier

a.c. current gain : It is defined as the ratio of the change in collector to the change in base current. It is denoted by β_{ac}.

Therefore, $\beta_{ac} = \left(\frac{\Delta I_c}{\Delta I_b}\right)$ $[V_{ce} = \text{const.}]$

Its value is quite large as compared to 1 and lies between 15 to 50.

Voltage gain : It is the ratio of the change in output voltage to the change in input voltage. It is denoted by A.

$$Av = \frac{(\Delta I_c) \times R_{out}}{(\Delta I_b) \times R_{in}} = \frac{\Delta I_c}{\Delta I_b} \times \frac{R_{out}}{R_{in}}$$

Or Av = β_{ac} × resistance gain.

a.c. power gain : It is the ratio of the change in output power to the change in input power.

$$\text{a.c. power gain} = \frac{\text{change in output power}}{\text{change in input power}} = \frac{(\Delta I_c)^2 R_{out}}{(\Delta I_b)^2 R_{in}}$$

Or a.c. power pain = β^2_{ac} × resistance gain.

2.13 Relation between α and β

For both the types of amplifier, we have

$$i_e = i_b + i_c$$

Dividing both sides of the above equation by I_c, we get

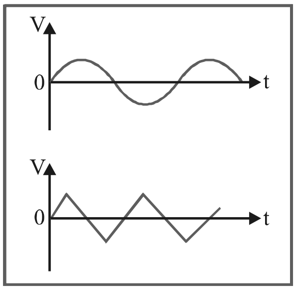
$$\frac{i_e}{i_c} = \frac{i_b}{i_c} + 1$$

∴ $1/\alpha = (1/\beta) + 1$ or $1/\beta = (1/\alpha) - 1 = (1-\alpha)/\alpha$

or $\beta = \alpha/(1-\alpha)$

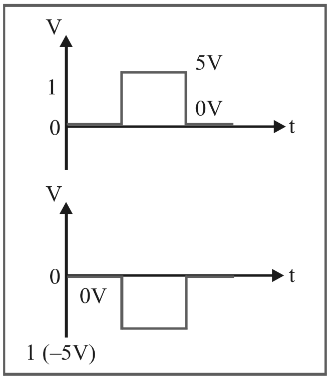
3. ANALOG SIGNALS

Signals which varies continuously with time is called analog signal. A typical analog signal is shown in figure. Circuit used for generating analog signal is called analog electronic circuit.



4. DIGITAL SIGNALS

Signals having either of the two levels, 0 or 1, are called digital signals.



5. LOGIC GATES

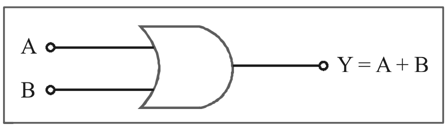
A digital circuit which either stops a signal or allows it to pass through it is called a gate. A logic gate is an electronic circuit which makes logical decisions. Logic gate has one or more inputs but one output. Logic gates are the basic building blocks for most of the digital systems. Variables used at the input and output are 1's and 0's. These are three basic logic gates:

(i) OR gate (ii) AND gate

(iii) NOT gate.

5.1 OR Gate

OR gate is an electronic device that combines A and B to give Y as output. In this figure two inputs are A and B and output is Y. In Boolean algebra OR is represented by +.



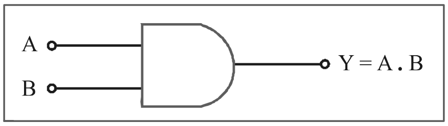
Truth Table: A truth table may be defined as the table which gives the output state for all possible input combinations.

Logic operations of OR gate are given in its truth table for all possible input combinations.

Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

5.2 AND Gate

In an AND gate there are two or more inputs and one output. In Boolean algebra AND is represented by a dot (.).

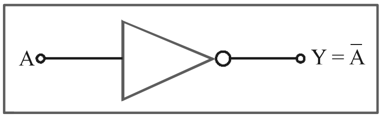


Truth Table

Input		Output
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

5.3 NOT Gate

NOT gate is an electronic circuit which has one input and one output. This circuit is so called because output is NOT the same as input.



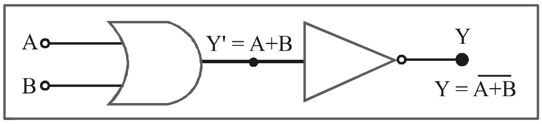
Boolean expression for NOT gate is Y = $\overline{A}$.

Truth Table:

Input	Output
A	**Y**
0	1
1	0

5.4 NOR Gate

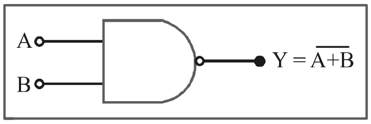
A NOR gate has two or more inputs and one output. Actually NOR gate is a NOT-OR gate. If a NOT gate is connected at the output of an OR gate, we get NOR gate as shown in figure and its truth table in table.



Truth Table :

A	B	Y′	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Boolean expression for NOT gate is and it is read as Y = $\overline{A+B}$ and it is read as Y equals A OR B negated. A NOR function is the reverse of OR function.

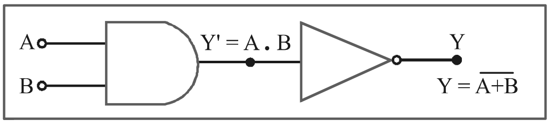


Truth Table :

Input		Output
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

5.5 NAND Gate

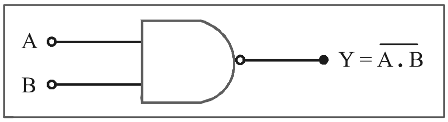
A NAND gate has two or more inputs and one output. Actually a NAND gate is a NOT–AND gate. If a NOT gate is connected at the output of a AND gate, we get NAND gate as shown in figure and its truth table is given in table.



A	B	Y′	Y
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Boolean expression for NAND gate, is $Y = \overline{A.B}$ and is read as Y equals A and B negated.

Logical symbol of NAND gate is shown in figure and its truth table in table.



Truth Table :

Input		Output
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

Like NOR gate, NAND gate can also be used to realize all basic gates : OR, AND and NOT. Hence it is also known as **universal Gate**.