SP6122C: 800 mW Driver Amplifier, 2.3 GHz – 4.2 GHz

General Description

The SP6122C is a wideband driver amplifier capable of 800mW peak power, suitable for application in FDD and TDD wireless infrastructure and general-purpose amplification over a wide frequency range of 2.3 to 4.2 GHz. The RF input and output ports are internally matched to 50 Ω for the full frequency range. This device incorporates a device enable pin with turn on/off times less than 1 us.

The driver amplifier has high gain and excellent stand-alone linearity. It will support the high instantaneous bandwidths required for 5G NR carrier aggregated signals. The device linearizes well in DPD systems, linearized on its own it can provide better than 55 dBc ACLR for a 20 MHz 5G NR signal.

Applications

- 4G/5G infrastructure applications multiple 3GPP bands
- MIMO Systems
- General purpose amplification

Features

- Extremely Wideband – 2.3 GHz to 4.2 GHz
- Average Output Power – 15 dBm
- High Peak Power – 29 dBm
- Excellent Linearity – > 40 dBc ACLR
- Low Bias Current – 120 mA
- High Small Signal Gain – 38 dB
- Supports Carrier Aggregation for 4G/5G
- Shutdown / Enable Pin
- Single Supply +5.0 V, adjustable Icq
- Package: 3x3 mm

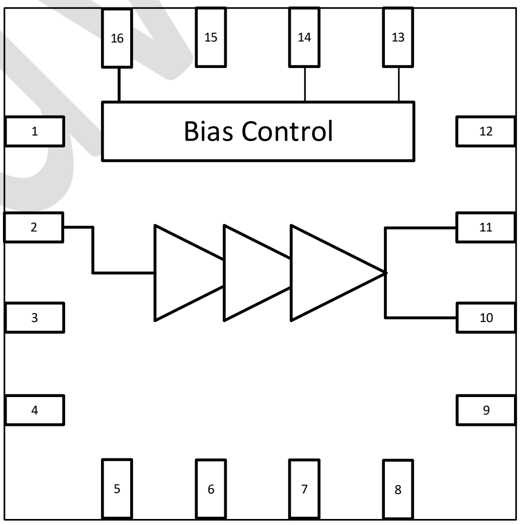

Figure 1 Functional Diagram

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1 Pin Configuration

1.1 Pin Configuration Diagram

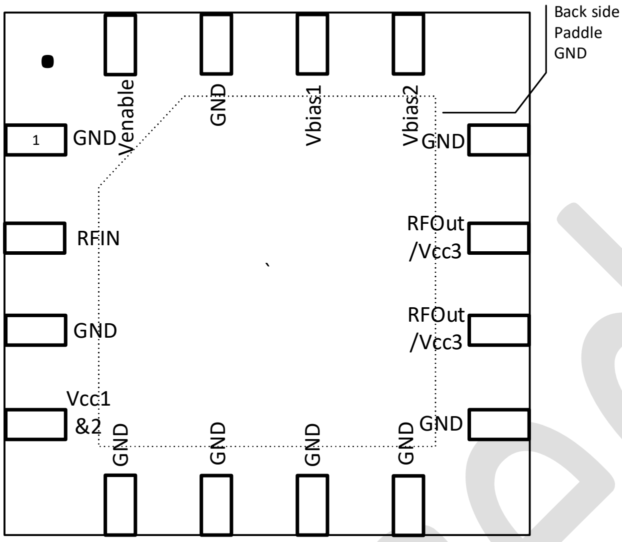


Figure 2 SP6122 Pin Diagram (top view)

1.2 Pin Description

Table 1 Pin Description

Pin No	Pin Name	Description
1	GND	Internally connected to Ground
2	RFIN	RF Input – Matched to 50 Ω
3	GND	Internally connected to Ground
4	Vcc1 & 2	Collector connection to stages 1 & 2
5	GND	Internally connected to Ground
6	GND	Internally connected to Ground
7	GND	Internally connected to Ground
8	GND	Internally connected to Ground
9	GND	Internally connected to Ground
10	RF Out/Vcc3	RF Output – Matched to 50 Ω, Collector connection to stage 3
11	RF Out/Vcc3	Internally connected to Pin 10
12	GND	Internally connected to Ground
13	Vbias1	Supply for bias circuit
14	Vbias2	Control input to adjust quiescent bias current – see
15	GND	Internally connected to Ground
16	Venable	Toggles between ON state and low power state Hi=Device On, Low=Device Off
GND	Backside Paddle	This is the ground connection and should be soldered directly to ground ensuring a low inductance and ow thermal resistance connection

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	Vcc1, Vcc2, Vcc3, Vbias			5.5	V
Control Pin Input Voltage	Vctrl			2.8	V
Peak RF Input Power (RFIN)	Pin			10	dBm
Maximum Case Temperature	Tcase max			125	°C
Storage Temperature		-55		125	°C
ESD voltage CDM, all pins	CDM			1000	V
ESD voltage HBM, all pins	HBM			500	V

Table 2 notes:

1. Exceeding absolute maximum ratings may cause permanent damage. Operation should only occur within the limits specified. Operating between the maximum operating range, Table 3, and the absolute maximum for extended periods may reduce the reliability of the device.

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage (VCC1,2,3, Vbias1,2)	Vcc1, Vcc2, Vcc3, Vbias	4.75	5	5.25	V
Quiescent Current (ICCQ), see notes	Iccq		130		mA
Control Input High	Venable	1.5	1.8		V
Control Input Low	Venable	0		0.7	V
Control Input Currents	Ictrl		1	12	µA
RF Output Power, average 5G NR 20 MHz 8.5 dB PAPR	Pout			15	dBm
Operating Temperature Range (Tcase)	Tcase	-40	25	105	°C

Table 3 notes:

1. Operation at the maximum recommend case temperature gives an MTTF > 10^6 hours. Heatsinking requirement is to maintain case at <105 °C at 0.7 W

Table 4 Device Truth Table

Control Input (PA Enable) State	Device State
High	Amplifier On
Low	Amplifier Off

Table 5 Electrical Characteristics

This table provides key electrical specifications at Tcase=25 °C, VCC = VBIAS = 5 V, Zin = Zout = 50 Ω, Venable = 1.8 V unless otherwise specified.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Frequency		f	2300		4200	MHz
Small Signal Gain	P_{IN} = -35 dBm, 2300 MHz	S21		38.1		dB
	P_{IN} = -35 dBm, 2600 MHz			38.4		
	P_{IN} = -35 dBm, 3600 MHz			38.9		
	P_{IN} = -35 dBm, 4200 MHz			39.5		
Input Return Loss	P_{IN} = -35 dBm, 2300 MHz	S11		-23.0		dB
	P_{IN} = -35 dBm, 2600 MHz			-12.0		dB
	P_{IN} = -35 dBm, 3600 MHz			-19.0		dB
	P_{IN} = -35 dBm, 4200 MHz			-11.0		dB
Output Return Loss	P_{IN} = -35 dBm, 2300 MHz	S22		-11.0		dB
	P_{IN} = -35 dBm, 2600 MHz			-14.0		dB
	P_{IN} = -35 dBm, 3600 MHz			-11.0		dB
	P_{IN} = -35 dBm, 4200 MHz			-12.0		dB
Reverse Isolation	P_{IN} = -35 dBm	S12		-50		dB
Forward Isolation	Device Off; PIN = -35 dBm	S21		-50		dB
Gain Flatness	In any 100 MHz bandwidth, Pin = -35 dBm	Gflat		0.3		dB
ACLR (without DPD)	5G NR 20 MHz, 8.5 dB PAR, +15.0 dBm av. Power, F = 2310 MHz	ACLR		-53.0		dBc
	5G NR 20 MHz, 8.5 dB PAR, +15.0 dBm av. Power, F = 2600 MHz	ACLR		-52.0		dBc
	5G NR 20 MHz, 8.5 dB PAR, +15.0 dBm av. Power, F = 3600 MHz	ACLR		-42.0		dBc
	5G NR 20 MHz, 8.5 dB PAR, +15.0 dBm av. Power, F = 4190 MHz	ACLR		-40.0		dBc
Output Power at 1dB compression. Pulsed using 10us/100us (on/off duty cycle)	At 2.3 GHz	P1dB		26.7		dBm
	At 2.6 GHz			27.8		
	At 3.6 GHz			24.2		
	At 4.2 GHz			26.7		
Output Power at 3dB compression. Pulsed using 10us/100us (on/off duty cycle)	At 2.3 GHz	P3dB		27.5		dBm
	At 2.6 GHz			28.7		
	At 3.6 GHz			27.8		
	At 4.2 GHz			27.5		
Noise Figure	At 3.6 GHz	NF		5.5		dB
Off current	Venable = 0 V	ICCQ_OFF		0.3		mA
Icc Quiescent	Venable = 1.8V	ICCQ_ON		125		mA
Turn-on time	50% Venable to 90% RF Power	Ton		180		ns

3 Typical Performance Characteristics

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA, Venable = 1.8 V unless otherwise specified.

Table 6 Typical Performance

Parameter	Conditions	Typical			Units
Frequency		2600	3600	4200	MHz
Small Signal Gain	P_{IN} = -35 dBm	38	38.5	39.5	dB
Input Return Loss	P_{IN} = -35 dBm	13.0	18.0	12.0	dB
Output Return Loss	P_{IN} = -35 dBm	14.0	12.0	10.0	dB
ACLR (without DPD)	5G NR 20 MHz, 15.0 dBm +8.5 dB PAR,	-54.4	-42.8	-40.1	dBc
Output Power at 1dB compression.	Pulsed using 10us/100us (on/off duty cycle)	27.8	24.2	26.7	dBm
Output Power at 3dB compression.	Pulsed using 10us/100us (on/off duty cycle)	28.5	27.5	27.8	dBm
Quiescent current	Venable = 1.8 V		125		mA

Table 7 Typical Performance 2600 MHz

Parameter	Conditions	Typical			Units
Quiescent current		90	125	150	
Small Signal Gain	P_{IN} = -35 dBm	36.8	38	38.2	dB
Input Return Loss	P_{IN} = -35 dBm	14.8	13.0	12.4	dB
Output Return Loss	P_{IN} = -35 dBm	13.9	14.0	16.1	dB
ACLR (without DPD)	5G NR 20 MHz, 15.0 dBm +8.5 dB PAR,	-48.6	-54.4	-56.4	dBc
Output Power at 1dB compression.	Pulsed using 10us/100us (on/off duty cycle)		27.8		dBm
Output Power at 3dB compression	Pulsed using 10us/100us (on/off duty cycle)		28.7		dBm

Table 8 Typical Performance 3600 MHz

Parameter	Conditions	Typical			Units
Quiescent current		90	125	150	
Small Signal Gain	P_{IN} = -35 dBm	37.3	38.5	39.2	dB
Input Return Loss	P_{IN} = -35 dBm	17.5	18.0	14.8	dB
Output Return Loss	P_{IN} = -35 dBm	14.8	12.0	13.7	dB
ACLR (without DPD)	5G NR 20 MHz, 15.0 dBm +8.5 dB PAR,	-37.0	-42.8	-46.2	dBc
Output Power at 1dB compression.	Pulsed using 10us/100us (on/off duty cycle)		24.2		dBm
Output Power at 3dB compression	Pulsed using 10us/100us (on/off duty cycle)		27.8		dBm

3.1 Typical Performance Plots

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA Venable = 1.8 V unless otherwise specified.

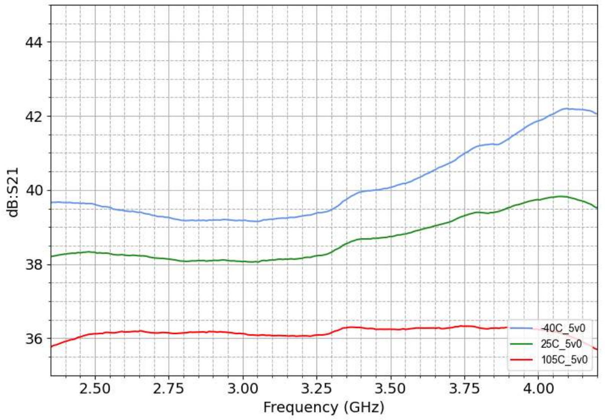


Figure 3 Small Signal Gain over Temperature

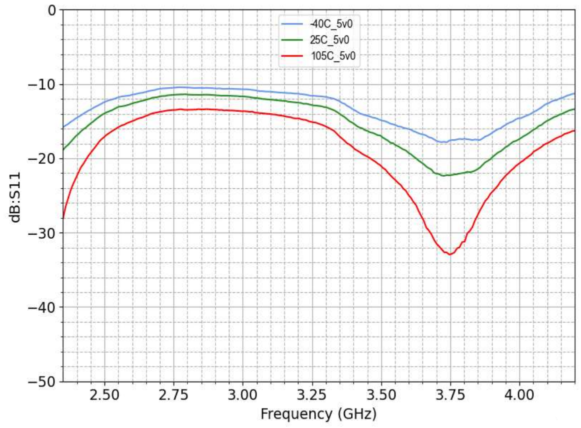


Figure 4 Input Return Loss over Temperature

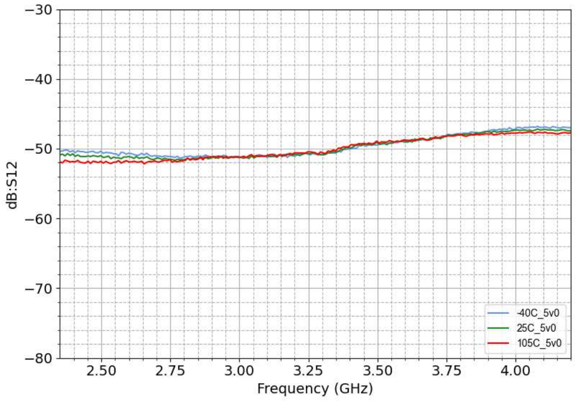


Figure 5 Reverse Isolation over Temperature

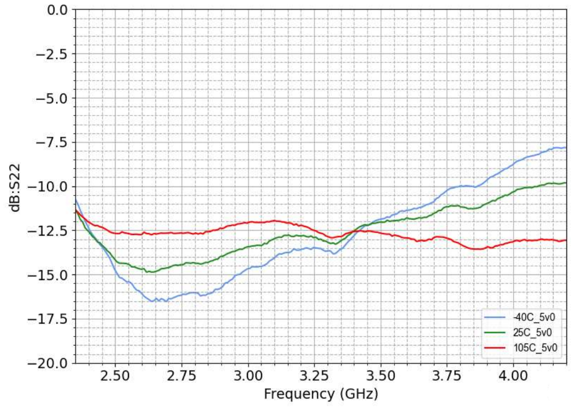


Figure 6 Output Return Loss over Temperature

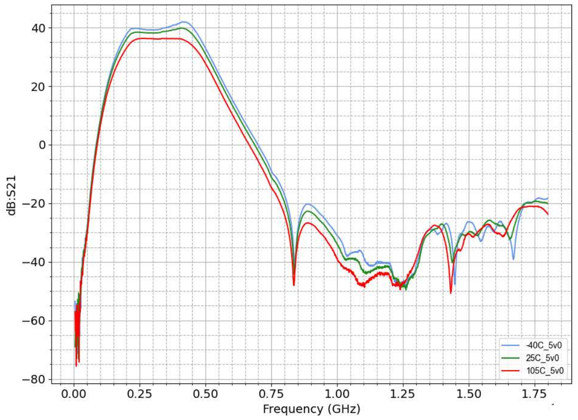


Figure 7 Wideband Small Signal Gain over Temperature

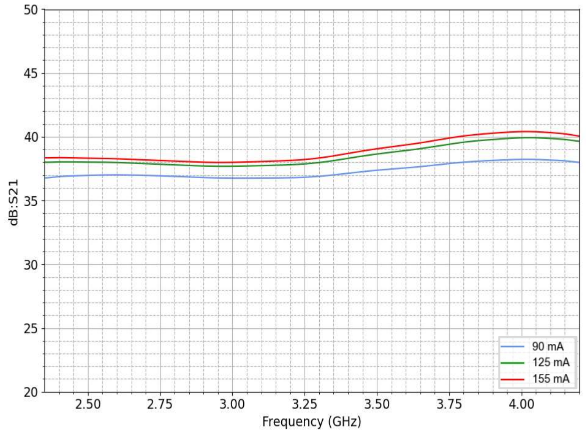


Figure 8 Small Signal Gain over Icc

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA, Venable = 1.8 V unless otherwise specified.

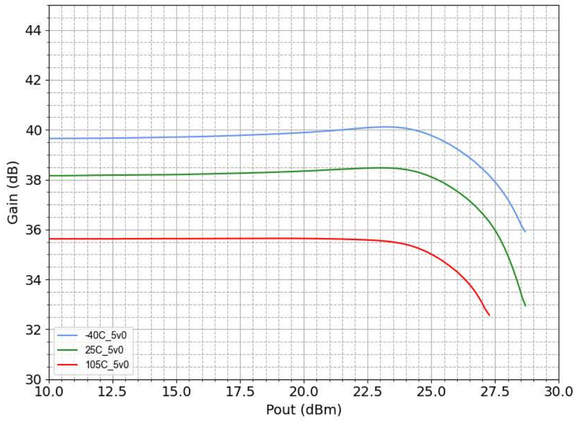


Figure 9 Large Signal Gain vs Output Power over Temperature at 2.3 GHz

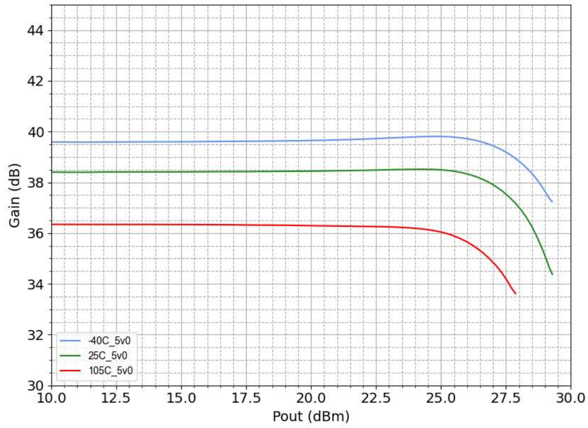


Figure 10 Large Signal Gain vs Output Power over Temperature at 2.6 GHz

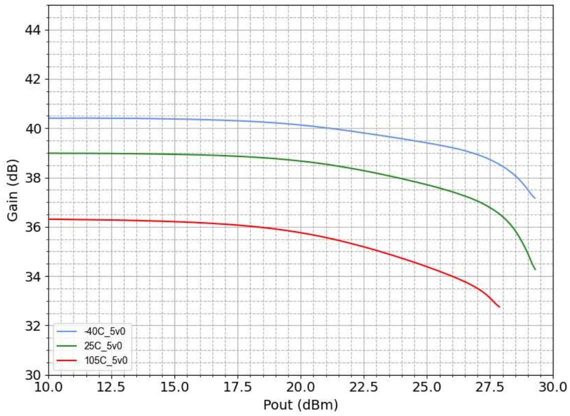


Figure 11 Large Signal Gain vs Output Power over Temperature at 3.6 GHz

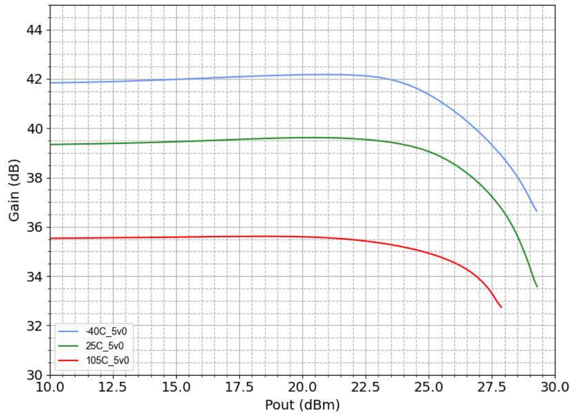


Figure 12 Large Signal Gain vs Output Power over Temperature at 4.2 GHz

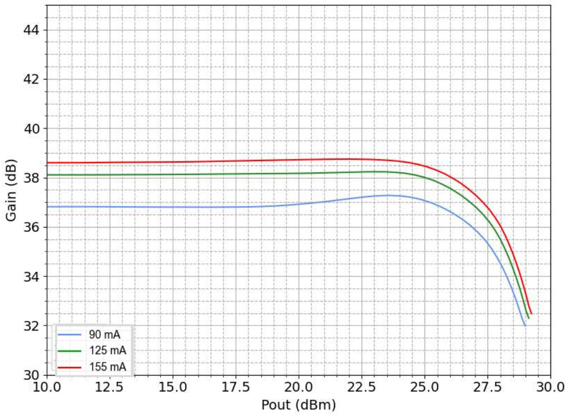


Figure 13 Large Signal Gain vs Output Power over Icc at 2.3 GHz

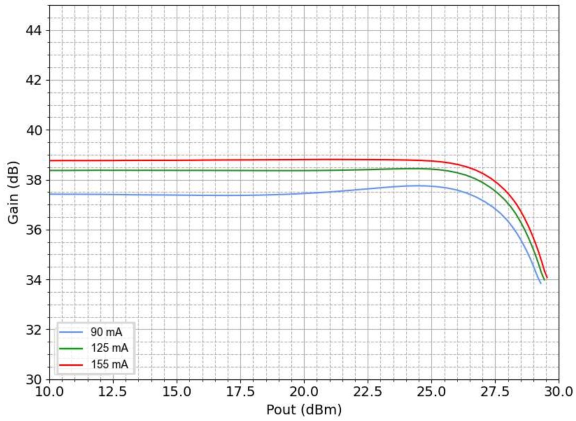


Figure 14 Large Signal Gain vs Output Power over Icc at 2.6 GHz

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA, Venable = 1.8 V unless otherwise specified.

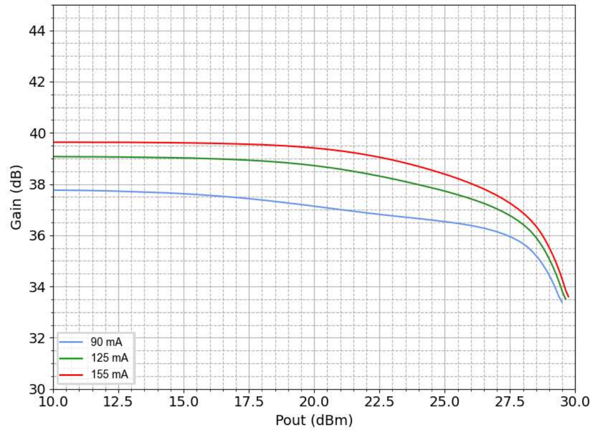


Figure 15 Large Signal Gain vs Output Power over Icc at 3.6 GHz

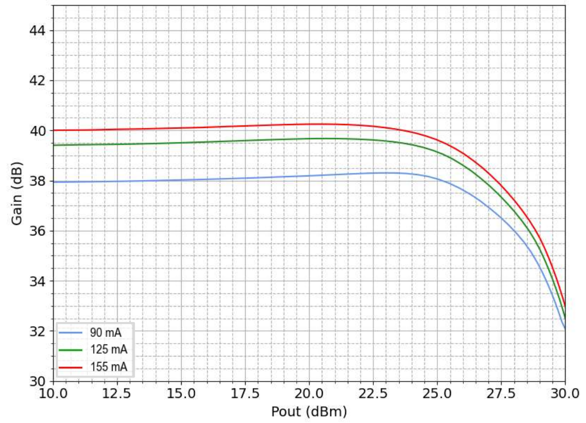


Figure 16 Large Signal Gain vs Output Power over Icc at 4.2 GHz

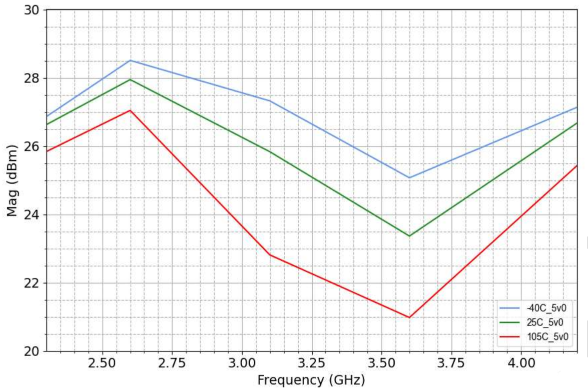


Figure 17 P1dB vs Frequency over Temperature

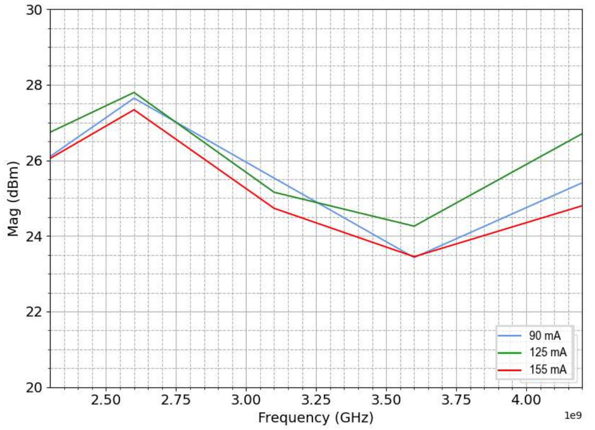


Figure 18 P1dB vs Frequency over Icc

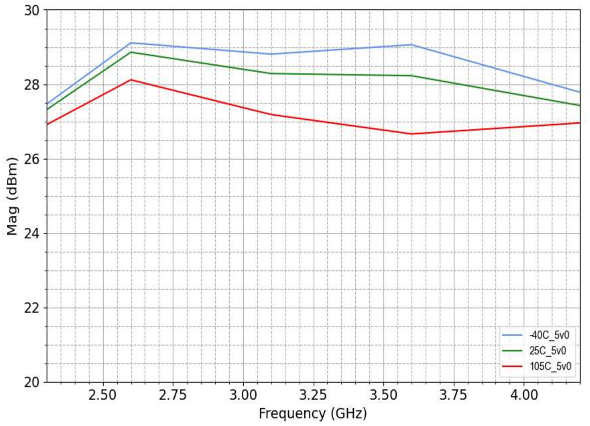


Figure 19 P3dB vs Frequency over Temperature

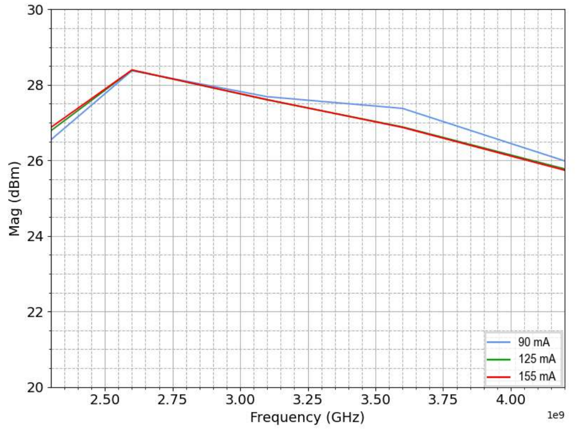


Figure 20 P3dB vs Frequency over Icc

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA, Venable = 1.8 V unless otherwise specified.

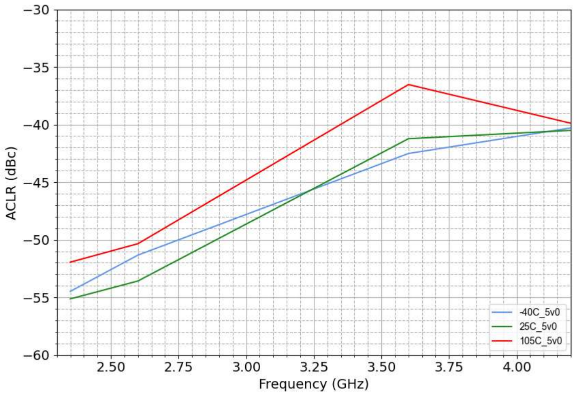


Figure 21 ACLR vs Frequency at 15 dBm Output Power 15 dBm (20 MHz LTE. PAR 8.5 dB)

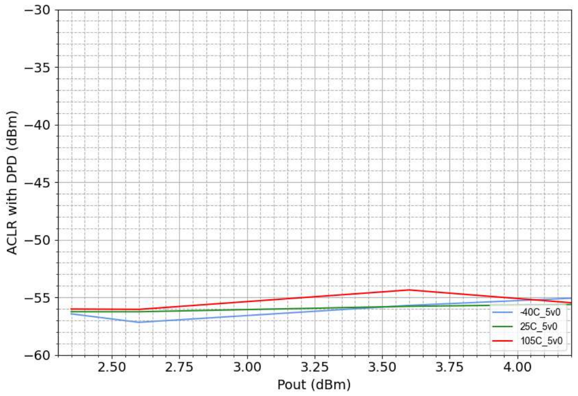


Figure 22 ACLR with DPD vs Frequency at 15 dBm Output Power (20 MHz LTE. PAR 8.5 dB)

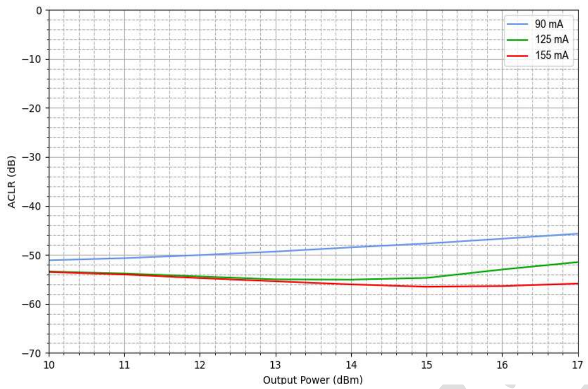


Figure 23 ACLR vs Bias Current at 2.6 GHz (20 MHz LTE PAR 8.5 dB)

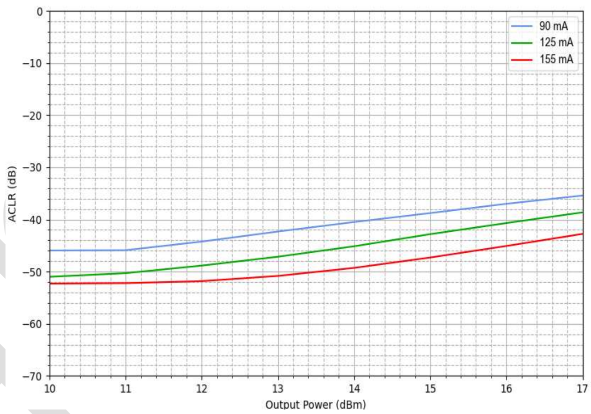


Figure 24 ACLR vs Bias Current at 3.6 GHz (20 MHz LTE PAR 8.5 dB)

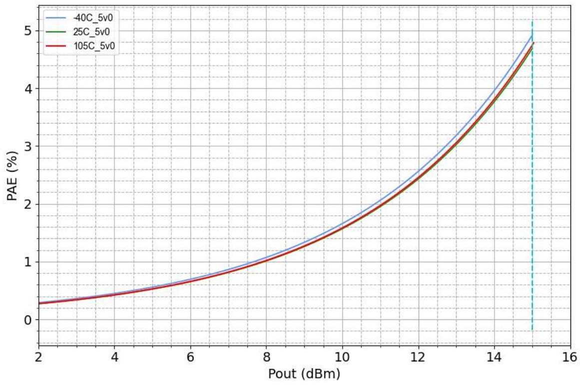


Figure 25 Efficiency vs Average Output Power over Temperature at 2.3 GHz

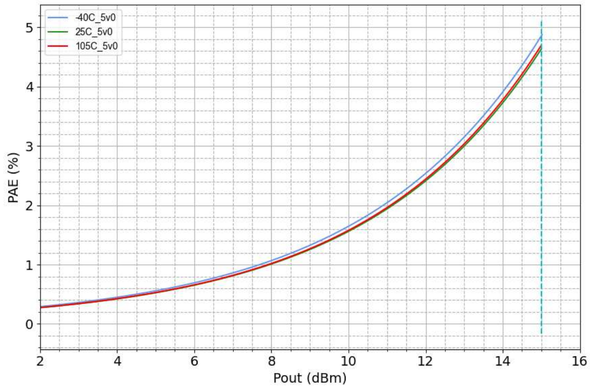


Figure 26 Efficiency vs Average Output Power over Temperature at 2.6 GHz

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA, Venable = 1.8 V unless otherwise specified.

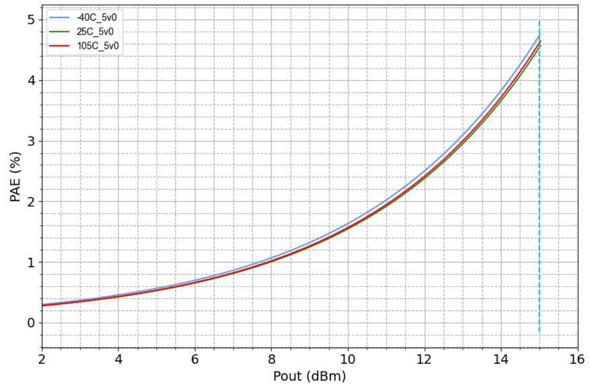


Figure 27 Efficiency vs Average Output Power over Temperature at 3.6 GHz

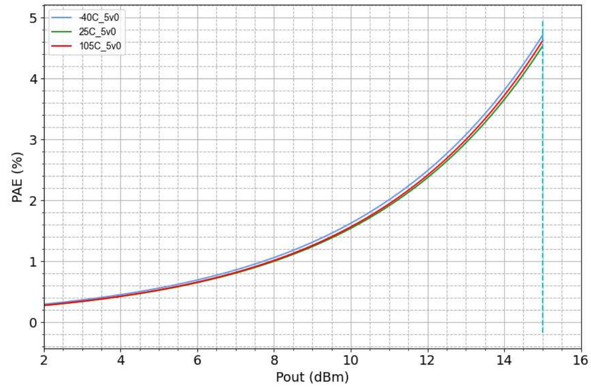


Figure 28 Efficiency vs Average Output Power over Temperature at 4.2 GHz

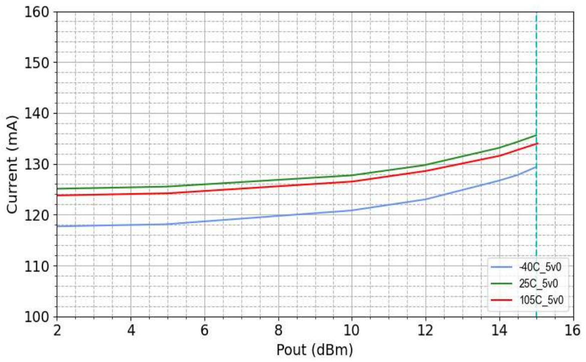


Figure 29 Current vs Average Output Power over Temperature at 2.3 GHz

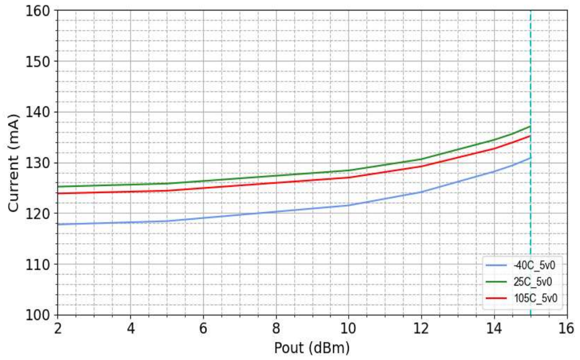


Figure 30 Current vs Average Output Power over Temperature at 2.6 GHz

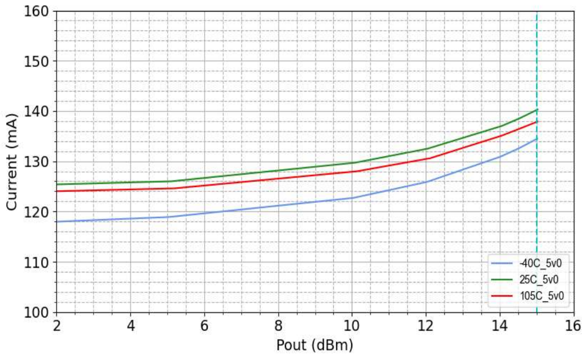


Figure 31 Current vs Average Output Power over Temperature at 3.6 GHz

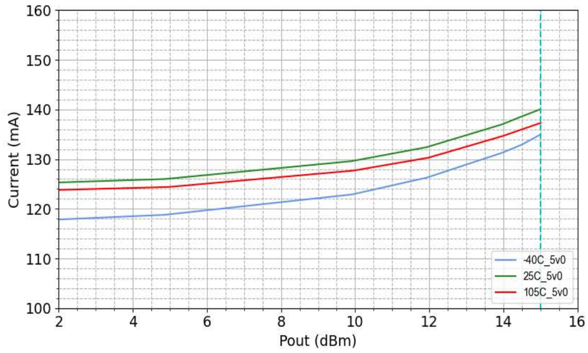


Figure 32 Current vs Average Output Power over Temperature at 4.2 GHz

Operating conditions unless otherwise stated: Tcase = 25 °C, Vcc = Vbias = 5 V, Zin = Zout = 50 Ω, Icq = 125 mA, Venable = 1.8 V unless otherwise specified.

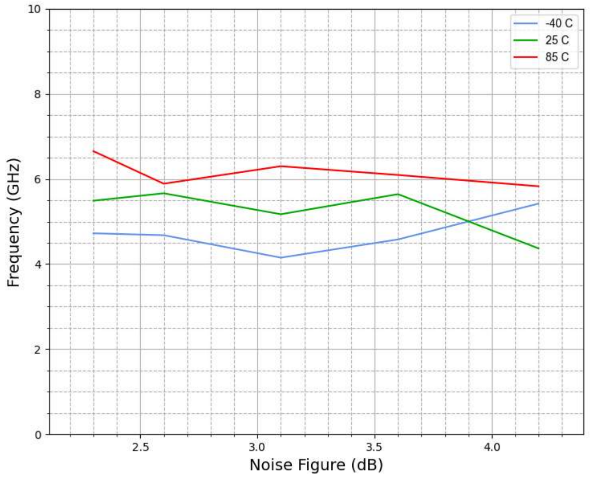


Figure 33 Noise Figure vs Frequency across Temperature

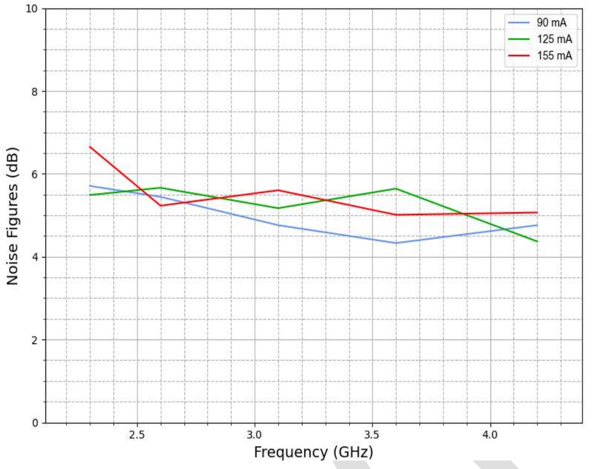


Figure 34 Noise Figure vs Frequency across Icc

4 Evaluation Board

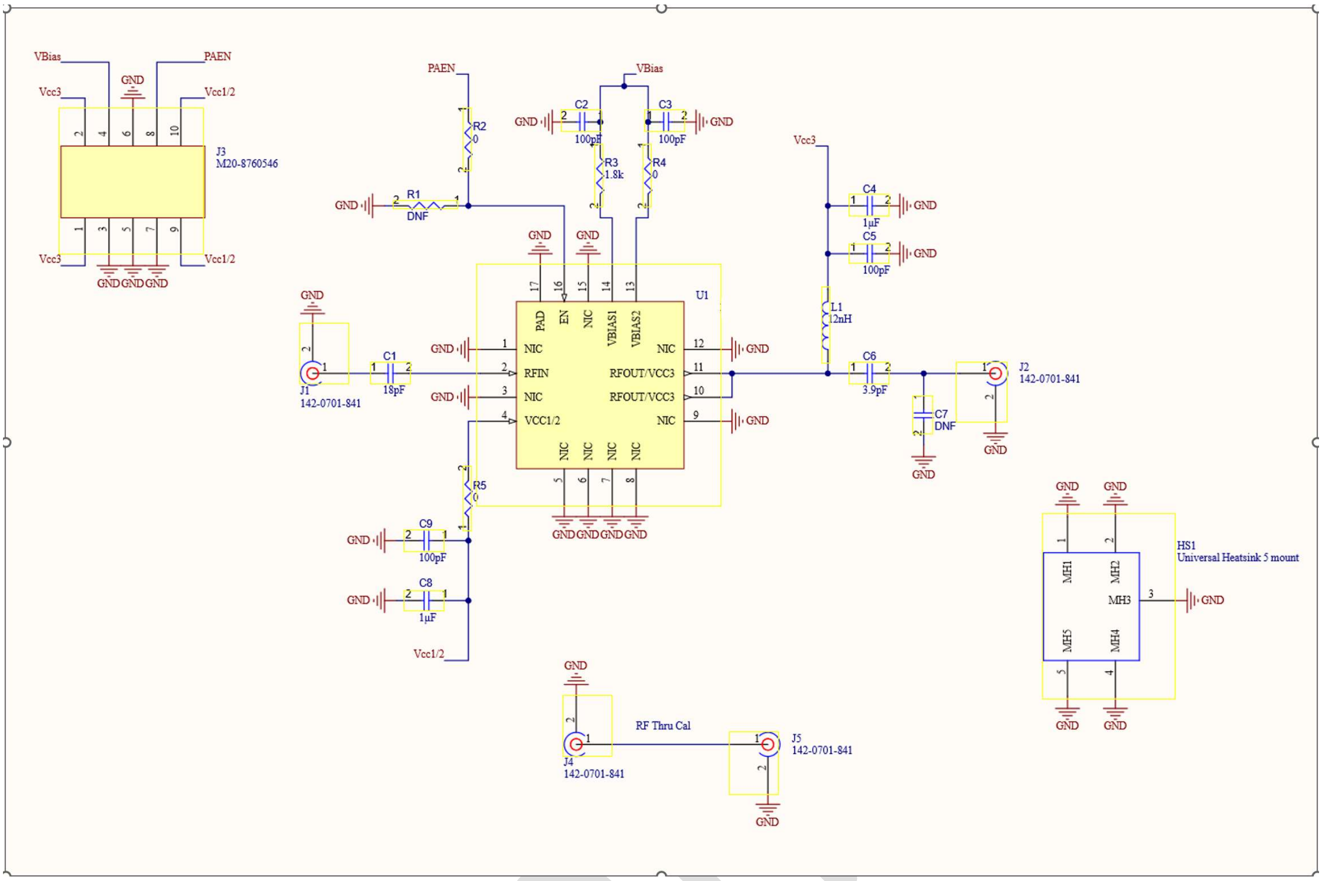


Figure 35 Evaluation Board Schematic Diagram

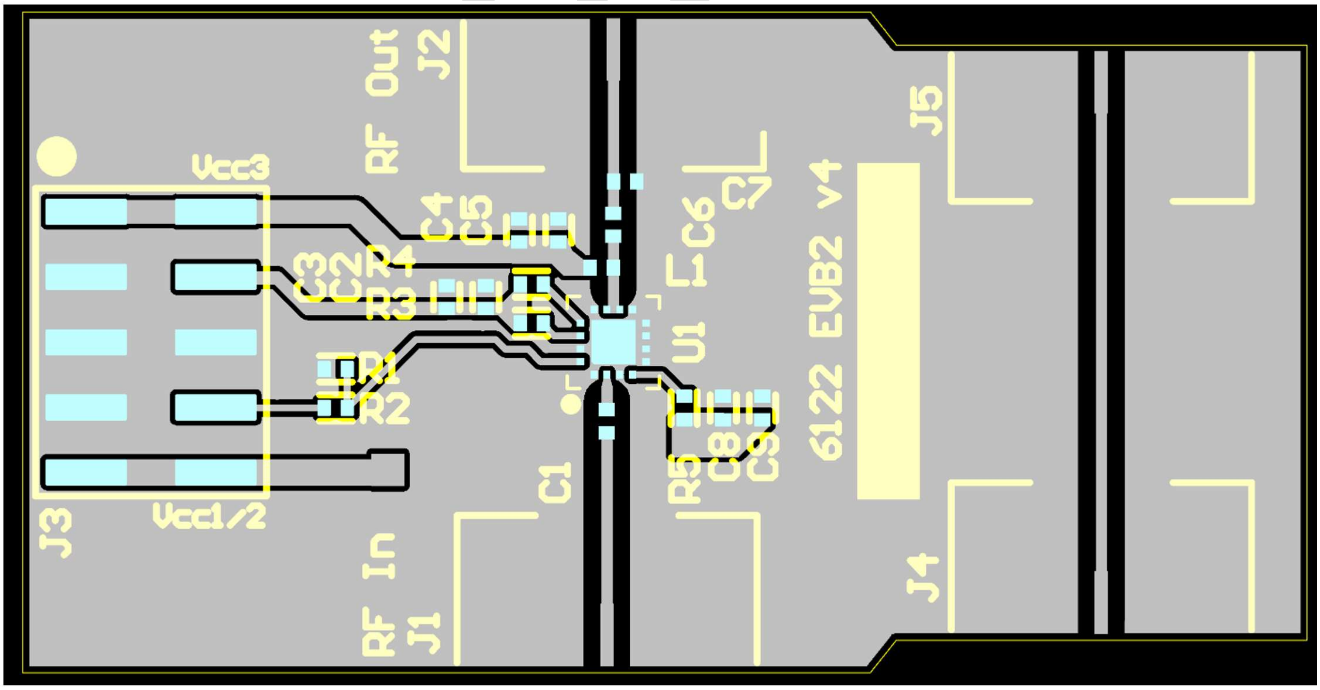


Figure 36 Evaluation Board Layout

Table 9 Evaluation Board Bill of Materials

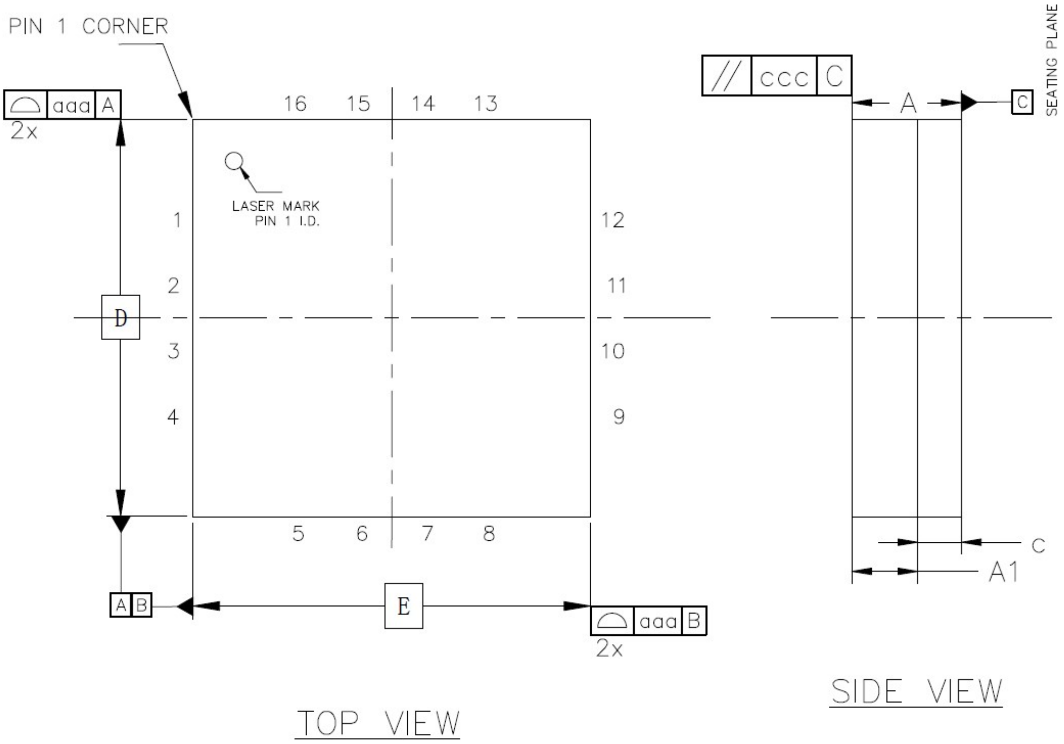
Component Reference	Value	Tolerance	Voltage	Manufacturer	Part Number
C1	18pF	+/-5%	50V	Murata	GJM1555C1H180JB01D
C6	3.9pF	+/-0.1pF	50V	Murata	GJM1555C1H3R9BB01D
C2, C3, C5, C9	100pF	+/-5%	50V	Murata	GCM1555C1H101JA16D
C4, C8	1uF	+/-10%	10V	Murata	GRM155Z71A105KE01D
C7	DNF				Not Fitted
R1	DNF				Not Fitted
R2, R4, R5	0Ω	+/-5%	50V	Panasonic	ERJ-2GE0R00X
R3	1.8kΩ	+/-5%	50V	Panasonic	ERJ-2GEJ182X
L1	12nH	+/-2%		Coilcraft	0402DC-12NXGRW
J1, J2, J4, J5				Johnson/Cinch	142-0701-841
J3				Harwin	M20-8760546
U1	SP6122			Spirit Semiconductor	SP6122C

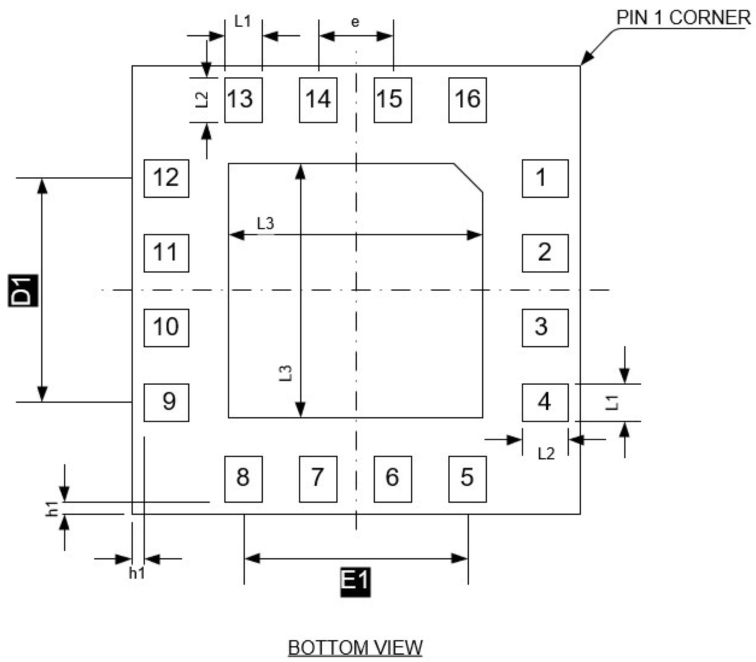
Table 10 Typical Iccq vs R3 Value

R3 (Ω)	0	620	1k8	3k3	DNP
Icc (mA)	210	155	125	117	90

5 Package Information

Package Dimensions shown below.





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.767	0.827	0.887
A1	0.50BASIC		
c	0.297	0.327	0.357
E	2.900	3.000	3.100
D	2.900	3.000	3.100
E1	1.50 BASIC		
D1	1.50 BASIC		
e	0.50 BASIC		
L1	0.200	0.250	0.300
L2	0.250	0.300	0.350
L3	1.650	1.700	1.750
h1	0.08 REF		
aaa	0.150		
ccc	0.080		

Figure 37 Package Drawing and Pin Details

6 Recommended PCB Footprint

The paste stencil has the same pad sizes the component package detailed above.

Solder Mask Pads are 50um larger per edge. as For example 300um x 250um pads are increased to 400um x 350um. Ground Paddle is defined as L3 (1.7mm)

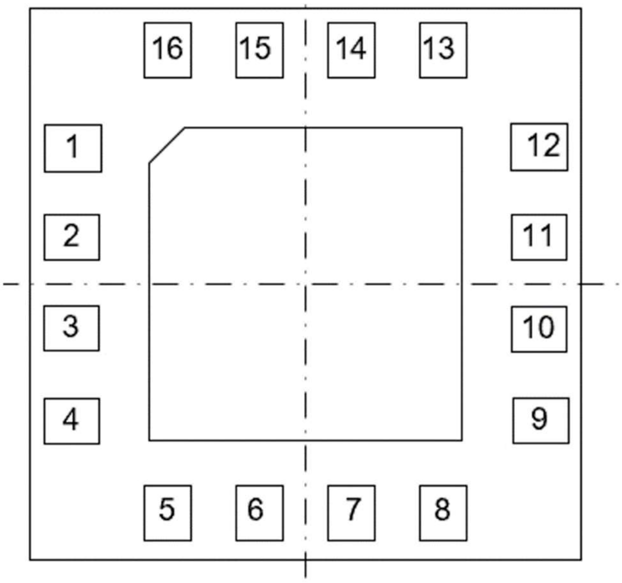


Figure 38 Stencil Aperture Top View

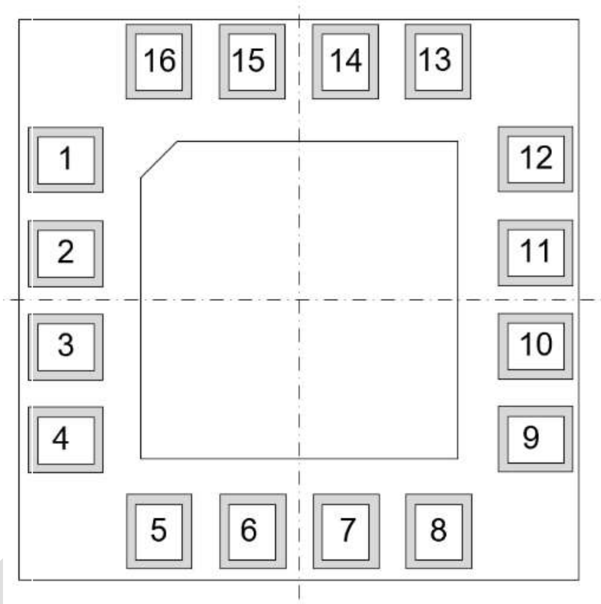
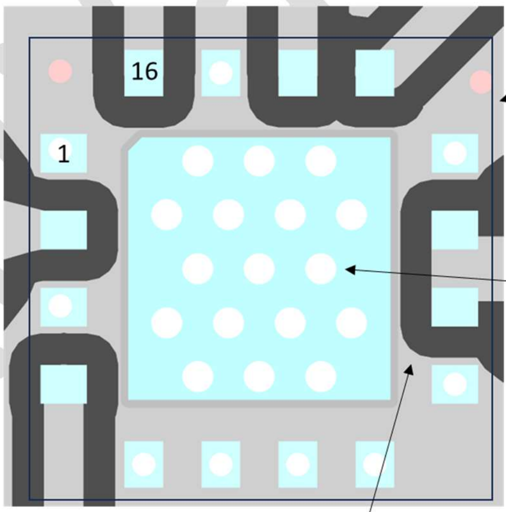


Figure 40 Solder Mask Top View

Maximum grounding under the device is required

Component footprint uses same size pads as package outline



PACKAGE OUTLINE

Thermal via array Ø 0.2mm on 0.4mm pitch improves thermal performance

0.2mm Typical Clearance around pads

Figure 39 Metalization Top View

7 Tape and Reel Information

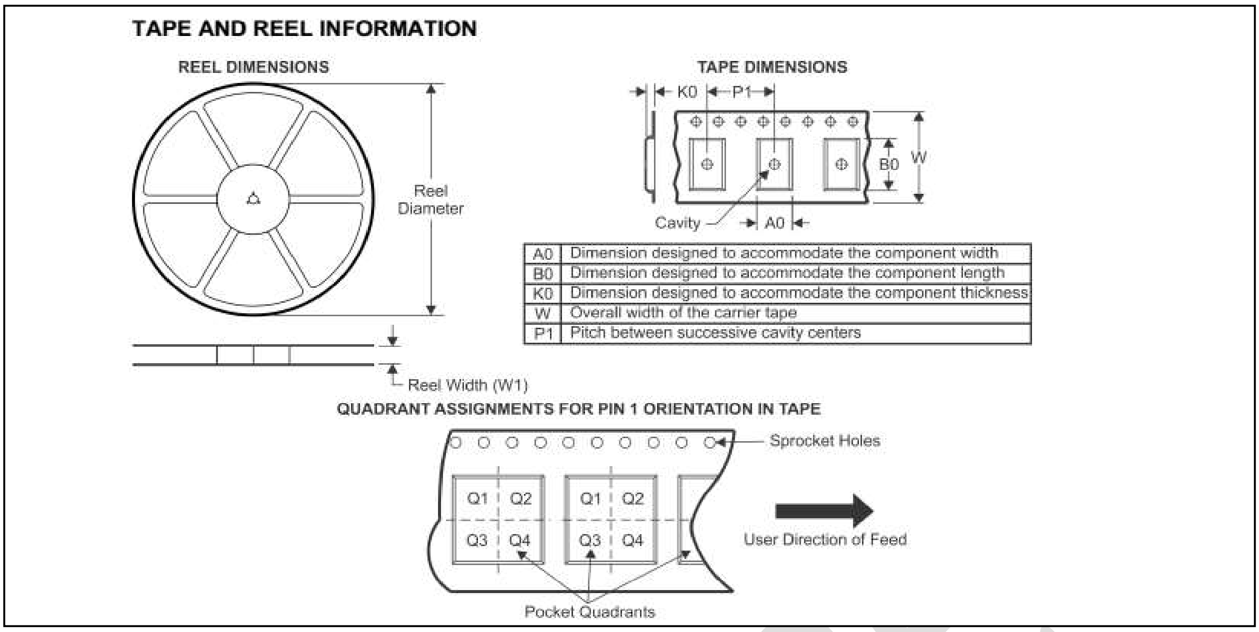


Figure 41 Carrier and Cover Tape Dimensions

Table 11 Carrier and Cover Tape Dimensions

Package type	Pins	Pin1 Quadrant	SPQ	Reel Diameter	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LGA3x3	16	Q1	TBD	178	12.4	3.3	3.3	1.1	4	12

8 Ordering Information

Table 12 Ordering Information

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temperature Range	MSL Level	Ecology
SP6122C-LMR	SP6122C	LGA 3x3	Tape and Reel	-	3	RoHS[1]

Table 12 notes:

1. This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

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