SP6317: Dual Channel, 3.3 GHz – 3.8 GHz, Receiver Switch & LNA Front End Module

General Description

The SP6317 is a dual-channel, integrated radio frequency (RF), front-end multichip module designed for time division duplexing (TDD) applications that operate in the 5G n78 frequency band (3.3 GHz to 3.8 GHz). The SP6317 is configured in dual channels with a cascading two-stage low noise amplifier (LNA) and a high-power silicon single-pole, double-throw (SPDT) switch.

The device comes in a RoHS compliant, compact, 6 mm × 6 mm, 40-lead package.

Applications

- Wireless Infrastructure
- TDD massive multiple input and multiple output and active antenna systems
- TDD-Based communication systems

Features

- Integrated dual-channel RF front end with 2 stage LNA and high power SPDT switch along with On-chip bias and matching
- Single supply operation
- Gain
  - High gain mode: 35 dB typical at 3.5 GHz
  - Low gain mode: 15 dB typical at 3.5 GHz
- Low noise figure
  - High gain mode: 1.0 dB typical at 3.5 GHz
  - Low gain mode: 1.0 dB typical at 3.5 GHz
- Low insertion loss: 0.5 dB typical at 3.5 GHz
- High Ch-Ch Isolation: -40dB typical in Rx mode
- High OIP3: 29 dBm typical in Rx High Gain mode
- High power handling at T_{CASE} = 105°C
  - Full lifetime 5G NR average power (9 dB PAR): 43 dBm
  - Single event (<10 sec operation) 5G NR average power (9 dB PAR): 46 dBm
- Low supply current
  - High gain mode: 100 mA typical at 5 V (per channel)
  - Low gain mode: 46 mA typical at 5 V (per channel)
  - Power-down mode: 10 mA typical at 5 V (per channel)
- 6 mm × 6 mm, 40-lead LFCSP package

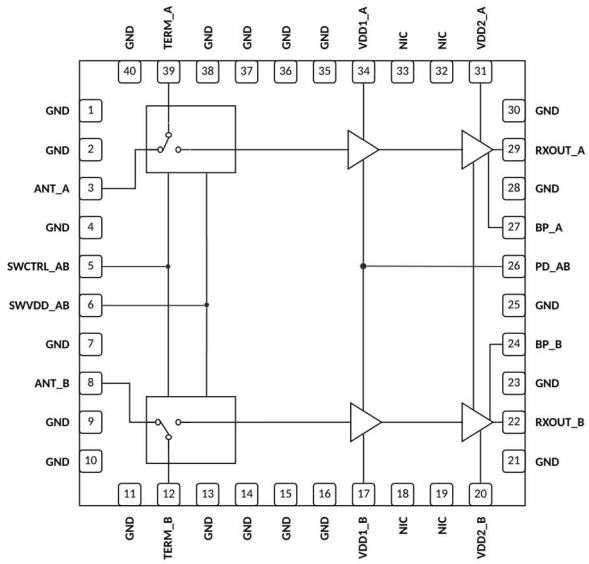

Figure 1 Functional Diagram

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1 Pin Configuration

1.1 Pin Configuration Diagram

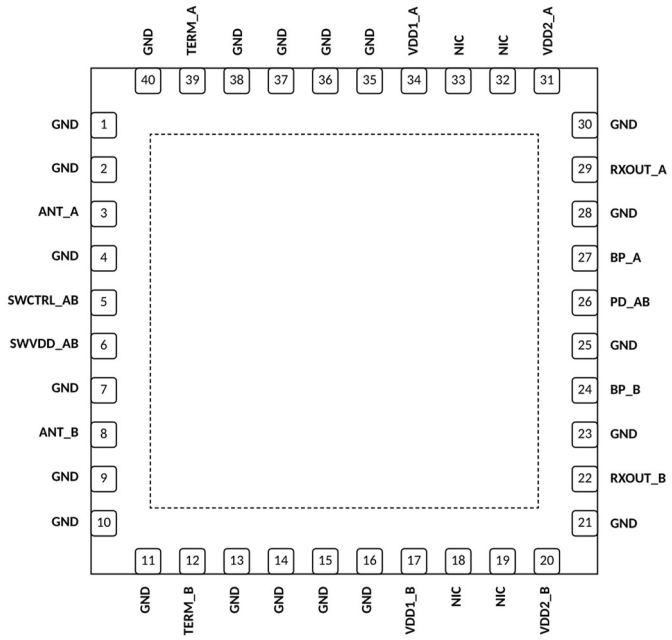


Figure 2 SP6317 Pin Configuration

1.2 Pin Description

Table 1 Pin Functions

PIN Name	Pin No.	Description
ANT_A	3	RF Input to Channel A.
SWCTRL_AB	5	Switch control for Channel A and B switch.
SWVDD_AB	6	Supply voltage for Channel A and B switch.
ANT_B	8	Switch control for Channel B switch.
TERM_B	12	Termination Output for Channel B. This pin is the transmit path for Channel B.
GND	1, 2, 4, 7, 9, 10, 11, 13, 14, 15, 16, 21, 23, 25, 28, 30, 35, 36, 37, 38, 40	Ground
NIC	18,19,32, 33	Not internally connected. It is recommended to connect NIC to the RF ground of the PCB.
VDD1_B	17	Supply voltage for Stage 1 LNA on Channel B.
VDD2_B	20	Supply voltage for Stage 2 LNA on Channel B.
RXOUT_B	22	RF Output. This pin is the receiver path for Channel B.
BP_B	24	Bypass second stage LNA of Channel B.
PD_AB	26	Power-Down all stages of LNA for Channel A and B.
BP_A	27	Bypass second stage LNA of Channel A.
RXOUT_A	29	RF Output. This pin is the receiver path for Channel A.
VDD2_A	31	Supply voltage for Stage 2 LNA on Channel A.
VDD1_A	34	Supply voltage for Stage 1 LNA on Channel A.
TERM_A	39	Termination Output for Channel A. This pin is the transmit path for Channel A.
EPAD		Exposed Pad. The exposed pad must be connected to RF or dc ground.

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Parameter	Conditions	Symbol	Min	Max	Units
Positive Supply Voltage	VDD1_A, VDD1_B, VDD2_A, VDD2_B		-0.3	5.5	V
	SWVDD_AB		-0.3	5.5	V
Digital Control Input Voltage	PD_AB, BP_A, BP_B		-0.3	5.5	V
	SWCTRL_AB		-0.3	3.6	V
RF Input Power	Transmit Input Power	5G NR Peak		55	dBm
	Receive Input Power	5G NR peak		25	dBm
Temperature	Storage		-65	150	°C
	Reflow			260	°C
Electrostatic Discharge Sensitivity (ESD)	Human Body Model	HBM		1000	V
	Charged Device Model	CDM		500	V

Notes:

- Operation of this device outside the parameter ranges given above may cause permanent damage.
- Operation of this device at the maximum operating ranges for extended periods of time may affect product reliability

Table 3 Electrical Specifications DC and Control

VDD1_A, VDD1_B, VDD2_A, VDD2_B, SWVDD_AB = 5 V; SWCTRL_AB = 0 V or 3.3V; BP_A/B =0 V or VDD1_A/B; PD_AB = 0 V or VDD1_A/B; Testing Frequency: 2.6 GHz. Case Temperature (TCASE) = 25 °C, 50 Ω system, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Current (IDD)	High Gain	VDD1_A/B and VDD2_A/B = 5 V per channel		100		mA
	Low Gain	VDD1_A/B and VDD2_A/B = 5 V per channel		46		mA
	Power-Down Mode	VDD1_A/B and VDD2_A/B = 5 V per channel		10		mA
	TX Current (Switch)	SWVDD_AB = 5 V		4		mA
Digital Currents	SWCTRL_AB	SWCTRL_AB = 3.3 V		200		uA
	PD_AB	PD_AB = 5 V		240		uA
	BP_A/B	BP_A/B = 5 V per channel		120		uA
DIGITAL INPUT						
SWCTRL_AB	Low (VIL)		0		0.63	V
	High (VIH)		1.17		3.3	V
PD_AB	Low (VIL)		0		0.63	V
	High (VIH)		1.17		VDD	V
BP_A/B	Low (VIL)		0		0.63	V
	High (V_{IH})		1.17		VDD	V

Table 4 Electrical Specifications at 3.5 GHz

VDD1_A, VDD1_B, VDD2_A, VDD2_B, SWVDD_AB = 5 V; SWCTRL_AB = 0 V or 3.3V; BP_A/B =0 V or VDD1_A/B; PD_AB = 0 V or VDD1_A/B; Testing Frequency: 3.5 GHz. Case Temperature (T_{CASE}) = 25 °C, 50 Ω system, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
GAIN[1]	High Gain Mode	Receive operation		35		dB
	Low Gain Mode			15		dB
GAIN FLATNESS[1]	High Gain Mode	Receive operation in any 100 MHz bandwidth		0.5		dB
	Low Gain Mode			0.5		dB
Noise Figure(NF)[1]	High Gain Mode	Receive operation		1.0		dB
	Low Gain Mode			1.0		dB
Output Third-Order Intercept Point (OIP3)[1]	High Gain Mode	Receive operation, two-tone output power = +3 dBm per tone at 1 MHz tone spacing		29		dBm
	Low Gain Mode	Receive operation, two-tone output power = -1 dBm per tone at 1 MHz tone spacing		25		dBm
Output 1 dB Compression (OP1dB)	High Gain Mode	Receive operation		17		dBm
	Low Gain Mode			11		dBm
Insertion Loss[1]		Transmit Operation		0.5		
Channel to Channel Isolation[1]	Between RXOUT_A AND RXOUT_B	Receive operation		-40		dB
Switch Isolation	ANT_A TO TERM_A AND ANT_B TO TERM_B[1]	Receive operation, PD_AB = 0 V		-15		dB
Input return loss		Receive operation, High Gain Mode		-20		dB
Output return		Receive operation, High Gain Mode		-13		dB
Input return loss		Receive operation, Low Gain Mode		-20		dB
Output return		Receive operation, Low Gain Mode		-13		dB
Input return loss		Transmit operation		-20		dB
Output return loss		Transmit operation		-15		dB
Switching time		50% control voltage to 90%, 10% of RF, Tx → Rx or Rx → Tx transition		700		ns

Notes:
1. Refer Truth Tables, Table 7 and Table 8

Table 5 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Bias Voltage Range	VDD1_A/B, VDD2_A/B, SWVDD_AB	4.75	5	5.25	V
Control Voltage Range	PD_AB, BP_A/B	0		VDD	V
	SWCTRL_AB	0		3.3	V
RF Input Power at ANT_A, ANT_B	SWCTRL_AB = 3.3 V, PD_AB = 5 V, BP_A/B = 0 V, T_{CASE} = 105°C				
	9 dB PAR 5G NR full lifetime average			43	dBm
	9 dB PAR 5G NR single event (<10 sec) average			46	dBm
Case Temperature Range T_{CASE} [2]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}[2]	Receive operation[1]			TBD	°C
	Transmit operation[1]			TBD	°C

Notes:
1. Refer Truth Tables, Table 7 and Table 8
2. Measured at EPAD

Table 6 Thermal Resistance

Package Type		θJC	Unit
CP-40-15	Transmit SW	12.5	°C/W
	Receiver LNA	25	°C/W

3 Detailed Functional Description

3.1 Functional Block Diagram

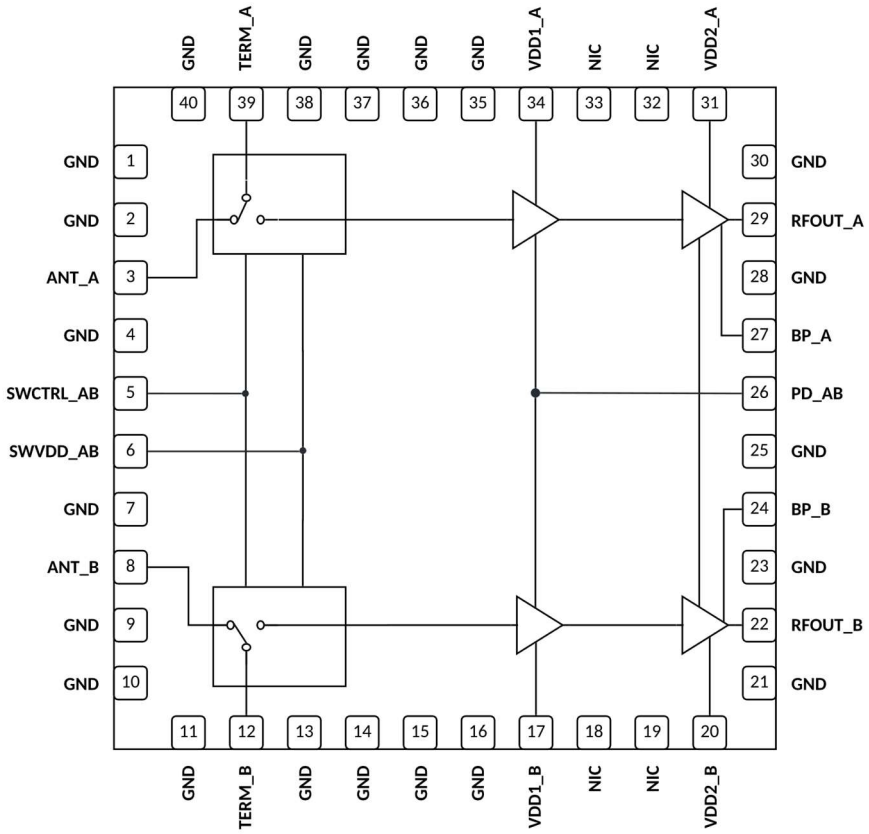


Figure 3 Functional Block Diagram

3.2 Overview

The SP6317 is a dual-channel, integrated radio frequency (RF), front-end multichip module designed for time division duplexing (TDD) applications that operate in the 5G n78 frequency band (3.3 GHz to 3.8 GHz). The SP6317 is configured in dual channels with a cascading two-stage low noise amplifier (LNA) and a high-power silicon single-pole, double-throw (SPDT) switch.

In Rx high gain mode, the cascaded two-stage LNA and switch offer a low noise figure (NF) of 1.2 dB, a high gain of 35 dB at 3.5 GHz, with current consumption of 100 mA per channel. In Rx low gain mode, one stage of the two-stage LNA is in bypass, providing 15 dB of gain at a lower current of 46 mA per channel. In power-down mode, the LNAs are turned off and the device draws 10 mA per channel.

In transmit operation, when RF inputs are connected to a termination pin (TERM_A or TERM_B), the switch provides a low insertion loss of 0.5 dB at 3.5 GHz and handles an 5G NR signal with an average power (9 dB peak to average ratio (PAR)) of 43 dBm for full lifetime operation and 46 dBm for single event (<10 sec). There is also an option of keeping the RX LNAs operational in the TX mode.

The SP6317 requires a positive supply voltage applied to VDD1_A, VDD2_A, VDD1_B, VDD2_B, SWVDD_AB. Correct decoupling is required on the power supply lines for optimum noise performance, see application diagram for details.

3.2.1 Transmit Operation

The SP6317 supports transmit operations when 3.3 V is applied to SWCTRL_AB. In transmit operation, when an RF input is applied to ANT_A and ANT_B, the signal path connection is from ANT_A to TERM_A and from ANT_B to TERM_B.

The SP6317 also supports receive LNA being powered up in transmit operation. This is achieved by applying 0 V to PD_AB.

3.2.2 Receive Operation

In receive operation, ANT_A is connected to RXOUT_A and ANT_B to RXOUT_B. SP6317 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table 8

When 0 V is applied to PD_AB, the LNA is powered up and the user can select high gain mode or low gain mode. To select high gain mode, apply 0 V to BP_A or BP_B. To select low gain mode, apply 5 V to BP_A or BP_B.

When 5 V is applied to PD_AB, the SP6317 enters power-down mode. To select power-down high isolation mode, apply 0 V to BP_A or BP_B. To select power-down low isolation mode, apply 5 V to BP_A or BP_B.

3.3 Biasing Sequence

To Bias up the SP6317, perform the following steps.

1. Connect GND to ground.
2. Bias up VDD1_A, VDD2_A, VDD1_B, VDD2_B, SWVDD_AB.
3. Bias up SWCTRL_AB.
4. Bias up PD_AB.
5. Bias up BP_A and BP_B.
6. Apply an RF input signal.

To Bias down, perform these steps in the reverse order

Table 7 Truth Table Signal Path

SWCTRL_AB	Signal Path Select	
	Transmit Operation[1]	Receive Operation
Low	Off	On
High	On	Off

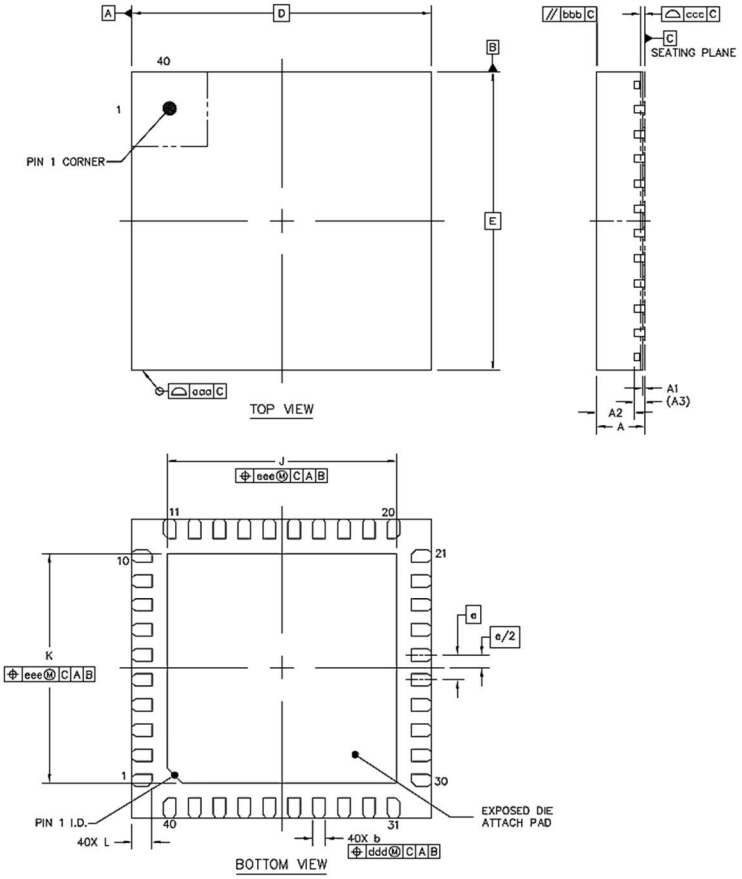
Notes:
1. See the signal path descriptions in Table 8

Table 8 Truth Table Operation

Operation		PD_AB	BP_A, BP_B	Signal Path
Receive operation	High Gain Mode	Low	Low	ANT_A to RXOUT_A, ANT_B to RXOUT_B
	Low Gain Mode	Low	High	
	Power Down High Isolation Mode	High	Low	
	Power Down Low Isolation Mode	High	High	
Transmit Operation	Insertion Loss Mode	High	Low	ANT_A to TERM_A, ANT_B to TERM_B

4 Package Information

4.1 Package Marking and Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.9	0.95	1
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.75	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 4 Package Dimensions

5 Ordering Information

Table 9 SP6317 Ordering Information

Ordering Part Number (OPN)	Marking	Package information	Temperature Range
SP6317-QMR	SP6317	40 QFN	-40°C to 105°C

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