SP6352: 3.3 – 3.8 GHz 100 W Receiver Switch & LNA Front End Module

General Description

The SP6352 is an integrated radio frequency (RF) front-end multichip module designed for time division duplexing (TDD) applications that operating from 3.3 to 3.8 GHz. The SP6352 is configured as a two-stage low noise amplifier (LNA) and a high-power silicon single-pole, double-throw (SPDT) switch.

The device comes in a RoHS compliant, compact, 6 mm × 6 mm, 40-lead package. **Note this package will be updated to a 28 pin version. Datasheeet to updated when new package is confirmed**

Applications

- Wireless Infrastructure
- TDD massive multiple input and multiple output and active antenna systems
- TDD-Based communication systems

Features

- Integrated RF front end with 2 stage LNA and high power SPDT switch along with On-chip bias and matching
- Single supply operation
- Gain
  - High gain mode: 35 dB typical at 3.5 GHz
  - Low gain mode: 15 dB typical at 3.5 GHz
- Low noise figure
  - High gain mode: 1.3 dB typical at 3.5 GHz
  - Low gain mode: 1.3 dB typical at 3.5 GHz
- Low insertion loss: 0.5 dB typical at 3.5 GHz
- High OIP3: 29 dBm typical in Rx High Gain mode
- High power handling at T_{CASE} = 105°C
  - Full lifetime 5G NR average power (9 dB PAR): 50 dBm
  - Single event (<10 sec operation) 5G NR average power (9 dB PAR): 53 dBm
- Low supply current
  - High gain mode: 100 mA typical at 5 V
  - Low gain mode: 46 mA typical at 5 V
  - Power-down mode: 10 mA typical at 5 V
- 6 mm x 6 mm, 40-lead LFCSP package.

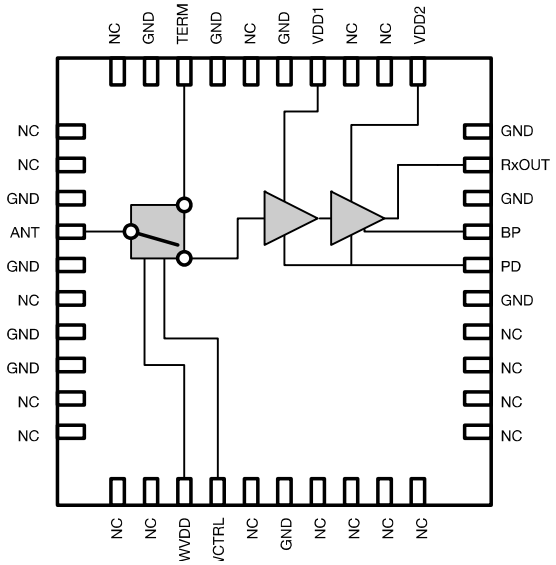

Figure 1 Functional Diagram

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1 Pin Configuration

1.1 Pin Configuration Diagram

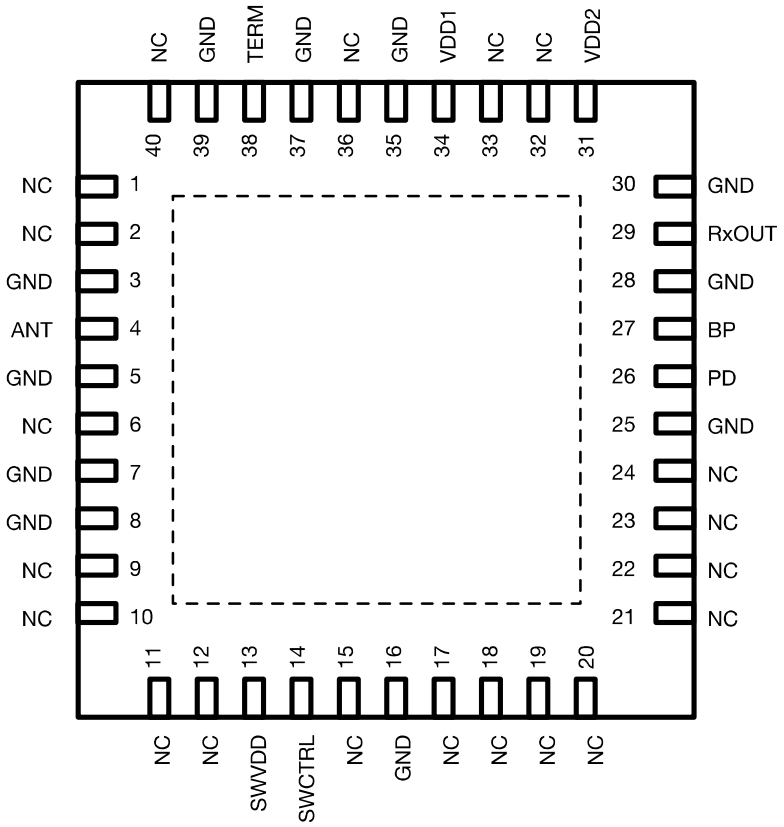


Figure 2 SP6352 Pin Configuration (Top View)

1.2 Pin Description

Table 1 Pin Functions

PIN Name	Pin No.	Description
TERM	38	Termination Output used in Tx mode.
ANT	4	RF Input.
SWCTRL	14	Switch control.
SWVDD	13	Supply voltage for switch.
GND	3, 5, 7, 8, 16, 25, 28, 30, 35, 37, 39	Ground
NC	1, 2, 6, 9, 10, 11, 12, 15, 17, 18, 19, 20, 21, 22, 23, 24, 32, 33, 36, 40	Not internally connected. It is recommended to connect NC to the RF ground of the PCB.
VDD1	34	Supply voltage for Stage 1 LNA.
VDD2	31	Supply voltage for Stage 2 LNA.
RXOUT	29	RF Output in Rx mode.
BP	27	Bypass second stage LNA.
PD	26	Power-Down all stages of LNA.
EPAD		Exposed Pad. The exposed pad must be bonded directly to RF Ground.

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Positive Supply Voltage	VDD1, VDD2		-0.3	5.5	V
	SWVDD		-0.3	5.5	V
Digital Control Input Voltage	PD, BP		-0.3	5.5	V
	SWCTRL		-0.3	3.3	V
RF Input Power (5G NR 20MHz Signal)	Transmit Input Power	TX Peak In		62	dBm
	Receive Input Power	RX Peak In		25	dBm
Temperature	Storage		-65	150	°C
	Reflow			260	°C

Notes:

- Operation of this device outside the parameter ranges given above may cause permanent damage.
- Operation of this device at between the recommentded and the maximum operating ranges for one or more parameters over extended periods of time may affect product reliability

Table 3 Electrical Specifications DC and Control

Parameter		Conditions	Min	Typ	Max	Unit
Supply Current (I_{DD})	High Gain	VDD1 and VDD2 = 5 V		100		mA
	Low Gain	VDD1 and VDD2 = 5 V		46		mA
	Power-Down Mode	VDD1 and VDD2 = 5 V		10		mA
	TX Current (Switch)	SWVDD = 5 V		2.5		mA
Digital Currents	SWCTRL_A/B	SWCTRL = 3.3 V		110		uA
	PA_A/B	PD = 5 V		167		uA
	BP_A/B	BP = 5 V		167		uA
DIGITAL INPUT						
SWCTRL	Low (V_{IL})		0		0.63	V
	High (V_{IH})		1.17		3.3	V
PD	Low (V_{IL})		0		0.63	V
	High (VIH)		1.17		VDD	V
BP	Low (V_{IL})		0		0.63	V
	High (V_{IH})		1.17		VDD	V

Table 4 Electrical Specifications at 3.5 GHz

VDD1, VDD2, SWVDD = 5 V; SWCTRL = 0 V or 3.3V; BP =0 V or VDD1; PD = 0 V or VDD1; Testing Frequency: 3.5 GHz. Case Temperature (T_{CASE}) = 25 °C, 50 Ω system, unless otherwise noted.

Parameter		Condition	Min	Typ	Max	Units
GAIN[1]	High Gain Mode	Receive operation		35		dB
	Low Gain Mode			15		dB
GAIN FLATNESS[1]	High Gain Mode	Receive operation in any 100 MHz bandwidth		0.3		dB
	Low Gain Mode			0.3		dB
Noise Figure(NF)[1]	High Gain Mode	Receive operation		1.3		dB
	Low Gain Mode			1.3		dB
Output Third-Order Intercept Point (OIP3)[1]	High Gain Mode	Receive operation, two-tone output power = +3 dBm per tone at 1 MHz tone spacing		29		dBm
	Low Gain Mode	Receive operation, two-tone output power = 0 dBm per tone at 1 MHz tone spacing		25		dBm
Output 1 dB Compression (OP1dB)	High Gain Mode	Receive operation		17		dBm
	Low Gain Mode			12		dBm
Insertion Loss[1]		Transmit operation		0.5		dB
Switch Isolation	ANT TO TERM [1]	Receive operation, PD = 0 V		-15		dB
Input return loss		Receive operation, High Gain Mode		-16		dB
Output return loss		Receive operation, High Gain Mode		-15		dB
Input return loss		Receive operation, Low Gain Mode		-16		dB
Output return loss		Receive operation, Low Gain Mode		-15		dB
Input return loss		Transmit operation		-20		dB
Output return loss		Transmit operation		-15		dB
Switching time		50% control voltage to 90%, 10% of RF			2000	ns
Current		RX Mode High Gain		100		mA
		RX Mode Low Gain		46		
		TX Mode		10		

Notes:
1. Refer Truth Tables, Table 7 and Table 8

Table 5 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Bias Voltage Range	VDD1, VDD2, SWVDD	4.75	5	5.25	V
Control Voltage Range	PD, BP	0		VDD	V
	SWCTRL	0		3.3	V
Operating Frequency		3.3		3.8	GHz
RF Input Power at ANT to TERM (TX Mode)[note 1]					
	9 dB PAR 5G NR full lifetime average			50	dBm
	9 dB PAR 5G NR single event (<10 sec) average			53	dBm
RF Input Power at ANT to LNA (RX Mode)[note 1]	High Gain Mode			-30	dBm
	Low Gain Mode			-15	
Case Temperature Range T_{CASE} [2]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}[2]	Receive operation[1]			TBD	°C
	Transmit operation[1]			TBD	°C

Notes:

1. Refer Truth Tables, Table 7 and Table 8
2. Measured at EPAD.

Table 6 Thermal Resistance

Package Type		θJC	Unit
CP-40-15	High Gain and Low Gain Mode	TBD	°C/W
	Power-Down Mode	TBD	°C/W

3 Detailed Functional Description

3.1 Functional Block Diagram

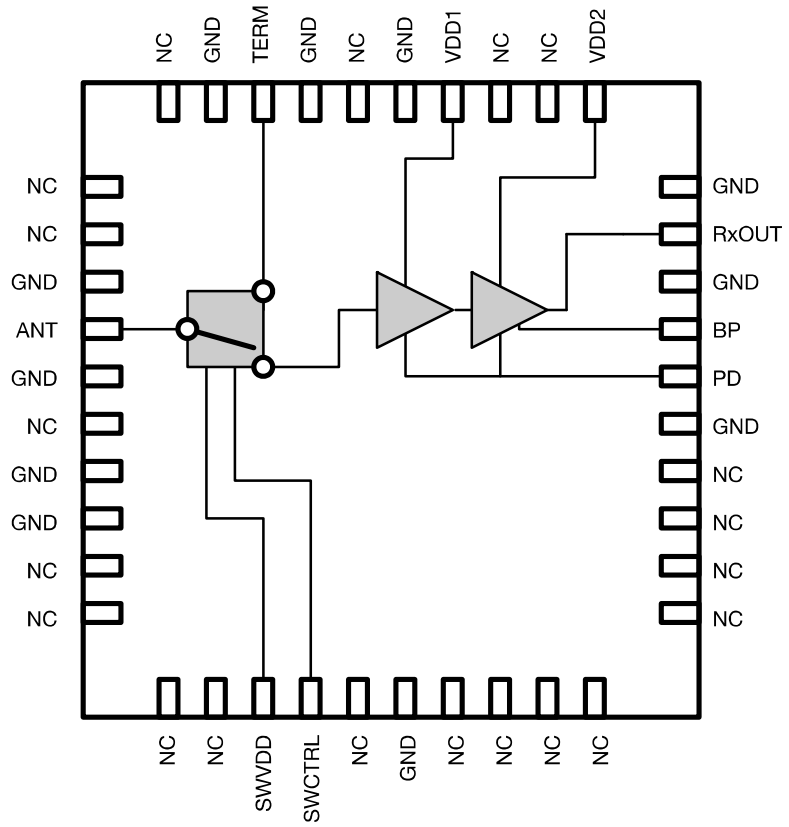


Figure 3 Functional Block Diagram

3.2 Overview

The SP6352 is an integrated radio frequency (RF), front-end multichip module designed for time division duplexing (TDD) applications operating from 3.3 to 3.8 GHz. The SP6352 is configured with a two-stage low noise amplifier (LNA) and a high-power silicon single-pole, double-throw (SPDT) switch.

In Rx high gain mode, the cascaded two-stage LNA and switch offer a low noise figure (NF) of 1.3 dB, a high gain of 35 dB at 3.5 GHz, with current consumption of 100 mA per channel. In Rx low gain mode, one stage of the two-stage LNA is in bypass, providing 15 dB of gain at a lower current of 46 mA per channel. In power-down mode, the LNAs are turned off and the device draws 10 mA per channel.

In transmit operation, when RF inputs are connected to a termination pin (TERM), the switch provides a low insertion loss of 0.5 dB at 3.5 GHz and handles an 5G NR signal with an average power (9 dB peak to average ratio, (PAR)) of 50 dBm for full lifetime operation and 53 dBm for single event (<10 sec). There is also an option of keeping the RX LNAs operational in the TX mode.

The SP6352 requires a positive supply voltage applied to VDD1, VDD2 and SWVDD. Correct decoupling is required on the power supply lines for optimum noise performance, see application diagram for details.

3.2.1 Transmit Operation

The SP6352 supports transmit operations when 3.3 V is applied to SWCTRL. In transmit operation, when an RF input is applied to ANT, the signal path connection is from ANT to TERM.

The SP6352 also supports receive LNA being powered up in transmit operation. This is achieved by applying 0 V to PD.

3.2.2 Receive Operation

In receive operation, ANT is connected to RXOUT. SP6352 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table 8

When 0 V is applied to PD, the LNA is powered up and the user can select high gain mode or low gain mode. To select high gain mode, apply 0 V to BP. To select low gain mode, apply 5 V to BP.

When 5 V is applied to PD, the SP6352 enters power-down mode. To select power-down high isolation mode, apply 0 V to BP. To select power-down low isolation mode, apply 5 V to BP.

3.3 Biasing Sequence

To Bias up the SP6352, perform the following steps.

1. Connect GND to ground.
2. Bias up VDD1, VDD2, SWVDD.
3. Bias up SWCTRL.
4. Bias up PD.
5. Bias up BP.
6. Apply an RF input signal.

To Bias down, perform these steps in the reverse order

Table 7 Truth Table Signal Path

SWCTRL	Signal Path Select	
	Transmit Operation[1]	Receive Operation
Low	Off	On
High	On	Off

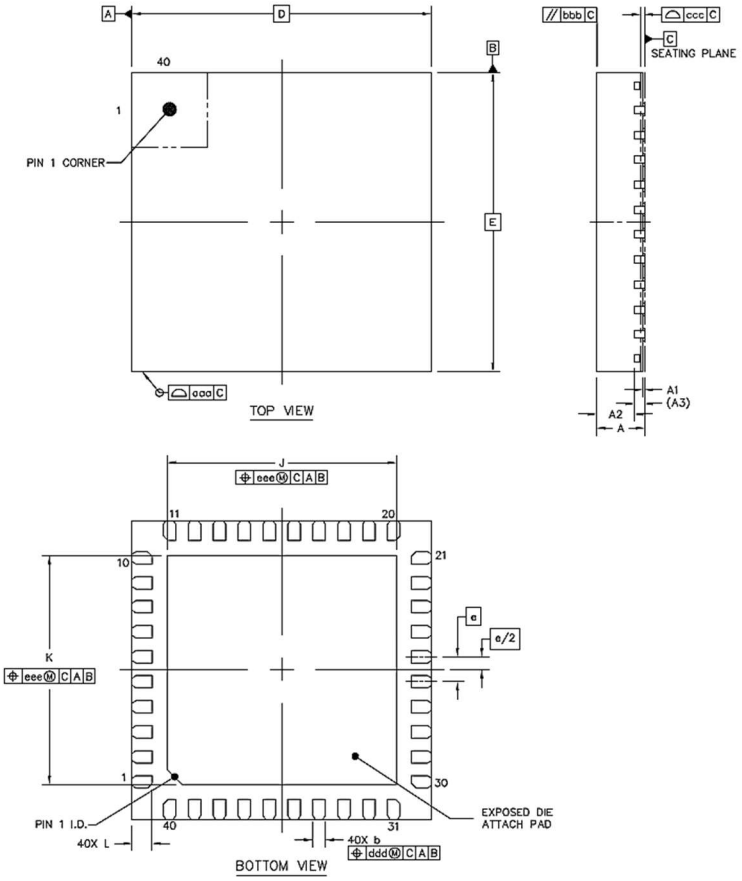
Notes:
1. See the signal path descriptions in Table 8

Table 8 Truth Table Operation

Operation		PD	BP	Signal Path
Receive operation	High Gain Mode	Low	Low	ANT to RXOUT
	Low Gain Mode	Low	High	
	Power Down High Isolation Mode	High	Low	
	Power Down Low Isolation Mode	High	High	
Transmit Operation	Insertion Loss Mode	High	Low	ANT to TERM

4 Package Information

4.1 Package Marking and Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.9	0.95	1
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.75	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 4 Package Dimensions

5 ESD / MSL

Table 9 – Handling Precautions

Test Condition	Rating	Reference
MSL (Moisture Sensitivity Level)	3	
ESD – HBM (Human Body Model)	TBD	JS-001-2017
ESD – CDM Charged Device Model)	TBD	JS-002-2018

6 Environmental

This part is compliant with 2011/65/EU RoHS directive.

7 Ordering Information

Table 10 SP6352 Ordering Information

Ordering Part Number (OPN)	Marking	Package information	Storage Temperature Range
TBD	TBD	40 QFN	-40°C to 125°C

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