SP6488: 8W Peak Power Amplifier, 3.3-3.7 GHz

General Description

The SP6488 is a high efficiency 8 W peak power amplifier designed to support FDD and TDD small cell base stations operating over a wide frequency range of 3.3 GHz to 3.7 GHz. The RF input and output ports are internally matched to 50 Ω for the full frequency range. This device incorporates a device enable pin with turn on/off times less than 1 us.

The power amplifier has high gain and peak power which linearizes well in DPD systems giving better than 50 dBc ACLR for 20 MHz modulation bandwidth.

This amplifier uses a Doherty architecture to improve back-off efficiency required by modern communications standards which employ high peak-to-average signals. A functional diagram of the SP6488 is shown in Figure 1. The RF input does not require a DC block provided the input connection is at 0 V DC. The RF output has an internal DC block.

Applications

- 5G Small Cell applications
- MIMO Systems
- 3GPP bands 42, n48, n77 n78.
- Driver amplifier
- General purpose wireless

Features

- Frequency 3.3 GHz to 3.7 GHz
- High Peak Envelope Power 39 dBm
- High Efficiency 24%
- High Small Signal Gain 36 dB
- Instantaneous Bandwidths up to 200 MHz
- Single Supply Domain +5 V
- Enable/shutdown pin
- Package: 5x5 mm

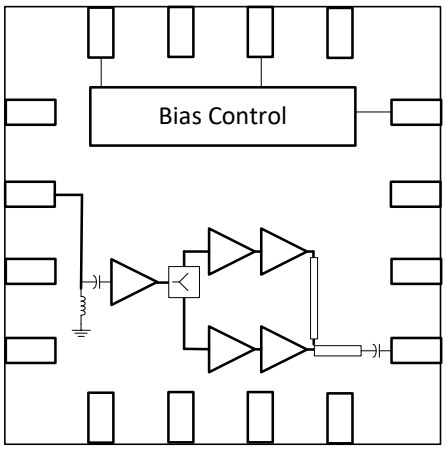

Figure 1 Functional Diagram

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1 Pin Configuration

1.1 Pin Configuration Diagram

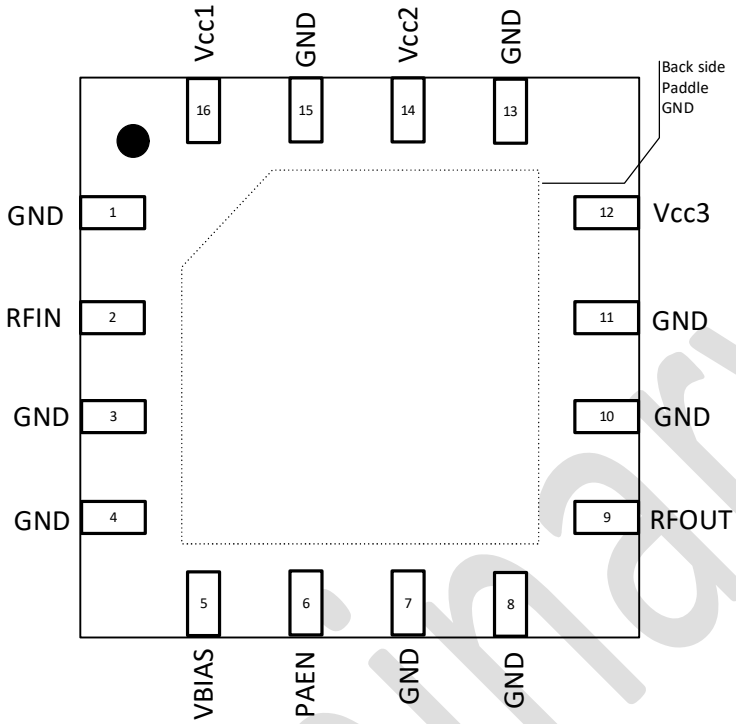


Figure 2 SP6488 Pin Diagram (Top View)

1.2 Pin Description

Table 1 Pin Description

Pin No	Pin Name	Description
1	GND	Ground connection
2	RF In	RF Input – Matched to 50 Ω
3	GND	Ground connection
4	GND	Ground connection
5	Vbias	Supply for bias circuit
6	PAEN	Controls operation between active and low power states
7	GND	Ground connection
8	GND	Ground connection
9	RF Out	RF Output – matched to 50 Ω
10	GND	Ground connection
11	GND	Ground connection
12	Vcc3	Supply for 3rd stage
13	GND	Ground connection
14	Vcc2	Supply for 2nd stage
15	GND	Ground connection
16	Vcc1	Supply for 1st stage
Backside Paddle	GND	This is the ground connection and should be soldered directly to ground, ensuring low inductance and low thermal resistance

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage		5.5	V
Control Pin Input Voltage		2.8	V
Peak RF Input Power (LTE 20 MHz modulated 8.5dB PAPR signal)		TBD	dBm
Maximum Junction Temperature		150	°C
Storage Temperature	-55	125	°C

Table 2 Absolute Maximum Ratings notes:

1. Exceeding absolute maximum ratings may cause permanent damage. Operation should only occur within the limits specified. Operating between the maximum operating range Table 5 and the absolute maximum for extended periods may reduce the reliability of the device.
2. Not recommended for pulsed CW operation

Table 3 Handling Precautions

Observe standard procedures as with other ESD-sensitive devices when handling the product. The product includes ESD protection circuitry, but precautions should be taken not to exceed the ratings specified in this table.

Parameter	Level	Test Standard
ESD voltage HBM, All Pins	TBD	JS-001-2017
ESD voltage CDM, All pins	TBD	JS-002-2018
Moisture Sensitivity Level	TBD	J-STD-020E

Table 4 Device Thermal Resistance

Parameter	θjc	Unit
Junction to case bottom	TBD	°C/W

Table 5 Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage ($V_{CC1,2,3}$, V_{BIAS})	Vcc1, Vcc2, Vcc3, Vbias	4.75	5	5.25	V
Control Input (PA Enable) High	Vctrl	1.7	2	2.5	V
Control Input (PA Enable) Low	Vctrl	0		0.7	V
RF Input Power, average (LTE)	Pin			TBD	dBm
Operating Temperature Range (T_{CASE})	Tcase	-40	25	85	°C

Table 6 Electrical Characteristics.

Operating conditions:
Tcase = 25 °C, Vcc = Vbias = 5 V , Zin = Zout = 50 Ω, Fc = 3500 MHz unless otherwise stated

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Frequency		f	2496		2690	MHz
Small Signal Gain	P_{IN} = -35 dBm	S21		33.5		dB
Input Return Loss	P_{IN} = -25 dBm	S11		16		dB
Output Return Loss	P_{IN} = -25 dBm	S22		20		dB
Reverse Isolation	P_{IN} = -25 dBm	S12		60		dB
Gain @ 29 dBm	P_{OUT} = 30 dBm	$S21_{@29\ dBm}$		35		dB
ACLR (RAW)	LTE 20 MHz, 8.5 dB PAPR, +30 dBm av. Power	ACLR		32		dBc
Output Power at 3 dB compression	CW, ref to small signal gain; PIN = -30 dBm	P3dB		39		dBm
2nd Harmonic	CW, P_{OUT} = 30 dBm	2fo		-50		dBc
3rd Harmonic	CW, P_{OUT} = 30 dBm	3fo		-60		dBc
Power-added Efficiency	P_{OUT}=30 dBm (CW)	PAE		21.5		%
PA Enable Current Draw		I_{PAEN}		260		uA
Quiescent Current	No RF signal	I_{CCQ}		270		mA

Table 7 Device Truth Table

Control Input (PA Enable) State	Device State
High	Amplifier On
Low	Amplifier Off

3 Example Application Diagram

For the Evaluation Board (EVB) details, including schematic, board stack-up and Gerber images please see the SP6488 Application Note.

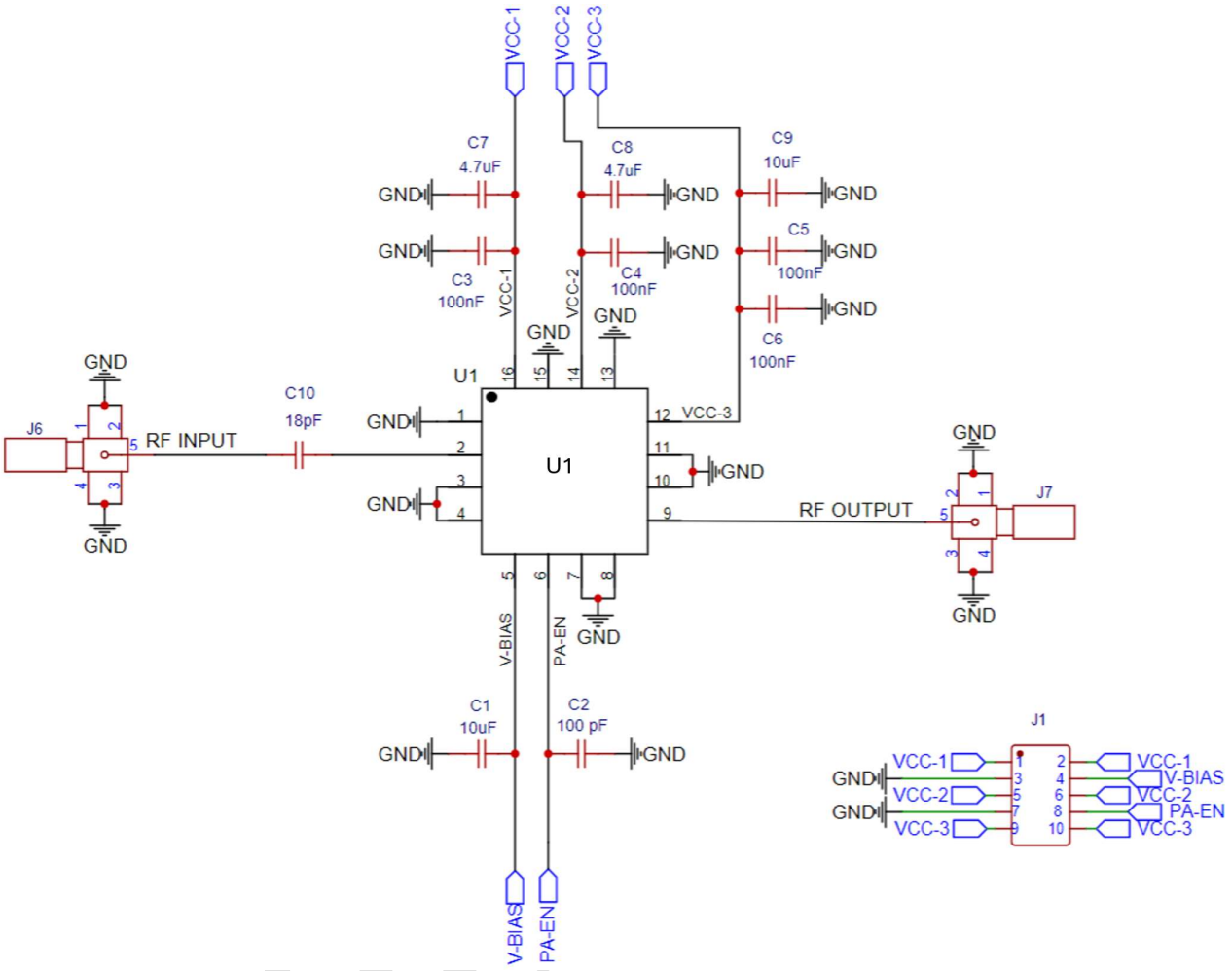


Figure 3 Schematic Diagram

Table 8 Bill of Materials

Component Reference	Value	Tolerance	Voltage	Manufacturer	Part Number
C1	10uF	+/-20%	10V	Samsung	CL05A106MP5NUNC
C2	100pF	+/-5%	50V	Murata	GCM1555C1H101JA16D
C3, C4, C5, C6	100nF	+/-10%	50V	Murata	GCM155R71H104KE02D
C7, C8	4.7uF	+/-10%	16V	Murata	GRM219C81C475KA73D
C9	10uF	+/-10%	16V	Murata	GRM21BC81C106KE15L
C10	18pF	+/-5%	50V	Murata	GJM1555C1H180JB01D
J1				Harwin	M20-8760546
J6, J7, J8, J9				Johnson/Cinch	142-0701-841
U1	SP648x			Spirit Semiconductor	SP6488

3.1 Power-Up / Down Sequence

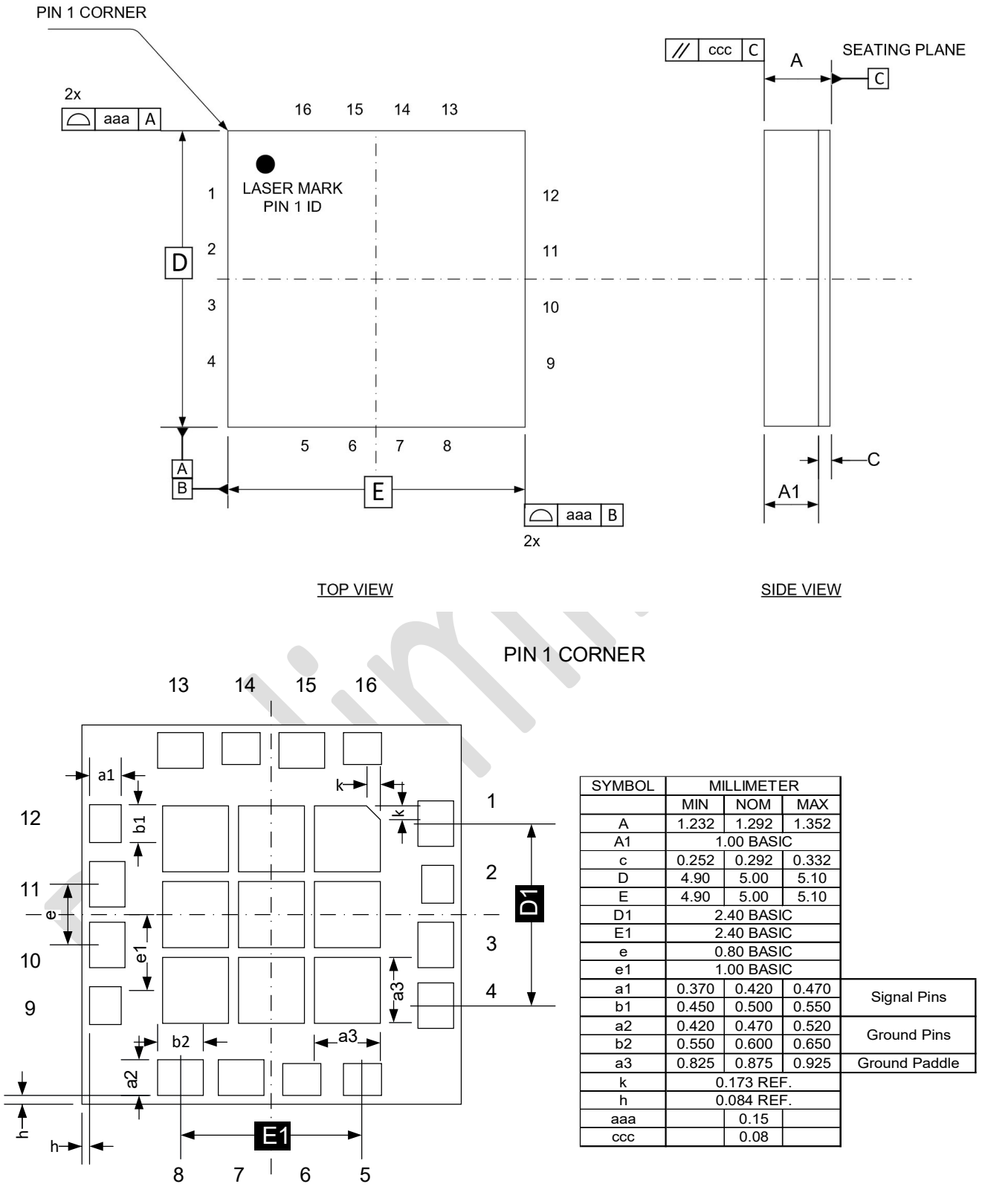
The device power-up sequence is as follows:

1) Terminate RF input and output with 50 Ohm
2) Connect DC ground
3) Ensure PA Enable is set to Low
4) Connect Vcc1, Vcc2, Vcc3 & Vbias to +5 V
5) Set PA Enable High to +2 V
6) Apply RF at PA Input at -30 dBm

The power-down sequence is the reverse of the power-up sequence.

It is important to ensure that ohmic losses in the power supply feed are accounted for and that the voltage at Vcc1,2,3 & Vbias are adjusted to 5.0 V at the operating condition.

4 Package Information



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	1.232	1.292	1.352	
A1		1.00 BASIC		
c	0.252	0.292	0.332	
D	4.90	5.00	5.10	
E	4.90	5.00	5.10	
D1		2.40 BASIC		
E1		2.40 BASIC		
e		0.80 BASIC		
e1		1.00 BASIC		
a1	0.370	0.420	0.470	Signal Pins
b1	0.450	0.500	0.550	
a2	0.420	0.470	0.520	Ground Pins
b2	0.550	0.600	0.650	
a3	0.825	0.875	0.925	Ground Paddle
k		0.173 REF.		
h		0.084 REF.		
aaa		0.15		
ccc		0.08		

Figure 4 Package Dimensions

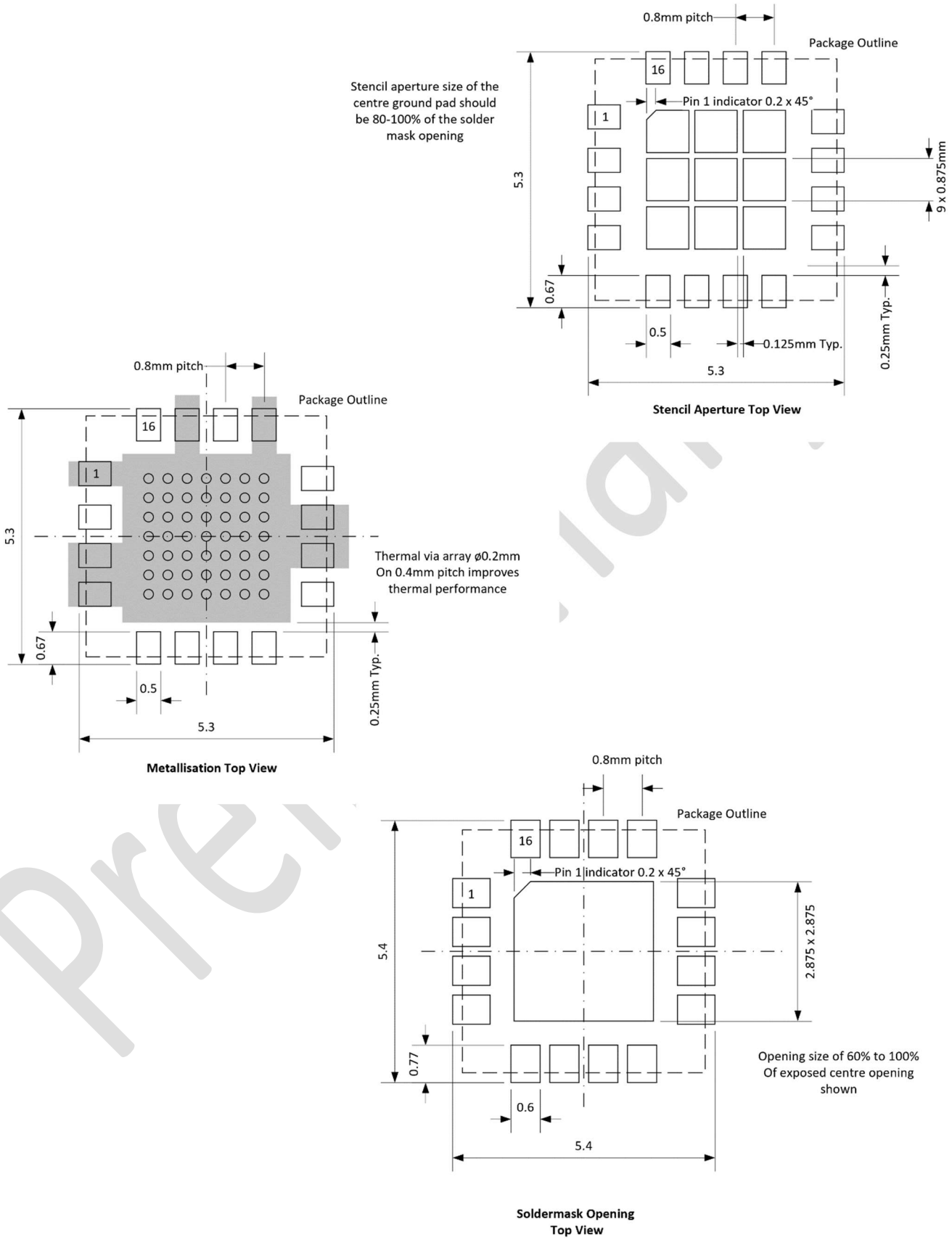


Figure 5 Solder Stencil and PCB Footprint Metallisation

5 Ordering Information

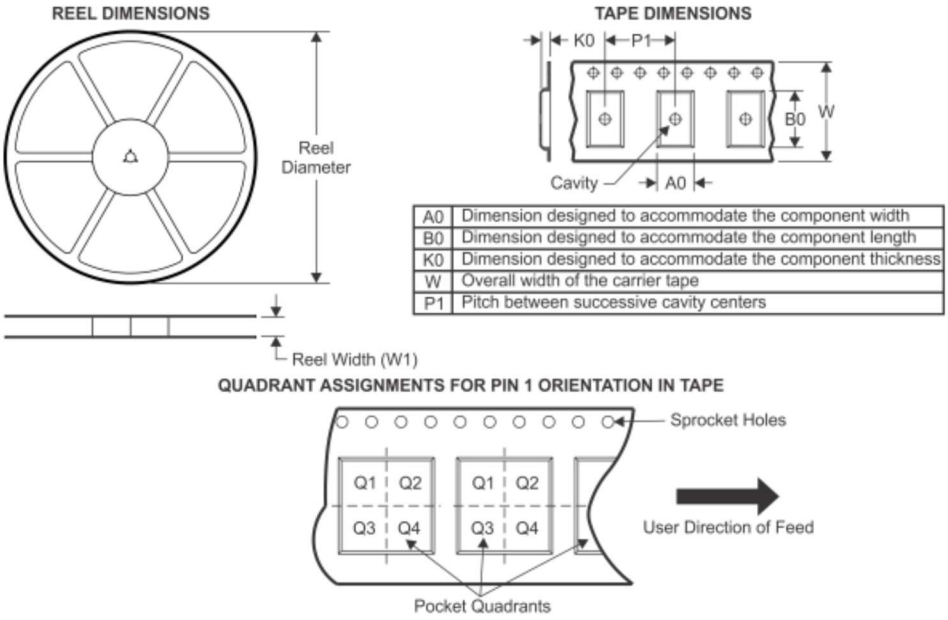
Table 9 Ordering Information

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temperature Range	MSL Level	Ecology
SP6488-LMR	SP6488	LGA 5x5	Tape and Reel	-	3	RoHS[1]

Notes:

1. This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Table 10 Tape and Reel Dimensions

Device	Package type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SP6488-LMR	LGA5x5	16	4000	330	12.4	5.35	5.35	1.5	8	12	Q1

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