

SP6498C: 8W Peak Power Amplifier, 2.5 GHz – 2.7 GHz

General Description

The SP6498C is a high efficiency 8 W peak power amplifier designed to support FDD and TDD small cell base stations operating over a wide frequency range of 2.5 GHz to 2.7 GHz. The RF input and output ports are internally matched to 50 Ω for the full frequency range. This device incorporates a device enable pin with turn on/off times less than 1 μ s.

The power amplifier has high gain and peak power which linearizes well with DPD systems, giving better than 50 dBc ACLR for 20 MHz modulation bandwidth. This amplifier uses a Doherty architecture and a functional diagram of the SP6498C is shown in Figure 1.

It is packaged in a compact 8 x 8 mm LGA20 package and uses a standard pin configuration.

Applications

- 5G Small Cell applications
- MIMO Systems
- 3GPP bands n7, n41.
- Driver amplifier
- General purpose wireless

Features

- Frequency 2.5 GHz to 2.7 GHz
- High Peak Envelope Power 39 dBm
- High Efficiency 23%
- High Small Signal Gain 36 dB
- Instantaneous Bandwidths up to 160 MHz
- Single Supply Domain +5 V
- Enable/shutdown pin
- Package: 8x8 mm

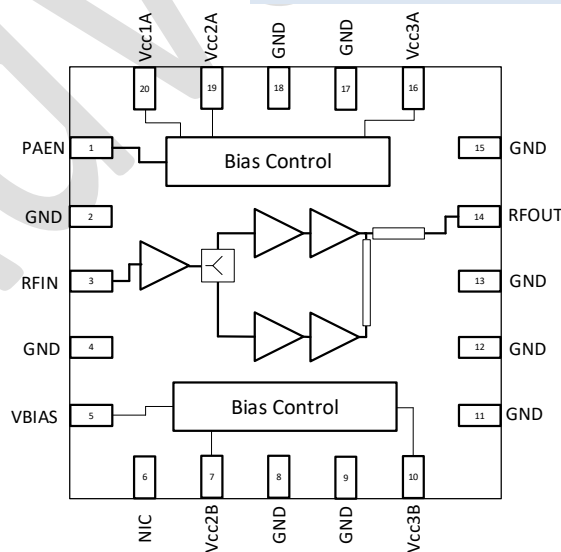


Figure 1 Functional Diagram

Table of Contents

General Description1

Applications.....1

Features1

Table of Contents2

List of Tables2

List of Figures2

1 Pin Configuration3

1.1 Pin Configuration Diagram3

1.2 Pin Description.....3

2 Electrical Specifications4

3 Example Application Diagram6

3.1 Power-Up / Down Sequence7

4 Package Information.....8

5 Ordering Information.....10

Contact Information12

Trademarks.....12

List of Tables

Table 1 Pin Description.....3

Table 2 Absolute Maximum Ratings4

Table 3 Handling Precautions.....4

Table 4 Device Thermal Resistances4

Table 5 Recommended Operating Conditions4

Table 6 Electrical Characteristics5

Table 7 Device Truth Table5

Table 8 Bill of Materials6

Table 9 Ordering Information.....10

Table 10 Table and Reel Data.....11

List of Figures

Figure 1 Functional Diagram1

Figure 2 SP6498C Pin Diagram (Top View).....3

Figure 3 Schematic Diagram6

Figure 4 Package Dimensions.....8

Figure 5 Solder Stencil and PCB Footprint metallization9

Figure 6 Tape and Reel Data11

1 Pin Configuration

1.1 Pin Configuration Diagram

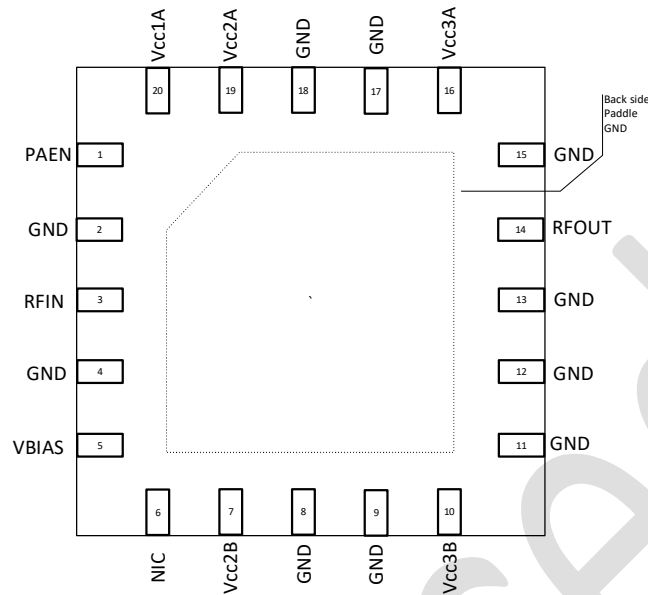


Figure 2 SP6498C Pin Diagram (Top View)

1.2 Pin Description

Table 1 Pin Description

| Name | Pin No. | I/O | Description |
|-------|-----------------|-----|---|
| PAEN | 1 | | Toggles between ON state and low power state |
| GND | 2 | | Ground connection |
| RFIN | 3 | | RF Input – Matched to 50Ω S/C to ground at DC |
| GND | 4 | | Ground connection |
| VBIAS | 5 | | Supply for bias circuit |
| NIC | 6 | | Not internally connected |
| Vcc2B | 7 | | Supply for 2 nd stage (Peaking) |
| GND | 8 | | Ground connection |
| GND | 9 | | Ground connection |
| Vcc3B | 10 | | Supply for 3 rd stage (Peaking) |
| GND | 11 | | Ground connection |
| GND | 12 | | Ground connection |
| GND | 13 | | Ground connection |
| RFOUT | 14 | | RF Output – Matched to 50Ω |
| GND | 15 | | Ground connection |
| Vcc3A | 16 | | Supply for 3 rd stage (Main) |
| GND | 17 | | Ground connection |
| GND | 18 | | Ground connection |
| Vcc2A | 19 | | Supply for 2 nd stage (Main) |
| Vcc1A | 20 | | Supply for 1 st stage |
| GND | Backside Paddle | | This is a ground connection and should be soldered directly to PCB ground |

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|------------------------------|-----|-----|-------|
| Supply Voltage | | 5.5 | V |
| Control Pin Input Voltage | | 2.8 | V |
| Peak RF Input Power CW | | TBD | dBm |
| Maximum Junction Temperature | | 150 | °C |
| Storage Temperature | -55 | 125 | °C |

Table 2 notes:

- Exceeding absolute maximum ratings may cause permanent damage. Operation should only occur within the limits specified. Operating between the maximum operating range Table 5 and the absolute maximum for extended periods may reduce the reliability of the device.

Table 3 Handling Precautions

Observe standard procedures as with other ESD-sensitive devices when handling the product. The product includes ESD protection circuitry, but precautions should be taken not to exceed the ratings specified in this table.

| Parameter | Level | Test Standard |
|----------------------------|-------|---------------|
| ESD voltage HBM, All Pins | TBD | JS-001-2017 |
| ESD voltage CDM, All pins | TBD | JS-002-2018 |
| Moisture Sensitivity Level | TBD | J-STD-020E |

Table 4 Device Thermal Resistances

| Parameter | θ_{jc} | Unit |
|-------------------------|---------------|------|
| Junction to case bottom | TBD | °C/W |

Table 5 Recommended Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|--|-------------------------|------|-----|------|-------|
| Supply Voltage (V _{CC1,2,3} , V _{BIAS}) | Vcc1, Vcc2, Vcc3, Vbias | 4.75 | 5 | 5.25 | V |
| Control Input (PA Enable) High | Vctrl | | 2 | | V |
| Control Input (PA Enable) Low | Vctrl | 0 | | 0.7 | V |
| RF Input Power, average (5G NR) | Pin | | | TBD | dBm |
| Operating Temperature Range (T _{CASE}) | Tcase | -40 | 25 | 85 | °C |

Table 6 Electrical Characteristics.
Operating conditions:
T_{case} = 25 °C, V_{cc} = V_{bias} = 5 V, Z_{in} = Z_{out} = 50 Ω, F_c = 2.593 GHz unless otherwise stated

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|------------------------|------|------|------|-------|
| Frequency | | f | 2496 | | 2690 | MHz |
| Small Signal Gain | P _{IN} = -35 dBm | S ₂₁ | | 35.5 | | dB |
| Input Return Loss | P _{IN} = -25 dBm | S ₁₁ | | 17 | | dB |
| Output Return Loss | P _{IN} = -25 dBm | S ₂₂ | | 19 | | dB |
| Reverse Isolation | P _{IN} = -25 dBm | S ₁₂ | | 70 | | dB |
| Gain @ 30dBm | P _{OUT} = 30 dBm | S _{21@30 dBm} | | 36 | | dB |
| ACLR (DPD uncorrected) | 20 MHz LTE, 8.5 dB PAR, +30 dBm av. Power | ACLR | | 31 | | dBc |
| Output Power at 3dB compression (10% Pulse) | | P _{3dB} | | 37.5 | | dBm |
| 2nd Harmonic | CW, P _{OUT} = 30 dBm | 2fo | | -66 | | dBc |
| 3rd Harmonic | CW, P _{OUT} = 30 dBm | 3fo | | -70 | | dBc |
| Power-added Efficiency | P _{OUT} = 30 dBm | PAE | | 23.5 | | % |
| PA Enable Current | V _{enable} = 2V | I _{PAEN} | | 260 | | uA |
| Quiescent Current | No RF signal | I _{CCQ} | | 290 | | mA |

Table 7 Device Truth Table

| Control Input (PA Enable) State | Device State |
|---------------------------------|---------------|
| High | Amplifier On |
| Low | Amplifier Off |

3 Example Application Diagram

For the Evaluation Board (EVB) details, including schematic, board stack-up and Gerber images please see the SP6498C Application Note.

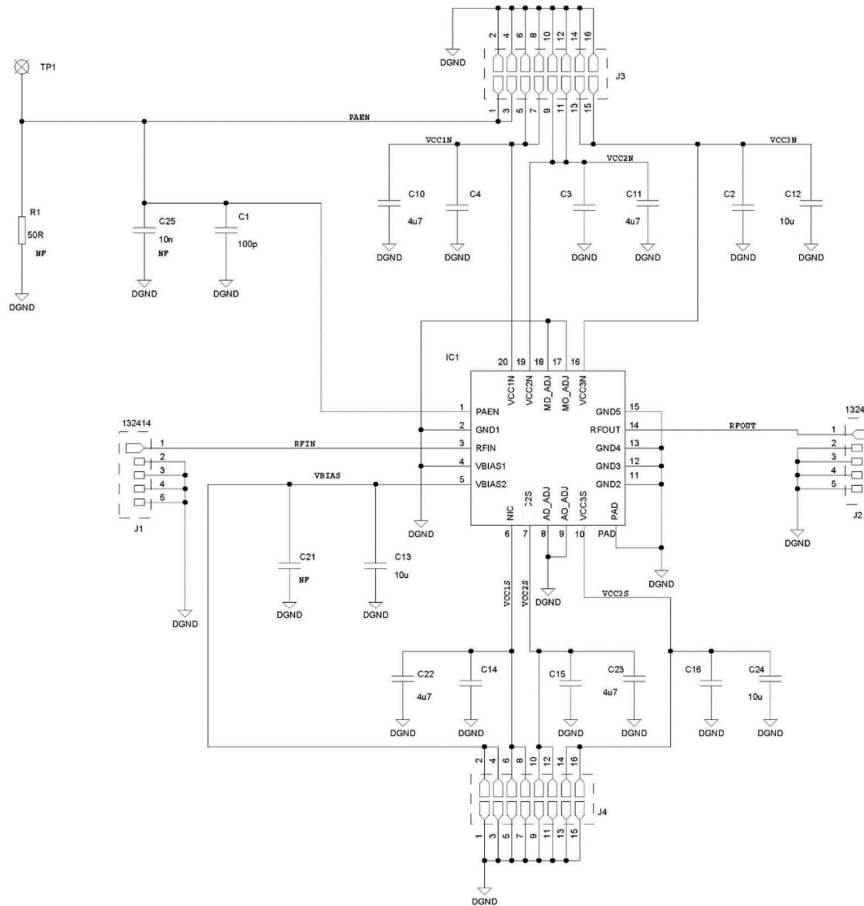


Figure 3 Schematic Diagram

Figure 3 shows the application schematic for the Spirit evaluation board. This board is used across a number of products that are footprint compatible with the SP6498C. Pin 6 is not internally connected and as such is compatible with this.

Table 8 Bill of Materials

| Reference Designator | Value | Description | Part Number | Mfr |
|------------------------|--------|-------------------|--------------------|---------------|
| C1 | 100pF | 50V, 0402, +/-5% | GCM1555C1H101JA16D | Murata |
| C15,C16 | 100nF | 50V, 0402, +/-10% | GCM155R71H104KE02D | Murata |
| C2,C3,C4 | 1uF | 16V, 0402, +/-10% | GRM155C81C105KE15D | Murata |
| C10,C11, C23 | 4.7uF | 16V, 0805, +/-10% | GRM219C81C475KA73D | Murata |
| C12,C24 | 10uF | 16V, 0805, +/-10% | GRM21BC81C106KE15L | Murata |
| C13 | 10uF | 10V, 0402, +/-20% | CL05A106MP5NUNC | Samsung |
| R1, C14, C21, C22, C25 | NF | | | |
| J1,J2 | | SMA F | 2213SM-16G-TB | Amphenol |
| J3,J4 | - | 2x8 0.1" header | 142-0701-841 | Johnson/Cinch |
| IC1 | SP6498 | | TBD | Spirit Semi |

3.1 Power-Up / Down Sequence

The device power-up sequence is as follows:

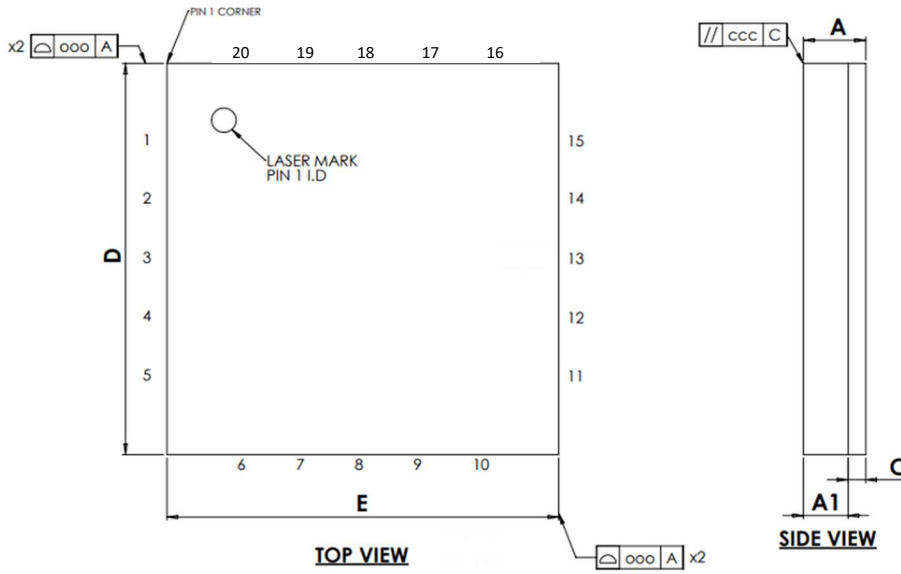
- 1) Terminate RF input and output with 50 Ohm
- 2) Connect DC ground
- 3) Ensure PA Enable is set to Low
- 4) Connect Vcc1, Vcc2, Vcc3 & Vbias to +5 V
- 5) Set PA Enable High to +2 V
- 6) Apply RF at PA Input at -30 dBm

The power-down sequence is the reverse of the power-up sequence.

It is important to ensure that ohmic losses in the power supply feed are accounted for and that the voltage at Vcc1,2,3 & Vbias are adjusted to 5.0 V at the operating condition.

Advanced

4 Package Information



| SYMBOL | MILLIMETER | | |
|--------|------------|-------|-------|
| | MIN | NOM | MAX |
| A | 1.19 | 1.25 | 1.31 |
| A1 | 1.00 BASIC | | |
| c | 0.33 | 0.36 | 0.39 |
| E | 7.90 | 8.00 | 8.10 |
| D | 7.90 | 8.00 | 8.10 |
| E1 | 4.80 BASIC | | |
| D1 | 4.80 BASIC | | |
| e | 1.20 BASIC | | |
| L1 | 0.370 | 0.420 | 0.470 |
| L2 | 0.450 | 0.500 | 0.550 |
| L3 | 0.825 | 0.875 | 0.925 |
| L4 | 0.125 REF | | |
| h1 | 0.10 REF | | |
| ooo | 0.10 | | |
| ccc | 0.08 | | |

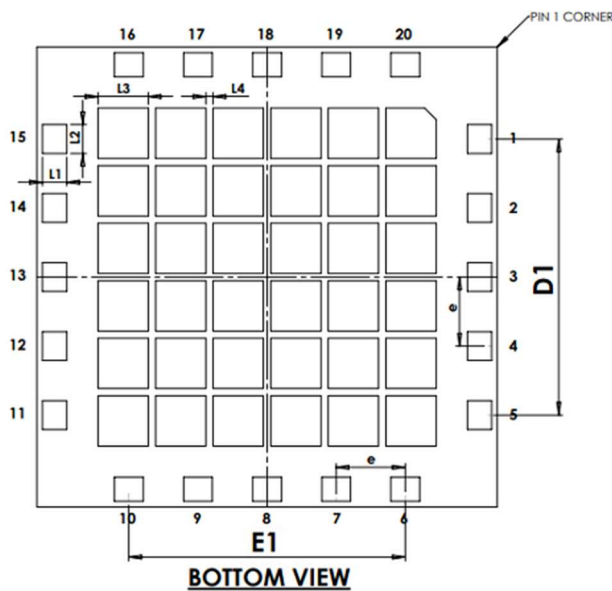
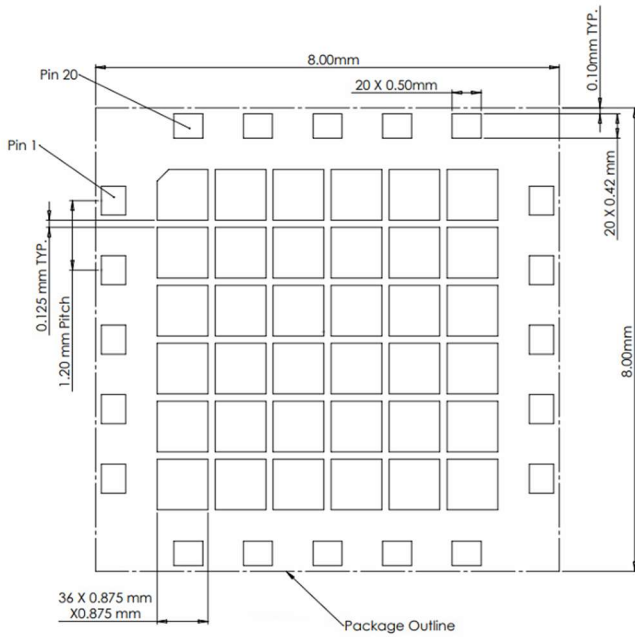
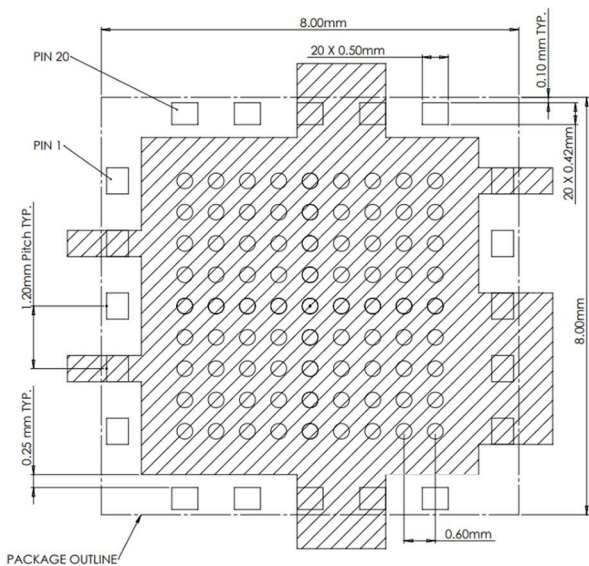


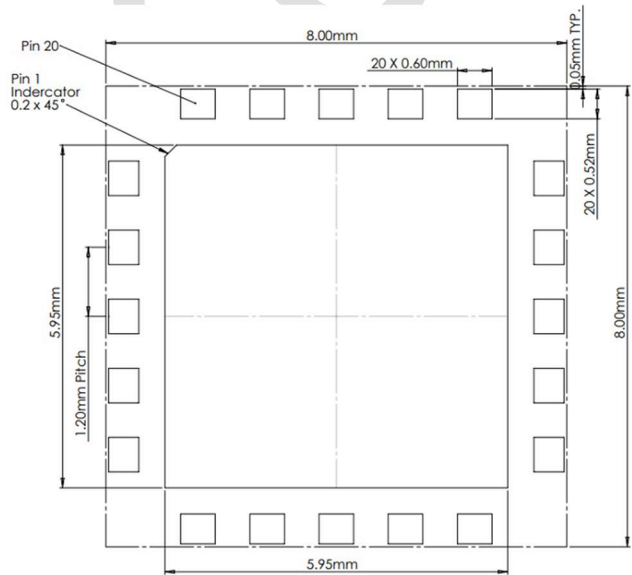
Figure 4 Package Dimensions



Stencil Aperture Top View



Metallisation Top View



Solder Mask Opening Top View

Figure 5 Solder Stencil and PCB Footprint metallization

5 Ordering Information

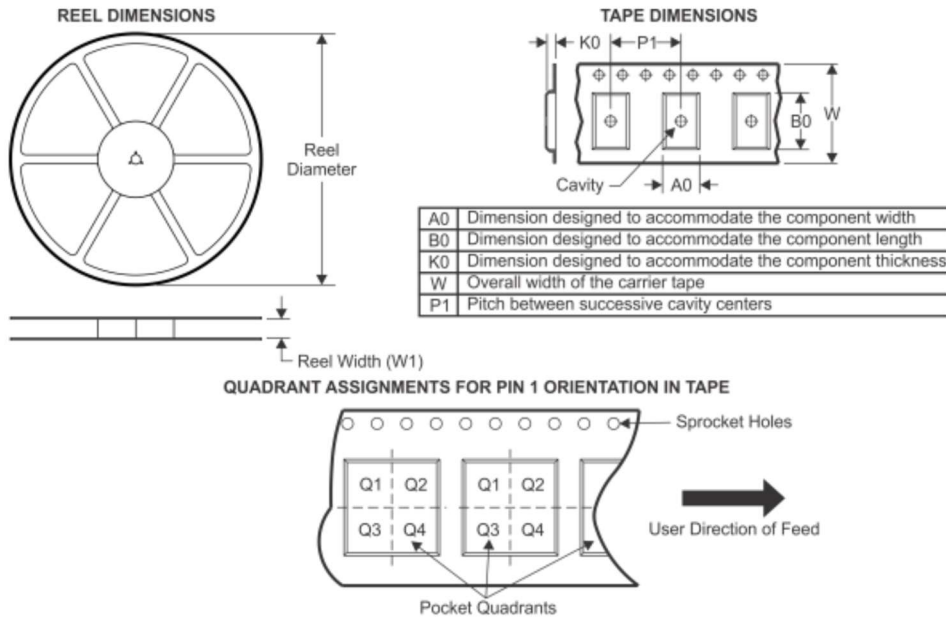
Table 9 Ordering Information

| Ordering Part Number (OPN) | Marking | Package | Shipping Package | Temperature Range | MSL Level | Ecology |
|----------------------------|---------|---------|------------------|-------------------|-----------|---------------------|
| TBC | TBC | LGA 8x8 | Tape and Reel | | 3 | RoHS ^[1] |

Notes:

1. This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

Advanced

TAPE AND REEL INFORMATION

Figure 6 Tape and Reel Data
Table 10 Table and Reel Data

| Device | Package type | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SP6498C-LMR | LGA 8x8 | 20 | TBC | TBC | TBC | TBC | TBC | TBC | TBC | TBC | Q1 |

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