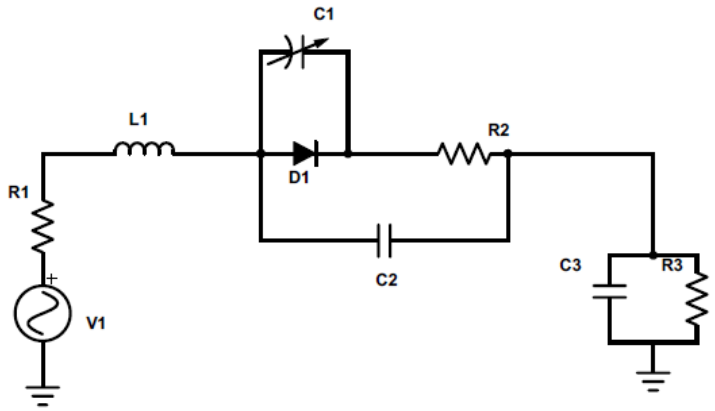
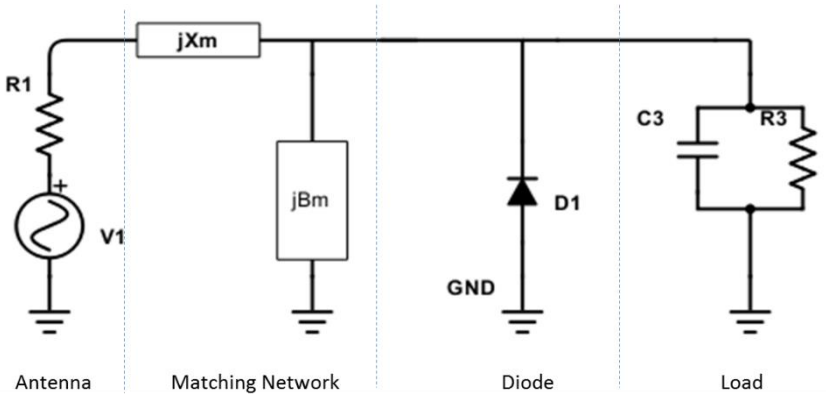
Rectifier Circuit and Impedance Matching

The equivalent circuit of the incorporation of a rectifier circuit to the antenna is shown in Figure 1. Either method of an insertion of a matching circuit or a complex conjugate impedance matched antenna can be implemented for maximizing the power delivers to the load. Both methods were experimented in [1] with a conclusion is that the power conversion efficiency may be further increased and the rectenna (rectifying antenna) size is reduced by the complex conjugate method compared to the introduction of a matching circuit method. However, the matching circuits are narrowband and at high frequency application a circuit with less element is preferred for the better loss control.




(a) D1 denotes an ideal diode, C1 is the junction capacitance, R2 is the bulk series resistance, L1 and C2 are the packaging parasitic inductance and capacitance, respectively; C3 and R3 are the load.




(b)

Fig. 1 an equivalent circuit of (a) packaged Diode with source and load; (b) an equivalent circuit of an antenna connects to a matching circuit and rectifier

The array antenna in the last section has been integrated with a rectifier circuit for power conversion efficiency measurement. The Schottky diode model MA4E2054A MACOM, a low turn on voltage at 0.24 mV to 0.34 mV, was used for implementing a full-wave Voltage

Doubler rectifier circuit. The Spice model parameters of this diode is shown in Table 1. This Schottky diodes were extensively experimented in [2] with a broadband antenna array.

| | | |
|---|---|---|
| $I_s$ | $3 \times 10^{-8}$ | A |
| $R_s$ | 11 | Ω |
| N | 1.05 | |
| TT | 0 | S |
| $C_j(0)$ | $0.13 \times 10^{-12}$ | pF |
| Cpar | $0.14 \times 10^{-12}$ | pF |
| $V_j$ | 0.40 | V |
| M | 0.50 | |
| EG | 0.69 | eV |
| BV | 5.0 | V |
| IBV | $1 \times 10^{-5}$ | A |

Table 1. Spice model parameters of MA4E2054A; Reference to Figure 1 (a) from datasheet: R2 is 12 Ohm, L1 is 1.5nH, and C2 is 0.1 pF + 0.22pF (SOD-323 package)

A Full Wave Voltage Doubler rectifier circuit was designed and integrated with a 4-element antenna array. The total input impedance of this circuit with loads was calculated for 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0 GHz and is shown in Table 2. VSWR and reflection coefficient (S11) of this circuit were also analyzed based on eq. (1) and (2) by using the characteristic impedance of the antenna for each frequency from the numerical analysis.

$$\text{Reflection coefficient, } S_{11} = \frac{(Z_L - Z_S)}{(Z_L + Z_S)} \qquad \text{eq. (1)}$$

$$\text{VSWR} = \frac{(1+S_{11})}{(1-S_{11})} \qquad \text{eq. (2)}$$

| Frequency (GHz) | Total input impedance (Z-Ohm) | S11 (dB) | VSWR |
|---|---|---|---|
| 2.0 | 50.09 - j15.98 | -6.914 | 2.644 |
| 2.5 | 46.08 - j6.68 | -11.899 | 1.681 |
| 3.0 | 43.65 + j1.27 | -12.512 | 1.621 |
| 3.5 | 42.00 + j8.29 | -11.259 | 1.753 |
| 4.0 | 40.81 + j14.67 | -10.666 | 1.828 |
| 4.5 | 39.86 + j20.61 | -10.511 | 1.850 |
| 5.0 | 39.00 + j26.22 | -10.612 | 1.836 |
| 5.5 | 38.37 + j31.61 | -12.168 | 1.654 |
| 6.0 | 37.72 + j36.82 | -9.948 | 1.933 |
| 6.5 | 37.12 + j41.91 | -7.846 | 2.363 |
| 7.0 | 36.54 + j46.90 | -8.959 | 2.108 |

Table 2. S11 and VSWR calculations for an array antenna incorporates rectifying diodes

**References:**

1. Hubregt J. Visser, Shady Keyrouz and A. B. Smolders.:'Optimized rectenna design', Wireless Power Transfer, Cambridge University Press, 2015, 2(1), 44-50

2. Joseph A. Hagerty, Nestor D. Lopez, Branko Popovic, and Zoya Popovic. :'Broadband Rectenna Arrays for Randomly Polarized Incident Waves', Department of Electrical and Computer Engineering, University of Colorado Boulder, CO 80309-0425 USA