Advanced Tech Engineering
Where Technical Performance & Integrity Matters

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DARPA Phase II SBIR Project Title/Number: Highly Integrated Silicon Based RF Electronics / SB082-044
Period of Performance: 26 April 2010 - 25 June 2012

Project Summary:
The overarching technical objective of our Phase II work is to develop disruptive and transformative RF technologies and radar techniques that results in new or advanced capabilities, enhanced performance, and at least and at least 10x reduction in cost, size, weight, and power (CSwaP) of silicon based RF electronic over contemporary type III-V technologies for emerging MIMO radar, Wideband AESA radars, communications and other RF sensor applications.

- A scalable, T/R module-on-a-chip for future generation MIMO radar, wideband AESA radar, digital radar, RF communications, RF sensors and current generation high performance LPD/LPI communications.
- Inherently resistant to jamming (multi-mode, multi-frequency - through and including 30 GHz, 2 GHz BW
- Delivers greater capability and performance over current systems with at a fraction of the cost, size, weight and power
- Ideal for UAV/UAS, SWaP constrained and other private sector applications

Radar applications are more demanding than conventional wireless communication systems in terms of system transmit power; receive linearity and noise-figure. The latter parameters govern the jammer-handling capability, and the dynamic range of the radar. During the Phase I work, we've shown that silicon is clearly capable of achieving or exceeding performance to their III-V counterparts, at reduced cost, and at much higher levels of integration for distinct radar scenario that were evaluated at 8, 10, 15 and 30 GHz. From Figure **1,** ATEIs MIMO multi-carrier STAR technique shows that the required transmit power is reduced as much as 40 dB as compared to modern AESA radar which is significant! This significant reduction in power enabled the use of si-based technologies for emerging MIMO or wideband AESA radar applications.

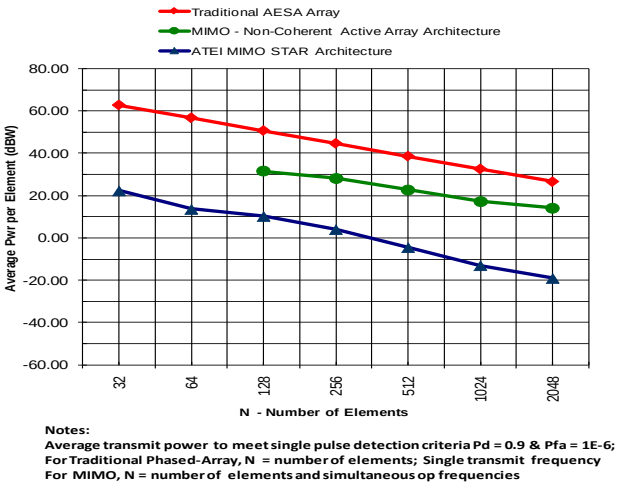


Figure 1 ATEI MIMO STAR Vs. Traditional AESA Radar - Avg Pwr per Element Vs Number of Elements based on Single Pulse Detection Criteria

In Phase II, we focused our efforts on scenario 3, Missile RF Seekers and UAS RF sensors and applications operating over 28-30 GHz bandwidth. Figure 2 shows an operational view (OV) used to derive MIMO radar performance requirements and front end RF/IF architecture for an all silicon RF front end or building block for longer range applications shown in Figure 3. This operational band and associated applications were chosen for the following considerations: Higher chip level integration of RF signal electronics vs. what's achievable/required at lower operating frequencies; Possibility of expanding to wafer-scale implementation; Improved radar performance and capabilities (e.g. multi-target separation, target angular accuracy, SAR resolution, High resolution radar (HRR), simultaneous multi-mode ops); Significant reductions in SWaP which enables radars, comms and RF sensor payloads ideal for small and SWaP constrained UAV applications; and exploitation of the lack of radar development in this band. All these considerations enhances our beyond Phase II transition and commercialization opportunities.

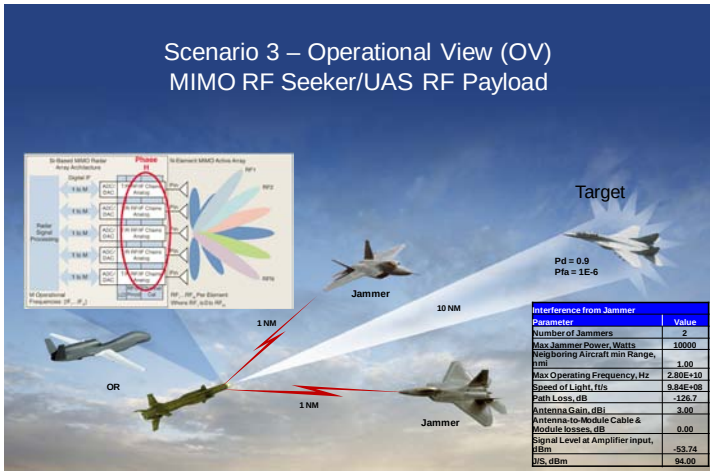


Figure 2 Scenario 3 - Operational View of MIMO RF Seeker or UAS RF Payload

In year 1 of the two-year phase II program, our work primarily focused on top-level MIMO radar system prediction models and requirements; MIMO radar front-end system architecture, analysis, and simulations; MIMO radar front-end circuit block requirements; and RFIC design and layout of key circuits. At the end of Phase II, ATEI fabricated and tested prototype RFIC chips and validated system performance predicts, RF architecture and key circuit level parameters. Specifically, we established or demonstrated the following: Capability of SiGe circuits to meet the stringent receiver IIP3 and NF specifications for radar applications; Capability of SiGe circuits to transmit linear combinations of N frequencies per element

while meeting minimum power per carrier and distorted SNR objectives to be defined in phase II; Superiority of the MIMO radar over traditional AESA (e.g., exploitation of targets through multi-carrier simultaneous transmit and receive techniques achieving high detection probability with low SNR per carrier or frequency); and Conceptual integration of key RF and baseband blocks of the radar's transmit and receive sections into a single SiGe chip, which later could be expanded to a full wafer-scale array radar

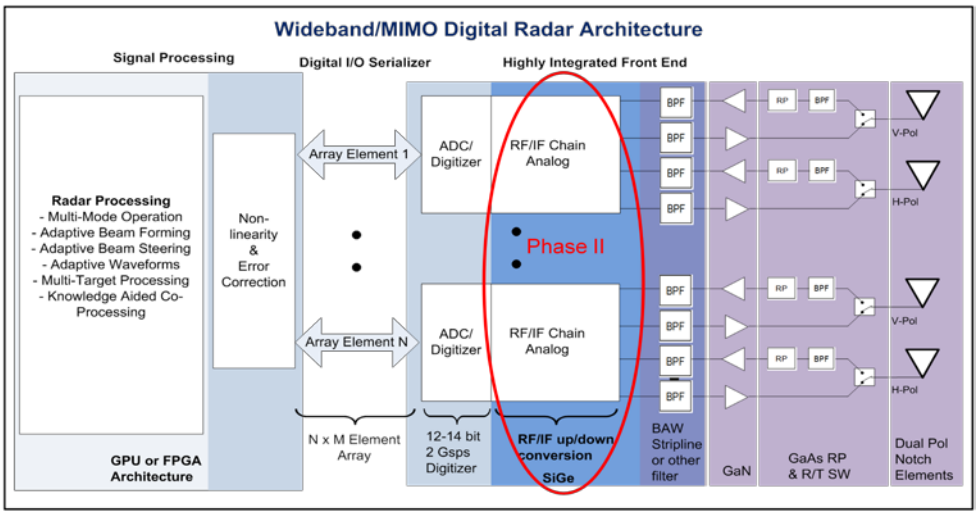
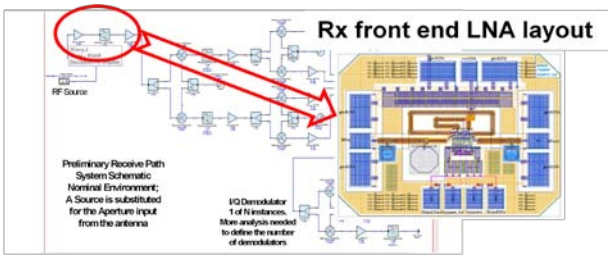
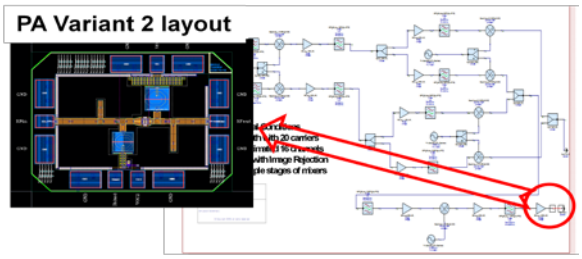


Figure 3 Objective Architecture Technology Map

Phase II project funds was insufficient to support comprehensive circuit design for the entire Rx/Tx RF Front End (RFFE). Key RFIC blocks were chosen to implement and fabricate. Key Tx RFIC includes the PA block since the achievable output power affects the entire system design and it is difficult to predict realistic performance limits. Doing this design work up front allows us to better optimize the Tx path based on realistic output powers and linearity. Key Rx RFIC includes the two stage LNA front end blocks. These blocks include the LNA, a band pass filter and an isolation amp. This block will also include an input gain switch to increase the usable signal range. These blocks were chosen because the achievable performance of this cascade is difficult to predict and strongly affects the overall performance of the Rx path. A total of 7 test chips were built and tested (total of 40 bare die received from IBM) which includes 3 transmit PA designs and 4 Rx frontend test chips. Full S-parameter data was collected for all the test chips

As of July 2012, the current statement of development of ATEI's Highly Integrated Silicon Based RF Electronics is as follows: Critical Tx & Rx circuit blocks designed/ fab/tested; Ka-band Rx Front End 2-stage LNA and Tx PA characterized; Fabrication and testing self funded (2nd year Phase II Option); TRL of critical Tx and Rx circuit blocks: 4-5 (see Figure 4 below); and TRL of complete RFFE Architecture: 3-4.





LNA	High Gain		Low Gain		units
	spec	simulated test chip perf.	spec	measured	
Gain	30	32.4	10	6	dB
NF	3.5	3.45	15	5 ±1.5	dB
IP1dB	-30	-26.6	-5	+1	dBm
IIP3	-20	-18	5	14	dBm
S11	< -10	-15	< -10	-20.2	dB
S22	< -10	-13.5	< -10	-15.8	dB

Power Amplifier Variant 2				
PA Parameter	Spec / Goal	Simulated Test Chip Perf	Measured	units
Small Signal Gain	15	8.9	8	dB
1 dB Compression Gain	15	7.9	7	dB
Output 1 dBCP	15 (20)	14.8	17	dBm
OIP3	25 (30)	27.5	31.7	dBm
S11	< -10	-17	-30	dB
S22	< -10	-15	-15	dB

Figure 4 Critical or Key 28-30 GHz RFIC Circuit Blocks Simulated, Fabricated and Tested

ATEI continues to seek additional funding to support development of this disruptive and transformational technology.