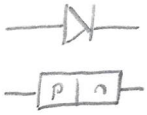
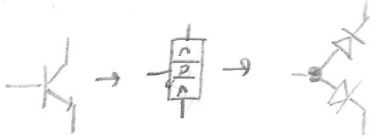
Bipolar Transistors

kind of like two diodes. (it's NPN, after all!)

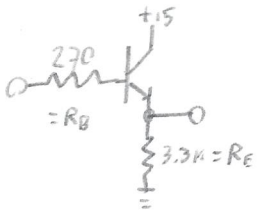
diode: 

BJT: 

So: $V_{BE} \sim$  $\sim 0.6V$

& $I_E = (1+\beta)\, I_C$ where β is the Current Gain. (h_{FE} in datasheets)

Emitter-Follower (8.2-8.3)



$V_{out} = I_E R_E = (1+\beta)\, I_C R_E$

$V_{out} + 0.6V + I_C R_B = V_{in} \Rightarrow \left[(1+\beta)R_E + R_B\right] I_C = V_{in} - 0.6V$

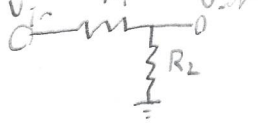
$$I_C = \frac{V_{in} - 0.6V}{\left[(1+\beta)R_E + R_B\right]} \Rightarrow V_{out} = (V_{in} - 0.6V)\left[1 + \frac{R_B}{R_E}(1+\beta)^{-1}\right]$$

$$\simeq (V_{in} - 0.6V)\left[1 + \mathcal{O}(1/\beta)\right] \simeq V_{in} - 0.6V.$$

($R_B/R_E < 1$ as well).

Impedances of Circuits

First, a refresher. Input impedance is impedance between V_{in} & all "grounds" (can be $V_{EE} \neq 0$). Output impedance is between output terminal & all inputs/references.

Ex. 

$Z_{in} = R_1 + R_2$

$Z_{out} = R_1 \| R_2 = \left(1/R_1 + 1/R_2\right)^{-1}$.

Also remember it can be thought of as $\Delta V/\Delta I$ as a test load is applied.

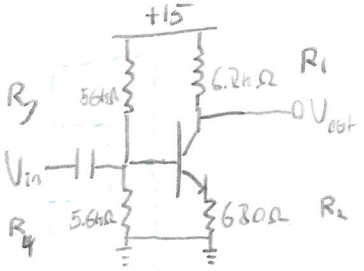
Applying impedances to transistor circuits

$$Z_{in} = V_B/I_B = V_{BE} + \frac{I_E R_E}{I_B} \simeq R_E(1+\beta) \quad \Rightarrow \quad Z_{in}/Z_{out} \sim \beta^2.$$

$$Z_{out} = V_E/I_E = \frac{I_B R_B}{I_E} - V_{BE} \simeq R_B(1+\beta)^{-1}$$

This is a good way to check your impedances and confirm your measured gain.

Common Emitter-Amplifier (8.5)



bias network

$V_{out} = 15V - I_c R_1$.

$I_c = \beta I_B$

$V_B = 15V \frac{R_4}{R_2+R_4} + V_{in}$

Solve just like 8.2.

Note the capacitor just eliminates offsets and (& protects F.G. from the bias network.)

System-wide feedback (8.6)

This brings "information" about the effects of the push-pull on the output back to the op-amp. You don't need to solve this explicitly, but it might be good practice for the final exam.