WinSystems®

The Embedded Systems Authority

PCM-C418

PC/104 Single Board Computer with Vortex86DX3 Processor

Product Manual

WinSystems, Inc. | 715 Stadium Drive, Arlington, Texas 76011 | 817-274-7553 | info@winsystems.com | www.winsystems.com

Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	9/29/17	Initial release
v1.1	12/8/17	Various edits

Copyright and Trademarks

Trademark Acknowledgments

Table of Contents

1 Before You Begin 5

1.1 Warnings 5

2 Introduction 5

3 Functionality 5

3.1 System 5

3.2 Memory 6

4 Features 6

5 Specifications 8

6 Configuration 10

6.1 Component Layout 10

6.1.1 Top View 10

6.1.2 Bottom View 12

6.1.3 Jumper Reference 13

6.2 I/O Port Map 13

6.3 Interrupt Map 15

6.4 DMA Map 16

6.5 Memory Map 16

6.6 Watchdog Timer 16

6.6.1 Advanced 17

6.6.2 Legacy 17

6.7 Real-time Clock/Calendar 18

6.8 Connectors 18

6.8.1 Power - ATPWRIN1 18

6.8.2 BAT1 - External, Battery Backup 19

6.8.3 BZ1 - Buzzer 19

6.8.4 MS1 - Mouse 20

6.8.5 MIO1 - Multi-I/O (COM1, COM2, Keyboard, LPT) Interface 21

6.8.6 VGA1 Analog Connector 26

6.8.7 Serial Interface - COM3, COM4 27

6.8.8 USB1 - USB 30

6.8.9 SATA Serial ATA (SATA) 31

6.8.10 PWROUT1 - SATA Power 31

6.8.11 CFD1 - CompactFlash 31

6.8.12 1 MB SRAM (Battery-backed User Data Space) . . . 32
6.8.13 LAN1 - 10/100 Mbps Ethernet . . . 34
6.8.14 LAN2 - 10/100/1000 Mbps Ethernet . . . 35
6.8.15 LED4 - User Controlled Status LED . . . 36
6.8.16 LED6 - Power Indicator LED . . . 36
6.8.17 DIO1 - Digital I/O . . . 36
6.8.18 CON1 and CON2 - PC/104 Bus . . . 37

7 BIOS Supplemental . . . 39

7.1 General Information . . . 39
7.2 Entering Setup . . . 39
7.3 Navigating the Menus . . . 39
7.4 BIOS Setting Storage Options . . . 47
7.4.1 CMOS Storage Locations . . . 47
7.4.2 Saving the CMOS Configuration . . . 47
7.4.3 Updating the BIOS FLASH PROM . . . 48

8 Cables and Batteries . . . 48

9 Software Drivers . . . 49

A Best Practices . . . 50

B Mechanical Drawings . . . 53

C Power-on Self-Test (POST) Codes . . . 55

D Warranty Information . . . 58

1. Before You Begin

Review the warnings in this section and the best practice recommendations (see “Best Practices” on page 50) when using and handling the WinSystems PCM-C418. Following these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the PCM-C418 before proceeding.

FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PCM-C418 AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the PCM-C418.

Please review the section “Best Practices” on page 50 and the other guidelines in this manual carefully and follow them to ensure you are successfully using your embedded PC.

This product ships with a heat sink. The product warranty is void if the heat sink is removed from the product.

2. Introduction

This manual provides configuration and usage information for the PCM-C418 single board computer. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WinSystems website for other accessories (including cable drawings and pinouts) that can be used with your PCM-C418.

3. Functionality

3.1 System

The PCM-C418 is a fan-less PC/104 single board computer (SBC) based on the low power Vortex86DX3 processor. It requires approximately 7 Watts under full load while operating over an extended temperature range of -40 to 85°C. The board has 2 GB soldered-on DDR3 SDRAM, Ethernet, USB, serial and parallel I/O, DIO, PC/104, and an optional external battery. The PCM-C418 provides an upgrade path for WinSystems'

PCM-VDX product line and other PC/104 applications requiring low power CPU with full ISA support.

3.2 Memory

The PCM-C418 board is built with 2 GB of SDRAM soldered directly to the PCB. 1 MB of battery-backed SRAM is included for user data space. When an external battery is connected, this SRAM is battery backed to maintain data integrity during power off conditions.

4. Features

The PCM-C418 provides the following features.

CPU

- DM&P 1 GHz Vortex DX3 SOC

Compatible Operating Systems

- Windows Embedded 7 (WES7)
- Linux
- DOS
- Other x86 RTOS

Memory

- 1 MB SRAM (battery-backed user data space)
- 2 GB of DDR3 SDRAM (soldered)

BIOS

- AMI

Ethernet

- One 10/100 Mbps (Vortex86DX LAN)
- One 10/100/1000 Mbps (Intel I210)

Storage

- One PATA CompactFlash socket
- Optional eMMC up to 64 GB (requires minimum order)
- One SATA channel

Digital I/O

- 24 bidirectional 5V I/O lines capable of event sense and interrupt generation

Serial I/O

- Four serial ports (RS-232/422/485)

Bus Expansion

- PC/104

Line Printer Port

- Bidirectional (SPP/ECP/EPP)

USB

- Four USB 2.0 ports with ESD suppression

VGA

- Single VGA output with resolutions up to 1920x1440

Watchdog Timer

- Up to 255 minute reset

CompactFlash

- Types I and II

Power

- +5V required, 1.5A typical

Industrial Operating Temperature

- -40 to +85°C (-40 to +185°F)

Form Factor

- 3.60 x 3.80” (90 x 96 mm)

Additional Features

- RoHS compliant
- Real-time clock
- Activity status LEDs on-board
- PS/2 keyboard and mouse supported

5. Specifications

The PCM-C418 adheres to the following specifications and requirements.

Table 1: Specifications

Feature	Specification
Electrical Specifications	
Model description	PCM-C418 PC/104-*Plus* single board computer
Processor	1-GHz Vortex DX3 SOC
Power	+5V DC +/- 5% Max: 1.5A Typical: 1.2A
PC/104 Interface	16-bit, stackthrough
Ethernet data rate	• Intel i210 - 10/100/1000 Mbps controller • Vortex 10/100 Mbps controller
USB interface	Four USB 2.0 ports
Serial interface	Four serial channels all with RS-232/422/485 transceiver levels
General purpose input/output (GPIO)	24 bidirectional I/O lines, 5V tolerant, with 12mA sink and 1mA source capability
VGA	Up to 1920x1440 resolution
LPT interface	Bidirectional (SPP/ECP/EPP)
SATA interface	Supports one serial ATA 1.0 channel
Keyboard	Standard PS/2 or USB interface
Mouse	Standard PS/2 or USB interface
System Memory	
Capacity	2 GB DDR3 RAM soldered
Solid state disk device	One Type I/II CompactFlash card

Table 1: Specifications (Continued)

Feature	Specification
Mechanical Specifications	
Dimensions	3.6 x 3.8 inches (90 x 96 mm)
Weight	6.4 oz (182 g) with spreader / 9.76 oz (277 g) with heatsink
Board thickness	0.078 inches
Environmental Specifications	
Temperature	Operational from -40 to +85°C (-40 to +185°F) with heat spreader (200 LFM airflow) Operational from -40 to +85°C (-40 to +185°F) with additional heat sink (still air)
Humidity (RH)	5% to 95% non-condensing
Mechanical shock testing	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis
Random vibration testing	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis
RoHS compliant	Yes
MTBF	46962 hours based on Bellcore TR-332 Issue 6 at 55°C, ground benign environment.
Operating Systems	
Runs Linux, DOS, Windows Embedded 7, and other x86-compatible operating systems	

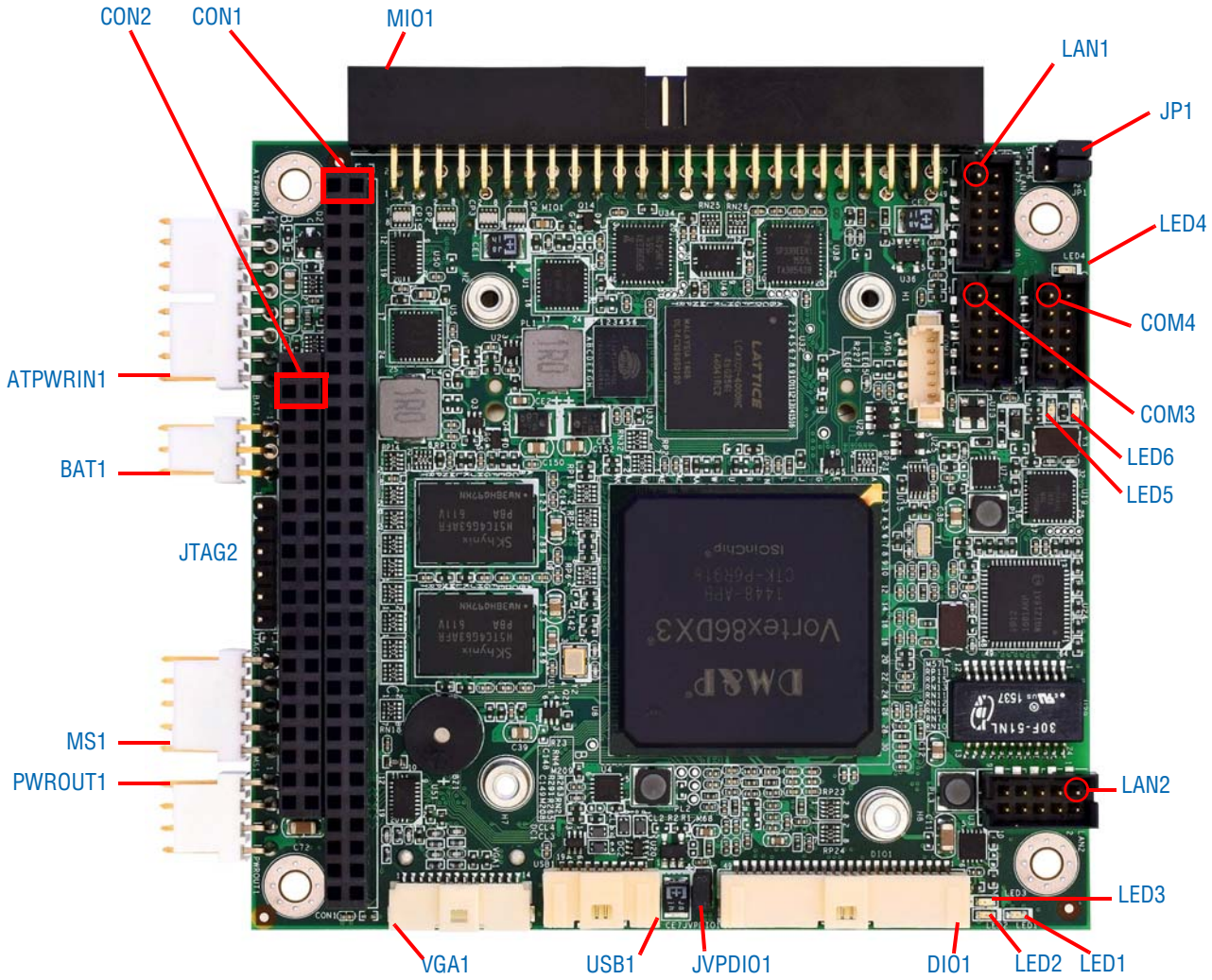
6. Configuration

This section describes the PCM-C418 components and configuration.

6.1 Component Layout

The PCM-C418 provides components on the top and bottom of the board.

6.1.1 Top View



NOTE The reference line to each component part has been drawn to Pin 1, and is also highlighted with a circle, where applicable.

Table 2: Top view components

Item	Reference
ATPWRIN1 - Power connector	page 18
BAT1 - External, battery backup	page 19
BZ1 - Buzzer/Speaker	page 19
MS1 - PS/2 Mouse	page 20
MIO1 - Multi-I/O (COM1, COM2, Keyboard, LPT)	page 21
COM3, COM4 - Serial interfaces	page 27
USB1 - USB 2.0 channels	page 30
LAN1 - 10/100 Mbps Ethernet	page 34
LAN2 - 10/100/1000 Mbps Ethernet	page 34
DIO1 - Digital I/O	page 36
CON1, CON2 - PC/104 bus	page 37
JP1 - Boot delay without optional battery	page 13
JVPDIO1 - Voltage jumper for DIO	page 13
JTAG - Reserved	page 13
VGA1 - Analog VGA connector	page 26
PWROUT1 - SATA power	page 31
LED1 = GRN = LAN2 activity	page 35
LED2 = YEL = LAN2 speed 100	page 35
LED3 = RED = LAN2 speed 1000	page 35
LED4 = RED = Status LED	page 36
LED5 = RED = CFlash activity	page 31
LED6 = GRN = Power applied	page 36

6.1.2 Bottom View

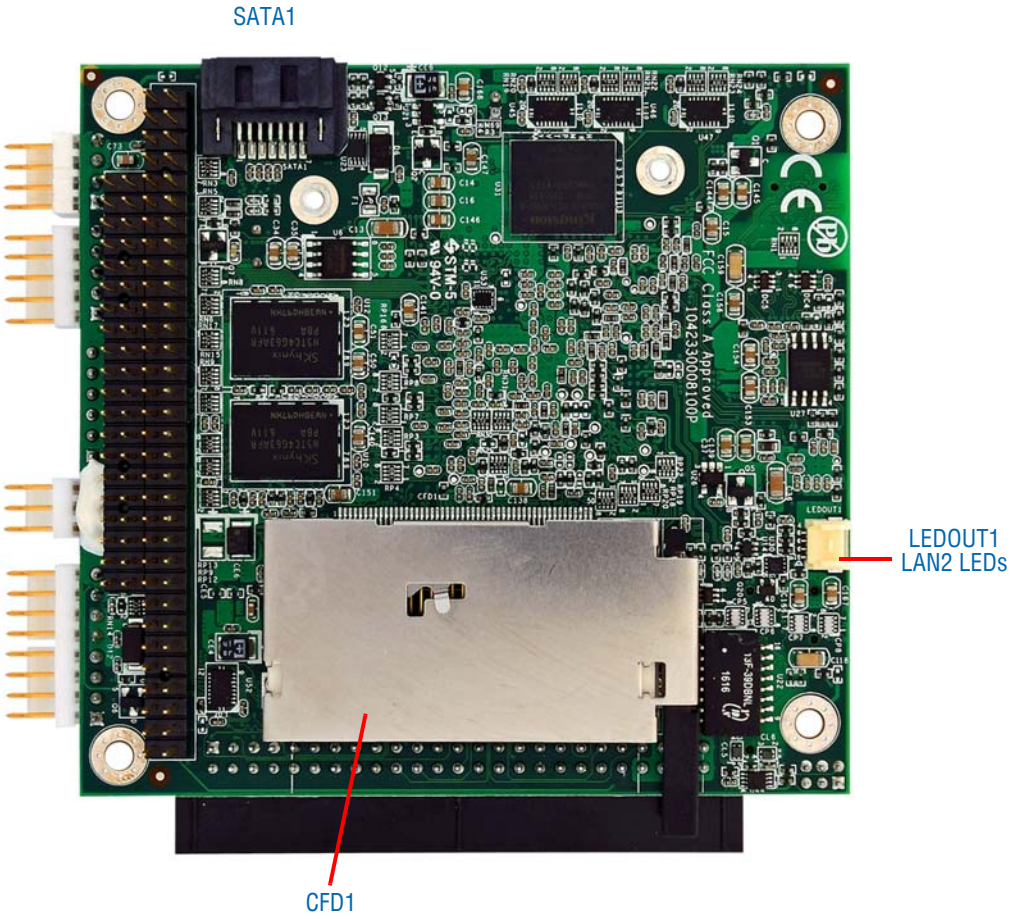


Table 3: Bottom view components

Item	Reference
SATA1 - Serial ATA (SATA)	page 31
LEDOUT1 - LAN2 Ethernet indicators	page 36
CFD1 - CompactFlash	page 31

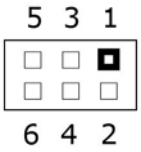
6.1.3 Jumper Reference

NOTE Jumper part# SAMTEC 2SN-BK-G is applicable to all jumpers. These are available in a ten-piece kit from WinSystems (Part# KIT-JMP-G-200).

JP1 - Boot Delay/JTAG

JP1 delays the boot by 6 seconds. It should be installed when no CMOS battery is connected.

Table 4: JP1 reference

	Default	Description
	1-3 (Default)	Battery installed - 0s delay
	3-5	No battery - 6s boot delay
	2-4 (Default)	Reserved
	4-6	Reserved

JVPDIO1 - Power Jumper for DIO

JVPDIO1 connects 5V to pin 49 of the DIO connector labeled **DIO1**.

6.2 I/O Port Map

Following is a list of I/O ports for the PCM-C418.

NOTE The PCM-C418 uses a PnP BIOS resource allocation. Take care to avoid contention with resources allocated by the BIOS.

Table 5: I/O ports

Hex Range	Usage
0000h-000Fh	DMA 8237-1
0010h-0017h	Reserved redundancy
0018h-001Fh	Free
0020h-0021h	PIC 8259-1
0022h-03Fh	Reserved
0040h-0043h	Timer counter 8254
0044h-0047h	Free
0048h-004Bh	PWM counter 8254
004Ch-004Dh	Free
004Eh-004Fh	Reserved for onboard configuration
0050h-005Fh	Free
0060h-006Fh	8042 keyboard/mouse controller
0070h-007Fh	CMOS RAM
0080h-008Fh	DMA page register

Table 5: I/O ports (Continued)

Hex Range	Usage
00A0h-00BFh	PIC 8259-2
00C0h-00DFh	DMA 8237-2
00E0h-00EFh	DOS/4G 32-bit DOS extender registers
0F0 - 0F1	Math co-processor control
0F2 - 0F7	Free
0F8 - 0FF	Math co-processor
0100h-0102h	Video controllers
0103h-011Fh	Free
0120h-012Fh	Digital IO (default)
1D0 - 1DF	Legacy watchdog
01E8h-01EBh	Reserved for onboard configuration
1EC	Interrupt status register
01EDh	Status LED
01EEh-01EFh	Watchdog timer control (legacy)
01F0h-01FF	IDE0 (IRQ 14)
0200h-0219h	Free
0220h-0227h	1 MB SRAM (battery-backed user data space)
0228h-0277h	Free
02B0h-02DFh	Video controllers (typically reserved, video)
02E0h-02E7h	Free
02E8h-02EFh	COM4 (IRQ6) (default)
02F0h-02F7h	Free
02F8h-02FFh	COM2 (IRQ3) (default)
0300h-0375h	Free
0376h	IDE1 ATAPI device control write only register
0378h-037Bh	LPT default (IRQ7, DM0) (default)
037Ch-03AFh	Free
03B0h-03BBh	Video controllers (typically reserved, video)
03C0h-03DFh	Video controllers (typically reserved, video)
03E0h-03E7h	Free
03E8h-03EFh	COM3 (IRQ5) (default)
03F0h-03F7h	Free
03F8h-03FFh	COM1 (IRQ4) (default)
04D0h-04D1h	8259 Edge/level control register
0564h-0568h	Advanced watchdog
0CF8h-0CFFh	PCI configuration port

6.3 Interrupt Map

Hardware interrupts (IRQs) are supported for both PC/104 (ISA) and PCIe devices. The user must reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS uses unreserved IRQs when allocating resources during the boot process. The table below lists IRQ resources as used by the PCM-C418.

Table 6: IRQ resources

IRQ	Device
IRQ0	18.2 Hz heartbeat
IRQ1	Keyboard
IRQ2	Chained to slave controller (IRQ9)
IRQ3	COM2
IRQ4	COM1
IRQ5	COM3
IRQ6	COM4
IRQ7	LPT
IRQ8	Real-time clock
IRQ9	Free
IRQ10	Digital I/O
IRQ11	Free
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	IDE
IRQ15	Free
These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the PCI Configurations section under Advanced Settings. Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.	

6.4 DMA Map

Table 7: DMA resources

DMA#	Description	Usage
DMA0	Available	
DMA1	Available	
DMA2	Available	
DMA3	Available	
DMA4	Available	
DMA5	Available	
DMA6	Available	
DMA7	Available	

6.5 Memory Map

Table 8: HEX ranges

HEX Range	Usage
0000:0000-9000:FFFF	System RAM
A000:0000-A000:FFFF	EGA/VGA video memory
B000:0000-B000:7FFF	MDA RAM, Hercules graphics display RAM
B000:8000-B000:FFFF	CGA display RAM
C000:0000-C000:7FFF	EGA/VGA BIOS ROM
C000:8000-C000:FFFF	Boot ROM enable
D000:0000-D700:FFFF	Expansion ROM space
D800:0000-DB00:FFFF	SPI FLASH emulation floppy A enable
DC00:0000-DF00:FFFF	Expansion ROM space
E000:0000-E000:FFFF	USB Legacy SCSI ROM space
F000:0000-F000:FFFF	Motherboard BIOS

6.6 Watchdog Timer

The PCM-C418 features an advanced watchdog timer that can be used to guard against software lockups. Two interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other interface option is provided for software compatibility with older WinSystems single-board computers.

6.6.1 Advanced

Enable the watchdog timer in the BIOS Settings by entering a value for Watchdog Timeout on the Chipset > SouthBridge Configuration screen. When the operating system is loaded, disable or reconfigure the watchdog in the application software.

NOTE WinSystems recommends using a long timeout if the watchdog is enabled when trying to boot any operating system.

Enable, disable, or reset the watchdog by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. Enable the watchdog by writing a timeout value other than zero to the I/O address 566h and disable it by writing 00h to this I/O address. Service the watchdog timer by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

Set the timeout value from 1 second to 255 minutes. If port 565h bit 7 equals **0**, the timeout value written into I/O address 566h is in minutes. The timeout value written to address 566h is in seconds if port 565 bit 7 equals **1**.

Table 9: Watchdog timer examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565H	x	566H	00h	Disabled
565H	1	566H	03h	3 seconds
565H	1	566H	1Eh	30 seconds
565H	0	566H	04h	4 minutes
565H	0	566H	05h	5 minutes

6.6.2 Legacy

Software watchdog timer PET = PORT 566H, write the timeout value.

The Legacy watchdog timer interface is provided for legacy software support only and is not recommended for new development.

Enable or disable the watchdog via software by writing an appropriate timeout value to I/O port 1EEH. See the chart provided below.

Table 10: Timeout values

Port Address	Value	Reset Interval
1EEH	00h 01h	Disabled 2 seconds
1EFH	Any	Reset timer

6.7 Real-time Clock/Calendar

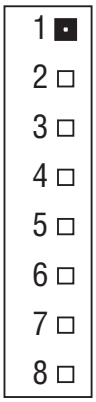
A real-time clock is used as the AT-compatible clock/calendar. The clock supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be installed for the real-time clock to retain time and date during a power down.

6.8 Connectors

6.8.1 Power - ATPWRIN1

Power is applied to the PCM-C418 via the connector at **ATPWRIN1**. The pins are listed in the table below. WinSystems offers the cable **CBL-174-G-1-1.5** to simplify this connection.

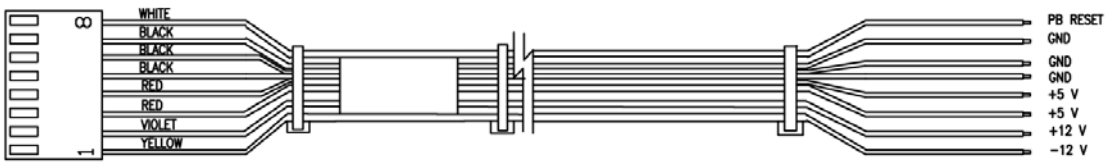
Layout and Pin Reference

ATPWRIN1	Pin	Name
	1	-12V
	2	+12V
	3	+5V
	4	+5V
	5	GND
	6	GND
	7	GND
	8	PBRESET

Connectors

- PCB connector: Molex 22-12-2084 (J4)
- Mating connector: Molex 10-11-2083 (housing)
- Mating connector: Molex 08-55-0124 (crimp)

CBL-174-G-1-1.5 Cable

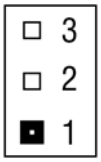


6.8.2 BAT1 - External, Battery Backup

An optional external battery, connected at **BAT1**, supplies the PCM-C418 board with standby power for the real-time clock, SRAM, and CMOS setup RAM. An extended temperature lithium battery capable of backing up these functions on the PCM-C418 is available from WinSystems, part number BAT-LTC-E-36-16-1 (or BAT-LTC-E-36-27-1 if applicable).

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the V_{CC} of the systems drops below the battery voltage and back OFF again when V_{CC} returns to normal.

Layout and Pin Reference

BAT1	Pin	Name
	1	GND
	2	+VBAT
	3	NC

Connectors

- PCB connector: Molex 22-12-2034
- Mating connector: Molex 22-01-3037 (housing)
- Mating connector: Molex 08-55-0109 (crimp)

WinSystems battery BAT-LTC-E-36-16-1 (or BAT-LTC-E-36-27-1) simplifies the connections to the board.

BAT-LTC-E-36-16-1

BAT-LTC-E-36-27-1

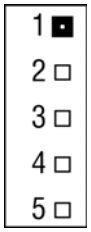
6.8.3 BZ1 - Buzzer

An on-board piezo buzzer, **BZ1**, is available for sound generation.

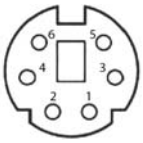
6.8.4 MS1 - Mouse

A PS/2 mouse port provides connection for a compatible mouse and is terminated at connector **MS1**. An adapter cable, CBL-343-G-1-1.375, is available from WinSystems to simplify the connection. Optionally, a USB mouse can be connected in addition to, or instead of the standard PS/2 mouse. The pinout for the cable is listed below.

Layout and Pin Reference

MS1	Pin	Description
	1	MSDATA
	2	NC
	3	GND
	4	V_{CC}
	5	MSCLK

Layout and Pin Reference

CBL-343-G-1-1.375	Pin	Description
	1	MSDATA
	2	NC
	3	GND
	4	V_{CC}
	5	MSCLK
	6	NC

CBL-343-G-1-1.375 Cable

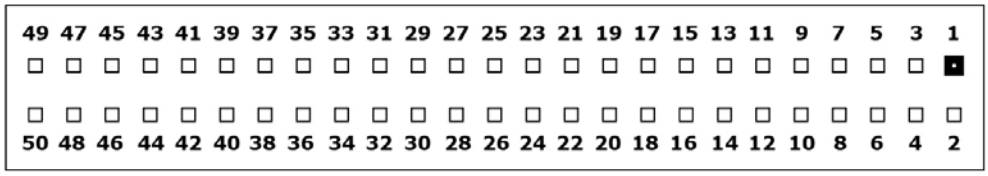
Connectors

- PCB connector: Molex 22-12-2054
- Mating connector: Molex 22-01-2057 (housing)
- Mating connector: Molex 08-55-0102 (crimp)

6.8.5 MIO1 - Multi-I/O (COM1, COM2, Keyboard, LPT) Interface

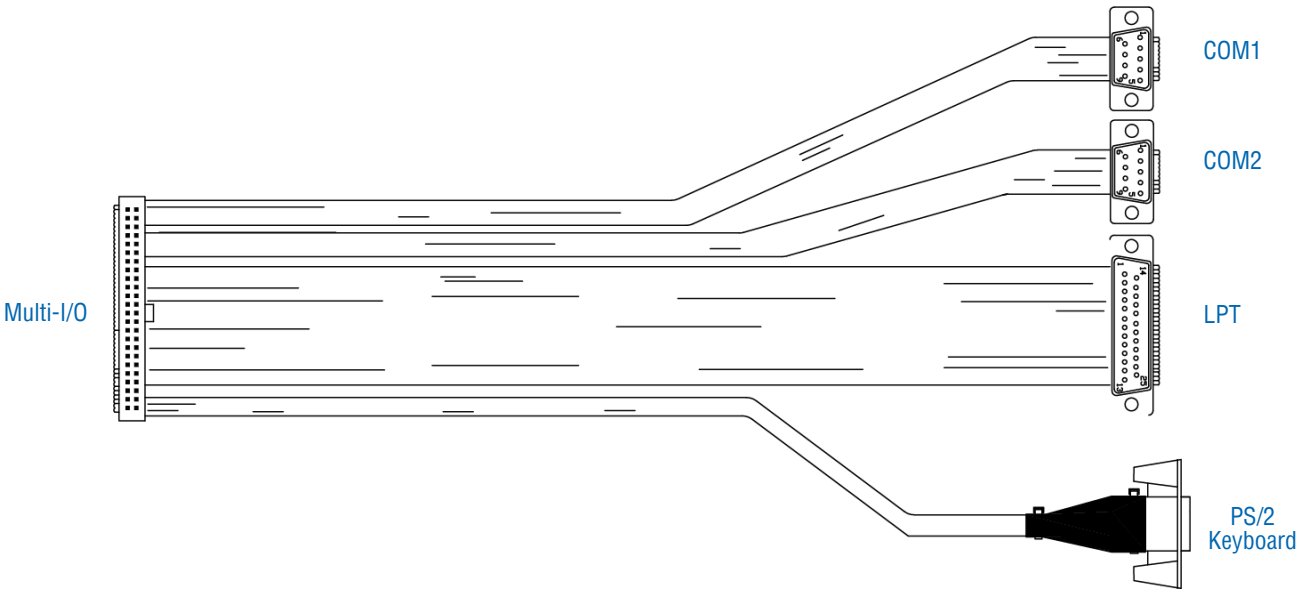
The interface to two of the serial ports (COM1/COM2), the printer port, and keyboard are all terminated via the connector at MIO1. A cable, part number CBL-247-G-1-1-0, is available from WinSystems to adapt to the conventional I/O connectors. The pinout definition for **MIO1** is listed below.

MIO1 - Layout and Pin Reference



Pin	Name	Pin	Name
50	(KEYBD) +5V	49	+5V (KEYBD)
48	(KEYBD) KCLK	47	KDATA (KEYBD)
46	(KEYBD) GND	45	GND (KEYBD)
44	(KEYBD) GND	43	SLCT (LPT)
42	(LPT) GND	41	PE (LPT)
40	(LPT) GND	39	BUSY (LPT)
38	(LPT) GND	37	ACK (LPT)
36	(LPT) GND	35	PD7 (LPT)
34	(LPT) GND	33	PD6 (LPT)
32	(LPT) GND	31	PD5 (LPT)
30	(LPT) GND	29	PD4 (LPT)
28	(LPT) GND	27	PD3 (LPT)
26	(LPT) SLCTIN	25	PD2 (LPT)
24	(LPT) INIT	23	PD1 (LPT)
22	(LPT) ERROR	21	PD0 (LPT)
20	(LPT) AUTOFD	19	STROBE (LPT)
18	(COM2) GND	17	RI (COM2)
16	(COM2) DTR	15	CTS (COM2)
14	COM2) TXD	13	RTS (COM2)
12	(COM2) RXD	11	DSR (COM2)
10	(COM2) DCD	9	GND (COM1)
8	(COM1) RI	7	DTR (COM1)
6	(COM1) CTS	5	TXD (COM1)
4	(COM1) RTS	3	RXD (COM1)
2	(COM1) DSR	1	DCD (COM1)

CBL-247-G-1-1.0 Cable

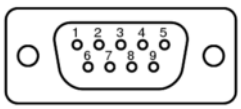


Connectors

- PCB connector: TEKA SRC225C425M126-0
- Mating connector: TW-PANCON 050-050-455A (housing)

COM1, COM2 [DB9 Male]

Layout and Pin Reference

DB9	Pin	RS-232	RS-422	RS-485
	1	DCD	TX-	TX/RX-
	2	RX	TX+	TX/RX+
	3	TX	RX+	
	4	DTR	RX-	
	5	GND	GND	GND
	6	DSR		
	7	RTS		
	8	CTR		
	9	RI		

All serial ports are configured as data terminal equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 transceivers have charge pumps to generate the plus and minus voltages so the PCM-C418 only requires +5V to operate.

Each port is setup to provide internal diagnostics such as loopback and echo mode on the data stream. An independent, software-programmable baud rate generator is

selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

COM1 and COM2 Configuration Options in BIOS

The PCM-C418 uses SP339 multi-mode transceivers, which include RS-232, RS-485, and RS-422 capability in a single device. When RS485 or RS422 modes are selected in the BIOS, a secondary configuration option for selecting the transmitter enable method appears. TXD is the default setting, which automatically toggles the RTS bit when data is in the transmit buffer. The second BIOS option is RTS, and requires that the UART RTS bit be toggled prior to data transmission in RS-422 or RS-485 modes.

- RS-232 mode
- RS-422 mode with RTS transmitter enable - (TX Direction = RTS)
- RS-422 mode with auto transmitter enable - (TX Direction = TXD)
- RS-485 mode with RTS transmitter enable - (TX Direction = RTS)
- RS-485 mode with auto transmitter enable - (TX Direction = TXD)

Additional COM1 and COM2 Configuration Options

The SP339 transceivers include RS-422/485 termination and SLEW control. These settings are disabled by default and can be enabled/disabled by writing to the appropriate mode control registers identified below.

UART Mode Controls

Table 11: Register (0x1E9) for device/function selection

Device/Function Register Window at 0x1E9			
Device	**Function**	**DEVFUN**	**Description**
0	0	0x00	UART 1-2 mode controls
0	1	0x01	UART 3-4 mode controls

UART 1-2 Mode Controls (DEVFUN=0x00)

Table 12: Register (0x1EA) for COM1

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	485TE	SLEW1	TERM1	EN1	UART1 mode (0-3)	

Table 13: Register (0x1EB) for COM2

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	485TE	SLEW2	TERM2	EN2	UART2 mode (0-3)	

Default = 0x05 = RS232 Enabled

- 485TE - Selects the Transmit Enable signal in RS-422/485 mode; 1=TXD enable, 0=RTS enable

  Default = 0 = RTS enable

- SLEW - Limit slew rate to 250 kbps

  Default = 0 = Max data rate

- TERM - Enables RS-422/485 terminations

  Default = 0 = Disabled

- EN - Enables the SP339 multimode UART

  Default = 1 = Enabled

MODE - Selects the communication mode of the serial port (set in BIOS and should be maintained).

Table 14: Modes

Mode	Description
0	LOOPBACK
1	RS232
2	RS485
3	RS422

Example: Set COM1 to RS-485 Auto with termination and COM2 RS-422 Auto with SKEW:

Write 0x00 to 0x1E9 Points to COM1-2 Mode controls

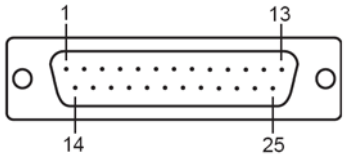
Write 0x2E to 0x1EA COM1 - 485TE, TERM2, EN1, MODE 2

Write 0x37 to 0x1EB COM2 - 485TE, SLEW2, EN2, MODE 3

LPT [DB25 Female]

The LPT port is a multimode parallel printer port that supports the PS/2 standard bidirectional parallel port (SPP), enhanced parallel port (EPP), and extended capabilities port (ECP) functionality. The output drivers support 8 mA per line.

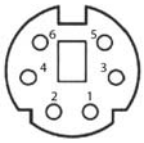
The printer port can also be used as two additional general-purpose I/O ports if a printer is not required. The first port is configured as eight input or output only lines. The other port is configured as five input and three output lines.

DB25	Pin	SPP Signal
	1	STROBE
	2-9	PD0-PD7
	10	ACK
	11	BUSY
	12	PE
	13	SLCT
	14	AUTOFD
	15	ERROR
	16	INIT
	17	SLCTIN
	18-25	GND

PS/2 Keyboard [6-Position]

This connector supports a PS/2 keyboard interface.

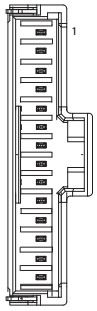
Layout and Pin Reference

PS/2	Pin	Description
	1	KDATA
	2	NC
	3	GND
	4	+5V
	5	KCLK
	6	NC

6.8.6 VGA1 Analog Connector

NOTE The PCM-C418 has one VGA analog video output interface.

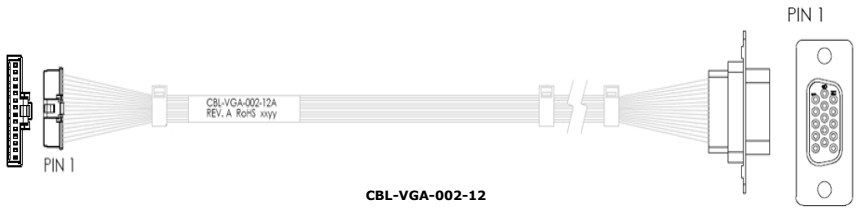
Layout and Pin Reference

	Pin	Name	Description
	1	RED	Red signal input
	2	GND	GND
	3	GREEN	Green signal input
	4	GND	GND
	5	BLUE	Blue signal input
	6	GND	GND
	7	HSYNC	Horizontal synchronization
	8	GND	GND
	9	VSYNC	Vertical synchronization
	10	GND	GND
	11	SDA	Data (synchronized)
	12	GND	GND
	13	SCL	Clock (synchronizes data)
	14	V_{CC}	5V input

Connectors

- PCB connector: Molex 501568-1407 (VGA)
- Mating connector: Molex 501330-1400 (housing)
- Mating connector: Molex 501334-0000 (crimp)

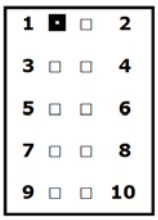
WinSystems offers CBL-VGA-002-12, to interface with an LCD panel.



6.8.7 Serial Interface - COM3, COM4

The connectors for COM3 and COM4 connectors are listed below. The first connector is the pinout on the PCM-C418 and the DB9 describes the pinout of the cable.

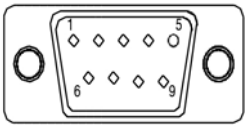
Layout and Pin Reference

RS-232	Pin	Description	Pin	Description
	1	DCD	2	DSR
	3	RXD	4	RTS
	5	TXD	6	CTC
	7	DTR	8	RI
	9	GND	10	V_{CC}

Connectors

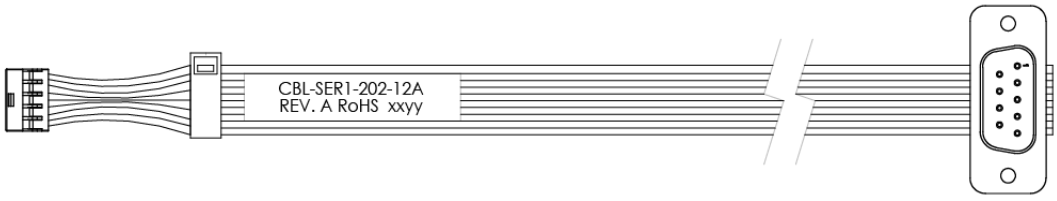
- PCB connector: Molex 87832-1006
- Mating connector: Molex 051110-1060 (housing)
- Mating connector: Molex 50394-8100 (crimp)

Layout and Pin Reference

DB9	Pin	RS-232	RS-422	RS-485
	1	DCD	TX-	TX/RX-
	2	RX	TX+	TX/RX+
	3	TX	RX+	
	4	DTR	RX-	
	5	GND	GND	GND
	6	DSR		
	7	RTS		
	8	CTR		
	9	RI		

Both ports are configured as data terminal equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 has a charge pump to generate the plus and minus voltages so the PCM-C418 only requires +5V to operate. An independent, software programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

CBL-SER1-202-12



COM3 and COM4 Configuration Options in BIOS

The PCM-C418 uses SP339 multi-mode transceivers, which include RS-232, RS-485, and RS-422 capability in a single device. When RS485 or RS422 modes are selected in the BIOS, a secondary configuration option for selecting the transmitter enable method appears. TXD is the default setting, which automatically toggles the RTS bit when data is in the transmit buffer. The second BIOS option is RTS, and requires that the UART RTS bit be toggled prior to data transmission in RS-422 or RS-485 modes.

- RS-232 mode
- RS-422 mode with RTS transmitter enable - (TX Direction = RTS)
- RS-422 mode with auto transmitter enable - (TX Direction = TXD)
- RS-485 mode with RTS transmitter enable - (TX Direction = RTS)
- RS-485 mode with auto transmitter enable - (TX Direction = TXD)

Additional COM3 and COM4 Configuration Options

The SP339 transceivers include RS-422/485 termination and SLEW control. These settings are disabled by default and can be enabled/disabled by writing to the appropriate mode control registers identified below.

UART Mode Controls

Table 15: Register (0x1E9) for device/function selection

Device/Function Register Window at 0x1E9			
Device	**Function**	**DEVFUN**	**Description**
0	0	0x00	UART 1-2 mode controls
0	1	0x01	UART 3-4 mode controls

UART 3-4 Mode Controls (DEVFUN=0x01)

Table 16: Register (0x1EA) for COM3

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	485TE	SLEW1	TERM1	EN1	UART1 mode (0-3)	

Table 17: Register (0x1EB) for COM4

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	485TE	SLEW2	TERM2	EN2	UART2 mode (0-3)	

Default = 0x05 = RS232 Enabled

- 485TE - Selects the Transmit Enable signal in RS-422/485 mode; 1=TXD enable, 0=RTS enable

  Default = 0 = RTS enable

- SLEW - Limit slew rate to 250 kbps

  Default = 0 = Max data rate

- TERM - Enables RS-422/485 terminations

  Default = 0 = Disabled

- EN - Enables the SP339 multimode UART

  Default = 1 = Enabled

MODE - Selects the communication mode of the serial port (set in BIOS and should be maintained).

Table 18: Modes

Mode	Description
0	LOOPBACK
1	RS232
2	RS485
3	RS422

Example: Set COM3 to RS-485 Auto with termination and COM4 RS-422 Auto with SKEW:

Write 0x01 to 0x1E9 Points to COM3-4 Mode controls

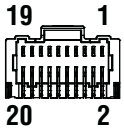
Write 0x2E to 0x1EA COM3 - 485TE, TERM2, EN1, MODE 2

Write 0x37 to 0x1EB COM2 - 485TE, SLEW2, EN2, MODE 3

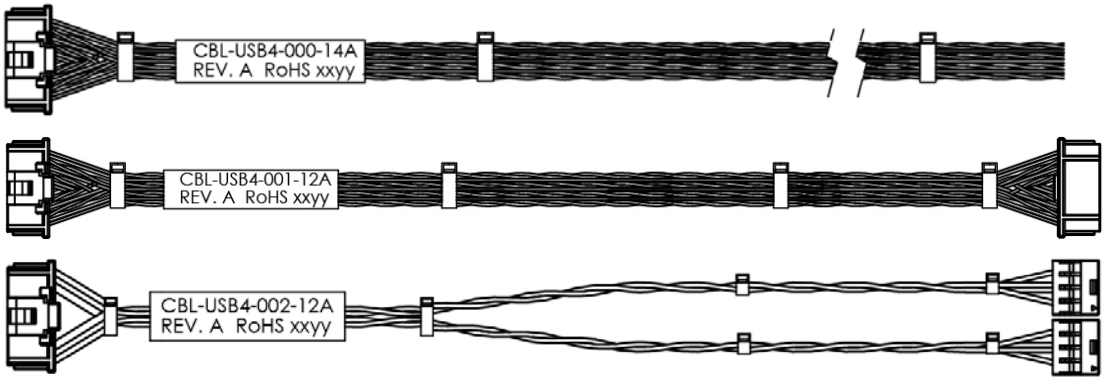
6.8.8 USB1 - USB

A USB cable may be attached to the PCM-C418 via the connector for a total of four USB 2.0 ports. Adapter cables CBL-USB4-000-14, CBL-USB4-001-12, and CBL-USB4-002-12 are available from WinSystems for connection.

USB1 (USB 0/1/2/3) - Layout and Pin Reference

Pin	Description	Pin	Description
			
1	USB0_PWR	2	USB1_PWR
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	USB_GND	8	USB_GND
9	USB_GND	10	USB_GND
11	USB_GND	12	USB_GND
13	USB2_PWR	14	USB3_PWR
15	USB2-	16	USB3-
17	USB2+	18	USB3+
19	USB_GND	20	USB_GND

CBL-USB4-000-14, CBL-USB4-001-12, CBL-USB4-002-12 Cables



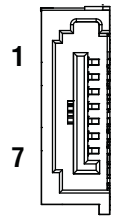
Connectors

- PCB connector: Molex 501571-2007 (USB1)
- Mating connector: Molex 501189-2010 (housing)
- Mating connector: Molex 501193-2000 (crimp)

6.8.9 SATA Serial ATA (SATA)

The PCM-C418 supports one SATA interface.

Layout and Pin Reference

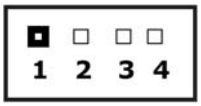
	Pin	Name
	1	GND
	2	A+
	3	A-
	4	GND
	5	B-
	6	B+
	7	GND

Connectors

- PCB connector: Molex 67490-1220 or equivalent
- Mating connector: 3M 5607-4200-SH 1x7, right angle or equivalent

6.8.10 PWROUT1 - SATA Power

Layout and Pin Reference

Pin	Name
	
1	+5V
2	GND
3	GND
4	+12V

Connectors

- PCB connector: Molex 22-11-2042 (SATA PWR)
- Mating connector: Molex 39-01-2105 (housing)
- Mating connector: Molex 08-55-0101 (crimp)

6.8.11 CFD1 - CompactFlash

The PCM-C418 supports solid state CompactFlash storage devices for applications where the environment is too harsh for mechanical hard disks.

The CompactFlash socket at **CFD1** supports modules with TrueIDE support. WinSystems offers industrial-grade CompactFlash modules that provide high performance and extended temperature operation (-40 to +85°C). A PATA activity LED is present at **LED5**.

NOTE The CompactFlash is a PATA device.

Optional On-board eMMC

The PCM-C418 can be ordered with an optional on-board eMMC device up to 64 GB for rugged OEM applications where a removal device is not desirable.

This option is mutually exclusive with CompactFlash since the two interfaces share some physical resources. On a board with eMMC present, there is no CFlash connector.

Contact an Applications Engineer if you are interested in this optional feature.

6.8.12 1 MB SRAM (Battery-backed User Data Space)

The PCM-C418 board provides 1 MB of battery-backed user SRAM. The 1 MB SRAM can be used as a solid state disk device under DOS when using a driver provided by WinSystems.

For example, the DOS driver **USSD.SYS** can be used to make the SRAM appear as a drive in the system by adding the following to **config.sys**.

```
Device = c:\ussd.sys /mod:u /pad:220 /dsz:1024
```

The base address for the SRAM is located at **0220h**.

There are four I/O registers used for accessing the memory array. The register definition and usage is defined below.

Table 19: Offset 0

OFFSET 0 - MSB Address Register
D7 - A23 of access address
D6 - A22 of access address
D5 - A21 of access address
D4 - A20 of access address
D3 - A19 of access address
D2 - A18 of access address
D1 - A17 of access address
D0 - A16 of access address

This register is write-only and holds the upper 8 bits of the 24-bit address used to access the 1 MB SRAM.

Table 20: Offset 1

OFFSET 1 - NSB Address Register
D7 - A15 of access address
D6 - A14 of access address
D5 - A13 of access address
D4 - A12 of access address
D3 - A11 of access address
D2 - A10 of access address
D1 - A9 of access address
D0 - A8 of access address

This register is write-only and holds the middle 8 bits of address used to access the 1 MB memory array. Writing this register also clears the LSB address counter to 0.

Table 21: Offset 2

OFFSET 2 - Data Access Register A
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is the primary window to the memory array. A value written to this port is written to the address in the memory array specified by the MSB register, the NSB register, and the current LSB counter address. In like fashion, a read from this I/O address results in the current memory array data at the address specified by the MSB register, the NSB register, and the LSB address counter.

In either case, read or write, an access to this register results in the LSB address counter being incremented immediately following the access so that the next access is at the next sequential address in the array. This incrementing process does **not** carry into the NSB or MSB register which must be rewritten every 256 bytes.

Table 22: Offset 3

OFFSET 3 - Data Access Register B
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is used to access the memory array when post incrementing of the LSB counter is not desired. The byte written or read is still specified by the 24-bit combination of the MSB register, the NSB register, and the LSB counter. However, the LSB counter is **not** altered following the access. It is then necessary to do one more read from Data Access Register A to bump the address to the next byte.

Table 23: Offset 4

OFFSET 4 - Write Protect Register
D7 - D6 - Reserved
D0 - Write Protect Bit, 0 = Protected, 1 = Writeable

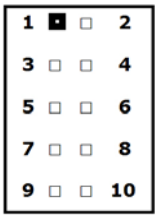
This write-only register controls the write protect function of the 1 MB SRAM board. On power up, the write protect bit is cleared (disabling writes) and must be explicitly enabled by writing a **1** to the I/O port at the BASE address +4. To re-enable the write protection, write a **0** at this register. The **USSD.SYS** device enables writing only during that time when a sector is being transferred, which contributes greatly to data safety and integrity.

6.8.13 LAN1 - 10/100 Mbps Ethernet

The PCM-C418 is equipped with a Vortex86DX LAN controller (**LAN1**), and a standard IEEE 802.3 Ethernet interface for 10/100 (**LAN1**).

See tables below for signal and pin definitions.

LAN1 Layout and Pin Reference

	Pin	Description	Pin	Description
	1	TX+	2	TX-
	3	RX+	4	NC
	5	NC	6	RX-
	7	LED0	8	NC
	9	LED1	10	NC

LAN1 Ethernet Port Indicators

Signal	Off-board
LINK/ACTIVITY	LAN1-P7
DUPLEX	LAN1-P9

Connector

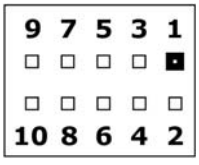
- PCB connector: Molex 87832-1006 (LAN1, LAN2)
- Mating connector: Molex 51110-1051 (housing)
- Mating connector: Molex 50394-8100 (crimp)

6.8.14 LAN2 - 10/100/1000 Mbps Ethernet

The PCM-C418 is equipped with an Intel I210 Ethernet controller (**LAN2**), and a standard IEEE 802.3 Ethernet interface for 10/100/1000 (**LAN2**) BASE-T networks.

On-board Ethernet activity LEDs **LED1-3** are provided for LAN2. See tables below for signal and pin definitions.

LAN2 Layout and Pin Reference

	Pin	Description	Pin	Description
	10	NC	9	NC
	8	MDI3N	7	MDI3P
	6	MDI1N	5	MDI2P
	4	MDI2N	3	MDI1P
	2	MDI0N	1	MDI0P

LAN2 Ethernet Port Indicators

LED	Color	Signal	Off-board
LED1	GREEN	ACTIVITY	LEDOUT1-P1
LED2	YELLOW	SPEED100	LEDOUT1-P2
LED3	RED	SPEED1000	LEDOUT1-P3

Connector

- PCB connector: Molex 87832-1006 (LAN1, LAN2)
- Mating connector: Molex 51110-1051 (housing)
- Mating connector: Molex 50394-8100 (crimp)

6.8.15 LED4 - User Controlled Status LED

A status LED is populated on the board at **LED4** that can be used for any application-specific purpose. The LED can be turned on in software by writing a **1** to I/O port 1EDH and toggled off by writing a **0** to the same address.

6.8.16 LED6 - Power Indicator LED

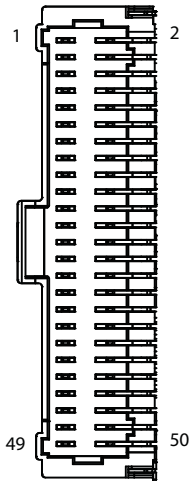
A power LED is populated on the board at **LED6** which indicates that 5V input power is applied.

6.8.17 DIO1 - Digital I/O

The PCM-C418 Digital I/O consists of 24 dedicated programmable I/O pins consisting of three individual 8-bit ports.

All GPIO pins are independent and can be configured as inputs or outputs. When configured as outputs, pins have 12 mA drive capability and are unterminated. When configured as inputs, pins are pulled-high with a 10kΩ resistance. Each input pin also supports interrupt triggers.

DIO1 - Layout and Pin Reference



Pin	Name	Pin	Name
1	Port2 Bit C7	2	GND
3	Port 2 Bit C6	4	GND
5	Port 2 Bit C5	6	GND
7	Port 2 Bit C4	8	GND
9	Port 2 Bit C3	10	GND
11	Port 2 Bit C2	12	GND
13	Port 2 Bit C1	14	GND
15	Port 2 Bit C0	16	GND
17	Port 1 Bit B7	18	GND
19	Port 1 Bit B6	20	GND
21	Port 1 Bit B5	22	GND
23	Port 1 Bit B4	24	GND
25	Port 1 Bit B3	26	GND
27	Port 1 Bit B2	28	GND
29	Port 1 Bit B1	30	GND
31	Port 1 Bit B0	32	GND
33	Port 0 Bit A7	34	GND
35	Port 0 Bit A6	36	GND
37	Port 0 Bit A5	38	GND
39	Port 0 Bit A4	40	GND
41	Port 0 Bit A3	42	GND
43	Port 0 Bit A2	44	GND
45	Port 0 Bit A1	46	GND
47	Port 0 Bit A0	48	GND
49	+3.3/5V	50	GND

Connectors

- PCB connector: Molex 501571-5007 (DIO1)
- Mating connector: Molex 501189-5010 (housing)
- Mating connector: Molex 501193-2000 (crimp)

6.8.18 CON1 and CON2 - PC/104 Bus

The PC/104 bus is electrically equivalent to the 16-bit ISA bus. Standard PC/104 I/O cards can be populated on PCM-C418's connectors, located at CON1 and CON2. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Specification for specific signal and mechanical specifications.

Layout and Pin Reference

CON2	Pin	Name	Pin	Name
	(C/D)			
D0 C0	D0	GND	C0	GND
	D1	MEMCS16#	C1	SBHE#
	D2	IOCS16#	C2	LA23
	D3	IRQ10	C3	LA22
	D4	IRQ11	C4	LA21
	D5	IRQ12	C5	LA20
	D6	IRQ15	C6	LA19
	D7	IRQ14	C7	LA18
	D8	DACK0#	C8	LA17
	D9	DRQ0	C9	MEMR#
	D10	DACK5#	C10	MEMW#
D19 C19	D11	DRQ5	C11	SD8
	D12	DACK6#	C12	SD9
	D13	DRQ6	C13	SD10
	D14	DACK7#	C14	SD11
	D15	DRQ7	C15	SD12
	D16	+5V	C16	SD13
	D17	MASTER#	C17	SD14
	D18	GND	C18	SD15
	D19	GND	C19	KEY

Pin	Name	Pin	Name	CON1
(A/B)				
A1	IOCHK#	B1	GND	A1 B1
A2	SD7	B2	RESET	
A3	SD6	B3	+5V	
A4	SD5	B4	IRQ9	
A5	SD4	B5	NC	
A6	SD3	B6	DRQ2	
A7	SD2	B7	-12V	
A8	SD1	B8	SRDY#	
A9	SD0	B9	+12V	
A10	IOCHRDY	B10	KEY	
A11	AEN	B11	SMEMW#	
A12	SA19	B12	SMEMR#	
A13	SA18	B13	IOW#	
A14	SA17	B14	IOR#	
A15	SA16	B15	DACK3#	A32 B32
A16	SA15	B16	DRQ3	
A17	SA14	B17	DACK1#	
A18	SA13	B18	DRQ1	
A19	SA12	B19	REFRESH#	
A20	SA11	B20	BCLK	
A21	SA10	B21	IRQ7	
A22	SA9	B22	IRQ6	
A23	SA8	B23	IRQ5	
A24	SA7	B24	IRQ4	
A25	SA6	B25	IRQ3	
A26	SA5	B26	DACK2#	
A27	SA4	B27	TC	
A28	SA3	B28	BALE	
A29	SA2	B29	+5V	
A30	SA1	B30	OSC	
A31	SA0	B31	GND	
A32	GND	B32	GND	

= Active Low Signal

Notes:

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

Connectors

- PCB connector: TEKA SBL PC232-A-1A7-M
- PCB connector: TEKA SBL PC220-A-1A7-M

7. BIOS Supplemental

7.1 General Information

The PCM-C418 includes an AMI BIOS to assure full compatibility with PC operating systems and software. The basic system configuration is stored in battery-backed CMOS RAM within the clock/calendar. As an alternative, the BIOS configuration may be stored in internal flash for operation without a battery. For more information of CMOS configuration, see “BIOS Setting Storage Options” on page 47.

7.2 Entering Setup

To enter setup, power up the computer and press **Delete** to enter the setup menu. It may take a few seconds before the main setup menu screen is displayed.

7.3 Navigating the Menus

Use the **Up** and **Down** arrow keys to move among the selections and press **Enter** when a selection is highlighted to enter a sub-menu or to see a list of choices. Following are tables of options from each menu screen in the default configuration. Menu values shown in **bold** typeface are factory defaults.

Main Menu	
System Overview	
Time	22:40:32
Date	06/09/2009
System BIOS	41216246
Build Date	09/02/2016
VGA BIOS	0.00.01
VBIOS Date	01/16/2015
FPGA Revision	0003
EC Support	Disabled
Processor	
Type	DMP (R) A9126
Speed	1000MHz
System Memory	
Size	
Speed	
System Information	
UUID	00020003-0004-0005-0006-000700080009
MAC1	00 1B EB 07 96 18
MAC2	00 01 45 07 53 34

Each available option is listed in detail in the following sections. Navigation to the screens is located at the top of each screen’s layout.

Advanced > Advanced Settings
Chipset
IDE Configuration
Serial/Parallel & GPIO Port Configuration
Watchdog Configuration
Remote Access Configuration
USB Configuration
Power Management Configuration
Smbios Configuration
Shadow RAM Configuration
Patcher ROM Setting

Advanced > Advanced Chipset Settings	
Warning: Setting wrong values in below sections may cause system to malfunction	
Platform ID	60236035 - Real
Board ID	80
Project ID	0002
Board ID Simulate [0]	
Codec...	
VID/DID	10EC0888
Revision	00100302
Verb Table	None (F)
NorthBridge Configuration	
SouthBridge Configuration	
Debug Mode	[Disabled]
Disable Reset Function	[No]
Begin Disable Watch-Dog Functi	[No]
uControl Support	[Disabled]
DRAM Refresh	[15uS]
Keyboard Control Select	[Auto]

Advanced > Chipset Settings - NorthBridge Configuration	
Customer ID	DMP6
CPU Configuration	
DRAM Configuration	
VGA Configuration	
MISC Configuration	
NB Function 0 Register 44	[2]
NB Function 0 Register 45	[11]
NB Function 0 Register 46	[0]
NB Function 0 Register 47	[0]
NB Function 0 Register 48	[10]
NB Function 0 Register 50	[3]
NB Function 0 Register 51	[6]
NB Function 0 Register 52	[0]
NB Function 0 Register 53	[40]

Advanced > Chipset Settings - NorthBridge Configuration - CPU Configuration	
Manufacturer	DMP
Brand String	DMP (R) A9126
Frequency	1.00GHz
L1 Cache	[Enabled]
Cache L1	16 KB
L2 Cache	[Enabled]
L2 Cache Method	[Write Back]
Cache L2	256 KB
CPU Fast Decode	[Normal]
CPU Pipeline-write	[Enabled]
DRAM Refresh Rate Double	[Double Refresh Rate]
MSR CFCFCF00 00:07	[FE]
MSR CFCFCF00 08:15	[F0]
MSR CFCFCF00 16:23	[55]
MSR CFCFCF00 24:31	[F7]
MSR CFCFCF00 32;39	[0]
MSR CFCFCF00 40:47	[5F]
MSR CFCFCF00 48:55	[8]
MSR CFCFCF00 56:63	[0]

Advanced > Chipset Settings - NorthBridge Configuration - DRAM Configuration	
DDR Setting By	[BIOS]
DDR PHY Control Setting By	[BIOS]
Enhanced RWP Policy	[Disabled]
NB Function 1 Register BC	[0]
NB Function 1 Register BD	[0]
NB Function 1 Register BE 0:3	[0]

Advanced > Chipset Settings - NorthBridge Configuration - VGA Configuration	
LCD Panel Index	[3]
LCD Backlight	[Disabled]
GPU Frame Buffer Mapping	[Enabled]
GPU Frame Buffer R/W Reorder	[Enabled]

Advanced > Chipset Settings - NorthBridge Configuration - MISC Configuration	
PCI Read CMD Select	[MRL like MR]
NB Function 0 Register F9	[5D]
PCI Prefetch Read Disable	[No]
PCI Master Burst Write Length	[3]
PCI Delay Line	[4]

Advanced > Chipset Settings - SouthBridge Chipset Configuration	
P.O.S.T. Forward To	[Disabled]
ISA Configuration	
WatchDog Configuration	
Driving Control Configuration	
MISC Configuration	
SB Function 0 Register 48	[10]
SB Function 0 Register 49	[36]
SB Function 0 Register 4A	[FF]
SB Function 0 Register 4B	[3F]
0 1 2	PLL 75MHz PLL 50MHz Ex [3]

Advanced > Chipset Settings - SouthBridge Chipset Configuration - ISA Configuration	
ISA Clock	[8.3MHz]
ISA 16bits I/O wait-state	[1 clock]
ISA 8bits I/O wait-state	[4 clock]
ISA 16bits Memory wait-state	[1 clock]
ISA 8bits Memory wait-state	[4 clock]

Advanced > Chipset Settings - SouthBridge Chipset Configuration - WatchDog Configuration	
WatchDog 1 Function	[Disabled]

Advanced > Chipset Settings - SouthBridge Chipset Configuration - Driving Control Configuration	
24MHz Clock Output	[Clock Output]
24MHz Clock	[16 mA]
24MHz Clock Slew Rate	[Fast]

Advanced Chipset Settings - SouthBridge Chipset Configuration - MISC Configuration	
IDE Compatibility	[Enabled]
SB PCI Target Decode Timing	[Sub Decode]

Advanced > IDE Configuration	
OnBoard PCI IDE Controller	[Both]
Primary IDE Master	[Hard Disk]
Secondary IDE Master	[Not Detected]
Hard Disk Write Protect	[Disabled]
IDE Detect Timeout (Sec)	[35]
Hard Disk Delay	[Disabled]
OnBoard IDE Operate Mode	[Native Mode]
Not program PIO mode	[Disabled]
SATA PHY Speed	[Auto]

Advanced > Serial/Parallel & GPIO Port Configuration	
SB Serial Port 1	[3F8]
Serial Port IRQ 1	[IRQ4]
Serial Port Baud Rate	[115200 BPS]
Serial Port 1 Mode	[RS232]
SB Serial Port 2	[2F8]
Serial Port IRQ 2	[IRQ3]
Serial Port Baud Rate	[115200 BPS]
Serial Port 2 Mode	[RS232]
SB Serial Port 3	[3E8]
Serial Port IRQ 3	[IRQ5]
Serial Port Baud Rate	[115200 BPS]
SB Serial Port 4	[2E8]
Serial Port IRQ 4	[IRQ5]
Serial Port Baud Rate	[115200 BPS]
Parallel Port Address	[3F8]
Parallel Port IRQ	[IRQ7]
Digital I/O	[120]
Digital I/O IRQ	[IRQ10]

Advanced > Watchdog Timer Configuration	
Watchdog Timer	[0 sec]

Advanced > Remote Access Configuration	
Remote Access	[Disabled]

Advanced > USB Configuration	
Module Version - 3.0.0-14.4	
USB Devices Enabled	[None]
USB Support	[Enabled]
USB port 1/2 Power Enable	[Enabled]
USB port 3/4 Power Enable	[Enabled]
Legacy USB Support	[Enabled]
USB 2.0 Controller Mode	[HiSpeed]
BIOS EHC Hand-off	[Enabled]
USB Beep Message	[Disabled]
Support USB Device Wakeup	[Disabled]

Advanced > Power Management Configuration	
APM Configuration	
ACPI Configuration	

Advanced > Power Management Configuration-APM Configuration	
APM Support	[Disabled]

Advanced > Power Management Configuration-ACPI Configuration	
ACPI Aware O/S	[Yes]
General ACPI Configuration	
Advanced ACPI Configuration	

Advanced > Power Management Configuration-ACPI Configuration-General ACPI Configuration	
Suspend Mode	[S3 (STR)]
Repost Video on S3 Resume	[No]

Advanced > Power Management Configuration-ACPI Configuration-Advanced ACPI Configuration	
ACPI Version Feature	[ACPI v3.0]
ACPI APIC Support	[Enabled]
AMI OEMB Table	[Enabled]
Headless Mode	[Disabled]
SLIC Table support	[Disabled]

Advanced > Smbios Configuration	
Smbios Support	[Enabled]

Advanced > Shadow RAM Configuration	
E000,32k Shadow	[Unchanged]
E800,32k Shadow	[Unchanged]

Advanced > Patcher ROM Setting	
Patcher ROM 1	Patcher ROM - Version 2.00
Build Date	08/01/2011
Patcher ROM 2	OSW Pro - Version 1.24
Build Date	03/31/2009
Patcher ROM Message Display	[Enabled]
Patcher ROM Trigger1	[Disabled]
Patcher ROM Trigger1 Position	[End of POST]
Patcher ROM Trigger2	[Disabled]
Patcher ROM Trigger2 Position	[End of POST]

PCIPnP > Advanced PCI/PnP Settings	
Warning: Setting the wrong values in these sections may cause the system to malfunction.	
Clear NVRAM	[No]
Plug & Play O/S	[No]
PLI Latency Timer	[64]
Allocate IRQ to PCI VGA	[Yes]
Palette Snooping	[Disabled]
PCI IDE BusMaster	[Enabled]
OffBoard PCI/ISA IDE Card	[Auto]
IRQ3	[Reserved]
IRQ4	[Reserved]
IRQ5	[Available]
IRQ6	[Available]
IRQ7	[Available]
IRQ9	[Reserved]
IRQ10	[Available]
IRQ11	[Available]
IRQ12	[Available]
IRQ14	[Available]
IRQ15	[Available]
DMA Channel 0	[Available]
DMA Channel 1	[Available]
DMA Channel 3	[Available]
DMA Channel 5	[Available]
DMA Channel 6	[Available]
DMA Channel 7	[Available]
Reserved Memory Size	[Disabled]

Boot > Boot Settings	
Boot Settings Configuration	
Boot Device Priority	
Hard Disk Drives	

Boot > Boot Settings-Boot Settings Configuration	
Quick Boot	[Enabled]
Fast Boot	[Disabled]
Quiet Boot	[Enabled]
AddOn ROM Display Mode	[Force BIOS]
Bootup Num-Lock	[Off]
PS/2 Mouse Support	[Auto]
Wait For 'F1' If Error	[Enabled]
Hit 'DEL' Message Display	[Enabled]
Interrupt 19 Capture	[Enabled]
Onboard VGA (GPUP)	[Enabled]
Onboard VGA (GPURST	[Enabled]
VGA Share Memory	[64 MB]
Boot Display Device	[CRT]
Beep Function	[Disabled]
Boot Menu Hot-Key	[Enabled]
Boot From LAN Hot-Key	[Enabled]
Boot From LAN	[Disabled]

Boot > Boot Settings-Boot Device Priority	
1st Boot Device	[Hard Drive]
2nd Boot Device	[CD/DVD]
3rd Boot Device	[USB]
4th Boot Device	[Removable Dev.]
5th Boot Device	[Network]

Boot > Boot Settings-Hard Disk Drives	
1st Drive	[HDD:PM-CF 32GB]

Security > Security Settings	
Supervisor Password	Not Installed
User Password	Not Installed
Change Supervisor Password	
Change User Password	
Boot Sector Virus Protection	[Disabled]
RDC Engineering Mode	[Enabled]
I/O Interface Security	
Hard Disk Security Setting	
RDC IDE Security Setting	

Security > Security Settings-I/O Interface Security	
USB Control 1 Interface	[Enabled]
USB Control 2 Interface	[Enabled]
USB Device Interface	[Disabled]
LAN Network Interface	[Enabled]
COM4 Port Interface	[Enabled]
COM1 Port Interface	[Enabled]
COM3 Port Interface	[Enabled]
COM2 Port Interface	[Enabled]
AUDIO/MODEM Interface	[Enabled]

Security > Security Settings-Hard Disk Security Setting	
Primary Master HDD Password Status	[Disabled]
Primary Master HDD Master Password	
Primary Master HDD User Password	

Security > Security Settings-RDC IDE Security Setting	
AES key Length	[128 bits]
PM-HDD Encryption Mode	[Disabled]

Exit > Exit Options	
Save Changes and Exit	
Discard Changes and Exit	
Discard Changes	
Load Optimal Defaults	
Load Failsafe Defaults	

7.4 BIOS Setting Storage Options

7.4.1 CMOS Storage Locations

The PCM-C418's BIOS configuration is stored in these locations:

- CMOS RAM (nonvolatile if battery backed)
- FLASH PROM (nonvolatile storage for factory defaults)

7.4.2 Saving the CMOS Configuration

The real-time clock and the CMOS RAM settings can be maintained by an optional battery when the board is powered off.

7.4.3 Updating the BIOS FLASH PROM

The most recent PCM-C418 BIOS is available on the WinSystems website at www.winsystems.com. However, it is highly recommended that an Applications Engineer be consulted prior to any BIOS FLASH ROM update.

8. Cables and Batteries

WinSystems cables and batteries simplify connection to the PCM-C418. The following tables list available items.

Table 24: Cables

Part Number	Description	
Cable Set		
CBL-SET-418-2	Set of cables for the PCM-C418 including these parts numbers:	
	CBL-VGA-002-12	1-ft. VGA adapter
	CBL-174-G-1-1.5	18-in., 8-wire power cable
	CBL-247-G-1-1.0	1-ft. Multi-I/O adapter
	2x CBL-SER1-202-12	Serial I/O cable (COM3/COM4)
	CBL-USB4-002-12	4x USB ports to two, 2-mm 2x4 connectors
	CBL-ENET1-204-12	2-mm 2x5 to 2-mm 2x6 connector (2 each)
	ADP-IO-ENET-002	Dual 12-pin, 2-mm to dual RJ-45 adapter
	ADP-IO-USB-002	Dual 8-pin, 2-mm to 4 Type A USB connectors
	BAT-LTC-E-36-16-1	External 3.6V, 1600 mAH battery with plug-in connector
Additional Cables		
CBL-174-G-1-1.5	18-in., 8-wire power cable	
CBL-343-G-1-1.375	PS/2 mouse adapter	
CBL-247-G-1-1.0	1-ft. Multi-I/O adapter	
CBL-ENET1-206-18	Ethernet cable with RJ-45 jack	
CBL-SER1-202-12	Serial I/O cable (COM3/COM4)	
CBL-USB4-000-14	4x USB ports - unterminated	
CBL-USB4-001-12	4x USB ports two, 2x20-pin Pico-Clasp connector	
CBL-USB4-002-12	4x USB ports to two, 2-mm 2x4 connectors	

Table 25: Batteries

Part Number	Description
BAT-LTC-E-36-16-1	External 3.6V, 1600 mAH battery with plug-in connector
BAT-LTC-E-36-27-1	External 3.6V, 2700 mAH battery with plug-in connector

9. Software Drivers

Go to www.winsystems.com for information on available software drivers.

Appendix A. Best Practices

This appendix outlines the best practices for operating the PCM-C418 in a safe, effective manner, that does not damage the board. Please read this section carefully.

Power Supply

The power supply and how it is connected to the PCM-C418 is very important.

Avoid Electrostatic Discharge (ESD)—Only handle the PCM-C418 and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Zero-load Power Supply

Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply does not regulate properly and can cause damage to the PCM-C418.

Use Proper Power Connections (Voltage)—When verifying the voltage, measure it at the power connector on the PCM-C418. Measuring it at the power supply does not account for voltage drop through the wire and connectors.

The PCM-C418 requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the PCM-C418, the better.

Adjusting Voltage

If you have a power supply that allows you to adjust the voltage, it is a good idea to set the voltage at the power connector of the PCM-C418 to 5.1V. The PCM-C418 can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for the small amount of voltage drop that occurs over time as the power supply ages and the connector contacts oxidize.

Power Harness

Minimize the length of the power harness. This reduces the amount of voltage drop between the power supply and the PCM-C418.

Gauge Wire

Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins.

Contact Points

WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high-speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion, resulting in unreliable connections.

Power Down

Make sure that the system is **completely off/ powered** down before making or breaking any connections.

Power Supply OFF—The power supply should always be off before it is connected to the PCM-C418.

I/O Connections OFF—I/O connections should also be off before connecting them to the PCM-C418 or any I/O cards. Connecting hot signals can cause damage whether the PCM-C418 is powered or not.

Mounting and Protecting the PCM-C418

The PCM-C418 must be mounted properly to avoid damage.

Do not bend or flex the PCM-C418—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around ball-grid-array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting holes—The mounting holes are plated on the top, bottom, and through the barrel of the hole, and are connected to the PCM-C418's ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.

- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes, you provide the support the embedded computer module needs to prevent bending or flexing.

Plug or unplug connectors only on fully mounted boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the embedded computer module to be flexed.

Avoid cutting the PCM-C418—Never use star washers or any fastening hardware that cut into the PCM-C418.

Avoid over-tightening of mounting hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use appropriate tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid conductive surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Adding PC/104 Boards to Your Stack

Be careful when adding PC/104 boards to your stack—Never allow the power to be turned on when a PC/104 board is improperly plugged into the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it causes the I/O board to be damaged beyond repair.

Operations/Product Manuals

Every single board computer has an operations manual or product manual.

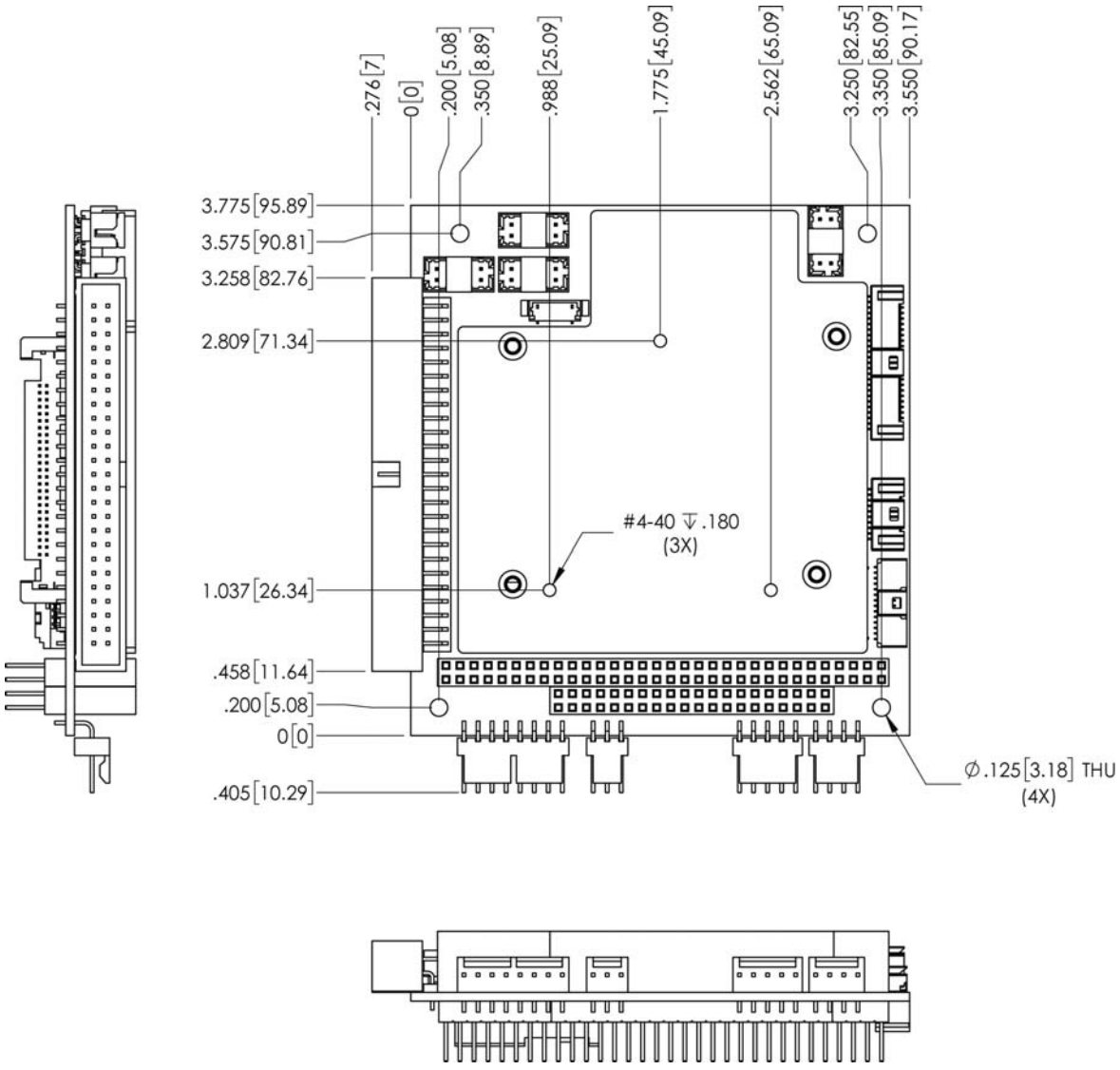
Periodic Updates—Operations/product manuals are updated often. Periodically check the WinSystems website (http://www.winsystems.com) for revisions.

Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

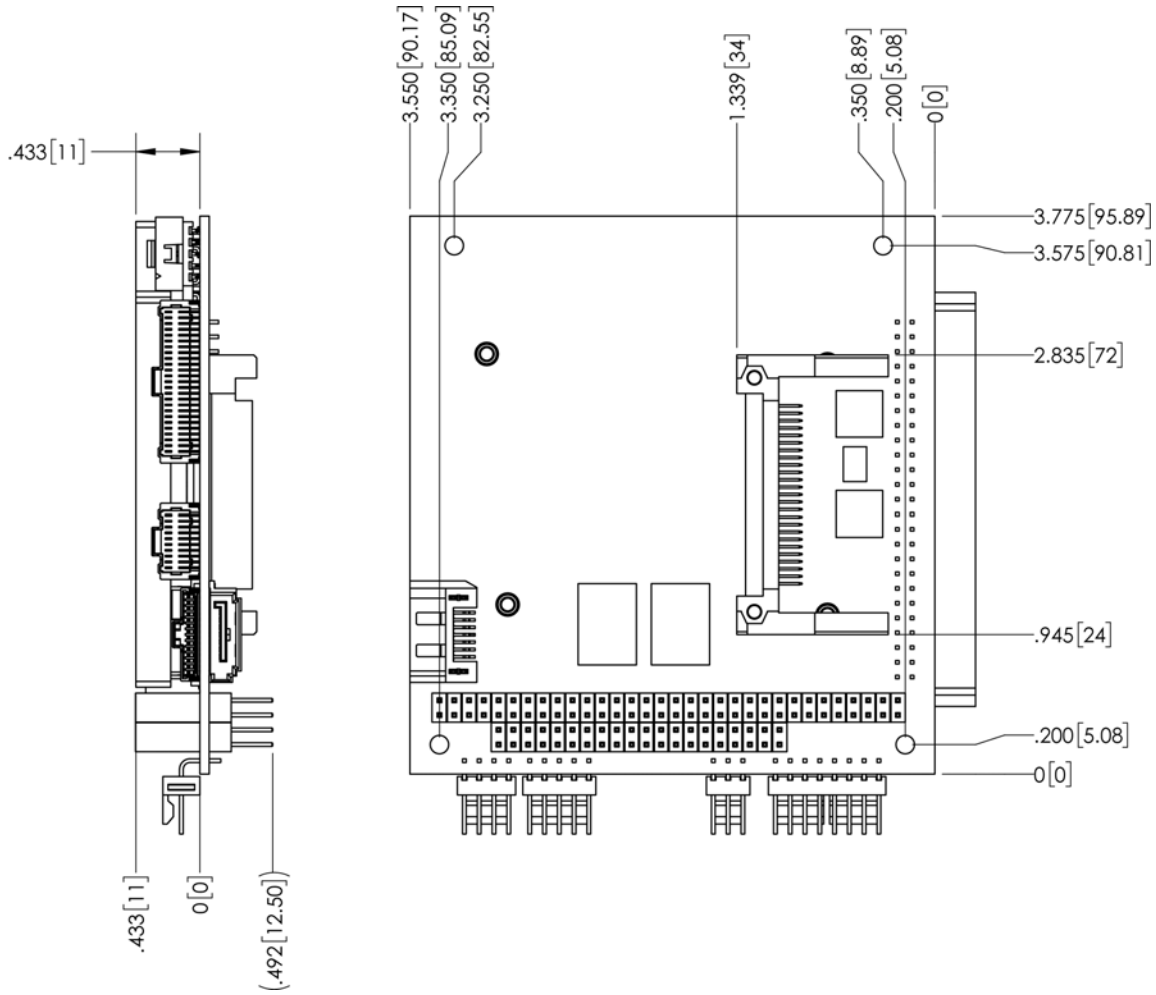
Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WinSystems Applications Engineer.

Appendix B. Mechanical Drawings

PCM-C418 Drawing, Top and Side Views



PCM-C418 Drawing, Bottom View



Appendix C. Power-on Self-Test (POST) Codes

NOTE This content is from https://www.ami.com/ami_downloads/AMIBIOS8_Checkpoint_and_Beep_Codes.pdf. Clicking this link downloads a PDF that includes additional code information.

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that can occur during the POST portion of the BIOS3.

Checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset, or option ROMs from add-in PCI devices.

Table 26: POST code checkpoints

Checkpoint	Description
03	Disables NMI, parity, video for EGA, and DMA controllers. Initializes BIOS, POST, runtime data area. Also initializes BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the kernel variable `wCMOSFlags`.
04	Checks CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verifies CMOS checksum manually by reading storage area. If the CMOS checksum is bad, updates CMOS with power-on default values and clear passwords. Initializes status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Performs R/W test to CH-2 count reg. Initializes CH-0 as system timer. Install the POSTINT1Ch handler. Enables IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to `POSTINT1ChHandlerBlock`.
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Programming the keyboard controller command byte is done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start – Disable Cache – Init Local APIC
C1	Sets up boot strap processor information.
C2	Sets up boot strap processor for POST.
C5	Enumerates and sets up application processors.
C6	Re-enables cache for boot strap processor.
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible keyboard controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of keyboard in KBC port.
0E	Tests and initializes different input devices. Updates the kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompresses all available languages, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers

Table 26: POST code checkpoints (Continued)

Checkpoint	Description
20	Relocates system management interrupt vector for all CPU in the system.
24	Uncompresses and initializes any platform-specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that has optional ROMs.
2E	Initializes all output devices.
31	Allocates memory for ADM module and uncompress it. Gives control to ADM module for initialization. Initializes language and font modules for ADM. Activates ADM module.
33	Initializes the silent boot module. Sets the window for displaying text information.
37	Displays sign-on message, CPU information, setup key message, and any OEM-specific information.
38	Initializes different devices through DIM. USB controllers are initialized at this point.
39	Initializes DMAC-1 and DMAC-2.
3A	Initializes RTC date/time.
3B	Tests for total memory installed in the system. Checks for DEL or ESC keys to limit memory test. Displays total memory in the system.
3C	Mid POST initialization of chipset registers
40	Detects different devices (parallel ports, serial ports, and coprocessor in CPU, etc.) successfully installed in the system and updates the BDA, EBDA, and so on.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for extended BIOS data area from base memory. Programs the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM LOCK status and programs the KBD typematic rate.
75	Initializes Int-13 and prepares for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generates and writes contents of ESCD in NVRAM.
84	Logs errors encountered during POST.
85	Displays errors to the user and gets the user response for error.
87	Executes BIOS setup if needed or requested. Checks boot password if installed.
8C	Late POST initialization of chipset registers
8D	Builds ACPI tables (if ACPI is supported).
8E	Programs the peripheral parameters. Enables or disables NMI as selected
90	Initializes system management interrupt by invoking all handlers. Note that this checkpoint comes right after checkpoint 20h.

Table 26: POST code checkpoints (Continued)

Checkpoint	Description
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ routing table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initializes runtime language module. Displays boot option popup menu.
A7	Displays the system configuration screen if enabled. Initializes the CPUs before boot, which includes the programming of the MTRRs.
A9	Waits for user input at config display if needed.
AA	Uninstalls POST INT1Ch vector and INT09h vector.
AB	Prepares BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Saves system context for ACPI. Prepares CPU for OS boot including final MTRR values.
00	Passes control to OS loader (typically INT19h).

Appendix D. Warranty Information

WARRANTY

(http://www.winsystems.com/company/warranty.cfm)

WinSystems warrants to Customer that for a period of two (2) years from the date of shipment any Products and Software purchased or licensed hereunder which have been developed or manufactured by WinSystems shall be free of any material defects and shall perform substantially in accordance with WinSystems' specifications therefore. With respect to any Products or Software purchased or licensed hereunder which have been developed or manufactured by others, WinSystems shall transfer and assign to Customer any warranty

of such manufacturer or developer held by WinSystems, provided that the warranty, if any, may be assigned. Notwithstanding anything herein to the contrary, this warranty granted by WinSystems to the Customer shall be for the sole benefit of the Customer, and may not be assigned, transferred or conveyed to any third party. The sole obligation of WinSystems for any breach of warranty contained herein shall be, at its option, either (i) to repair or replace at its expense any materially defective Products or Software, or (ii) to take back such Products and Software and refund the Customer the purchase price and any license fees paid for the same. Customer shall pay all freight, duty, broker's fees, insurance charges for the return of any Products or Software to WinSystems under this warranty. WinSystems shall pay freight and insurance charges for any repaired or replaced Products or Software thereafter delivered to Customer within the United States. All fees and costs for shipment outside of the United States shall be paid by Customer. The foregoing warranty shall not apply to any Products of Software which have been subject to abuse, misuse, vandalism, accidents, alteration, neglect, unauthorized repair or improper installations.

THERE ARE NO WARRANTIES BY WINSYSTEMS EXCEPT AS STATED HEREIN, THERE ARE NO OTHER WARRANTIES EXPRESS OR IMPLIED INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, IN NO EVENT SHALL WINSYSTEMS BE LIABLE FOR CONSEQUENTIAL, INCIDENTIAL OR SPECIAL DAMAGES INCLUDING, BUT NOT LIMITED TO, DAMAGES FOR LOSS OF DATA, PROFITS OR GOODWILL. WINSYSTEMS' MAXIMUM LIABILITY FOR ANY BREACH OF THIS AGREEMENT OR OTHER CLAIM RELATED TO ANY PRODUCTS, SOFTWARE, OR THE SUBJECT MATTER HEREOF, SHALL NOT EXCEED THE PURCHASE PRICE OR LICENSE FEE PAID BY CUSTOMER TO WINSYSTEMS FOR THE PRODUCTS OR SOFTWARE OR PORTION THEREOF TO WHICH SUCH BREACH OR CLAIM PERTAINS.

Warranty Service

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WinSystems' Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.
2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WinSystems is not responsible for damage to the product due to static electricity.