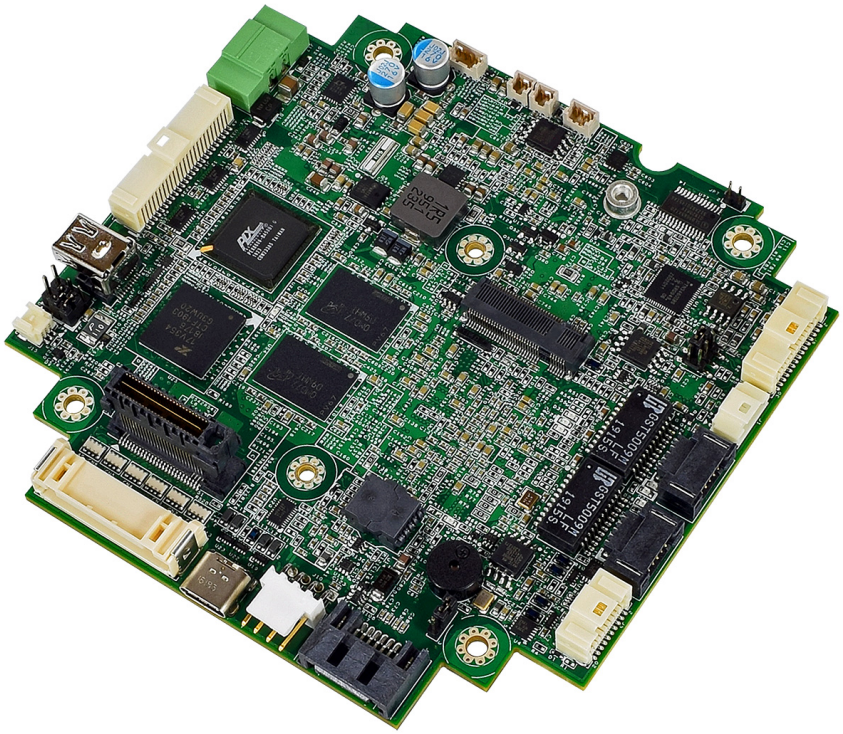
WINSYSTEMS®

PX1-C441

PCIe/104 OneBank™ Intel® Atom™ E3900 Single Board Computer with Dual Ethernet

Product Manual



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Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	7/1/2021	Initial release
v1.01	2/24/2022	Removed references to high temperature grade DRAM

Copyright and Trademarks

Trademark Acknowledgments

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1. Before You Begin

Review the warnings in this section and the best practice recommendations (see “Best Practices” on page 53) when using and handling the WINSYSTEMS PX1-C441. Following these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the PX1-C441 before proceeding.

FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PX1-C441 AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the PX1-C441. While observing best practices, pay particular attention to the following.

Avoid electrostatic discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

2. Introduction

This manual provides configuration and usage information for the PX1-C441. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WINSYSTEMS website at http://www.winsystems.com/ for other accessories (including cable drawings and pinouts) that can be used with your PX1-C441.

3. Functionality

The WINSYSTEMS PX1-C441 single board computer features the Intel® Atom™ Apollo Lake-I Dual core or Quad core system on chip (SOC) for processing and graphics. It includes up to 8 GB of soldered down LPDDR4 system memory and a non-removable eMMC device for solid state storage. In addition, the board supports M.2 and SATA devices.

This full-featured SBC has onboard I/O and supports simultaneous DisplayPort and LVDS video. It provides dual Gigabit Ethernet interfaces, eight USB 2.0 channels, one SuperSpeed USB 3.2 Gen 1 channel, four serial ports and one serial console port, 24 general purpose I/O (GPIO) lines, one I2C bus, stereo audio, and a watchdog timer.

Additionally, the board has an M.2 socket and a PCIe/104 OneBank connector that provides four PCIe and two USB 2.0 I/O expansion channels.

NOTE WINSYSTEMS can provide custom configurations for OEM clients. Contact an application engineer for details.

4. Features

The PX1-C441 provides the following features.

Single Board Computer

- Multi-core Intel Atom E3900 processors
  - X5 E3930 dual core, up to 1.8 GHz (base frequency 1.3 GHz)
  - X5 E3940 quad core, up to 1.8 GHz (base frequency 1.6 GHz)
  - X7 E3950 quad core, up to 2.0 GHz (base frequency 1.6 GHz)

Operating Systems (compatibility)

- Windows 10 x64, IoT Core, and Professional
- Linux x64
- Most x86 operating systems

Memory

- Up to 8 GB soldered down LPDDR4

BIOS

- AMI UEFI-compliant BIOS in SPI flash device

Video Interfaces (supports dual simultaneous displays)

- Up to 24 bpp color panel support
- Flat-panel resolution up to 1920 x 1200 in dual bus mode
- Low-voltage differential signaling (LVDS)
- Dual Mode Mini DisplayPort++ (version 1.2)
  - 4096 x 2160 at 60 Hz

Ethernet

- Two Intel 10/100/1000 Mbps controllers using Intel i210
- Wake-on-LAN support, both channels

Storage

- One SATA 3.0 (6.0 Gb/s) channel
- One M.2 SSD support (M.2 socket)
- Optional eMMC solid state disk

Digital Input/Output

- 24 GPIO bidirectional lines

Bus Expansion

- PCIe/104 OneBank connection
  - Four PCIe channels
  - Two USB 2.0 channels
- SATA 3.1 Gen 1 channel
- M.2 B-Key

Serial Interface

- Two RS232/422/485 serial ports
- Two dedicated RS232 ports
- One RS232 serial console port
- All RS232 ports support RTS/CTS, DTR/DSR, RI, and CD signaling

USB

- Eight USB 2.0 ports
  - Four USB 2.0 available on USB header
  - Two USB 2.0 on PCIe/104 OneBank
  - One USB 2.0 on M.2
- USB 3.2 Gen 1 (5 Gbps) port on USB Type-C, with over-current protection

Audio

- Hi-definition (HD) audio on DisplayPort interface
- Stereo audio (line in, line out, mic) on LVDS interface

Power

- Wide range input power: 9 to 36 VDC
- External battery connector, operates with no battery connected
- +5 V and +12 V SATA power

Industrial Operating Temperature

- -40 to +85°C (-40 to +185°F)[1]

Additional Features

- Hardware security - Trusted Platform Module (TPM 2.0) enabled
- Watchdog timer adjustable from 1 second to 255 minute reset
- RoHS compliant

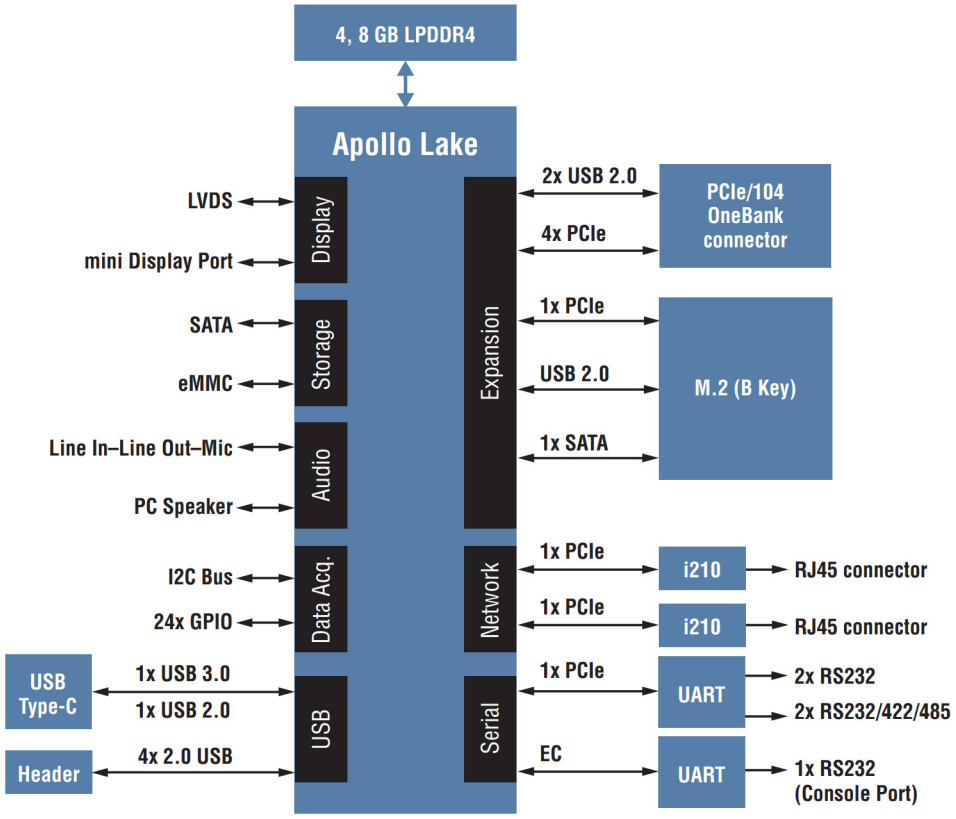
1. Requires airflow.

- Backlight power supported
- Custom splash screen on startup
- Intel low-power Gen9 graphics engine
- Intel security engine

5. General Operation

5.1 System Block Diagram

WINSYSTEMS' PX1-C441 single board computer (SBC) is a PC/104 form factor SBC with PCIe/104™ OneBank™ expansion featuring the latest generation Intel Apollo Lake-I SOC processor. Its small size, rugged design and extended operational temperature make it a great fit for industrial IoT applications and embedded systems in the industrial control, transportation, Mil/COTS, and energy markets.



The SBC is software-compatible with Linux, Windows, and most x86 operating systems, including legacy support for DOS.

Drivers are available from the WINSYSTEMS website.

6. Specifications

The PX1-C441 adheres to the following specifications and requirements.

Feature	Specification
Electrical	
V_{CC}	Supports a wide range DC input of 9 to 36 V
Models	PX1-C415-39xx-0-0
Processor	E3930 x5 dual core up to 1.8 GHz E3940 x5 quad core up to 1.8 GHz E3950 x7 quad core up to 2.0 GHz
Mechanical	
Dimensions	4.55 x 4.393 in. (115.6 x 111.6 mm)
Weight	4.3 oz. (120 g), without heat sink
PCB thickness	0.078 in. (1.98 mm)
Environmental	
Temperature	-40 to +85°C (-40 to +185°F)[a]
Humidity (RH)	5% to 95% non-condensing
Mechanical shock testing	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis
Random vibration testing	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis
Mean time between failure (MTBF) [b]	Simulation: • Predication standard: Bellcore TR-332, Issue 6 (SR-332 Issue 1), Electronics • Environmental: Temperature 40°C, L1 • Failure rate: 8.876 (FPMH) • MTBF: 112,664.891 (hrs)
RoHS compliant	Yes
Operating Systems	
Runs 64-bit Windows, Linux, and other x86-64-compatible operating systems.	

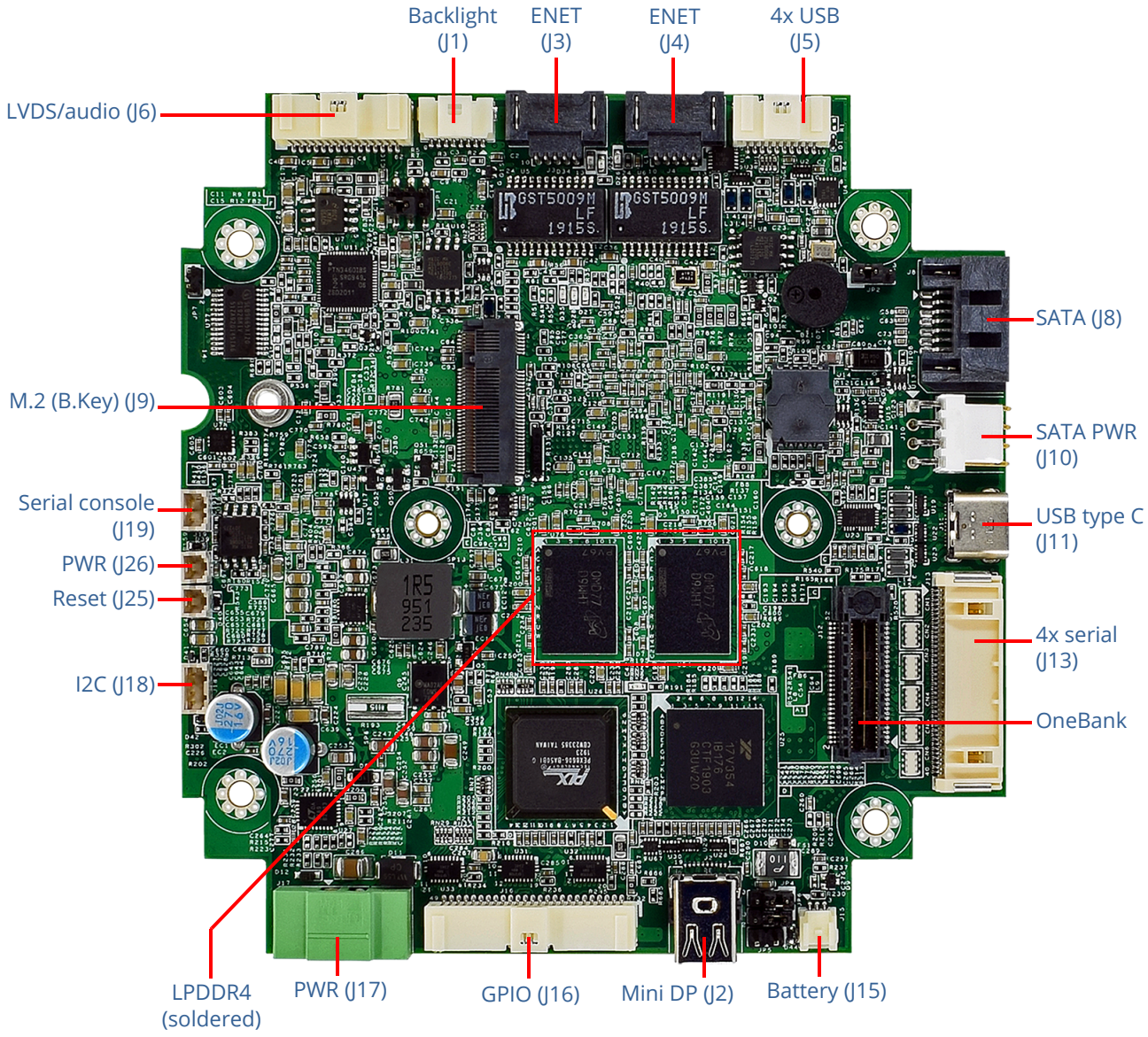
a. Requires airflow.
b. A MTBF measurement is based on a statistical sample and is not intended to predict any one specific unit's reliability; thus MTBF is not, and should not be construed as, a warranty measurement.

7. Configuration

This section describes the PX1-C441 components and configuration.

7.1 Component Layout

7.1.1 Top View

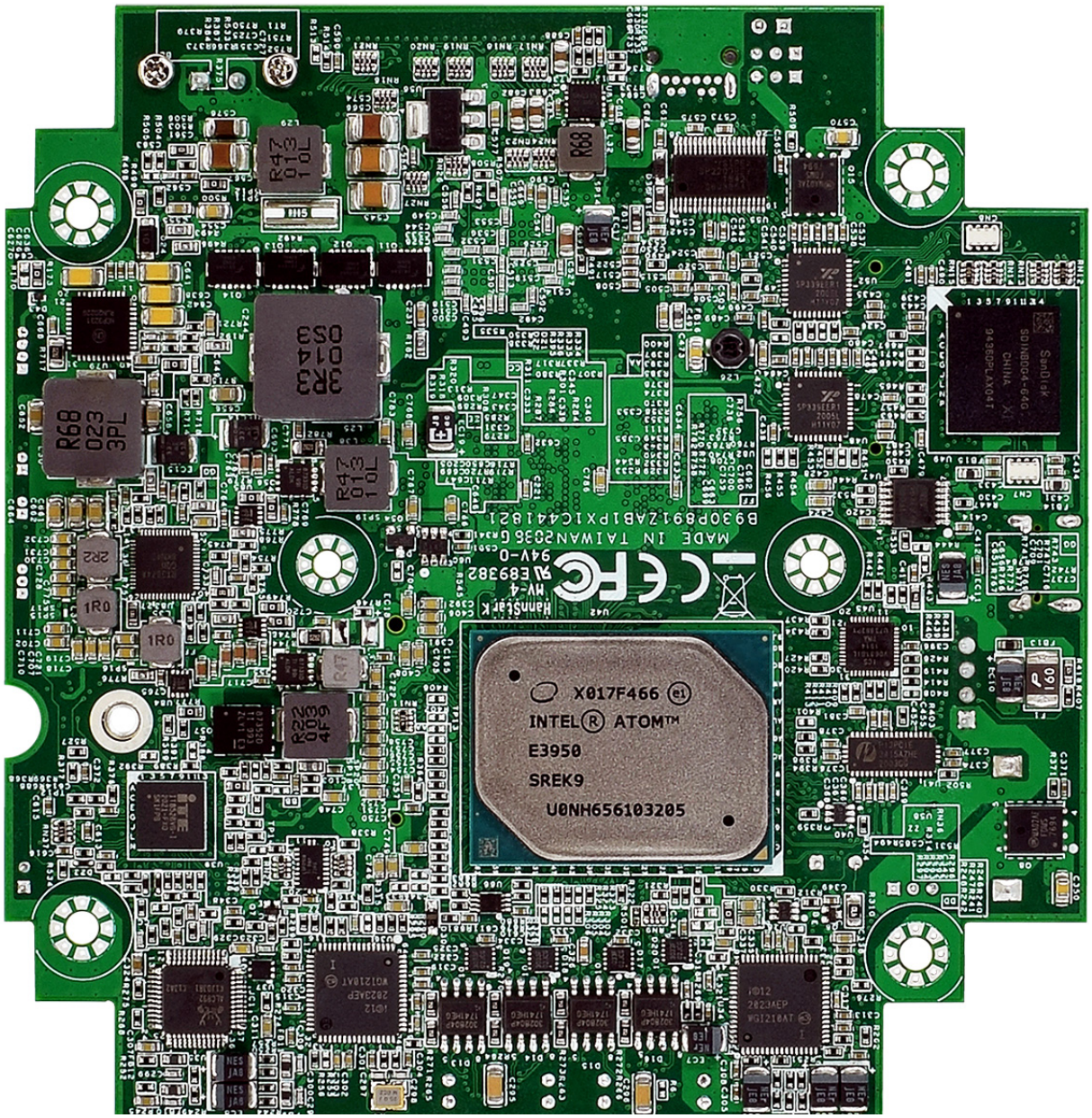


Top view components

Item	Description	Reference
Power		
J17	Power input	page 16
J15	CMOS battery input	page 16
J10	SATA power output	page 18
J1	LVDS backlight power	page 18
J26	Power button	page 19
J25	Reset button	page 19
Memory and Storage		
	LPDDR4 memory	page 19
	eMMC onboard	page 19
J9	M.2 SSD	page 19
J8	SATA 3 (6 Gbps)	page 26
Video and Audio		
J2	Mini DisplayPort++	page 20
J6	LVDS data and HD audio	page 20
BZ1	Buzzer speaker	page 21
System I/O		
J3/J4	Ethernet 1 and 2	page 21
J5	USB 2.0 ports	page 22
J11	USB 3.2 Gen 1 Type-C	page 23
J13	Serial ports 1–4	page 23
J19	Serial RS232 console	—
J16	GPIO (general purpose digital I/O)	page 25
J18	I2C bus	—
Jumpers and LEDs		
JP1	LVDS voltage select	page 27
JP2	M.2 device type select	page 27
JP4	Backlight voltage select	page 27
JP7	BIOS reset defaults	page 27
D3	System power good/activity LED	page 28
D7	PCIe power link	page 28
D25	Ethernet 1 operating at 1000 Mbps	page 28
D28	Ethernet 2 operating at 1000 Mbps	page 28
D26	Ethernet 1 link activity	page 28
D27	Ethernet 2 link activity	page 28
D34	Ethernet 1 operating at 100 Mbps	page 27
D35	Ethernet 2 operating at 100 Mbps	page 27

7.1.2 Bottom View

There are no connectors on the bottom of the board.



7.2 PCI Devices and Functions

Internal devices

Bus	Device	Function	Device ID	Device/Function Description
0	0	0	0F00h	Device: SoC transaction router
0	2	0	0F31h	Device: Graphics and display
0	19	0	0F20h (IDE) 0F21h (IDE) 0F22h (AHCI) 0F23h (AHCI)	Device: SATA
0	26	0	0F18h	Device: Trusted execution engine
0	27	0	0F04h	Device: HD audio
0	28	0	0F48h	Device: PCI Express*
				Function: Root port 1
		1	0F4Ah	Device: PCI Express*
				Function: Root port 2
		2	0F4Ch	Device: PCI Express*
				Function: Root port 3
		3	0F4Eh	Device: PCI Express*
				Function: Root port 4
0	29	0	0F34h	Device: EHCI USB
0	31	0	0F1Ch	Device: Platform controller unit
				Function: LPC: Bridge to Intel legacy block
0	31	3	0F12h	Device: Platform controller unit
				Function: SMBus port

External devices

Bus	Device	Function	Device ID	Device/Function Description
3	0	0	104Ch	Device: 8240
				Function: PCI/PCI bridge
5	0	0	12D8h	Device: 2304
				Function: PCI/PCI bridge
6	1	0	12D8h	Device: 2304
				Function: PCI/PCI bridge
6	2	0	12D8h	Device: 2304
				Function: PCI/PCI bridge
7	0	0	8086h	Device: 8086
				Function: Intel Ethernet controller
8	0	0	8086h	Device: 8086
				Function: Intel Ethernet controller

7.3 Watchdog Timer (WDT)

The PX1-C441 features an advanced watchdog timer (WDT) to guard against software lockups; it resets the system if software does not pet the watchdog within the given time-out period. The WDT is implemented in the ITE8528 embedded controller present on the platform. The registers

for the WDT can be accessed using the ACPI port 62/66 access mechanism. WINSYSTEMS supports the PX1-C441 WDT in the System Management tools for the PX1-C441. Ask your sales representative for details of this software package.

WDT Registers

ACPI Shared RAM Offset of WDT Register	WDT Register Description
0x06	WDT CONFIGURATION
0x07	WDT MINUTES COUNTER
0x08	WDT SECONDS COUNTER

7.3.1 WDT Register Usage

Configuration Register (offset 0x06)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not used	Not used	Not used	Not used	Not used	Not used	WDT mode	WDT enable

WDT enable	0 = disabled, 1 = enabled
WDT mode	0 = seconds mode, 1 = minutes mode

Minutes Counter Register (0x07)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB							LSB

In minutes mode, this register is programmed with the countdown values in minutes. The maximum countdown time when in minutes mode is (2^8 - 1 minutes).

Seconds Counter Register (0x08)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB							LSB

In seconds mode, this register is programmed with the countdown values in seconds. The maximum countdown time when in seconds mode is (2^8 - 1 seconds).

To use the WDT, set the *WDT mode* bit in the configuration register to the desired mode (seconds or minutes), then program the appropriate counter register (minutes or seconds) with the desired countdown value. Then start the WDT by setting the *WDT enable* bit in the configuration register. The WDT begins counting down in the selected mode, and unless the WDT is disabled or reset/pet (see below), the board is reset when the counter register is equal to 0.

To reset or "pet" the watchdog timer, rewrite the minutes or seconds counter register with the countdown value.

To stop the WDT, clear the *WDT enable* bit in the configuration register.

7.4 Real-time Clock/Calendar

A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date-keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be enabled for the real-time clock to retain time and date during a power down.

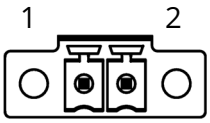
WINSYSTEMS has software available for manipulating the CMOS RTC from a high-level application.

7.5 Connectors

7.5.1 J17 - VIN Power Connector

Use this connection to supply power to the PX1-C441. This computer supports a wide range DC input power from 9 V to 36 V.

Layout and Pin Reference



Pin	Name
1	PWR+
2	GND

Connector

- Phoenix 1827868 (J17)

Matching Connectors

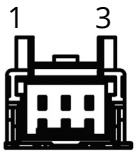
- Phoenix 1827703 (housing)

7.5.2 J15 - CMOS Battery Input

An external battery connected to the PX1-C441 provides standby power for the real-time clock (RTC). An extended temperature lithium battery is available from WINSYSTEMS, part number BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2.

A power supervisory circuit controls an internal power switch to route the battery or standby voltage to the RTC. If power is removed from the system, or the power input voltage drops below the battery voltage, the RTC circuit automatically fails over to battery power.

Layout and Pin Reference

Pin	Name	Description
		
1	GND	Ground
2	VBAT	Battery input voltage
3	NC (no connect)	No connect

WARNING: BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2 must be connected at **J15**. Improper installation of the battery could result in explosive failure. Be careful to note the correct connection at location **J15**.

Connector

- Molex 501953-0307 1x3, 1 mm pitch (Pico-Clasp™) (**J15**)

Matching Connectors

- Molex 501939-0300 (housing)
- Molex 501334-0100 OR 501334-0000 (crimp)

WINSYSTEMS battery BAT-LTC-E-36-16-2 and BAT-LTC-E-36-27-2 simplify these connections to the board.

BAT-LTC-E-36-16-2

BAT-LTC-E-36-27-2

7.5.3 J10 - SATA Power Output

Layout and Pin Reference

Pin	Name
	
1	+12V
2	GND
3	GND
4	+5V

Connector

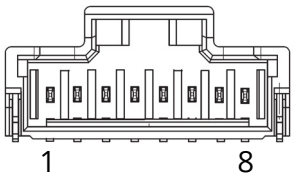
- Molex 22-12-2044, 1x4 (J10)

Matching Connectors

- Molex 10-11-2043 (housing)
- Molex 08-55-0124 OR 08-55-0129 (crimp)

7.5.4 J1 - LVDS Backlight Power

Layout and Pin Reference

	Pin	Name	Description
	1	+5VDC	Power
	2	LBKLT_EN_N	Active low backlight enable
	3	LBKLT_EN_P	Active high backlight enable
	4	GND	Ground
	5	+12VDC	+12V backlight power
	6	PWM	PWM dimmer signal
	7	NC	Not connected
	8	NC	Not connected

Connector

- Molex 50156-0807, 1x8, 1 mm pitch (Pico-Clasp) (**J1**)

Matching Connectors

- Molex 501330-0800 (housing)
- Molex 501334-0000 (crimp)

Cable

- CBL-LVDSAB-009-18 (LVDS with analog audio)

add these two sections before LPDDR4 Memory

7.5.5 J26 - Power Button

The PX1-C441 turns on automatically when power is applied to the computer and does not require the power button to be pressed.

The power button connector can be used to wake the computer after shutdown, sleep, or system standby if power is not removed. A momentary switch that shorts the power pin and GND pin together activates the power button input.

This power button also functions with operating system power options, such as safely shutting down the computer or putting the computer to sleep.

Holding the power button for roughly 5 seconds performs a hard reset to the computer.

7.5.6 J25 - Reset Button

The reset button instantly performs a hard reset to the computer.

NOTE To avoid potential operating system corruption, the reset button should only be used when the computer cannot safely shutdown or restart due to a software crash or hardware fault. If the reset button operation is desired, an OS write protect filter is highly recommended.

7.5.7 LPDDR4 Memory

The PX1-C441 provides up to 8 GB of soldered down LPDDR4 system memory (RAM).

7.5.8 eMMC Onboard

The PX1-C441 offers an eMMC solid state disk that provides up to 64 GB of soldered down, onboard storage.

Contact a WINSYSTEMS applications engineer at +1-817-274-7553 for details.

7.5.9 J9 - M.2 Connector (B Key)

The M.2 expansion socket provides support for B key, 2230, and 2242 modules. The M.2, B key interface provides PCIe Gen 2 x2, 1x SATA channel, 1x USB 2.0, and 1x USB 3.2 Gen 1. B key modules typically support M.2 SSDs.

7.5.10 J8 - SATA 3 (6 Gbps)

The PX1-C441 supports one SATA 3 (6 Gbps) interface.

7.5.11 J2 - Mini DisplayPort++

Standard mini DisplayPort++ (Version 1.2).

NOTE Both Mini DisplayPort and LVDS outputs may be active simultaneously.

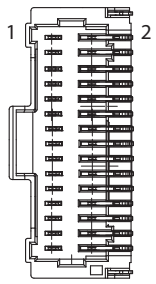
7.5.12 J6 - LVDS Data and HD Audio

The PX1-C441 provides one single channel, low voltage differential signaling (LVDS) interface and backlight power (see “J1 - LVDS Backlight Power” on page 18).

The LVDS panel voltage (SWVDD) is user selectable via jumper **JP1**. Voltage options available are 3.3 V, 5 V, and 12 V (see “JP1 - LVDS Voltage Select” on page 27).

NOTE Both LVDS and Mini DisplayPort outputs may be active simultaneously.

Layout and Pin Reference



Pin	Name	Pin	Name
1	SWVDD	2	GND
3	D0-	4	D0+
5	D1-	6	D1+
7	SWVDD	8	GND
9	D2-	10	D2+
11	D3-	12	D3+
13	SWVDD	14	GND
15	CLK-	16	CLK+
17	DDC_CLK	18	GND
19	DDC_DATA	20	GND
21	GND	22	AGND
23	OUT_R	24	MIC1_R
25	OUT_L	26	MIC1_L
27	AGND	28	AGND
29	LINE_R	30	LINE_L

Additional Information

WINSYSTEMS offers these cables for the LVDS interface:

- CBL-LVDSAB-009-18 (LVDS with analog audio)
- CBL-SPL-001-14 (analog audio, unterminated LVDS lines)

Connector

- Molex 501571-3007, 2x15, 1 mm pitch (Pico-Clasp) (**J6**)

Matching Connector

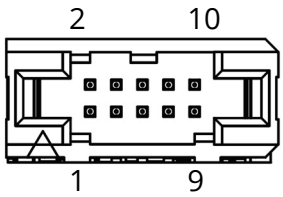
- Molex 501189-3010 (housing)
- Molex 501193-2000 (crimp)

7.5.13 BZ1 - Buzzer Speaker

An onboard speaker, BZ1, is available for sound generation. The BIOS activates the buzzer during POST. In case of POST failure, each error has its own unique beep code. Refer to “BIOS Status and Errors” for details.

7.5.14 J3 and J4 - LAN Ethernet Ports

Layout and Pin Reference

J3/J4	Pin	100Base-T	1000Base-T
	1	TX+	BI_DA+
	2	TX-	BI_DA-
	3	RX+	BI_DB+
	4		BI_DC+
	5		BI_DC-
	6	RX-	BI_DB-
	7		BI_DD+
	8		BI_DD-
	9	GND	GND
	10	GND	GND

Additional Information

The PX1-C441 is equipped with two Intel i210 Gigabit Ethernet controllers. Each controller provides a standard IEEE 802.3 Ethernet interface for 1000/100/10BASE-T networks. The connections for each Ethernet port are available at **J3** and **J4**.

Onboard Ethernet activity LEDs D26, D25, and D24 provide status for Port 1. LEDs D27, D28, and D35 provide status for Port 2. These LEDs indicate operation at 1 Gbps, link activity, and operation at 100 Mbps. (See “LED Indicators D3 - D35” on page 28.)

WINSYSTEMS offers the cable CBL-ENET1-302-12 to simplify this connection. This cable interfaces with one Ethernet connection only. A second cable is required for dual Ethernet operation.

Connector

- Samtec TFM-105-02-L-DH (**J3** and **J4**)

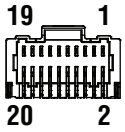
Mating Connector

- Samtec ISDF-05-D-M (housing)
- CC03L-2830-01-G or CC03R-2830-01-G (crimp)

7.5.15 J5 - USB 2.0 Ports

The PX1-C441 supports four USB 2.0 ports through one onboard connector. They feature ESD suppression, as well as short circuit and overload protection.

Layout and Pin Reference

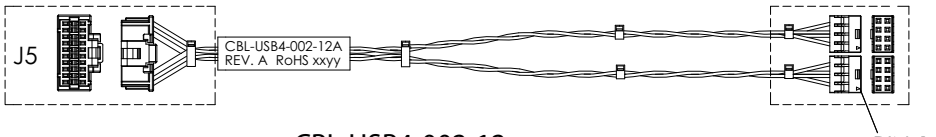
Pin	Name	Pin	Name
USB (J5) 			
1	USB0_PWR	2	USB1_PWR
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	USB_GND	8	USB_GND
9	USB_GND	10	USB_GND
11	USB_GND	12	USB_GND
13	USB2_PWR	14	USB3_PWR
15	USB2-	16	USB3-
17	USB2+	18	USB3+
19	USB_GND	20	USB_GND

Connector

- Molex 501571-2007, 2x10, 1 mm pitch (Pico-Clasp) (**J5**)

Matching Connectors

- Molex 501189-2010 (housing)
- Molex 501193-2000 (crimp)



CBL-USB4-002-12

The USB cable terminates to the 20-pin connector at **J5**. Use WINSYSTEMS cable CBL-USB4-000-14, CBL-USB4-001-12, or CBL-USB4-002-12, along with ADP-IO-USB-001.

7.5.16 J11 - USB 3.2 Gen 1 Type-C

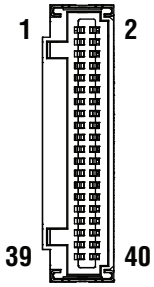
One USB 3.2 Gen 1 (5 Gbps) port is supported with a Type-C onboard connector.

7.5.17 J13 - Serial Ports 1–4

Serial Ports 1–4 RS232/RS422/RS485 Connectors

The PX1-C441 provides four 16550-compatible serial ports through COM A to COM D. COM C and COM D support RS232, RS422, and RS485 modes. COM A and COM B are RS232 only. Mode selection (RS232/RS422 or RS485 half duplex/full duplex) is selectable in the BIOS. All other capabilities are enabled/disabled through the provided device driver.

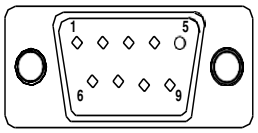
Layout and Pin Reference



Pin	Name	Pin	Name
1	COM1_DCD	2	COM1_DSR
3	COM1_RX	4	COM1_RTS
5	COM1_TX	6	COM1_CTS
7	COM1_DTR	8	COM1_RI
9	GND	10	NC
11	COM2_DCD	12	COM2_DSR
13	COM2_RX	14	COM2_RTS
15	COM2_TX	16	COM2_CTS
17	COM2_DTR	18	COM2_RI
19	GND	20	NC
21	COM3_DCD	22	COM3_DSR
23	COM3_RX	24	COM3_RTS
25	COM3_TX	26	COM3_CTS
27	COM3_DTR	28	COM3_RI
29	GND	30	NC
31	COM4_DCD	32	COM4_DSR
33	COM4_RX	34	COM4_RTS
35	COM4_TX	36	COM4_CTS
37	COM4_DTR	38	COM4_RI
39	GND	40	NC

Serial Ports 1–4 DB9 Male Connector

Layout and Pin Reference

	Pin	RS232	RS422	RS485
	1	DCD	NA	NA
	2	RX	TX+	TX/RX+
	3	TX	TX-	TX/RX
	4	DTR	NA	NA
	5	GND	GND	GND
	6	DSR	RX+	NA
	7	RTS	RX_	NA
	8	CTR	NA	NA
	9	RI	NA	NA

All ports are configured as data terminal equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS232 has a charge pump to generate the plus and minus voltages so the PX1-C441 only requires +5 V to operate. An independent, software-programmable baud rate generator is selectable from 300 through 921.6 kbps. Individual modem handshake control signals are supported for all ports.

WINSYSTEMS cables simplify connections to the board:

- CBL-SER4-000-14: Duo-Clasp™ to unterminated
- CBL-SER4-001-12: Duo-Clasp to Duo-Clasp
- CBL-SER4-002-12: Duo-Clasp to 4xDB9

Connector

- Molex 502046-4070, 2x20, 1.25 mm pitch (Duo-Clasp) (**J13**)

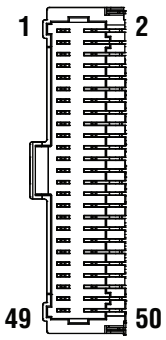
Matching Connectors

- Molex 503110-4000 (housing)
- Molex 501930-1100 (crimp)

7.5.18 J16 - GPIO24 General-Purpose Input/Output

The PX1-C441 supplies 24, 5 V-tolerant GPIO lines with rising/falling edge event sense interrupt generation.

Layout and Pin Reference



Pin	Name	Pin	Name
1	GPIO1_C7	2	GND
3	GPIO2_C6	4	GND
5	GPIO3_C5	6	GND
7	GPIO4_C4	8	GND
9	GPIO5_C3	10	GND
11	GPIO6_C2	12	GND
13	GPIO7_C1	14	GND
15	GPIO8_C0	16	GND
17	GPIO9_B7	18	GND
19	GPIO10_B6	20	GND
21	GPIO11_B5	22	GND
23	GPIO12_B4	24	GND
25	GPIO13_B3	26	GND
27	GPIO14_B2	28	GND
29	GPIO15_B1	30	GND
31	GPIO16_B0	32	GND
33	GPIO17_A7	34	GND
35	GPIO18_A6	36	GND
37	GPIO19_A5	38	GND
39	GPIO20_A4	40	GND
41	GPIO21_A3	42	GND
43	GPIO22_A2	44	GND
45	GPIO23_A1	46	GND
47	GPIO24_A0	48	GND
49	+5V	50	GND

Connector

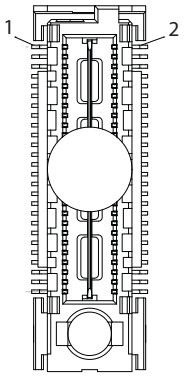
- Molex 501571-5007 2x25, 1 mm pitch (Pico-Clasp) (**J16**)
- (WS G650-2050-7HB)

Cables

- CBL-DIO24-001-12: Pico-Clasp to Pico-Clasp
- CBL-DIO24-002-12: Pico-Clasp to 2x25, 0.1” pitch housing

7.5.19 J12 - PCIe OneBank

Layout and Pin Reference



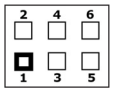
Pin	Name	Pin	Name
1	USB_OC#	2	PE_RST#
3	3.3V_1	4	3.3V_2
5	USB_1P	6	USB_0P
7	USB_1N	8	USB_0N
9	GND1	10	GND2
11	PEx1_1TP	12	PEx1_0TP
13	PEx1_1TN	14	PEx1_0TN
15	GND3	16	GND4
17	PEx1_2TP	18	PEx1_3TP
19	PEx1_2TN	20	PEx1_3TN
21	GND5	22	GND6
23	PEx1_1RP	24	PEx1_0RP
25	PEx1_1RN	26	PEx1_0RN
27	GND7	28	GND8
29	PEx1_2RP	30	PEx1_3RP
31	PEx1_2RN	32	PEx1_3RN
33	GND9	34	GND10
35	PEx1_1CLKP	36	PEx1_0CLKP
37	PEx1_1CLKN	38	PEx1_0CLKN
39	+5V_SB_1	40	+5V_SB_2
41	PEx1_2CLKP	42	PEx1_3CLKP
43	PEx1_2CLKN	44	PEx1_3CLKN
45	DIR	46	PWRGOOD
47	SMB_DAT	48	NC
49	SMB_CLK	50	NC
51	SMB_ALERT	52	PSON#

7.6 Jumpers

NOTE Jumper part number SAMTEC 2SN-BK-G applies to all jumpers. These are available in ten-piece kits from WINSYSTEMS. Order part number KIT-JMP-G-200.

7.6.1 JP1 - LVDS Voltage Select

Layout and Pin Reference

	Selection	Jumper Positions
	3.3V	Jumper pins 1 and 3 together
	5V	Jumper pins 3 and 5 together
	12V	Jumper pins 3 and 4 together

7.6.2 JP2 - M.2 Device Type Select

Select either MiniPCIe or mSATA at socket **J9**.

Layout and Pin Reference

	Selection	Jumper Positions
	mSATA	Jumper pins 1 and 2 together
	mPCIe	Jumper pins 2 and 3 together

7.6.3 JP4 - Backlight Voltage Select

Select either 5 or 12 V for backlight voltage level.

Layout and Pin Reference

	Selection	Jumper Positions
	Backlight voltage 5V	Jumper pins 1 and 2 together
	Backlight voltage 12V	Jumper pins 2 and 3 together

7.6.4 JP7 - CMOS Clear

A jumper provided onboard enables you to reset the BIOS CMOS settings to factory defaults. The BIOS reads this pin during system boot and forces the settings to reset if the pin is at ground.

To reset the BIOS CMOS parameters, place jumper **JP7** in the **Clear CMOS entries** mode, apply power to the board, and let it boot into the BIOS. Power off the board, and restore **JP7** to the **Normal operation** position.

Layout and Pin Reference

	Selection	Jumper Positions
	Normal operation	Jumper pins 1 and 2 together
	Clear CMOS entries	Jumper pins 2 and 3 together

7.7 LED Indicators D3 - D35

The activity LED is on the Atom E3900 GPIO_27 and can be accessed at address 0xD0C505D8. Setting the GPIO pin high turns on the LED, setting it low turns off the LED.

LED Reference

LED	Description	Color
D3	System power good	
D7	PCIe power link	Green
D25	Ethernet 1 1000 Mbps	Amber
D26	Ethernet 1 Link	Green
D27	Ethernet 2 Link	Green
D28	Ethernet 2 1000 Mbps	Amber
D34	Ethernet 1 100 Mbps	Green
D35	Ethernet 2 100 Mbps	Green

8. BIOS Functionality

The BIOS used in this design is a custom version of the AMI Aptio V x86 BIOS.

8.1 References

The following Intel Atom E3900 BIOS specification documents can assist developers in the creation of firmware for the Intel Atom E3900:

- Intel Atom E3900 Platform Intel Architecture Firmware Specification (Volume 1 of 2), Document Number 559810
- Intel Atom E3900 Platform Intel Architecture Firmware Specification (Volume 2 of 2), Document Number 559811
- Intel Dynamic Platform and Thermal Framework (Intel DPTF) v8.x 201 - Rev 1.1, Document Number 556073

8.2 Glossary

- **advanced configuration and power interface (ACPI):** Specification that establishes industry standard interfaces enabling OS directed configuration, power management and thermal management of mobile, desktop, and server platforms.
- **dynamic video memory technology (DVMT):** Allows dynamic allocation of system memory for use as video memory to ensure the most efficient use of available resources in order to maximize 2D/3D graphics performance.
- **graphics processing unit (GPU):** Specialized electronic circuit designed to rapidly manipulate and alter memory to accelerate the creation of images in a frame buffer.
- **integrated graphics device (IGD):** Graphics processor integrated into the Intel Atom E3900 SOC. The IGD in the Atom E3900 SOC is an Intel 9th Generation GPU, also called Gen9 GPU.
- **Unified Extensible Firmware Interface (UEFI):** Specification that defines a software interface between an operating system and platform firmware. UEFI replaces the basic input/output system (BIOS) firmware interface

8.3 BIOS Settings

This section provides details on the system parameters that are managed by the BIOS. If a BIOS parameter can be changed, details on the possible parameter values are included.

8.3.1 Main

The Main page of the BIOS displays general information related to the current BIOS build, including the BIOS and embedded controller firmware revisions, the revision of built in SOC device firmware, and CPU-specific values (processor stepping and name).

The Main BIOS page also contains information related to the amount and configuration of the system RAM (the type of RAM used in the design).

The following BIOS build information is available on the Main BIOS page.

Project Name:	PX1-C441
BIOS Version & Build Date:	71215T00 (12/15/2017 18:18:05)
EC Version & Build Date:	70605T01 (06/05/2017)
Access Level:	Administrator
Processor information Brand String	Intel Atom Processor E39X0 @ 1.30 GHz

Platform Firmware Information	
BXT SOC	B1
TXE FW	3.1.50.2222
GOP	10.0.1035
CPU Flavor	BXT Notebook/Desktop [a]
Memory Information	
Total Memory	8192 MB
Memory Slot 0	8192 (DDR3L ECC)
Memory Speed	1600 MHz
System Date	[Mon 03/27/2017]
System Time	[09:51:15]

a. The CPU Flavor field reflects the actual Atom E3900 processor installed on the PX1-C441 platform. In this case, it indicates that the processor is an industrial Intel Atom E39x0 processor, but it could also indicate the processor is a Celeron N3350 @ 1.10 GHz, or a Pentium N4200 @ 1.10 GHz.

8.3.2 Configuration

The BIOS Configuration page serves as the top-level BIOS page for configuring peripherals and devices present on the PX1-C441 platform. The configuration sub-pages include but are not limited to pages for the CPU, network interfaces, serial ports, USB ports, and SATA. The settings for each configuration sub-page are described in the device sections.

CPU Configuration

The configuration values related to the CPU cores, CPU cache, CPU patch level, and integrated CPU capability are detailed on this BIOS page.

CPU signature	506C9
Microcode patch level	20
Max CPU speed	1300 MHz
Min CPU speed	800 MHz
Processor cores [a]	2
Intel HT Technology [b]	Not supported
Intel VT-x Technology [c]	Supported
64-bit [d]	Supported
L1 data cache	24 kB x 2
L1 code cache	32 kB x 2
L2 cache	1024 kB x 1
L3 cache	Not present

Active Processor Cores [e]	[Disabled/enabled]
Core 0 [f]	[Enabled/disabled]
Core 1 [g] [h]	[Enabled/disabled]
Intel Virtualization Technology [i]	[Enabled/disabled]
VT-d [j]	[Enabled/disabled]
CPU power management configuration	
EIST [k]	[Enabled/disabled]
Turbo Mode	[Enabled/disabled]
C-States	[Enabled/disabled]
Enhanced C-states	[Enabled/disabled]

a. The PX1-C441 used to help define the BIOS requirements contained an E3930 dual-core SOC. The PX1-C441 board also supports the use of the E3940 and E3950 quad-core SOCs.
b. Intel Hyper Threading technology - a proprietary technology that enhances the CPU's multi-threading capability to allow parallelization of computations. HTT is not implemented in the Intel Atom E3900 SOC.
c. VT-x is Intel's proprietary processor virtualization technology.
d. 64-bit technology is the ability of the CPU to execute 64 bit instructions.
e. Allows individual processor cores to be enabled or disabled.
f. Core 0 is not visible if Active Processor Cores is disabled.
g. Core 1 is not visible if Active Processor Cores is disabled.
h. If the board is populated with an E3940 or E3950 SOC, this list includes Core 2 and Core 3 devices.
i. If the CPU contains the Intel VT-x technology, then this field can be used to enable/disable the built-in virtualization capabilities.
j. VT-d is the ability of the SOC to allow direct access to built-in peripherals by running virtual machines. It is sometimes referred to as IO MMU virtualization.
k. EIST is also known as SpeedStep technology. This technology allows the clock speed of the processor to be dynamically modified by software.

Memory Configuration

ECC Error Rate Injection	No Error
Refresh Rate of 2x [a]	Enable

a. Ensures that refresh rate never drops below 2x. Enable:2x Disable:1x.

Chipset Configuration

High Precision Timer	[Enable/disable]
HD-Audio Support	[Enable/disable]
8254 Clock Gating [a]	[Enable/disable]

a. 8254 clock gating allows shutdown of the crystal. It is used for maximum power saving.

LAN Configuration

The LAN configuration page displays the MAC addresses for the built-in Ethernet NICs, and allows network features to be enabled or disabled. Features that can be enabled in the BIOS include Wake On LAN and PXE network boot.

Wake On LAN [a]	[Enable/disable]
Intel Ethernet Controller WGI210AT LAN MAC Address	XX:XX:XX:XX:XX:XX
Intel Ethernet Controller WGI210AT LAN MAC Address	XX:XX:XX:XX:XX:XX
Launch UEFI RXE Rom	[Enabled/disabled]
PXE ROM [b]	
IPv4 PXE Support	[Enabled/disabled]
IPv6 PXE Support	[Enabled/disabled]

a. Wake On LAN is a feature that allows a computer to be awoken or powered on when a wake packet is detected on the network interface.
b. PXE boot is a BIOS feature that allows a computer to boot its operating system and root file system across a network. It is useful when implementing diskless workstation.

Graphics Configuration

The graphics configuration page of the BIOS allows the user to specify settings used by the Intel Gen9 GPU.

DVMT Pre-Allocated [a]	[64M/96M/128M/160M/192M/224M/256M/288M/320M/352M/384M/416M/448M/480M/512M]
IGD Output Display Control - GOP	
GOP driver	[Enable/Disable]
IGD Output Display Control - CSM [b]	
Primary IGFX Boot Display	[AUTO, EFP, LFP, EFP2]
Secondary IGFX Boot Display [c]	[Disabled,EFP,LFP,EFP2]

a. The DVMT RAM amount selects the pre-allocated (fixed) graphics memory size used by the IGD.
b. These settings select the video device that is activated during the POST.
c. The Secondary IGFX Boot Display selection is not enabled unless the Primary IGFX Boot Display is set to some value other than AUTO. If the Primary IGFX Boot Display is set to EFP, LFP, or EFP2, then the Secondary IGFX Boot Display settings become visible, and can be set to one of the built in values (EFP, LP, EFP2).

eDP-to-LVDS Configuration

The parameters under this configuration page define how the embedded DisplayPort is mapped to the LVDS display interface, and permit the user to set the LVDS panel profile.

Panel Profile [a]	[640x480,800x480,800x600,1024x768,1280x800,1280 x1024,1366x768,1440x900,1920x1080, OEM Profile]
Color Depth and data format [b]	[VESA 24BPP, JEIDA 24BPP, VESA and JEIDA 18BPP]
Channel Mode	[Single Channel, Dual Channel]
Clock Mode	[Even Bus, Odd Bus, Both Buses]
OEM Profile [c]	
Profile Name	
Color Depth and data	
Channel Mode	
Pixel Clock	
H Active Pixels	
H Blank Pixels	
H Offset Pixels	
H Width Pixels	
V Active Lines	
V Blank Lines	
V Offset Lines	
V Width Lines	
H & V sync Signal Polarity	[Positive, Non-Positive]

a. Specifies the geometry and mode of the attached LVDS display.
b. Allows the bits per pixel and pixel data format to be specified.
c. The OEM profile allows a user to define a non-standard LVDS display profile.

PCI/PCIe Configuration

This section allows the user to set the PCI, PCI-X and PCI-express parameters.

PCI Express Root Port 1 - 6	
PCI Express Root Port #	[Enable/disable]
ASPM [a]	[Enable/disable]
Hot Plug	[Enable/disable]

PCIe Speed	[Auto/Gen1/Gen2/Gen3]
PCIe Selectable De-emphasis	[Enable/disable]
PCIe Port configuration table [b]	

a. Active State Power Management - A power conservation protocol used with PCI serial devices that places the device into a low power mode as the device becomes less active over time.
b. Displays PCIe port configuration, link width, and link speed for any PCIe device present

SATA Configuration

The SATA configuration page is used to configure and enable the PX1-C441's SATA functionality.

SATA Controller [a]	[Enable/Disable]
SATA Speed Selection [b]	[Auto/Gen1/Gen2/Gen3]
SATA Port 0	{Installed device name}
Port 0	[Enable/Disable]
SATA Port 0 Hot Plug Capability	[Enable/Disable]
SATA Device Type	[Hard Disk Drive/Solid State Drive]
SATA Port 1	{Installed device name}
Port 1	[Enable/Disable]
SATA Port 1 Hot Plug Capability	[Enable/Disable]
SATA Device Type	[Hard Disk Drive/Solid State Drive]

a. Enables or disables the built in SATA controller.
b. Selects the SATA interface speed. SATA Gen1 speed is 1.5 Gbits/second, Gen2 is 3.0 Gbits/second, and Gen3 is 6.0 Gbits/second.

USB Configuration

This set of BIOS parameters specifies the setup and configuration of the USB interfaces present on the PX1-C441 board.

USB Controller	
1 XHCI	
USB Devices	
1 Drive, 1 Keyboard, 1 Mouse, 1 Hub [a]	
SOC USB Configuration	
USB Port #0	[Enable/Disable]
USB Port #1	[Enable/Disable]

USB Port #2	[Enable/Disable]
USB Port #3	[Enable/Disable]
USB Port #4	[Enable/Disable]
USB Port #5	[Enable/Disable]
USB Port #6	[Enable/Disable]
USB Port #7	[Enable/Disable]
Common USB Configuration	
Legacy USB Support [b]	[Enable/Disable]
USB Mass Storage Driver Support	[Enable/Disable]
USB hardware delays and time-outs	
USB Transfer time-out	[1/5/10/20 seconds]
Device reset time-out	[10/20/30/40 seconds]
Device power-up delay	[Auto/Manual]
Device power-up delay in seconds [c]	[1..40 seconds]
Mass Storage Devices [d]	
SanDisk	[Auto/Floppy/Forced FDD/Hard Disk/ CD-ROM]

a. Contents of this line depend upon the devices connected to the USB ports at boot time.
b. Legacy USB support and USB mass storage driver support are used with the Compatibility System Module to support the booting of legacy (non-UEFI) operating systems.
c. This field only appears when **Device power-up delay** is set to **Manual**.
d. Devices displayed below this line depend on the devices plugged into USB ports at the time the system booted.

Power Control Configuration

Enable Hibernation [a]	[Enable/Disable]
ACPI Sleep State [b]	[Suspend disabled/S3 (Suspend to RAM)]
Restore AC Power Loss [c]	[Power On/Power Off/Last State]
RTC Wakeup [d]	[Enabled/disabled]
System Time	[HH:MM:SS]
Wake up day [e]	0..31
Wake up Time	[HH:MM:SS]

a. Allows the system ability to hibernate (S4) to be enabled or disabled.
b. Selects the highest ACPI sleep state the system enters when the **SUSPEND** button is pressed.

c. Specifies the state the system enters when power is reapplied after a power failure. If set to **POWER ON**, the system boots as soon as power is enabled. If set to **POWER OFF**, the system remains powered off until the power button is pressed.
d. Enables or disables the system wake on alarm event. If this setting is **enabled**, the BIOS allows the user to set the **Wake up day** and **Wake up Time** fields below.
e. Day of the month.

Thermal Configuration

Thermal Configuration Parameters

Automatic Thermal Reporting [a] [Enabled/Disabled]

a. When enabled, Automatic Thermal Reporting automatically configures the CRITICAL, PASSIVE, and ACTIVE trip points based on recommended values.

Dynamic Platform and Thermal Framework

The dynamic platform and thermal framework (DPTF) is a platform-level software framework that serves as a base for any power, thermal, or other platform-level control technology. DPTF uses advanced configuration and power interface (ACPI) as the primary interface to communicate with the platform and to gather policy inputs and preferences for each technology. The ACPI specification was developed to establish industry common interfaces enabling robust operating system (OSPM) directed motherboard device configuration and power management.

The DPTF allows thermal points to be set for various participants. When the trip points are reached, the DPTF configuration specifies what actions are initiated to address the thermal and power conditions. Actions range from turning on active cooling devices (i.e., a fan), to down clocking the CPU.

DPTF		[Enable/Disable]
DPTF Configuration		[six bit bitmap value]
BIT 0	Generic UI Access Control	[0=enable/1=disable]
BIT 1	Restricted UI Access Control	[0=enable/1=disable]
BIT 2	Shell Access Control	[0=enable/1=disable]
BIT 3	Environment Monitoring Report Control	[0=enable/1=disable]
BIT 4	Thermal Mitigation Report Control	[0=enable/1=disable]
BIT 5	Thermal Policy Report Control	[0=enable/1=disable]
DPTF Processor		[Enable/Disable]
Active Thermal Trip Point [a b]		90

Passive Thermal Trip Point [a]	100
S3/CS Thermal Trip Point [a]	110
Hot Thermal Trip Point [a]	110
Critical Thermal Trip Point [a]	105
Thermal Sampling Period [c]	0
S3/CS Thermal Trip Point [a]	110
Hot Thermal Trip Point [a]	110
Critical Thermal Trip Point [a]	105
Thermal Sampling Period [c]	0

a. Temperature, in Celsius; a value of 0 disables trip point.
b. If DPTF processor is **Disabled**, these fields are no visible.
c. Polling Interval in 1/10 seconds; a value of 0 enables interrupts

Serial Port Configuration

COM1 Mode	[RS232/RS485 HALF DUPLEX/RS485.422 FULL DUPLEX]
COM2 Mode	[RS232/RS485 HALF DUPLEX/RS485.422 FULL DUPLEX]

The built-in serial ports may be configured using the Serial Port Configuration page of the BIOS.

Serial ports A and B are RS232 only ports. Serial ports C and D may be configured as RS232, RS422, or RS485 devices. The BIOS serial port settings support the simultaneous transmission and reception of data on the discrete RX and TX lines (full-duplex), or the shared transmission and reception of data on a single data line pair (half-duplex).

Additional serial port configuration is performed using the Windows Device Manager and the EXAR Quad UART device driver.

Watch Dog Timer Configuration	
Watch Dog Timer	[Enabled/Disabled]
Timer Unit	[Second/Minute]
Timer Value	N

The PX1-C441's watchdog timer can be enabled or disabled using the BIOS. When enabled, the WDT timer unit value may be specified as either seconds or minutes. The watchdog timer value N can also be set on this BIOS page.

If the watchdog timer is disabled on this page, the Timer Unit and Timer Value fields are disabled.

H/W Monitor

The BIOS supports monitoring of CPU temperature, CPU voltages, and system voltages. The currently measured values may be displayed using the H/W Monitor BIOS page. The H/W Monitor page displays the following values.

CPU Temperature	Current Temperature (in Celsius)
Fan1 Speed	
Vcore	Current detected voltage
+3.3V	Current detected voltage
+5V	Current detected voltage
+12V	Current detected voltage
VDIMM	Current detected voltage

Debug Configuration

The Debug Configuration page enables or disables the built in DCI-USB debug interface.

DCI Enable (HDCIEN)	[Enabled/Disabled]

Intel I210 Gigabit Network Connection - XX:XX:XX:XX:XX:XX

NIC Configuration	
Blink LEDs	[0/1]
UEFI Driver	Intel PRO/1000 7.3.20 PCI-E
Adapter PBA	000300-000
Device Name	Intel I210 Gigabit Network Connection
Chip Type	Intel i210
PCI Device ID	1533
PCI Address	08:00:00
Link Status	[Connected]
MAC Address	XX:XX:XX:XX:XX:XX
Virtual MAC Address	00:00:00:00:00:00

8.3.3 Security

The BIOS Security page allows various passwords to be set, and specifies how and when the passwords is used to protect the system.

Password Check Mode	[Setup/Power On]
Setup Administrator Password	
HDD Security Configuration	
Security configuration for selected	
Security Supported	Yes/No
Security Enabled	Yes/No
Security Locked	Yes/No
Security Frozen	Yes/No
HDD User Pwd Status	Installed/Not Installed
HDD Master Pwd Status	Installed/Not Installed

8.3.4 Boot

Boot Configuration

Setup Prompt Timeout	2

Specifies the number of seconds the system waits for the setup activation key to be pressed before booting the systems. Permitted values range from 0 (no wait) to a maximum wait of 65534 seconds (18.2 hours). A value of 65535 sets the boot wait to indefinite.

Bootup NumLock State	[On/Off]

Sets the state of the **Num Lock** key on boot. If set to **On**, the system powers up with keyboard **Num Lock** set. When **Off**, the system powers up with keyboard **Num Lock** clear.

Post Report	[Enabled/Disabled]

Enables or disables support for POST report.

Summary Screen	[Enabled/Disabled]

Enables or disables support for the boot summary screen. When enabled, the system pauses before booting and display a summary of the system configuration, including boot devices, display type, and PCI bus

configuration. After being displayed, the boot process continues when the user presses **ESC**.

CSM Support [Enabled/Disabled]

Enables or disables the compatibility support module (CSM). The CSM is a component of the UEFI firmware that provides legacy BIOS compatibility by emulating a BIOS environment, allowing legacy operating systems and some option ROMs that do not support UEFI to still be used.

OS Selection [Default/Others/Legacy System/Intel Linux]

Specifies the type of the selected OS. The OS selection effects LPSS and XHCI hand off settings. DEFAULT indicates a boot to Win8/8.1/10. OTHER indicates a boot of non-Intel Linux or Android. LEGACY indicates a boot of Win7 or MS-DOS.

Full Screen Logo [Enabled/Disabled]

If enabled, the BIOS loads the full screen logo from the BIOS image and display it during the early OS boot phase. If disabled, no logo is loaded/displayed.

Boot Mode Select [LEGACY/UEFI]

When set to LEGACY, the firmware maintains a list of installed storage devices that support booting. The devices are enumerated in a prioritized list. After the POST, the firmware scans the first sector of each bootable device in the prioritized list, looking for a valid master boot record (MBR). If a valid MBR is located, the firmware passes control to the boot loader code located in the MBR. This boot loader code allows the user to select the boot partition on the boot device.

When set to UEFI, the firmware maintains a list of valid boot volumes called EFI service partitions. During POST, the UEFI firmware scans all the bootable storage devices connected to the system, searching for a valid GUID partition table (GPT). The UEFI firmware scans all the GPTs searching for an EFI service partition to boot from.

FIXED BOOT ORDER Priorities

Boot Option #1	[LIST OF POSSIBLE BOOT DEVICES/DISABLED]
Boot Option #2	[LIST OF POSSIBLE BOOT DEVICES/DISABLED]
Boot Option #3	[LIST OF POSSIBLE BOOT DEVICES/DISABLED]
Boot Option #4	[LIST OF POSSIBLE BOOT DEVICES/DISABLED]

The LIST OF POSSIBLE BOOT DEVICES is the prioritized list of either bootable installed storage (legacy boot mode), or EFI service partitions (UEFI boot mode)

When **Boot Mode Select** is set to **UEFI**, a new set of menus appear that allow the user to define the boot order from the set of UEFI bootable devices.

UEFI Hard Disk Drive BBS Priorities

BOOT OPTION #1 [LIST OF POSSIBLE UEFI BOOTABLE HARD DRIVES]

NOTE If more than one UEFI bootable devices is detected, they are displayed in the above list.

UEFI USB Drive BBS Priorities

BOOT OPTION #1 [LIST OF POSSIBLE UEFI BOOTABLE USB DRIVES]

NOTE If more than one UEFI bootable devices is detected, they are displayed in the above list.

UEFI Network Drive BBS Priorities

BOOT OPTION #1 [LIST OF POSSIBLE UEFI BOOTABLE HARD DRIVES]

NOTE If more than one UEFI bootable devices is detected, they are displayed in the above list.

8.3.5 Save and Exit

Save Options

SAVE CHANGES and RESET

Saves the current set of boot parameters to non-volatile storage, and resets the system.

DISCARD CHANGES and RESET

Discards the current set of boot parameters, and resets the system using the saved (unchanged) parameters.

Default Options

Restore Defaults

Selecting this option causes the system to reload the saved parameters, overwriting any changes.

Boot Override

A list of boot devices that contain either a MBR (legacy boot mode) or a GPT (UEFI boot mode). Highlighting an boot device and pressing **Enter** causes the system to attempt to boot from the selected device.

8.4 Software Description

This section provides details on the AMI BIOS components to be used in the implementation of the PX1-C441 BIOS firmware.

8.4.1 Software Design Specification: UEFI Operating System Support

The BIOS supports the booting of the following UEFI compliant operating systems:

- Microsoft Windows 10 x32/x64 (including Win10 IoT)
- Ubuntu 16.XX x32/x64

8.4.2 Software Design Specification: Legacy Operating System Support

- Compatibility support module (CSM)
- Legacy boot support required
- Legacy option ROM support required

The BIOS supports the booting of the following legacy OS:

- MS-DOS 6

8.4.3 Software Design Specification: Boot Device Configuration

The BIOS supports booting an OS from the following devices:

- USB mass storage device
- Serial ATA (SATA) device
- Network boot - PXE
- eMMC
- M.2 mass storage device

8.4.4 Software Design Specification: BIOS Update Mechanisms

The BIOS supports the following update mechanisms:

- Software utilities
- Flash recovery via USB mass storage device
- Flash recovery via eMMC device

8.4.5 Software Design Requirements: BIOS Components

The BIOS includes the following components:

- **Advanced host controller interface (AHCI) support:** Provides SATA host controller functionality.
- **Display switching in setup:** Implements display switching using the UEFI GOP driver under the SETUP environment.
- **Boot order:** Generates the default boot order on the platform's first boot.
- **Boot/resume from S4 device:** Allows the platform to boot from the last S4 hibernated device, disregarding the current boot priority.
- **Cryptographic support:** Provides cryptographic related libraries, PPI, and UEFI protocols for security modules (secure FW update, secure boot, etc.)
- **Source level support:** Provides source level debug functionality for the BIOS project.
- **Fastboot:** Provides optimization of the boot time.
- **Fixed boot order:** Provides infrastructure that allows custom handling of available boot options to meet specific customer needs. Custom boot behavior may include different requests, such as always boot from specific device, default support of various kinds of grouping of boot devices
- **Generic error logging:** Provides support for logging POST and runtime errors to the GPNV area.
- **Keyboard controller emulation:** For USB keyboard/mouse.
- **Physical memory testing:** Supports testing of physical memory present in the system.
- RTC registration and ability to handle wakeup from S5 sleep state.
- **Secure boot support:** Provides support and functionality to conform with UEFI 2.3.1 secure boot requirements and includes the following components:
  - Extended functionality of EFI NVRAM driver with support for authenticated EFI variables.
  - EFI image authentication module that installs EFI security architecture protocol with image authentication and image execution policy.
  - Secure boot variable (PK, KEK, db, and dbx) provisioning.
- Support for booting to the built-in UEFI shell.

8.5 BIOS Update with UEFI Shell

8.5.1 Scope

The Unified Extensible Firmware Interface (EFI or UEFI for short) is a new model for the interface between operating systems and firmware. It provides a standard environment for booting an operating system and running pre-boot applications.

An optional feature of a UEFI implementation is the ability to boot the system to a built-in shell. The UEFI shell provides a command prompt and a rich set of commands that extend and enhance the capability of the UEFI BIOS.

This section describes the process for updating the PX1-C441 BIOS firmware image using the built-in UEFI shell.

8.5.2 Process

1. Insert a USB flash drive containing the BIOS update program into a USB socket on the PX1-C441 platform.
2. Turn on the PX1-C441 and press the **ESC** or **DEL** key during the boot process, which starts the BIOS setup utility.
3. In the BIOS setup utility, use the cursor keys to highlight the **Save & Exit** menu option.
4. Use the cursor keys to select **UEFI: Built-In EFI Shell** from the list of boot devices displayed under the **Boot Override** section.
5. Press **Enter**.

   The PX1-C441 executes the built-in UEFI shell, and displays a list of attached storage devices. The USB flash drive shows up in the list; depending on other boot devices attached, it may be listed as **fs0**, **fs1**, etc.

6. From the UEFI shell command prompt, enter the following command where `N` is the number of the fs device representing the USB flash drive:

   ```
   fsN:
   ```

   Example: `fs1:`

   The shell prompt changes to indicate that device fsN is now the active storage device, for example, `fs1:`

7. Execute the following command:

   ```
   ls
   ```

   The output of the `ls` command is similar to the display listing available with the Linux or MS-DOS list directory command. If the correct storage device was selected in step 6 above, the `ls` command f should show the BIOS update program in the directory listing obtained with the ls command.

8. Assuming the BIOS update program is named `Update.efi`, enter the following command at the shell command prompt:

   ```
   Update.efi
   ```

   The BIOS update program begins executing.

9. When the update program completes, power cycle the platform to force the new BIOS image to load and execute.
10. Verify BIOS update was successful by comparing displayed BIOS version with version specified in the BIOS update notification.

8.6 BIOS Status and Errors

8.6.1 BIOS Status and Error Reporting

BIOS status is reflected using a hexadecimal value displayed in the left lower corner of the display device. See “Standard Checkpoints” on page 45 for a list of the status and error codes.

8.6.2 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 resume (PEI)
0xE9 – 0xEF	S3 resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.6.3 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on; reset type detection (soft/hard)
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading

Status Code	Description
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

SEC Beep Codes

None

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-memory North Bridge initialization (North Bridge module specific)
0x17	Pre-memory North Bridge initialization (North Bridge module specific)
0x18	Pre-memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization; serial presence detect (SPD) data reading
0x2C	Memory initialization; memory presence detection
0x2D	Memory initialization; programming memory timing information
0x2E	Memory initialization; configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL

Status Code	Description
0x31	Memory installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization; cache initialization
0x34	CPU post-memory initialization; application processor(s) (AP) initialization
0x35	CPU post-memory initialization; boot strap processor (BSP) selection
0x36	CPU post-memory initialization; system management mode (SMM) initialization
0x37	Post-memory North Bridge initialization is started
0x38	Post-memory North Bridge initialization (North Bridge module specific)
0x39	Post-memory North Bridge initialization (North Bridge module specific)
0x3A	Post-memory North Bridge initialization (North Bridge module specific)
0x3B	Post-memory South Bridge initialization is started
0x3C	Post-memory South Bridge initialization (South Bridge module specific)
0x3D	Post-memory South Bridge initialization (South Bridge module specific)
0x3E	Post-memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed.
0x51	Memory initialization error. SPD reading has failed.
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected.
0x54	Unspecified memory initialization error
0x55	Memory not installed
0x56	Invalid CPU type or speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
0x5C	PEI phase BMC self-test failure
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 resume is stared (S3 resume PPI is called by the DXE IPL)

Status Code	Description
0xE1	S3 boot script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 resume failed
0xE9	S3 resume PPI not found
0xEA	S3 resume boot script error
0xEB	S3 OS wake error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (auto recovery)
0xF1	Recovery condition triggered by user (forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not installed
2	Recovery started
3	Typically for development use. The beep code is generated when DXEIPL PPI or DXE core is not found.
4	Recovery failed
4	S3 resume failed
7	Typically for development use. The beep code is generated when platform cannot be reset because reset PPI is not available.

DXE Phase

Status Code	Description
0x60	DXE core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge runtime services
0x63	CPU DXE initialization is started

Status Code	Description
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE initialization (South Bridge module specific)
0x74	South Bridge DXE initialization (South Bridge module specific)
0x75	South Bridge DXE initialization (South Bridge module specific)
0x76	South Bridge DXE initialization (South Bridge module specific)
0x77	South Bridge DXE initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot device selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI bus initialization is started
0x93	PCI bus hot plug controller initialization
0x94	PCI bus enumeration
0x95	PCI bus request resources
0x96	PCI bus assign resources
0x97	Console output devices connect
0x98	Console input devices connect
0x99	Super IO initialization
0x9A	USB initialization is started
0x9B	USB reset
0x9C	USB detect
0x9D	USB enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE reset

Status Code	Description
0xA2	IDE detect
0xA3	IDE enable
0xA4	SCSI initialization is started
0xA5	SCSI reset
0xA6	SCSI detect
0xA7	SCSI enable
0xA8	Setup verifying password
0xA9	Start of setup
0xAA	Reserved for ASL
0xAB	Setup input wait
0xAC	Reserved for ASL
0xAD	Ready to boot event
0xAE	Legacy boot event
0xAF	Exit boot services event
0xB0	Runtime set virtual address MAP begin
0xB1	Runtime set virtual address MAP end
0xB2	Legacy option ROM initialization
0xB3	System reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some architectural protocols not available
0xD4	PCI resource allocation error; out of resources
0xD5	No space for legacy option ROM
0xD6	No console output devices are found
0xD7	No console input devices are found
0xD8	Invalid password
0xD9	Error loading boot option (LoadImage returned error)
0xDA	Boot option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available
0xDD	DXE phase BMC self-test failure

DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Typically for development use. The beep code is generated when some of the architectural protocols are not available.
5	No console input or output devices are found [a] [b]
6	Flash update is failed
7	Typically for development use. The beep code is generated when platform cannot be reset because reset protocol is not available.
8	Platform PCI resource requirements cannot be met

a. Serial console redirection is considered a console out device if enabled.
b. Serial console redirection is considered a console in device if enabled. Also, depending on configuration PS/2 driver may always report a console in device even if one is not connected.

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode; interrupt controller is in PIC mode
0xAA	System has transitioned into ACPI mode; interrupt controller is in APIC mode

8.6.4 OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

9. Accessories and Cables

WINSYSTEMS cables and batteries simplify connection to the PX1-C441. The following table lists available items.

Item	Part Number	Connection	Description
Cables	CBL-USB4-002-12	See "J5 - USB 2.0 Ports" on page 22.	Pico-Clasp to two 2x5, 2mm pitch
	ADP-IO-USB-002		
	CBL-ENET1-302-12	See "J12 - PCIe OneBank" on page 26.	Ethernet 2x5, 1.27mm to RJ-45 female/ jack 12"
	CBL-LVDSAB-009-18	See "J8 - SATA 3 (6 Gbps)" on page 20.	Backlight 1x8 1 mm, unterminated Pico-Clasp
	CBL-DIO24-001-12	See "J12 - PCIe OneBank" on page 26.	DIO 2x25 1 mm to 2x25 1 mm, 12"
	CBL-DIO24-002-12		DIO cable 2x25 1 mm to 2x25 .1 CNTRS 12"
	CBL-LVDSAB-009-18	See "J1 - LVDS Backlight Power" on page 18.	LVDS with analog audio
	CBL-SPL-001-14		Analog audio, unterminated LVDS lines
	CBL-SER4-002-12B	See "J11 - USB 3.2 Gen 1 Type-C" on page 23.	Cable for serial ports (**J13**), four DB9, 12 inch
	CBL-SER4-000-14		Cable for serial ports (**J13**) to unterminated
	CBL-SER4-001-12		Cable for serial ports (**J13**): Duo-Clasp to Duo-Clasp
Batteries	BAT-LTC-E-36-16-2	See "J15 - CMOS Battery Input" on page 16.	External 3.6 V, 1650 mAh battery with plug-in connector
	BAT-LTC-E-36-27-2		External 3.6 V, 2700 mAh battery with plug-in connector

Standoff kits are available and recommended for use with the PX1-C441. The following table lists the items contained in each kit.

Kit	Component	Description	Qty
KIT-PCM-STANDOFF-4 4 pc. nylon hex PC/104 standoff kit	Standoff	Nylon 0.25" hex, 0.600" long male/female 4-40	4
	Hex nut	Hex nylon 4-40	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4" stainless steel	4
KIT-PCM-STANDOFF-B-4 4 pc. brass hex PC/104 standoff kit	Standoff	Brass 5 mm hex, 0.600" long male/female 4-40	4
	Hex nut	4-40 x 0.095 thick, nickel finish	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4" stainless steel	4

10. Software Drivers

Go to http://www.winsystems.com/ for information on available software drivers.

Appendix A. Best Practices

The following paragraphs outline the best practices for operating the PX1-C441 in a safe, effective manner, that does not damage the board. Read this section carefully.

Power Supply

Avoid electrostatic discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Zero-load Power Supply

Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply does not regulate properly and can cause damage to the PX1-C441.

Use proper power connections (voltage)
When verifying the voltage, measure it at the power connector on the PX1-C441. Measuring it at the power supply does not account for voltage drop through the wire and connectors.

The PX1-C441 requires 9 to 36 V to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

The PX1-C441 has a single power connector at **J17**. A single 9-36 VDC input and ground is required to power the board.

Power Harness

Minimize the length of the power harness. This reduces the amount of voltage drop between the power supply and the PX1-C441.

Gauge Wire

Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins.

Contact Points

WINSYSTEMS boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high-speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion, resulting in unreliable connections.

Pin Contacts

Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex or Trifurcon designs, which provide three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power supply OFF
Always turn off the power supply before connecting to the I/O module. Do not hot-plug the PX1-C441 on a host platform that is already powered.

I/O connections OFF—Turn off all I/O connections before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the I/O Module

To avoid damage, mount the PX1-C441 properly. Standoff kits are available and recommended for use with the PX1-C441. See “Accessories and Cables” on page 52 for the items contained in each kit.

- KIT-PCM-STANDOFF-4: Four-piece nylon hex PC/104 standoff kit
- KIT-PCM-STANDOFF-B-4: Four-piece brass hex PC/104 standoff kit

Placing the PX1-C441 on mounting standoffs—Be careful when placing the PX1-C441 on the mounting standoffs. Sliding the board around until

the standoffs are visible from the top can cause component damage on the bottom of the board.

Do not bend or flex the PX1-C441—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around ball grid array (BGA) devices. BGA devices are extremely rigid by design, and flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting holes—The mounting holes are plated on the top, bottom, and through the barrel of the hole, and are connected to the embedded computer module's ground plane. Traces are often routed in the inner layers right below, above, or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes, you provide the support the embedded computer module needs to prevent bending or flexing.

Plug or unplug connectors only on fully mounted boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the embedded computer module to be flexed.

Avoid cutting the PX1-C441—Never use star washers or any fastening hardware that cut into the PX1-C441.

Avoid over-tightening of mounting hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use appropriate tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid conductive surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Adding PCIe/104 OneBank Boards to Your Stack

Be careful when adding PCIe/104 OneBank boards to your stack—Never allow the power to be turned on when a PCIe/104 OneBank board has been improperly plugged onto the stack.

Conformal Coating

Applying conformal coating to a WINSYSTEMS product does not in itself void the product warranty, if it is properly removed prior to return. Coating can change thermal characteristics and impedes our ability to test, diagnose, and repair products. Any coated product sent to WINSYSTEMS for repair are returned at customer expense and no service is performed.

Operations/Product Manuals

Every single board computer has an Operations manual or Product manual.

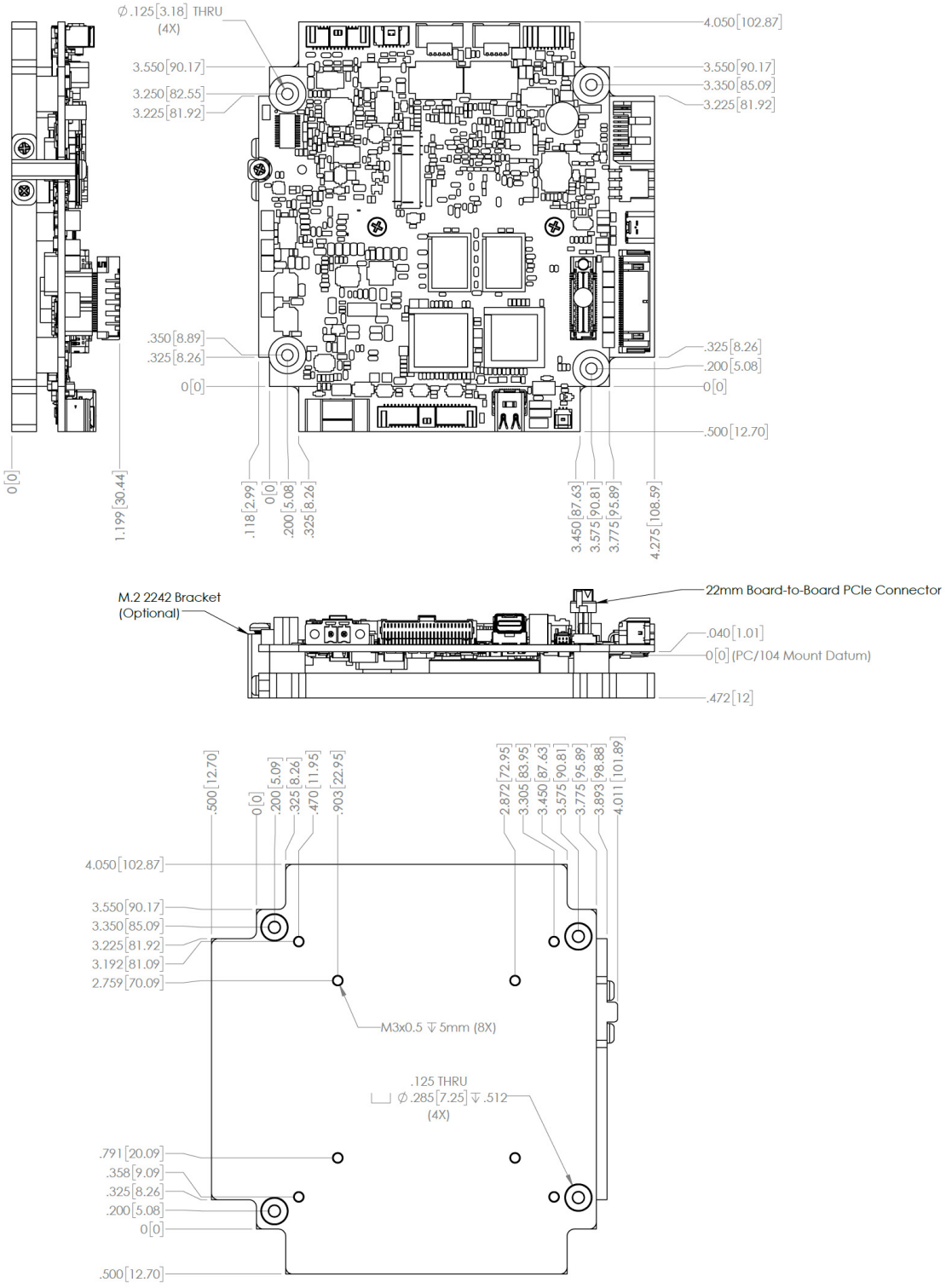
Periodic updates—Operations/Product manuals are updated often. Periodically check the WINSYSTEMS website at http://www.winsystems.com/ for revisions.

Check pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

Contact an applications engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WINSYSTEMS applications engineer at +1-817-274-7553.

Appendix B. Mechanical Drawings

PX1-C441 Mechanical Drawing



Appendix C. Warranty Information

WINSYSTEMS warrants that for a period of two (2) years from the date of shipment, any Products and Software purchased or licensed hereunder which have been developed or manufactured by WINSYSTEMS shall be free of any defects and shall perform substantially in accordance with WINSYSTEMS' specifications therefor. With respect to any Products or Software purchased or licensed hereunder which have been developed or manufactured by others, WINSYSTEMS shall transfer and assign to Customer any warranty of such manufacturer or developer held by WINSYSTEMS, provided that the warranty, if any, may be assigned. The sole obligation of WINSYSTEMS for any breach of warranty contained herein shall be, at its option, either (i) to repair or replace at its expense any materially defective Products or Software, or (ii) to take back such Products and Software and refund the Customer the purchase price and any license fees paid for the same. Customer shall pay all freight, duty, broker's fees, insurance, charges and other fees and charges for the return of any Products or Software to WINSYSTEMS under this warranty. WINSYSTEMS shall pay freight and insurance charges for any repaired or replaced Products or Software thereafter delivered to Customer within the United States. All fees and costs for shipment outside of the United States shall be paid by Customer. The foregoing warranty shall not apply to any Products or Software which have been subject to abuse, misuse, vandalism, accident, alteration, neglect, unauthorized repair or improper installation.

THERE ARE NO WARRANTIES BY WINSYSTEMS EXCEPT AS STATED HEREIN. THERE ARE NO OTHER WARRANTIES EXPRESS OR IMPLIED INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL WINSYSTEMS BE LIABLE FOR CONSEQUENTIAL, INCIDENTAL OR SPECIAL DAMAGES FOR LOSS OF DATA, PROFITS OR GOODWILL. WINSYSTEMS' MAXIMUM LIABILITY FOR ANY BREACH OF THIS AGREEMENT OR OTHER CLAIM RELATED TO ANY PRODUCTS, SOFTWARE, OR THE SUBJECT MATTER HEREOF, SHALL NOT EXCEED THE PURCHASE PRICE OR LICENSE FEE PAID BY CUSTOMER TO WINSYSTEMS FOR THE PRODUCTS OR SOFTWARE OR PORTION THEREOF TO WHICH SUCH BREACH OR CLAIM PERTAINS.

Title to the Products shall remain vested in WINSYSTEMS until complete payment is made by Customer. Title to any Software shall remain vested in WINSYSTEMS, or WINSYSTEMS' licensor from whom WINSYSTEMS has obtained marketing rights, both before, during and after the term of the License. Nonpayment when due of the purchase price for any Products or the License fees for any Software, or, if applicable, taxes and/or the cost of any freight and insurance for any Products and/or Software, shall entitle WINSYSTEMS to take possession of the Products and/or Software without notice to Customer or prejudice to WINSYSTEMS' rights under contract or any other legal remedy.

Until title to the Products pass in accordance with the provision set out above, except with the prior written approval of WINSYSTEMS, no Products shall be modified, altered, moved or in any way assigned, sublet, mortgaged or charged nor may Customer part with possession of all or part of the same.

There are no understandings, agreements or representations, express or implied, other than those set forth herein. This Order embodies the entire agreement between the parties and may be waived, amended or supplemented only by a written instrument executed jointly by WINSYSTEMS and Customer as evidenced only by the signature of duly authorized officers of each party. The foregoing terms and conditions of any order which may be issued by Customer for the purchase of Products or licensing of Software hereunder.

In the event this Order is placed in the hands of an attorney or collection agency by WINSYSTEMS to collect any sums due hereunder to WINSYSTEMS, Customer shall pay all reasonable attorney's fees, expenses, collection and court costs incurred by WINSYSTEMS.

THIS AGREEMENT SHALL BE GOVERNED AND CONSTRUED UNDER THE TEXAS UNIFORM COMMERCIAL CODE AND THE APPLICABLE LAWS OF THE STATE OF TEXAS. THE PARTIES ACKNOWLEDGE THAT ANY ACTION BROUGHT HEREUNDER SHALL ONLY BE BROUGHT IN A COURT OF COMPETENT JURISDICTION IN TARRANT COUNTY, TEXAS.

Warranty Service

1. To obtain service under this warranty, obtain a return authorization number. In the United States, contact the WINSYSTEMS Service Center for a return authorization number. Outside the United States, contact your local sales agent for a return authorization number.
2. You must send the product postage prepaid and insured. You must enclose the products in an anti-static bag to protect from damage by static electricity. WINSYSTEMS is not responsible for damage to the product due to static electricity.