IEEE WMED 2024 Technical Program

7:15 AM	**Check-In, Registration, and Continental Breakfast (Double R Ranch Room)**	
8:00am	**Welcome Address**	
	Double R Ranch Room	
	Curtis Cahoon, General Chair, IEEE WMED 2024	
	Plenary Session	
	Double R Ranch Room, Session Chair: Jai Jaiprakash, Micron	
8:15am	**Keynote Talk I:** **Meeting Workforce Demands for the AI Revolution** Janine Rush-Byers and Shawn Siddoway, Micron Technology	
9:15am	**Keynote Talk II:** **Analog-memory-based In-Memory-Computing Accelerators for Deep Neural Networks** Sidney Tsai, IBM	
10:15am	**Break**	
	Invited Talks: Session 1	
	Track 1	**Track 2**
	Double R Ranch Room, Session Chair: Tim Hollis and Curtos Cahoon, Micron	**Skyline Room, Chair: Kurtis Cantley, Boise State University**
10:30am	**Application of machine learning techniques to chip design** Sunil Sudhakaran, NVIDIA and Stanford University	**Spiking Neural Network Design for Neuromorphic Hardware** Adarsha Balaji, Argonne National Laboratory
11:15am	**Advanced Packaging: A critical enabler for AI Computing needs** Bharat Penmecha, Intel	**Neuromorphic Computing for Future AI Systems** Cory Merkel, Rochester Institute of Technology
12:00pm	**Lunch Break (Double R Ranch and Skyline Room)**	
12:45pm	**Poster Session (Double R Ranch)**	
	Invited Talks: Session 2	
	Track 1	**Track 2**
	Double R Ranch Room, Session Chair: Sumeet Pandey, Micron	**Skyline Room, Session Chair: Omiya Hassan, Boise State University**
1:30pm	**On Digital Twins for Semiconductor Manufacturing** Surya Kalidindi, Georgia Tech	**HBM Technology, an Overview** Joe McCrate and Raghu Sreeramaneni, Micron Technology
2:15pm	**Materials Morphology Engineering by Deep Learning** Mahmood Mamivand, Boise State University	**Dimensionality Reduction and Manifold Optimization for Sensor Arrays** Justin Romberg, Georgia Tech
3:00pm	**Break**	
	Contributed Papers*	
	Double R Ranch Room, Chair: Siva Naga Sandeep Chalamalasetty, Micron Technology	
3:15pm	**Flip-Chip Bonding of SiC Chips Onto Alumina Substrate for High-Temperature Applications** Feng Li, University of Idaho	
3:40pm	**A Study of the Effects of Thermal Budget on 3D-NAND Charge Trap Cell Reliability** Marc Aoulaiche, Micron Technology Inc.	
4:05pm	**Advancing Semiconductor Manufacturing Through DNA-Templated Lithography and Molecular-Scale Patterning of 2D Materials** Arpan De, University of Washington	
4:30pm	**Cryogenic Behaviors of 65nm Transistor: On-State IV and Parameters** Hiu Yung Wong, San Jose State University	
5:00pm	**Panel Discussion**	
	Double R Ranch Room, Moderator: Curtis Cahoon, Micron Technology	
	Navigating the AI Frontier: Trends, Training, and Transformation in the Semiconductor Industry Panelists: Andi Morey Peterson, Micron Casey Kennington, Boise State University Cory Merkel, Rochester Institute of Technology Omiya Hassan, Boise State University	
6:00pm	**Closing Remarks**	

*Co-authored Papers, only presenter's name is mentioned. For a complete author and affiliations list, please see the Contributed Papers section of the Program Booklet.