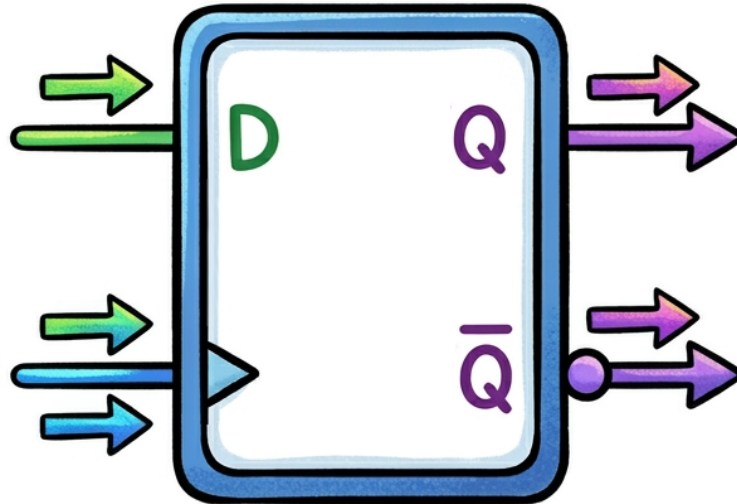


Topic 103 Sequential Logic Systems Question Pack

for

Eduqas GCE A-Level Electronics



Student Name:

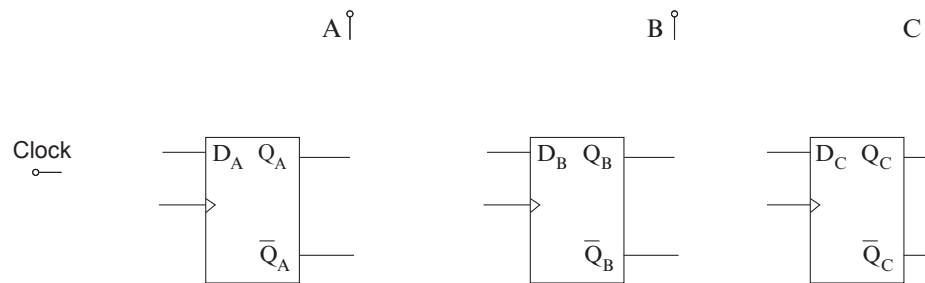
Class / Group:

Question 1

7

4. The diagram shows three D-type flip-flops, which form part of a binary **down-counter**. Outputs A, B and C are used to indicate the binary output. A is the **least significant bit**.

Examiner
only



- (a) Complete the diagram to make a three-bit binary **down-counter**. [3]

- (b) The initial state of the counter is shown in the table. Complete the table, using 0 or 1, to indicate the logic state of each output after the stated number of clock pulses. [2]

	OUTPUT C	OUTPUT B	OUTPUT A
Initial State	1	1	1
After ONE clock pulse			
After FIVE clock pulses			

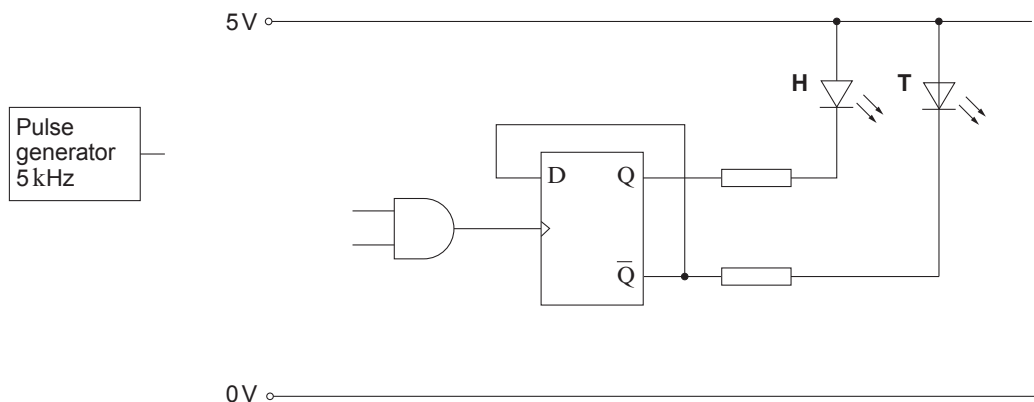
1141
010007

Question 2

8

Examiner
only

5. The diagram shows an incomplete circuit for an electronic coin-tossing game in which **LED H** represents heads and **LED T** represents tails. A switch is pressed to start the LED's flashing. When the switch is released either **H** or **T** stays lit.



- (a) Add the necessary components and connections to the diagram to complete the circuit so that it meets the specification. [3]

- (b) What is the logic state of $\bar{Q}$ when **LED T** is off? [1]

Logic state of $\bar{Q}$ = ...

- (c) Why is a frequency of 5 kHz suitable for this application? [1]

.....

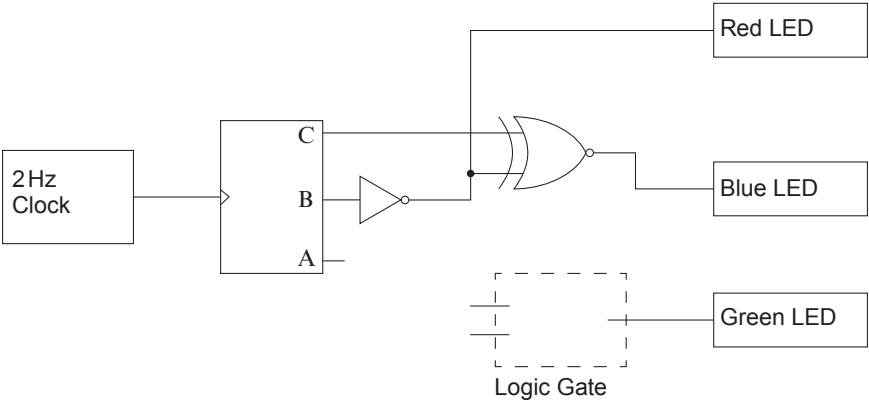
.....

Question 3

9

Examiner
only

6. The diagram shows the control system for a LED display that uses a 3-bit counter. A LED is on when a logic 1 is applied to the input. All the LEDs are initially off.



- (a) (i) Complete the truth table for columns red and blue.

[2]

C	B	A	Red	Blue	Green
0	0	0			1
0	0	1			1
0	1	0			1
0	1	1			1
1	0	0			1
1	0	1			0
1	1	0			1
1	1	1			0

- (ii) In the dotted box above draw the 2-input logic gate that will produce the green output and include the connections to the counter.

[2]

- (b) (i) How many pulses does the 2 Hz clock produce in 20 seconds?

[1]

.....

- (ii) How many times does the red LED flash in 20 seconds?

[1]

.....

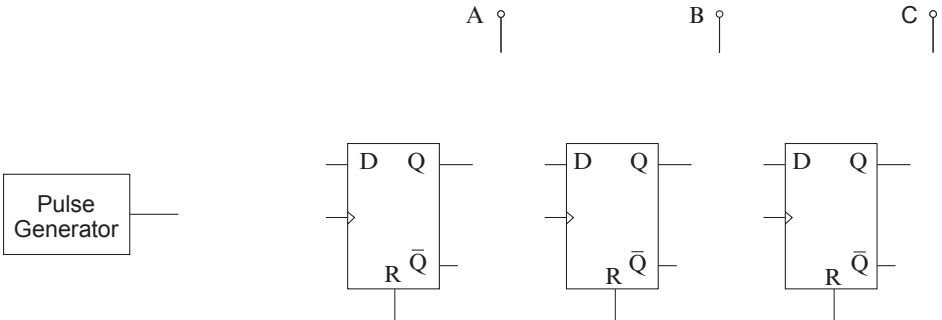
Question 4

8

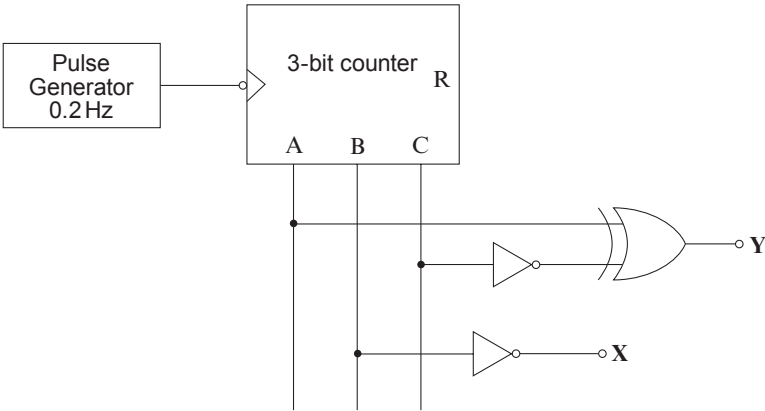
4. (a) Complete the diagram to make a 3 bit up-counter.

[3]

Examiner
only



(b) The following circuit uses a 3-bit **falling edge-triggered** counter.



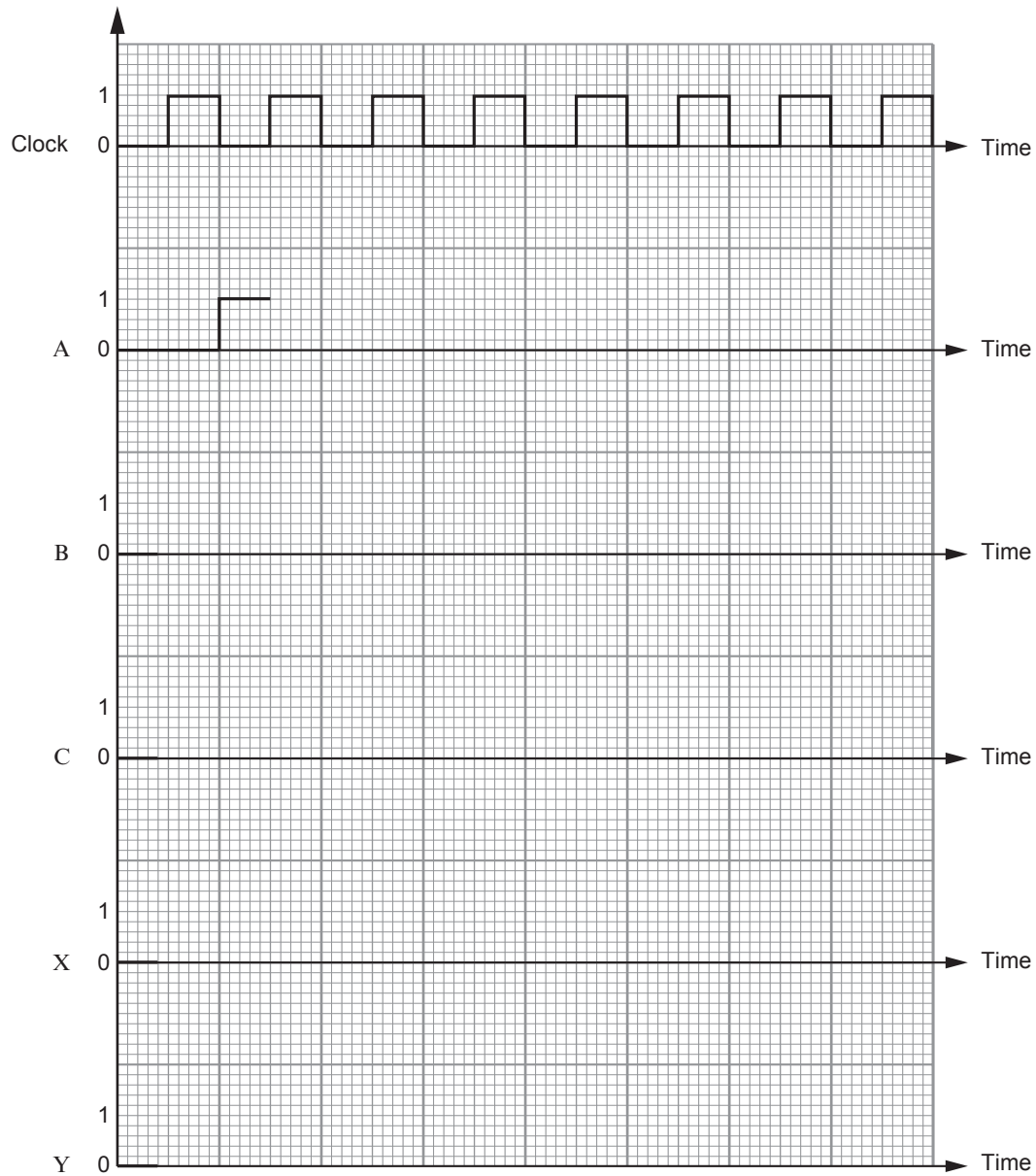
(i) Complete the truth table for circuit.

[2]

C	B	A	X	Y
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(ii) Complete the timing diagram for this system.

[5]

Examiner
only1141
010009

(c) The pulse generator has a frequency of 0.2 Hz. Determine how long output C is high. [2]

.....

.....

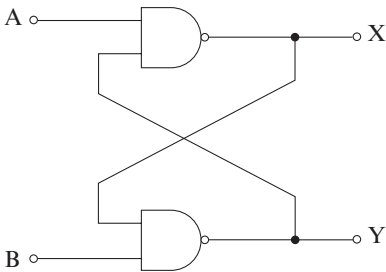
Question 5

10

5. NAND gates can be used in the construction of both a transition gate and a bistable latch.
- (a) What is the function of the transition gate?
- [1]

- (b) In the space below draw a transition gate using 2-input NAND gates.
- [2]

- (c) The following circuit shows a NAND gate bistable.



Complete the truth table to show the sequence of outputs at X and Y, for the given sequence of inputs.

[3]

A	B	X	Y
1	1	0	1
0	1		
1	1		
1	0		
1	1		
0	0		

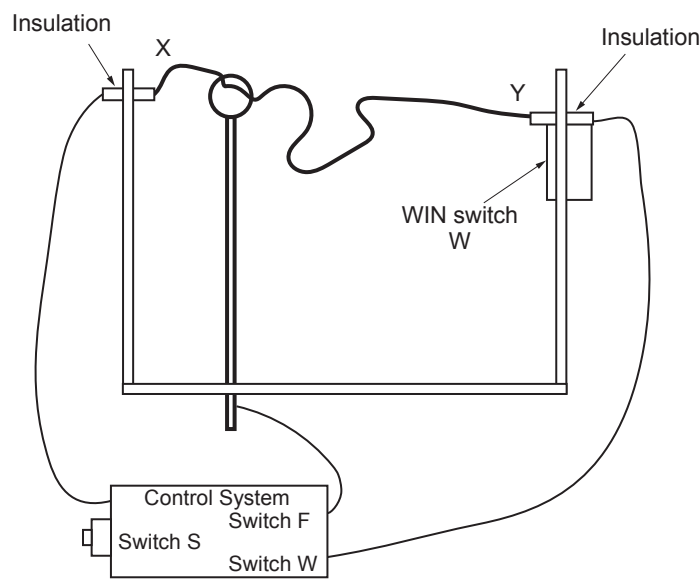
Question 6

8

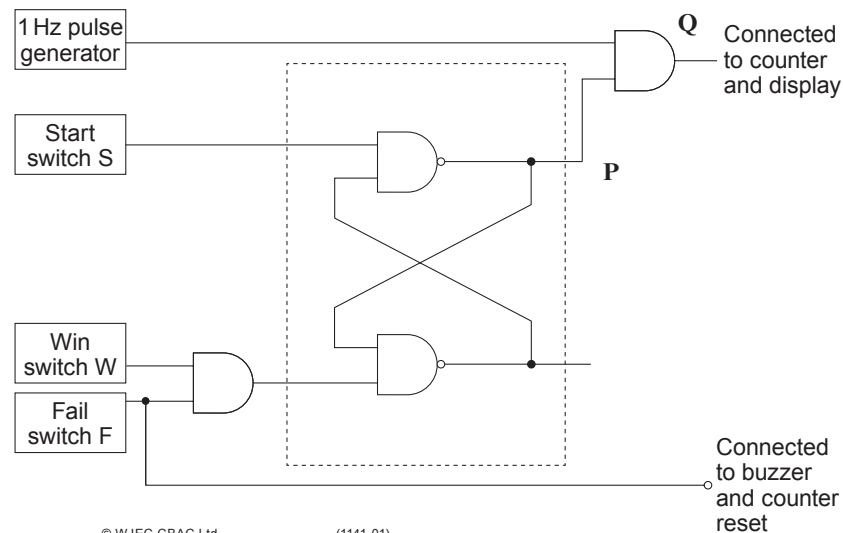
4. A student's design for a 'steady-hand' game is shown below.

- When the START switch S is pressed the counter starts and the contestant moves the metal loop along the wire from point X to point Y as quickly as possible.
- If the metal loop reaches WIN switch W without touching the wire the count shown on the display indicates the time taken.
- If the loop touches the wire before the point Y this acts as a FAIL switch F and the counter resets and a buzzer sounds.

Switches S, W and F are active low.



Part of the control system is shown below.



© WJEC CBAC Ltd.

(1141-01)

(a) What name is given to the sub-system shown in the dashed box?

[1]

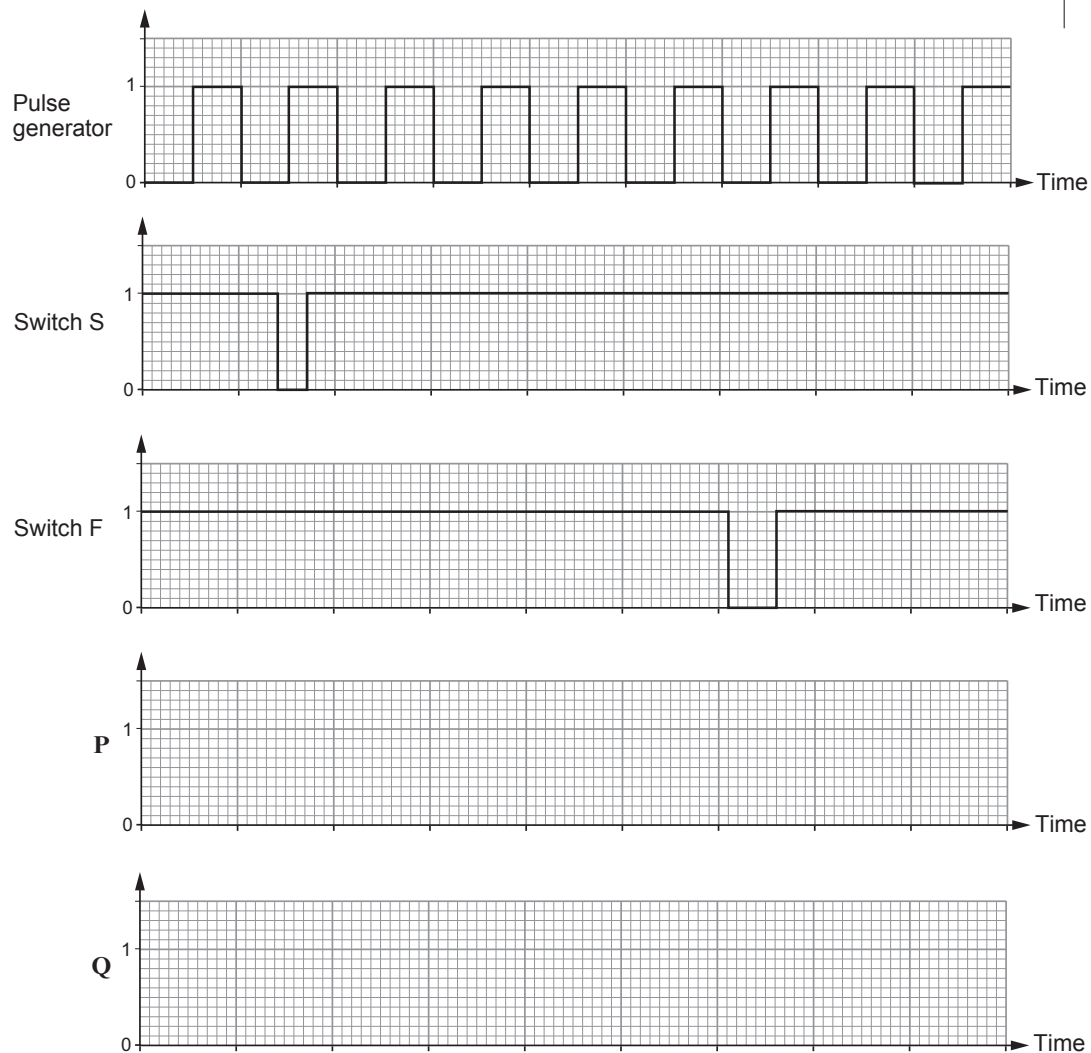
Examiner
only

(b) Whilst being attempted the loop touches the wire part way along. The timing diagram below shows:

- the output from the pulse generator
- the signal from switch S
- the signal from switch F

(i) Complete the diagram to show the outputs P and Q.

[3]

1141
010009

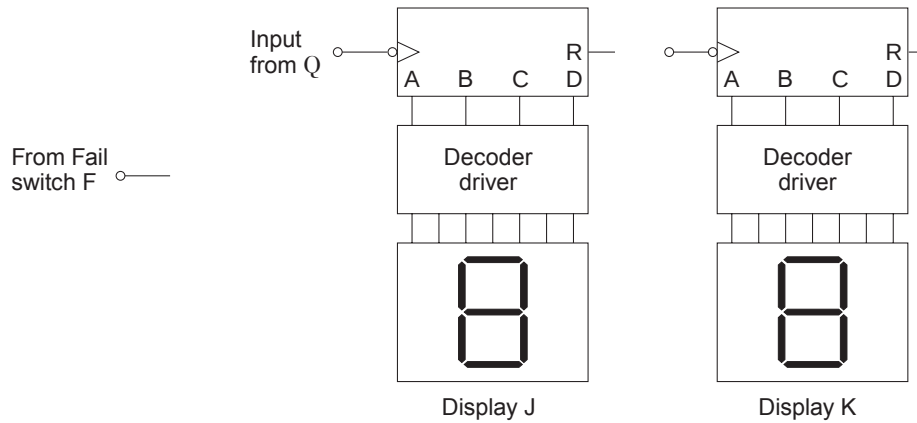
(ii) How many pulses will be fed into the counter/display?

[1]

10

Examiner
only

(c) The counter/display sub-system is shown below.



Each counter resets automatically on the tenth pulse.

(i) What type of counter is this?

[1]

The counters are falling-edge-triggered.

(ii) **Complete the diagram** so that the display can show a maximum of '99'.

[1]

(iii) A player takes 25 s to complete the game successfully. Which display, J or K shows the number 2? [1]

[1]

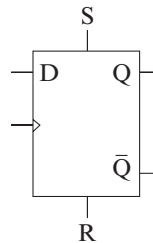
(d) Switch F can reset both counters. Explain how this can be achieved. (You can either write below or draw your solution on the diagram.)

[2]

Question 7

12

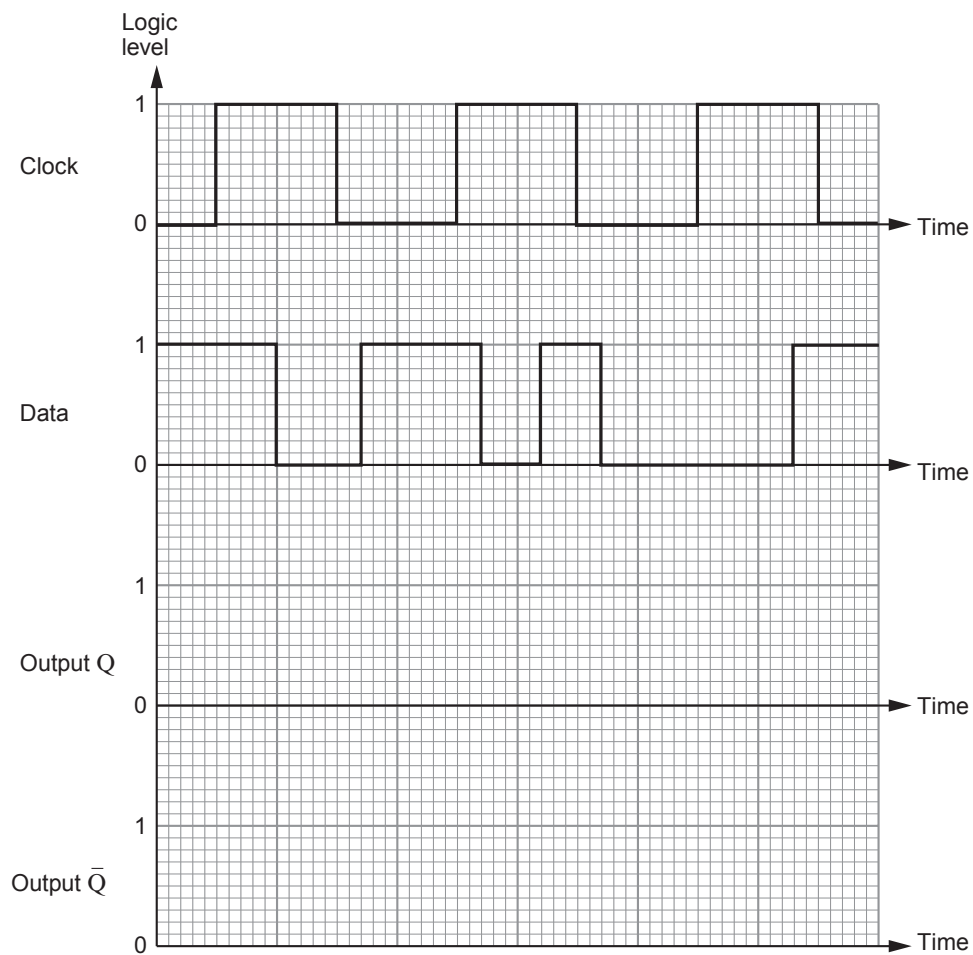
5. (a) The D-type flip-flop in the diagram is rising-edge triggered.

Examiner
only

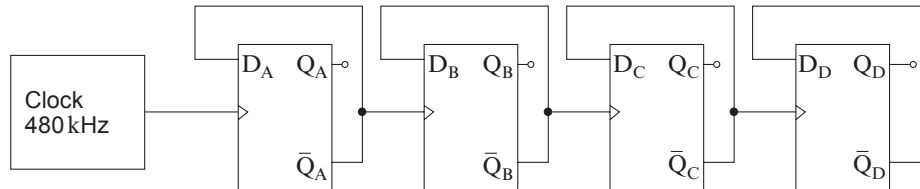
The signals applied to the clock and data inputs are shown below.

Complete the timing diagram for the Q and $\bar{Q}$ outputs.

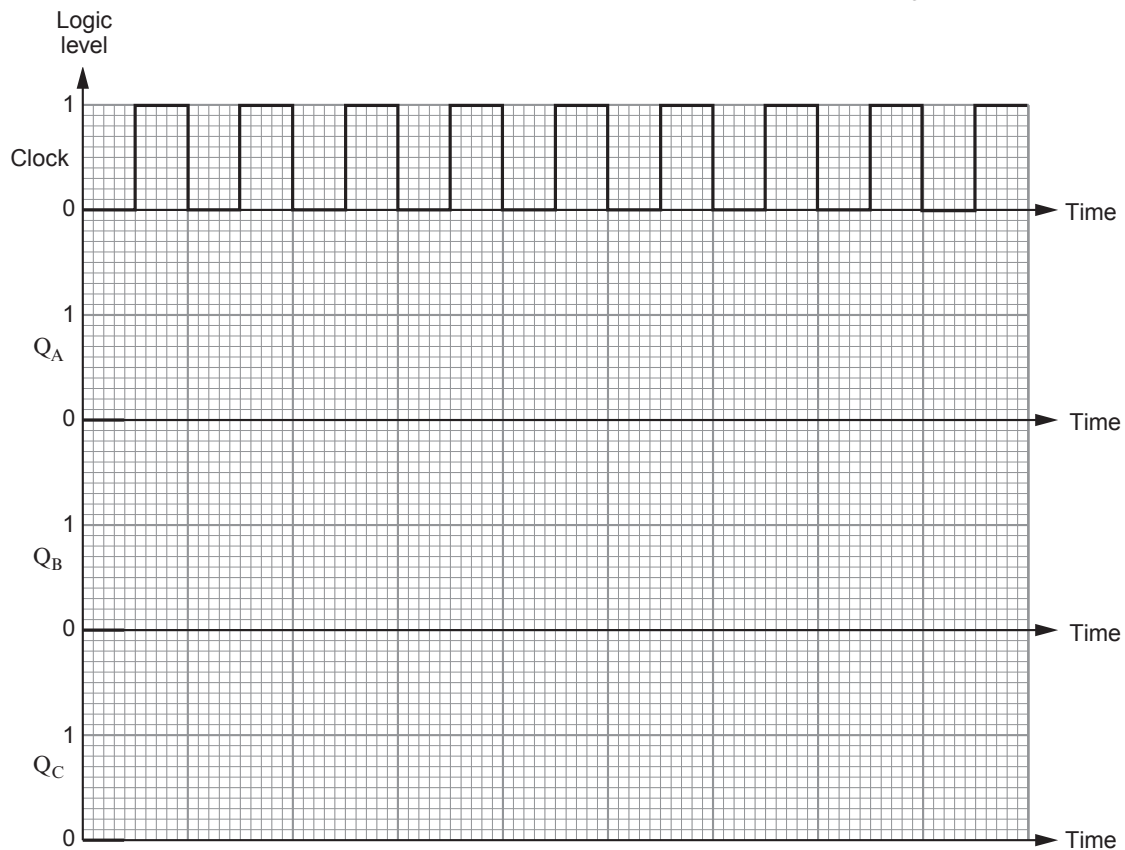
[2]



- (b) The clock in the following diagram produces a square wave output of 480 kHz. This is fed into the series of 4 D-type flip-flops shown below. The D-type flip-flops are rising-edge triggered.



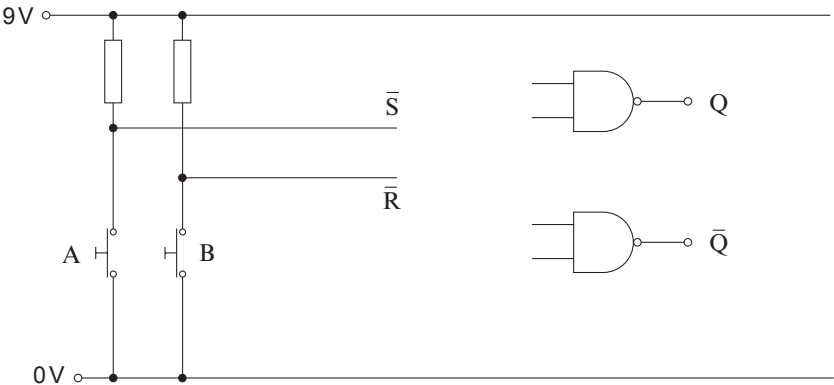
- (i) What is the frequency at the output Q_A ? [1]
-
- (ii) Which output will produce a frequency of 60 kHz? [1]
-
- (iii) The timing diagram below shows the output from the clock. Complete the diagram to show the signal at outputs Q_A , Q_B and Q_C . [3]



Question 8

8

5. (a) Complete the diagram to show how two NAND gates can be connected to make a bistable latch and how the two switches A and B can be used to set and reset the system. [2]

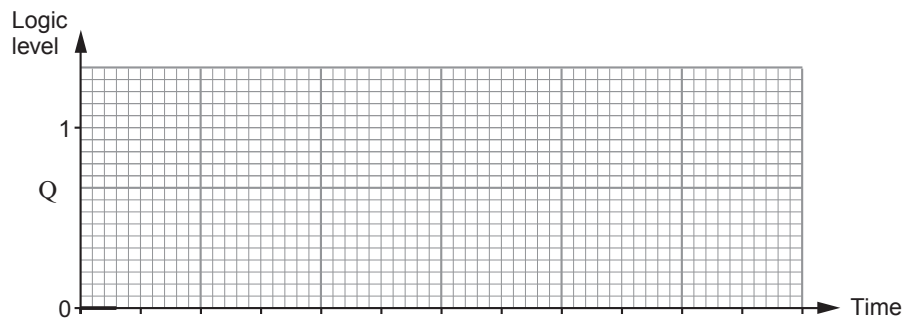
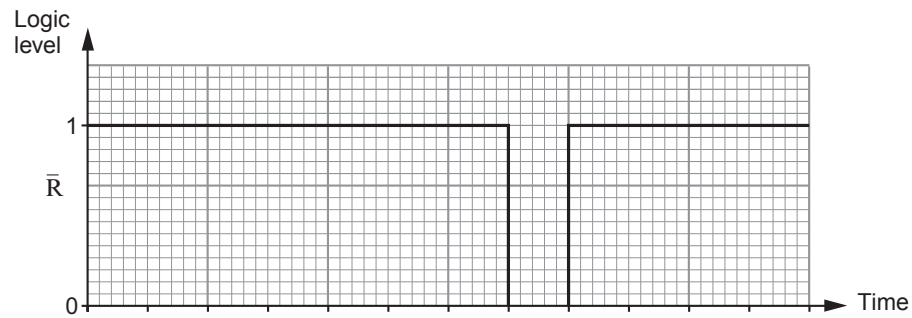
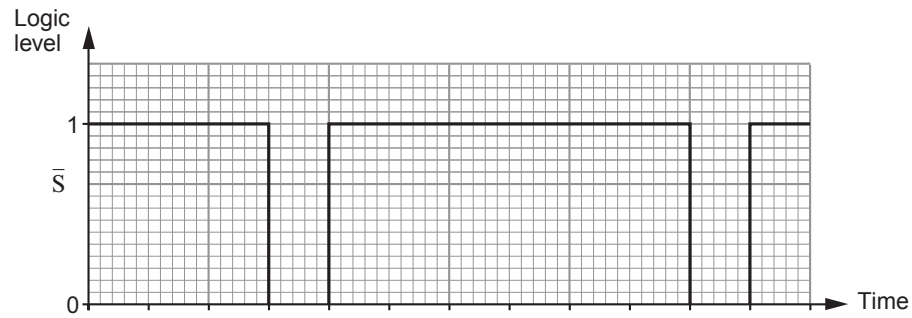


- (b) Complete the table with the correct logic levels. Output Q is initially low. [2]

Switch position		Logic levels		
A	B	$\bar{S}$	$\bar{R}$	Q
OPEN	OPEN			
CLOSED	OPEN			
OPEN	CLOSED			
CLOSED	CLOSED			

Examiner
only

- (c) The input logic states of the bistable is shown below. Draw the output signal Q on the axes provided. [1]



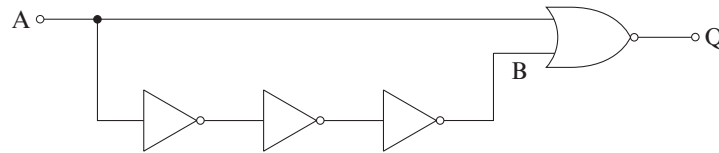
- (d) Why is it desirable that $\bar{S}$ and $\bar{R}$ are prevented from being logic 0 at the same time? [1]

.....

Question 9

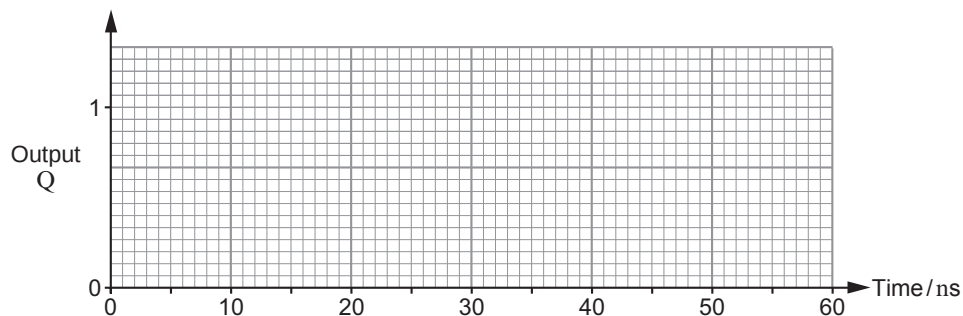
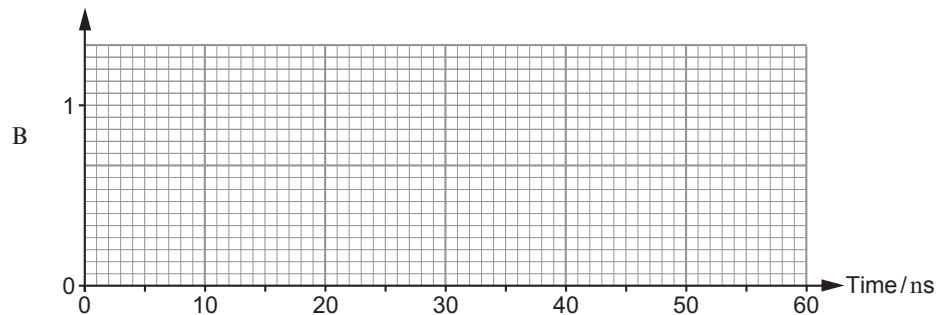
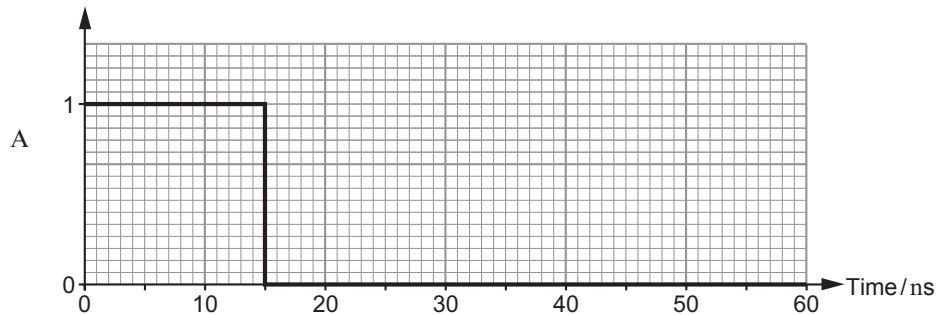
10

6. Consider the following arrangement of logic gates.



Each gate has a propagation delay of 5 ns.

- (a) Complete the following diagram to show how the signal at B and the output Q change when the pulse shown is applied to input A. **Initially, output Q is at logic 0** and input A has been high for a long time. [4]

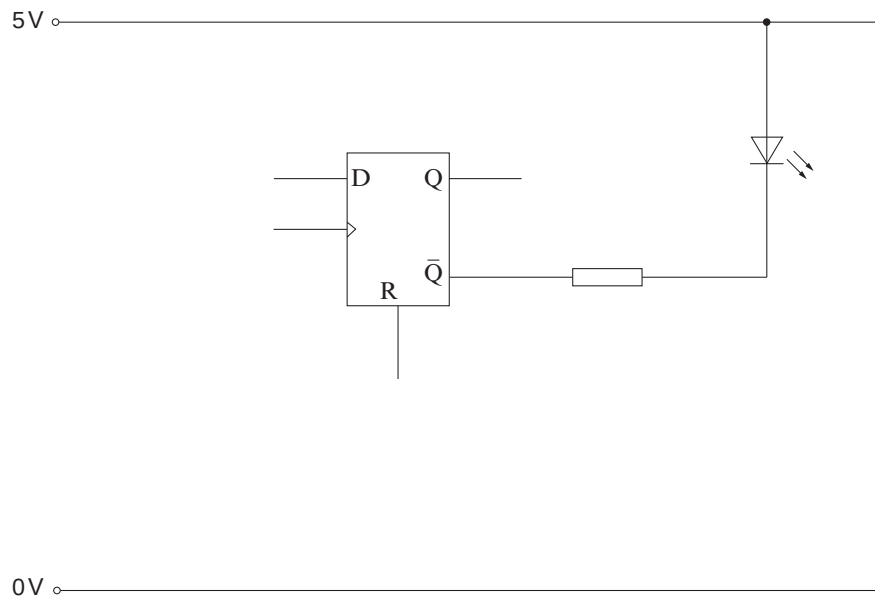


- (b) Give an application for this arrangement of logic gates. [1]

Question 10

12

7. The diagram shows a *rising-edge triggered* D-type flip-flop. R is *active high*.



- (a) Add the necessary components to the diagram such that the D-type can be **reset** with the momentary press of a switch. [2]

- (b) Complete the following sentence.

When the D-type is reset the output $\bar{Q}$ will be at logic and the LED will be

[1]

- (c) The signals shown in the timing diagrams below are applied to the circuit. Complete the timing diagram for the outputs Q and $\bar{Q}$.

[3]

Examiner
only