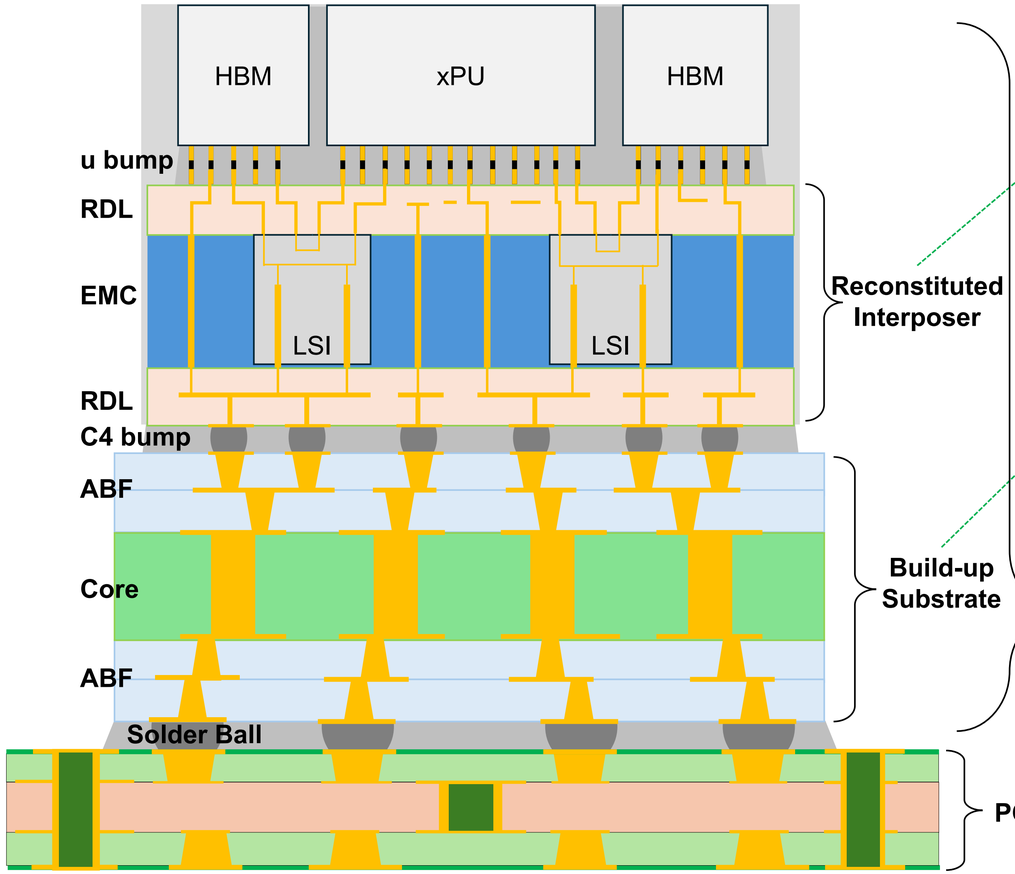
Challenges of CoWoS and AI Server



ISSUE - 1 : Interposer Yield:

- CTE mismatch between LSI / EMC & RDL (PSPI/Cu)

We propose **HBI** (Hybrid Interposer) : LSI in **XENOMAX** PI (CTE 3 ppm/C)

ISSUE - 2 : Substrate Warpage:

- CTE mismatch between Silicon, Interposer and Substrate
- Industry is developing Glass Core but
  - Challenge in TGV electroplating
  - Micro-crack in Glass Core

We propose **Ceramic Core** **oToC**

We propose **Ceramic IIS** (Interposer Integrated Substrate) **CToG**

ISSUE - 3 : (CoW)oS Shortage & Cost:

We propose **Co(FoS)** **HBS step-1**

→ upgrade substrate resolution

ISSUE - 4 : Complicated stack-up limits the performance of AI server

- **Electrical interconnect :** massive and long electrical paths → High power consumption — We propose **n*(CoR)o(FoS)** **HBS step-2**
- **Optical interconnect** : Industry is developing CPO → Challenges in Fiber/Chip connect and networking

We propose **eo-HBS** (Hybrid Substrate) : RDL**(e)** & Waveguide**(o)** on a large substrate as **Motherboard** **HBS step-3**

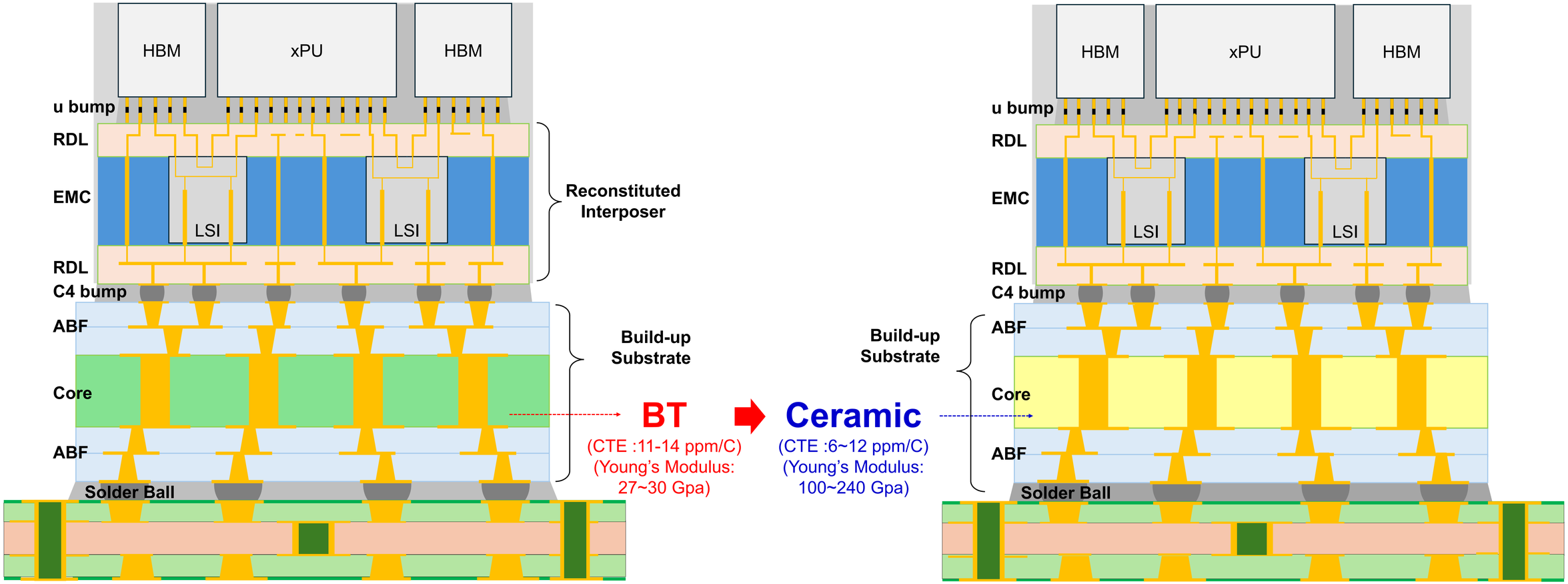
PanelSemi Proposal for Issue-2

●Build-up substrate

➢ Organic Core → Ceramic Core

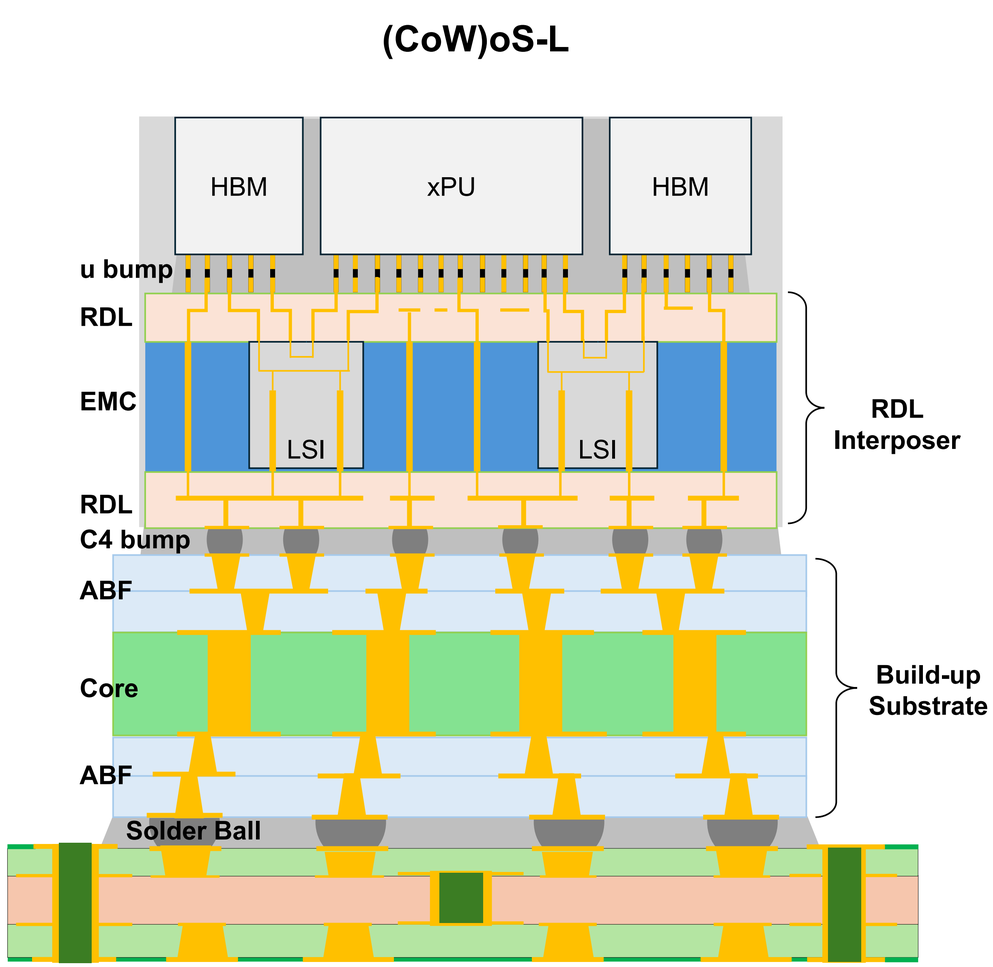
CTE : ppm/C

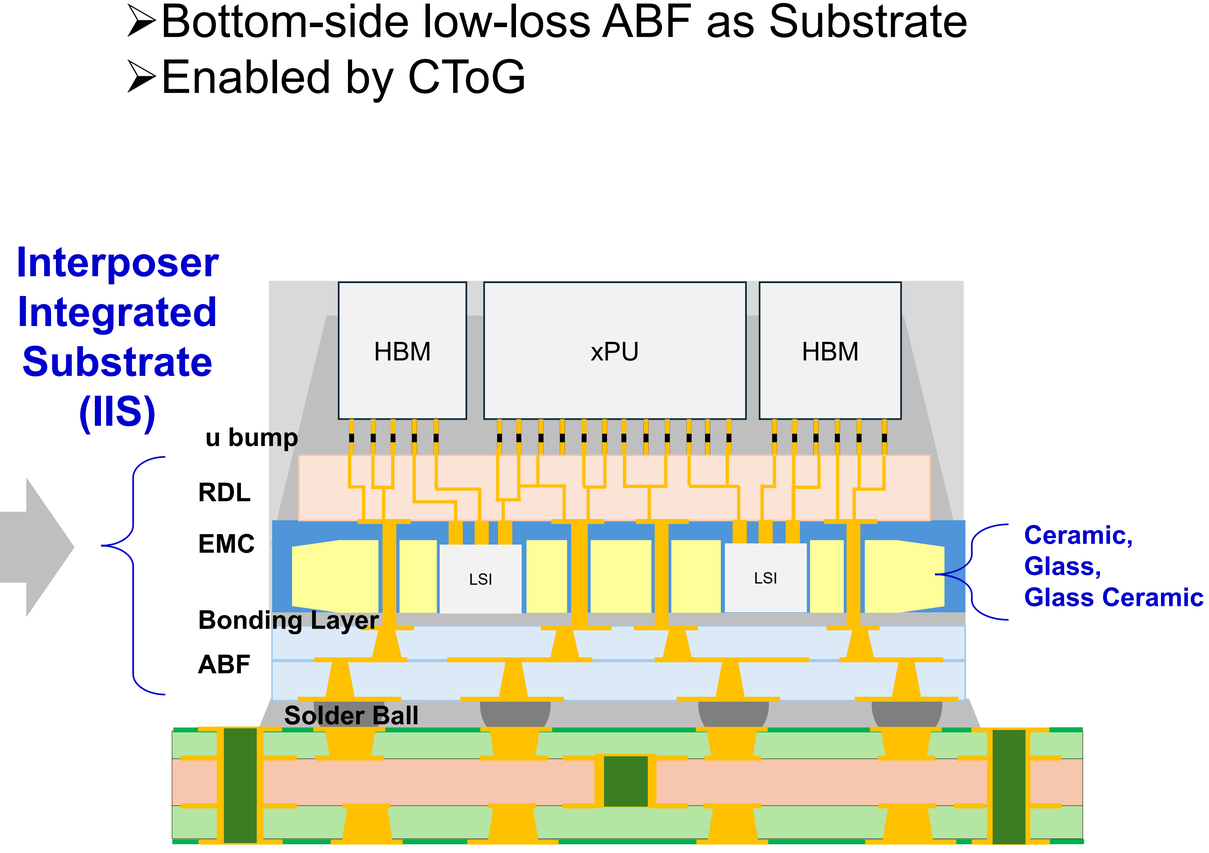
Layer	(CoW)oS-L	PanelSemi Proposal
xPU, HBM	Si Chip: ~3	Si Chip: ~3
Reconstituted Interposer	LSI :~3 EMC : 10-16 PSPI in RDL : ~40 Cu in RDL: ~17	LSI :~3 XENOMAX: ~3 PSPI in RDL : ~40 Cu in RDL: ~17
Build-up Substrate	**Substrate : 11-14**	**Ceramic Core : 6~12**



Ceramic/Glass IIS (Interposer Integrated Substrate)

- **Utilizing the excellent rigidity of Ceramic/Glass**
  - ➢Asymmetric buildup layer stack
  - ➢Top-side fine-pitch RDL as Interposer
  - ➢Bottom-side low-loss ABF as Substrate
  - ➢Enabled by CToG



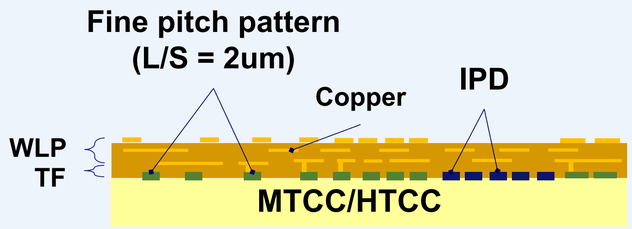


Fine-pitch Ceramic Substrate & FoS (Film on Substrate)

•Fine-pitch Ceramic Substrate Process

➢Fabricate fine-pitch pattern (L/S = 2um) directly on **MTCC/HTCC** substrate by WLP ecosystem

WLP: Wafer Level Packaging

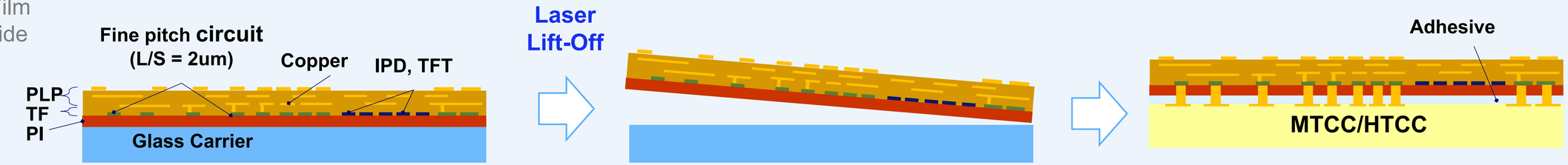


•Fine-pitch FoS (Film on Substrate) Process

➢Fabricate fine-pitch pattern (L/S = 2 um) onto **PI (XENOMAX PI)** on Glass by PLP ecosystem

➢Lift off **PI w/ pattern** from glass then laminate **PI w/ pattern** onto **MTCC/HTCC** substrate

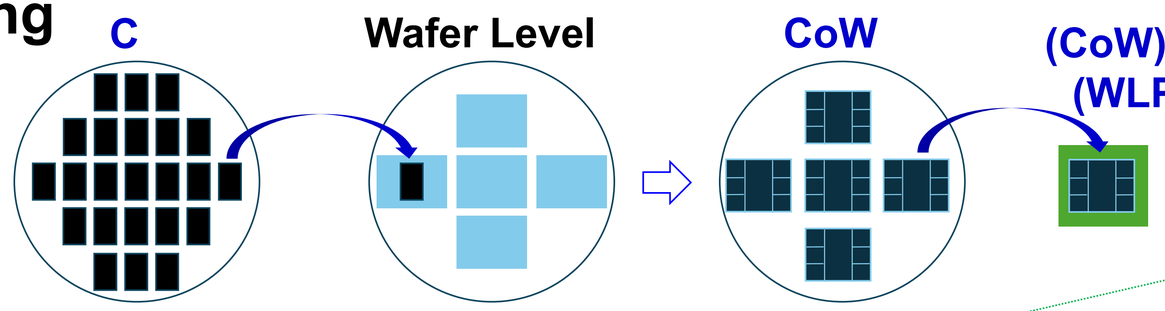
PLP: Panel Level Packaging
IPD: Integrated Passive Devices
TF: Thin Film
PI: Polyimide



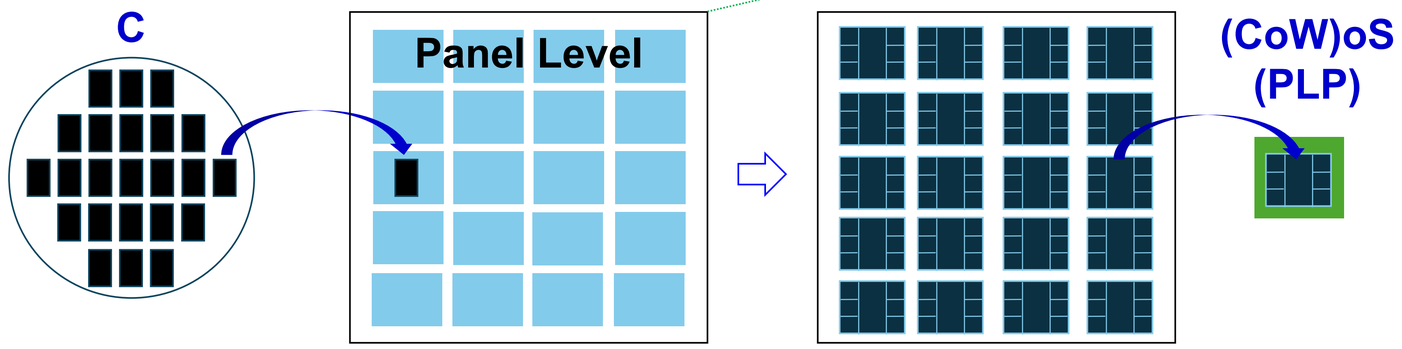
(CoW)oS and Co(FoS) Ecosystem

Path finding

1. Now : WLP



2. Next : PLP

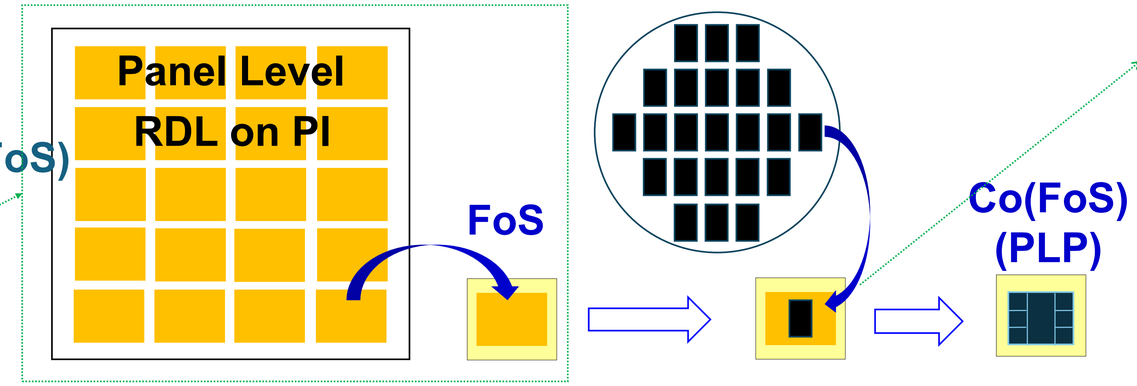


Difficult processes after die-bond
→difficult for OSAT (Yield responsibility)
→heavy burden for Chip maker

- May use TFT G4.5 (730x920mm) for RDL, then cut it into 600x600mm for die-bond, molding,..
- A substrate larger than 600x600mm → better uniformity, less warpage
- The only waste of BOM is glass, other materials cover 600x600mm only

3. PanelSemi Proposal : Co(FoS)

Leverage existing miniLED process & IP



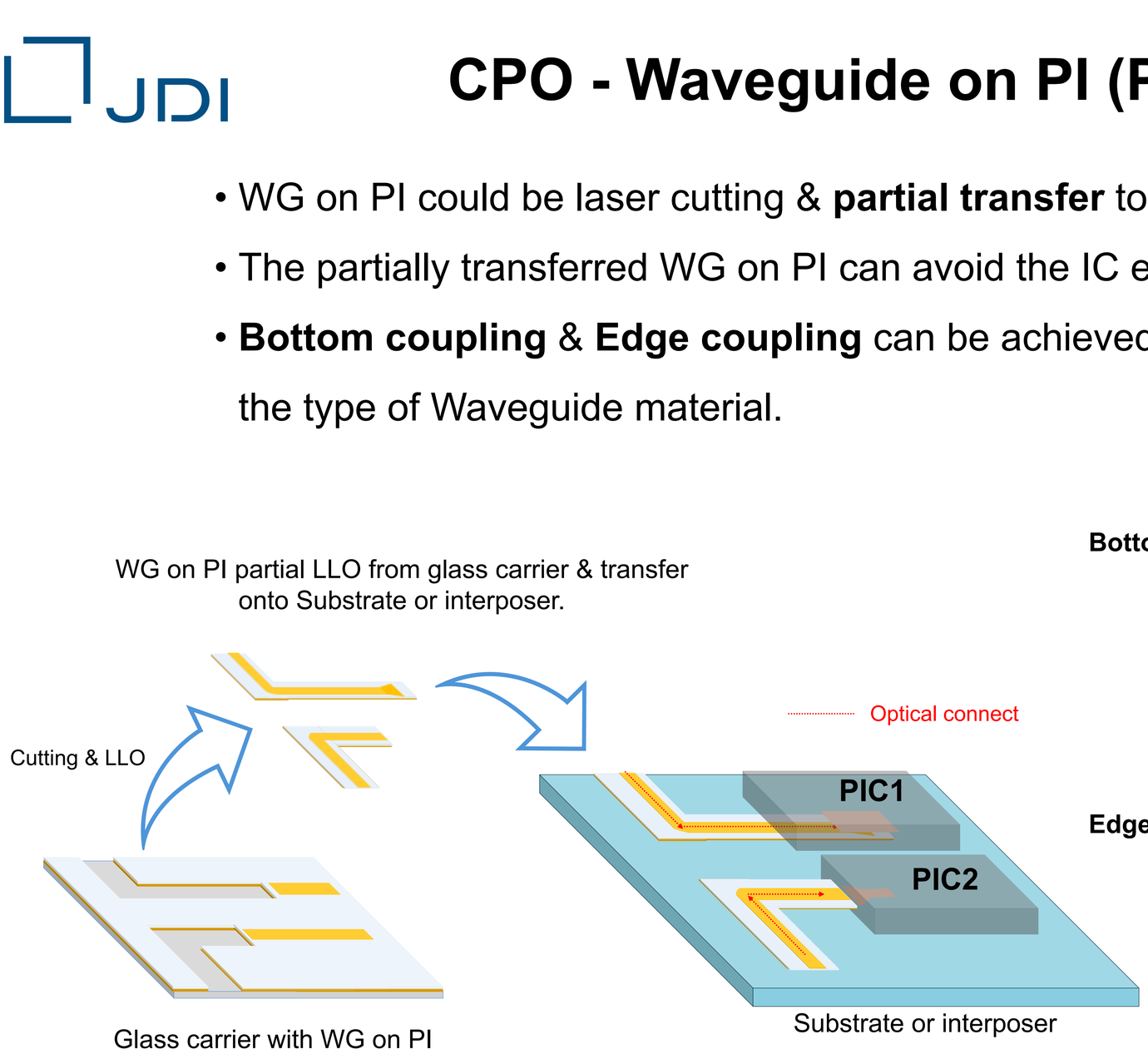
Share burden by Substrate & OSAT

- Bond Known-Good-Die on Known-Good-Substrate → high yield
- Clear supply-chain responsibilities among Chip, Substrate and OSAT
- Solve (CoW)oS shortage & cost issues

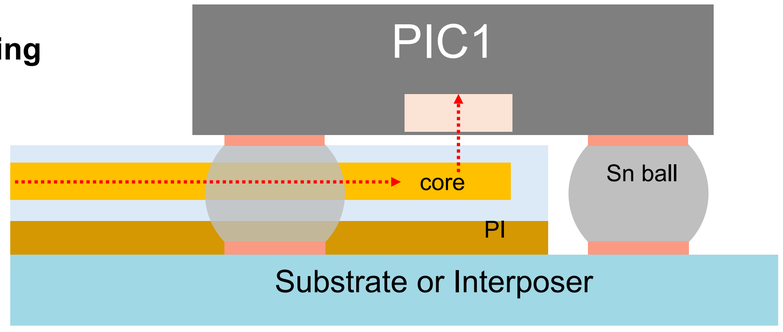
CPO - Waveguide on PI (Partial Transfer)

- WG on PI could be laser cutting & **partial transfer** to Substrate or Interposer.
- The partially transferred WG on PI can avoid the IC electrical connection pad.
- **Bottom coupling** & **Edge coupling** can be achieved by adjusting the cladding thickness according to the type of Waveguide material.

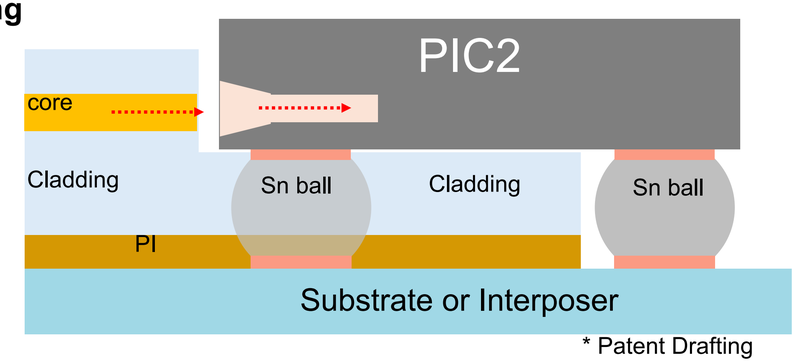
WG on PI partial LLO from glass carrier & transfer onto Substrate or interposer.



Bottom Coupling



Edge Coupling



* Patent Drafting

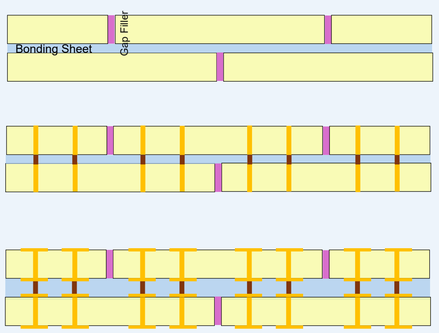
Overcome the Size Limitation of Ceramic

1.oToC (Offset Tiling of Ceramic)

Blank Ceramic

TCV

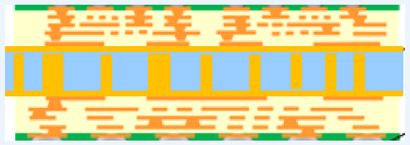
TCV + 2-Metal



+ Laser drill
Metal fill

Build-up Substrate Maker

ABF Process

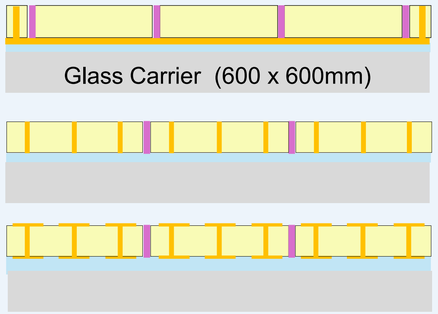


2.CToG (Ceramic Tiling on Glass)

Blank Ceramic

TCV

TCV + 2-Metal

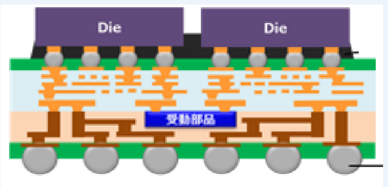


+ Laser drill
Metal fill

PLP Maker

(Ceramic IIS)
1.RDL only
2.ABF + RDL

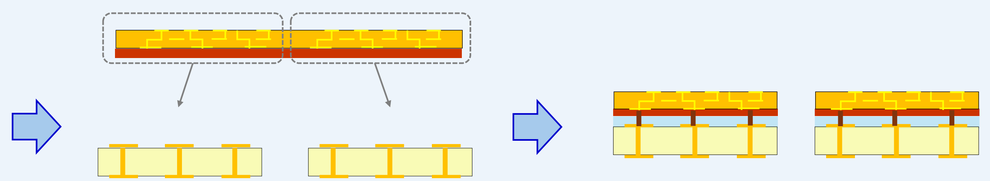
\+ Die Bond etc



3.FoS (PI RDL on Ceramic)

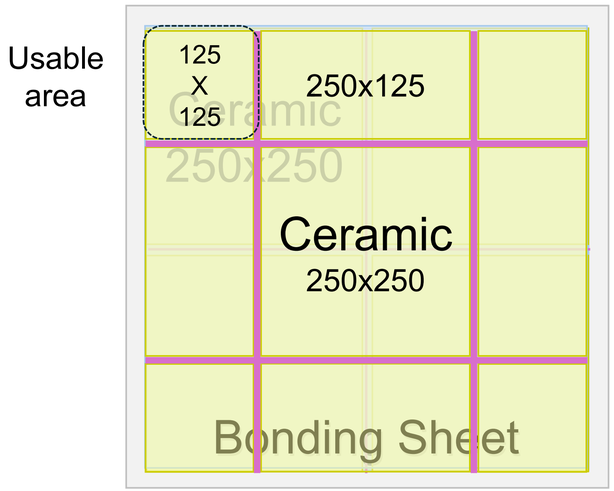
PI RDL on Glass

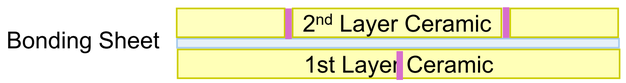
TCV + 2-Metal



Offset Tiling of Ceramic (oToC)

- **oToC is a method of tiling ceramic substrates to achieve a larger size, which is suitable for the double-sided process commonly used by build-up substrate makers. It may also be used for the single-sided process by TFT or PLP makers.**





- **Prepare a glass carrier**
- **Attach bonding sheet to the glass carrier**
- **Attach ceramic tiles (1st Layer) onto the carrier**
- **Dispense gap filler between the ceramic tiles**
- **Attach another bonding sheet**
- **Attach ceramic tiles (2nd Layer) with an offset to the 1st Layer**
- **Dispense gap filler between the ceramic tiles**
- **Remove the carrier**
- **4 x 4 usable areas, each 125 x 125 mm**
- **Cross-Section**

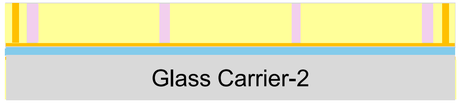
- **oToc Size could be**
  - **(1) 510x515mm, (2) 600x600mm, (3) 620x750mm [G3.5 TFT], (4) 730x920mm [G4.5 TFT] above and more.**
- **Polishing process can be added if needed.**

Ceramic Tiling on Glass (CToG)

PANEL SEMI 方略電子

•**CToG is a method of tiling ceramic substrates onto a larger size glass carrier.**

•**Prepare a glass carrier-1**
•**Attach bonding sheet to the glass carrier-1**
•**Attach ceramic tiles onto the carrier**
•**Attach ceramic bars with through via onto the carrier**
•**Attach dummy ceramic tiles at corners**
•**Dispense gap filler between the ceramic tiles**
•**Deposit Cu seed layer**
•**Attach bonding sheet above Cu seed layer**
•**Attach glass carrier-2 on top and remove glass carrier-1**



•**Cross-Section**

•**CToG Size could be**
(1) 730x920mm, (2) 600x600mm, (3) 510x515mm and more.
•**Polishing process can be added if needed.**