IEEE WMED 2026 Technical Program

7:15 - 7:55	**Check-In, Registration, and Breakfast (Double R Ranch Room)**		
8:00 - 8:10	**Welcome Address by General Chair, IEEE WMED 2026**		
	Double R Ranch Room		
	Chunhua Yao, Principal Engineer, Micron Technology Inc.		
8:10 - 9:10	**Plenary Session**		
	Double R Ranch Room, Session Chair: Brian Callaway		
	Visionary Talk **Powering the AI Era: Memory Technology at the Center of Compute Scaling** Shigeru Shiratake, Senior VP, DRAM Technology and Products Group, Micron Technology Inc.		
9:10 - 10:50	**Keynotes Session**		
	Double R Ranch Room, Session Chair: Nidish Vashistha		
	9:10 - 10:00	**Keynote Talk I:** **Decomposing At-Scale AI Inference: The Where, What, and Why of Memory Technologies** Dave Nellans, Senior Director, Architecture Research Group, Nvidia	
	10:00 - 10:50	**Keynote Talk II:** **Hardware Security: The Next Frontier** Tamara Schmitz, Director, Product Security Group, Micron Technology Inc.	
10:50 - 12:10	**Invited Tutorial**		
	Double R Ranch Room, Session Chair: Tim Hollis		
	Machine Learning-Based Interface Design for Equalization-Less (or Minimal-Equalization) Channel Compensation Tejasvi Anand, Ramin Javadi, and Jong Hyun (John) Kim, Oregon State University		
12:10 - 13:00	**Lunch Break (Double R Ranch and Skyline Room)**		
12:10 - 13:00	**Poster Session (Double R Ranch)**		
13:00 - 13:45	**Invited Talk**		
	Double R Ranch Room, Session Chair: Mandar S. Bhoir		
	Lithography Technology for Future Computing Technology Michael Lercel, Senior Director, Strategic Marketing, ASML Holding N.V.		
13:45 - 14:40	**Panel Discussion**		
	Double R Ranch Room, Moderator: Alex Sheldon		
	Hardware Innovation in the AI Era: Memory, Compute and Security Panelists: Tamara Schmitz, Director, Product Security, Micron Technology Inc. Zain Ul Abideen, Assistant Professor, ECE Department, University of Idaho Dave Nellans, Senior Director, Architecture Research Group, Nvidia Corporation		
14:40 - 14:50	**Break (Double R Ranch and Skyline Room)**		
14:50 - 15:20	**Special Talk**		
	Double R Ranch Room, Session Chair: Alex Sheldon		
	On-Chip Data-Path Equalization Using Distributed and Interleaved Inverted Feedback Timothy Hollis, Chulkyu Lee and Chris Holub, Micron Technology Inc.		
15:20 - 16:50	**Parallel Talks**		
	Track 1 (Devices and Process)		**Track 2 (Circuits and Systems)**
	Double R Ranch Room, Session Chair: Amit Ohri		**Skyline Room, Chair: Curtis Cahoon**
	15:20 - 16:00	**Scaling 2D CMOS: From Transistors to 3D Integrated Systems** Saptarshi Das, Ackley Professor of Engineering and MRI Fellow, Pennsylvania State Univ.	**AI-Driven Design and Synthesis of High-Performance Analog Integrated Circuits** Mohamed Elamien, Assistant Professor, McMaster Unviersity
	16:00 - 16:25	**Study of Access Region Sheet Resistance in Superlattice U-GaN HEMT and its Compact Modeling** Vikram Magendar and Hiu Yung Wong, San Jose State University	**Machine Learning-Based Flaky Test Detection and Suppression for UVM Verification Regressions** Vikash Kumar, Yunus Akhtar and Ravi Gupta, Intel Corporation
	16:25 - 16:50	**Design Tradeoffs of Through-Silicon-Carbide Vias for High-Temperature 3D SiC IC Integration** Sahithi Thota, Li Song and Feng Li, University of Idaho	**Validation Proportion Matters: Generalization Stability of YOLO-Based Wafer Defect Detection with Limited Data** Chih-Kuan Ho and David Parent, San Jose State University
17:00 - 17:10	**Closing Remarks by General Chair - Announcement of Poster Winners, End-of-Conference Raffle Winners, and WMED 2027**		