

INSTITUTE OF ENGINEERING AND MANAGEMENT

GOURAHARI VIHAR, PO: RANIPUT, JEYPORE – 764 005

LESSON PLAN

Name of the Subject: Digital Electronics

Name of the Faculty: Suvendu Swain

Semester: Third Semester

Semester From: July to December

Branch: ETC Engineering

No. of Weeks: 15 Weeks

Week	Class Day	Theory/ Practical Topics
1 st	1 st	1.1 Introduction to Digital Electronics
	2 nd	1.1 Introduction to various number systems and conversion from one system to another number system
	3 rd	1.2 Arithmetic operations of Binary numbers, 1's & 2's compliment form and subtraction using compliment method
	4 th	1.3 Weighted & non-weighted codes- Binary,excess-3 and Gray
2 nd	1 st	1.4 Logic Gates – symbol, function, truth table & timing diagram
	2 nd	1.5 Concept of Universal gates and realization of various gates using NAND gate
	3 rd	1.5 Realization of various gates using NOR gate
	4 th	1.6 Boolean algebra, Boolean expression
3 rd	1 st	1.6 Various Boolean laws and De-Morgan's Theorem
	2 nd	1.7 SOP and POS representation of Logic Expressions
	3 rd	1.8 Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don't care conditions
	4 th	Revision of Unit – 1 and solving numerical from the chapter
4 th	1 st	2.1 Introduction to various Combinational logic circuits
	2 nd	2.1 Adder- half adder and Full Adder
	3 rd	2.1 Subtractor – Half and Full Subtractor
	4 th	2.1 Serial and Parallel Binary 4-bit adder
5 th	1 st	2.2 Multiplexer(4:1)
	2 nd	2.2 De-multiplexer (1:4)
	3 rd	2.2 Encoder
	4 th	2.2 Priority encoder
6 th	1 st	2.2 3-bit Comparator
	2 nd	2.3 Seven segment Decoder
	3 rd	Revision of Unit – 2
	4 th	3.1 Differentiation between Combinational & Sequential Logic circuit
7 th	1 st	3.1 Principle of Latch and Flip-flop and its operation
	2 nd	3.1 Types of Flip-flop – SR, JK, D, T
	3 rd	3.2 SR Flip-flop using NAND & NOR latch(unclocked)
	4 th	3.3 Clocked SR flip flop
8 th	1 st	3.3 Clocked JK, D and T flip-flop
	2 nd	3.3 Circuit diagram, Truth table and logical expression of SR and JK flip-flop
	3 rd	3.3 Circuit diagram, Truth table and logical expression of D and T flip-flop
	4 th	3.3 Operation of Master- Slave JK flip-flop
9 th	1 st	3.4 Concept of Racing and how it can be avoided

	2 nd	3.4 Advantages and Disadvantages of Master- Slave JK flip-flop
	3 rd	Revision of Unit – 3
	4 th	4.1 Shift registers- SISO, SIPO, PISO, PIPO
10 th	1 st	4.1 Operations of shift registers
	2 nd	4.2 Universal shift registers-Applications
	3 rd	4.3 Counters and its types and operation 4.4 Binary counter, Asynchronous ripple counter
	4 th	4.4 Operation of Decade counter, Synchronous counter and Ring counter
11 th	1 st	4.5 Concept of memories- RAM, ROM, SRAM, DRAM & PS RAM
	2 nd	4.6 Concept of PLD and its applications
	3 rd	Revision of unit – 4
	4 th	5.1 Introduction to A/D & D/A convertors and its need
12 th	1 st	5.2 D/A conversion using weighted resistors methods
	2 nd	5.3 D/A conversion using R-2R ladder network
	3 rd	5.4 A/D conversion using counter method
	4 th	5.5 A/D conversion using Successive approximate method
13 th	1 st	Revision of unit – 5
	2 nd	6.1 Concept of Integrated circuit and its need in present.
	3 rd	6.1 IC Fabrication process
	4 th	6.1 Description of various steps involved in IC Fabrication process
14 th	1 st	6.2 Digital ICs and its characteristics- propagation Delay , Fan-in, fan-out, power dissipation
	2 nd	6.2 Explaining terms like Noise margin, Power supply requirement and Speed with reference to logic Families
	3 rd	6.3 Features, Circuit operation & applications of TTL(NAND) logic circuit
	4 th	6.3 Features, Circuit operation & applications of CMOS logic circuit using NAND gate
15 th	1 st	6.3 Features, Circuit operation & applications of CMOS logic circuit using NOR gate
	2 nd	6.3 Comparing different logic circuits
	3 rd	Revision of Unit – 6
	4 th	Overall revision of the subject