Gryphon100 Series

Complete Rackmount 33 Mbps Bit Synchronizer System

Dual or Quad Channel / Bit Sync / Frame Sync / IRIG Time Code Reader / Frame Archiver

ULYSSIX TECHNOLOGIES, INC.

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A Woman-Owned Small Business
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Gryphon100 Series

The Gryphon100 Multiple Bit Synchronizer/Frame Synchronizer System is a fully integrated chassis solution that may be configured for 2 or 4 bit synchronizers/ frame synchronziers with an internal IRIG time code reader. the chassis is a 2U rackmount system containing a large LCD graphic display, an integrated keypad with external computer Ethernet interface and large LED indicators for lock status.

Gryphon102 2U Dual Bit Frame Sync System

Gryphon104 2U Quad Bit Frame Sync System

Dual or Quad Bit Synchronizer

Designed using all DSP filter algorithms in FPGA technology for maximum performance capability

Accepts all IRIG 106-09 PCM codetypes

Bit Sync programmable input rates from 1 bps to 33 Mbps

Less than 1 dB to theoretical bit sync BER performance

All IRIG 106-09 codetypes are selectable for PCM output

Up to 4 inputs per Bit Sync, program selectable

Also available with I&Q interleaving

Handles PCM streams from 1 bps up to 33 Mbps

Supports all IRIG Class II 16 to 33 bit frame synchronizer patterns

Supports minor frame lengths up to 16,777,216 bits with up to 1024 subframes per Major Frame

Programmable number of minor frame bit slips and allowable sync errors

Advanced algorithm to allow for varying frame sizes

IRIG Time Code Reader

Separate analog path onto card

Supports IRIG A, B, G & NASA-36

Used for both IRIG time display and/or minor frame time tag header information

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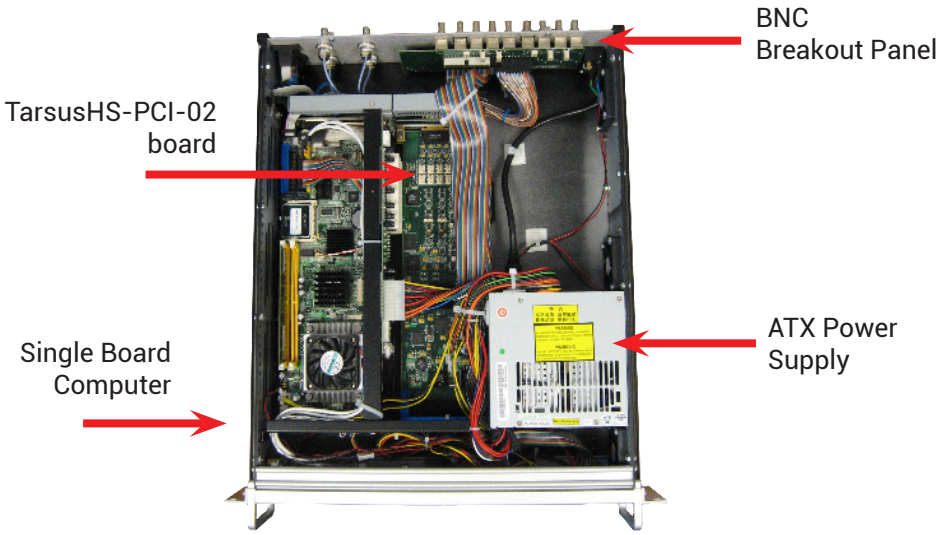
The Gryphon100 gives the ability to archive frame synced data from each of its channels to an external memory drive via 2 USB ports. The internal IRIG time code reader time stamps the archied data at the beginning of each minor frame for enhanced post-processing analysis.

Gryphon102 Internal View



Dual Channel Frame Sync Archive

Can archive 2 PCM streams simultaneously from 1 bps up to 33 Mbps.

Records PCM data to a raw binary file to external memory via USB ports

All archived data has 96 bit minor frame IRIG Time Header inserted in front of sync including 64 bits of BCD Julian time, minor frame counter and status bits

Additional Features

Viterbi
- Using a 7 bit Soft Decision, this algorithm allows for the decoding of a convolutionally encoded data stream
- Results in a 3-5 dB improvement in noise tolerance

I&Q Ambiguity
- Utilizes frame lock to determine the I&Q stream identity of demodulated QPSK signals

Best Source Selection
- Based off of Frame Sync data and/or Eb/N0 calculation

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Specifications

Bit Synchronizer Input Specifications

Input Data Rate	Bit Sync programmable input tunable rates from 1 bps to 33 Mbps for NRZ-L/M/S, RNRZ-L and 1 bps to 16.5 Mbps for Bi-Φ L/M/S
Input Source	4 independent inputs per bit sync (3 single ended BNC, 1 differential input BNC)
Input Impedance	Hi-Z/75Ω/50Ω, single ended input, software selectable with reed relay isolation
Maximum Safe Input	± 35 VDC
Input Signal Level	30 mVpp to 10 Vpp
DC Input Level	+/- 5 VDC
Input PCM Codetypes Modes	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S, program selectable (consult factory for other codetypes)
Derandomizer Input	RNRZ-11/15, forward/reverse, program selectable
Input Polarity	Normal, inverted or auto selectable using frame sync correlator

Bit Synchronizer Data Specifications

Loop Bandwidth	0.01% to 3.0%, to the programmed bit rate
Capture Range	+/-3 times of the programmed loop bandwidth
Data Tracking Range	+/-5 times of the programmed loop bandwidth
Sync Acquisition	less than 32 bits, typically 100 bits max
Bit Error Probability	Less than 1 dB to theoretical bit sync BER performance for bit rates up to 20 Mbps, less than 2 dB to theoretical from 20 Mbps to 30 Mbps, less than 2.7 dB to theoretical to 33 Mbps

Bit Synchronizer Output Specifications

Number of Outputs	Gryphon102 -3 sets of Clock and Data per bit sync with independent PCM code encoders (2 sets single ended BNC, 1 set differential triax) Gryphon104 -2 sets of Clock and Data per bit sync with independent PCM code encoders (2 sets single ended BNC)
Clock Output	0°, 90°, 180°, 270°, program selectable per output
Output Signal Levels	TTL Level driven and RS-422 differential
PCM Output	TTL Level driven and RS-422 differential
PCM Output Code Types	NRZ-L/M/S, RNRZ-L, RZ, Bi-Φ L/M/S or RNRZ 11/15, program selectable
PCM Output 2 Input Selection	Internal Bit Sync or excepts an external NRZ-L input signal
PCM Tape Output	1 bipolar per bit sync, programmable level 1 to 10 Vpp, ± 5 VDC offset 0.1 steps, BNC (data only)

Frame Synchronizer Specifications

Input Data Rate	Up to 33 Mbps
Input Signals	TTL Level single ended, RS-422 differential or direct from Bit Sync section of the PCM Processor, NRZ-L and clock
Minor Frame Length	3 to 16,777,216 bits
Major Frame Length	1 to 1024 minor frames per major frame
Frame Sync Pattern	16 to 33 bits
Frame Sync Location	Leading the minor frame
Frame Sync Strategy	Search-Check-Lock, programmable counts per step
Subframe Sync	FCC or SFID
Sync Error Tolerance	0 to 8 bits, program selectable
Bit Slip Window	0 to 9999 bits, program selectable
Data Polarity	Normal or inverted on a channel by channel basis

Time Code Reader Specifications

IRIG Codetypes	IRIG A, B, G & NASA-36

System Specifications

Processing	Single Board Processor with minimum 2 Gb Flash Drive
Memory	1 GB minimum RAM
Operating System	Custom Ulyssix operating system with TCP/IP, USB and RS232 Interfaces
Display	240 x 64 Graphic LCD Display
Input	Integrated 24 button keypad
Dimensions	2U rackmount 19" x 3.5" x 20"
Ethernet	10/100 BaseT with TCP/IP
Power	300 Watt ATX power supply, 100-240 VAC Full Range
Temperature Range	Operating: 0°C to 50°C Storage: -20°C to 60°C

Ordering Options

Gryphon102	Two Channel 33 Mbps Digital Bit Sync/Frame Sync with IRIG Time Code Reader and frame archive system including 2U rackmount chassis with Ulyssix embedded operating system, built-in graphic display, embedded keypad entry system and RS-232 HyperTerminal and TCP/IP interface
Gryphon104	Four Channel 33 Mbps Digital Bit Sync/Frame Sync with IRIG Time Code Reader and frame archive system including 2U rackmount chassis with Ulyssix embedded operating system, built-in graphic display, embedded keypad entry system and RS-232 HyperTerminal and TCP/IP interface
Gryphon102-OPT-VIT	Viterbi Decoder Upgrade for the Gryphon102 Chassis
Gryphon104-OPT-VIT	Viterbi Decoder Upgrade for the Gryphon104 Chassis
Gryphon102-OPT-CRC	Cyclic Redundancy Checker is for use on PCM data streams with embedded error detection data within each minor frame
Gryphon104-OPT-CRC	yclic Redundancy Checker is for use on PCM data streams with embedded error detection data within each minor frame
Gryphon102-OPT-BSS	Best Source Selector Option is for selection between 2 identical streams of data based on frame sync status
Gryphon104-OPT-BSS	est Source Selector Option is for selection between 2 identical streams of data based on frame sync status
ULX-C-300-S-124	General Devices C-300-S-124 24" rack mount slides
ULX-B308	General Devices B308 extension slides to 36"
Gryphon Remote Control Software	Windows GUI for remote operation of multiple units

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***Specifications are subject to change without notice.** Revised: May 8, 2019*