HyperScape100

Datasheet

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Document History

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1	2019-10-07	First Release
2	2019-10-10	Updated mechanical drawings
3	2021-02-16	Added filter option 4 Updated power consumption figures Updates to interface options Updated Section 7
4	2022-01-12	Removed filter options 1, 2 and 3 Updated Section 1.3 Updated Section 7

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List of Abbreviations

Abbreviation	Description
ADC	Analog to Digital Converter
BOL	Beginning of Life
BW	Bandwidth
CAN	Controller Area Network
CCD	Charge Coupled Device
CE	Control Electronics
CMOS	Complementary Metal Oxide Semiconductor
CSKB	CubeSat Kit Bus
DC	Direct Current
DDR	Double Data Rate
dTDI	Digital Time Delay Integration
FPGA	Field Programmable Gate Array
FEE	Front-End Electronics
FWHM	Full Width at Half Maximum
GND	Ground
g_{rms}	Gravitation Constant, Root Mean Square ($g = 9.81\ m/s^2$)
GPIO	General Purpose Input Output
GSD	Ground Sampling Distance
HPP	Half Power Point
Hz	Hertz
I^2C	Inter-Integrated Circuit
I/O	Input / Output
LEO	Low Earth Orbit
lp	Line Pairs
LVDS	Low Voltage Differential Signalling
OD	Optical Density
OOB	Out Of Band
OFE	Optical Front-End
PCB	Printed Circuit Board
SDR	Single Data Rate
SEL	Single Event Latch-up
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SU	Sensor Unit
TDI	Time Delay Integration
TID	Total Ionising Dose
U	Unit (CubeSat)
VNIR	Visible and Near-Infrared

1. Overview

The HyperScape100 is a hyperspectral push-broom imager primarily designed for earth observation applications as a payload for CubeSat satellites. It is based on a CMOS image sensor and custom optical filter in the visible and near-infrared (VNIR) spectral range. The HyperScape100 provides line-scan imaging in up to 32 spectral bands, each with digital time delay integration (dTDI). In addition to a panchromatic band, the HyperScape100 has 442 hyperspectral bands with central frequencies ranging from 442 nm to 884 nm in steps of 1 nm.

The optical front-end (OFE) has a large aperture diameter and long focal length within a compact form factor, resulting in a ground sampling distance (GSD) of 4.75 m at an orbital height of 500 km. The modified Cassegrain optical design brings performance to the edge of the field over the whole spectral range at an ultra-low distortion. The HyperScape100 is engineered to withstand the rigours of the space environment and maintain performance across a wide temperature range. Its compact form factor is optimised for integration into 3U or larger CubeSat structures. Figure 1-1 shows the HyperScape100 Imager mounted to mechanical ground support equipment (shown in red) used during shipping of the Imager. The components shown in red are to be removed before flight.

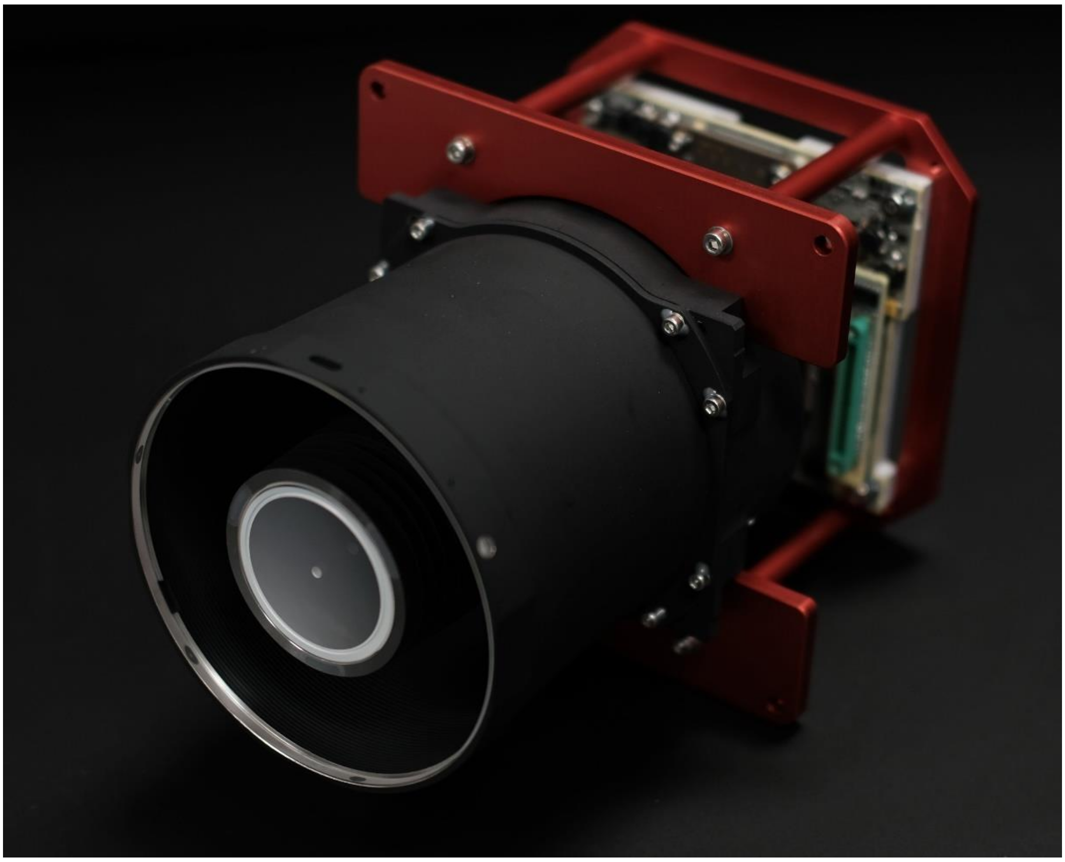

Figure 1-1: HyperScape100 Imager Mounted to Shipping Mechanics

1.1 Features

- 4.75 m GSD (at 500 km orbit height)
- Swath width of 19.4 km (at 500 km orbit height)
- Simultaneously image up to 32 user selectable bands in the VNIR range
- Panchromatic plus 442 hyperspectral bands available
- Hyperspectral FWHM bandwidth of 3.5% of the central wavelength
- Hyperspectral OOB energy less than 0.5% of inband energy over the entire spectral range
- 128 Gigabyte non-volatile ECC storage capacity
- On-board image processing and compression (optional)
- Comprehensive onboard telemetry and health monitoring
- Latch-up current monitoring and on-board power switch with quick turn-off
- Inject AOCS/ADCS parameters and time information into data stream
- Option to integrate pulse per second signal
- Configurable CubeSat Kit Bus (CSKB) compatible connector interface
- Configurable wirable connector interface
- Control options include I^2C, SPI, SpaceWire, RS422
- Image data output options include LVDS, SpaceWire, USART
- Environmental verification based on GSFC-STD-7000

1.2 Applications

- Precision agriculture
- Forestry and land use
- Air quality
- Research

1.3 Key Specifications

Optics	
Focal Length	580 mm ±1 mm
Aperture	95 mm
Full Field of View	2.22° (across-track); < 1.5° (along-track)
Imaging	
Configuration	Line-scan (push broom)
Sensor Technology	CMOS
Cross Track	4096 pixels
Pixel Size	5.5 µm
Pixel Depth	12-bit
Spectral Bands	1 Panchromatic Band 442 Hyperspectral Bands from 442 – 884 nm spaced 1 nm apart
HyperSpectral FWHM	3.5% of the central wavelength
HyperSpectral Accuracy	± 0.5 nm in High Accuracy Mode ± 3.5 nm in High Band Count Mode
Line Rate	Up to 2200 Hz
Signal to Noise Ratio	51 for Panchromatic band using 2 dTDI stages (1)(2) 44 for HyperSpectral band at 700 nm using 8 dTDI stages (1)(2)
On-Board Electronics	
Storage Capacity	128 Gigabyte ECC NAND Flash
Continuous Strip Length	Up to 100000 km in 1 uncompressed, full resolution band (1)
Image Processing	On-the-fly Binning and Thumbnailing
Image Compression	CCSDS 122.0-B-2 Lossy/Lossless (optional) (3)
Control Interface	I^2C or SPI SpaceWire (ECSS-E-ST-50-12C) (optional) RS-422 or RS-485 (optional)
Data Interface	LVDS SpaceWire (ECSS-E-ST-50-12C) (optional) USART (optional) AES-256 Data Encryption (optional)
Physical Interface Options	CSKB Compatible PC-104 connector Wirable high-speed connector
Power Supply	5 V_{DC} ± 250 mV, 1.8 A
Power Consumption	3.5 W when idle or during image data readout 7.0 W during imaging
Mechanical	
Mass	1.18 kg ± 5%
Dimensions	98 x 98 x 176 mm
Environmental	
Operating Temperature	-10 °C to 50 °C
Survivable Temperature Range	-25 to 65 °C
Sun-facing Duration	Sun can be within FFOV for up to 5 minutes
Radiation (TID)	Tested beyond 25 kRad, without shielding, using a ^{60}Co source

(1) Dependant on orbit height, see Figure 3-1. Value calculated at 500 km orbit height.
(2) At-aperture radiance function equal to 100 $W{\cdot}m^{-2}{\cdot}sr^{-1}{\cdot}\mu m^{-1}$ is assumed.
(3) https://public.ccsds.org/Pubs/122x0b2.pdf

1.4 Functional Components

The HyperScape100 imager consists of the following functional components:

- **Optical Front-End (OFE)**: The xScape100 VNIR OFE is used to focus the incoming light onto the focal plane.
- **Sensor Unit (SU):** It consists of the CMOS sensor front-end electronics (FEE) with integrated optical filter. It also includes the sensor plate mechanics, allowing it to be mounted at the OFE's focal plane.
- **Control Electronics (CE)**: The CE provides control and data interfaces to the satellite bus. It performs sensor control, data handling, data storage, and image processing. It is also responsible for power regulation and management, as well as health monitoring and telemetry.

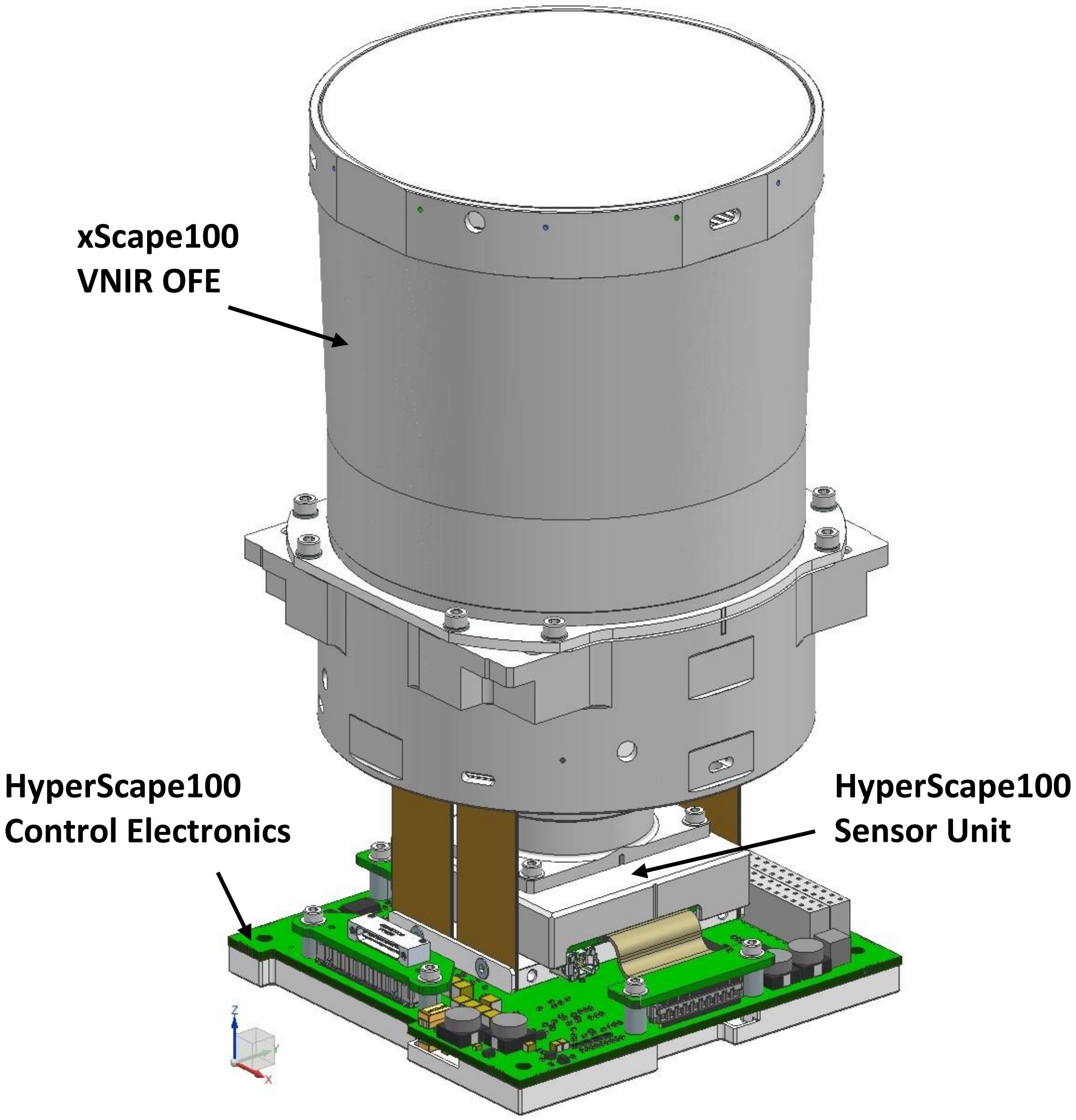

Figure 1-2: HyperScape100 Functional Components

2. Theory of Operation

The Imager is controlled and monitored through the Control Interface to capture images, perform optional image processing, and to read out the image data over its Data Interface.

The HyperScape100 offers two imaging modes: “High Accuracy Mode” caters for high spectral accuracy (± 0.5 nm) with limited dTDI and/or simultaneous bands; “High Band Count Mode” caters for high band and/or dTDI count but with lower spectral accuracy (± 3.5 nm). The imager can switch between these modes in flight. See Section 3.2 for more details and calculating the number of bands/dTDI stages for each mode.

The HyperScape100 is a line scan Imager capable of performing TDI in the digital domain (aka dTDI). This is done by using sensor windowing modes and setting the sensor frame rate equal to the line rate. As the target is being scanned, the same line on the target is imaged N times, where N is the number of TDI stages as configured by the user. These N lines are accumulated to increase the Signal to Noise Ratio (SNR) by factor $\sqrt{N}$. 10-bit Pixel data from the sensor is captured to a buffer, TDI operations are performed as well as binning and thumbnailing, before the image lines are stored at 12-bit pixel depth to the non-volatile flash memory. Binning and thumbnailing is performed in real time. The image data is stored in a packet-based format which may be read out via the Data Interface as a continuous stream. During an imaging session, pixel data from each sensor line is formatted into individual packets. Additional packets are injected into the stream while imaging, so that relevant ancillary data from the user and Imager itself may be included. User ancillary packets are generated using data received from the satellite bus, which typically includes attitude data, ephemeris data and timing information. Imager ancillary packets allow the exact Imager settings applied during the session to be stored with the image data. During image data read out (via the Data Interface) the entire data stream can be read out, or it can be filtered to pass only a sub-set of the packets, and/or only a portion of the image.

The Imager keeps a local 64-bit microsecond timer (unsigned integer) that starts counting from zero when the Imager is turned on. This timer value is referred to as the Imager time and is used as a time stamp when required for various packets. In order to synchronise the Imager time with the platform time, the satellite bus should send the platform time to the Imager at the start of an imaging session. This platform time value will be stored as a Time Synchronization ancillary data packet, which also includes the Imager timer value, so that the relationship between the two is known. Some satellites include a Pulse Per Second (PPS) signal which may also be used by the Imager to generate additional Time Synchronisation PPS packets containing the Imager timer value at the instant the PPS signal was asserted. The Imager can also be configured to use the PPS signal as a trigger to initiate image capture.

3. Detailed Description

3.1 Optical Front-End

The xScape100 VNIR OFE is used as Optical Front-End for the HyperScape100. Following the unique demands of space-based imaging payloads, the xScape100 VNIR OFE was designed to accommodate a wide spectral range, be robust and maintain performance across a wide temperature range. The optical design of the imaging payload incorporates a modified Cassegrain optical design with a meniscus entrance lens which defines the entrance pupil of the payload and adds additional environmental protection to the OFE during integration, launch and in operation.

Table 3-1: OFE Characteristics

Description	Value
Focal Length	580 mm ± 1 mm
F-Number	6.1
Front Aperture Diameter	95 mm
Obscuration Diameter	47.2 mm
Distortion	< 0.165%
On-Axis MTF	18% at Nyquist (91 lp/mm)

For further information, see “036218 – xScape100 VNIR Optical Front-End Datasheet”.

3.2 Sensor Unit

The HyperScape100 Sensor Unit houses the Front-End Electronics (FEE) which is based on a CMOS sensor fitted with an optical filter that includes a panchromatic band as well as continuously variable hyperspectral bands. The Sensor Unit specification is provided in Table 3-2. The out-of-band transmittance of the filter is less than 0.01% (OD4).

Table 3-2: Sensor Unit Specification

Hyperspectral λ_c Range	Hyperspectral Bandwidth (FWHM)	Hyperspectral Resolution	Panchromatic Band
442 – 884 nm	3.5% of λ_c	1 nm	500 – 750 nm

The windowing mode of the sensor allows the simultaneous capturing of up to 32 user-selectable spectral bands. The hyperspectral bandwidth is shown in Table 3-2 and depends on the band central wavelength, λ_c. The central wavelength of each band is user-selectable in steps of 1 nm. The optical filter consists of a continuously variable filter causing the FWHM bandwidth to increase by 0.24 nm with each dTDI stage applied to the hyperspectral band. For example, if 4 dTDI stages are applied to a hyperspectral band, that hyperspectral band's FWHM bandwidth is increased by 0.96 nm.

The number of dTDI stages for each band may be individually selected by the user, but is limited by both the maximum allowed per band (Equation 1), as well as the sum total of the dTDI stages selected for all the enabled bands (Equation 2). Equations 1a and 2a must both be satisfied for High Band Count Mode, while Equations 1b and 2b must both be satisfied for High Accuracy Mode.

High Band Count Mode :

$$N_{dTDI}^{k} \leq 8 \qquad \textit{(Equation 1a)}$$

$$\sum_{k=1}^{32} M^{k} \cdot N_{dTDI}^{k} < S \qquad \textit{(Equation 2a)}$$

High Accuracy Mode :

$$N_{dTDI}^{k} \leq 8 \qquad \textit{(Equation 1b)}$$

$$\sum_{k=1}^{32} M^{k} \cdot (N_{dTDI}^{k} + 24) < S \qquad \textit{(Equation 2b)}$$

where

k is the spectral band number, ranging from 1 to 32,
M^{k} is 1 when spectral band k is enabled or 0 if it is disabled,
N_{dTDI}^{k} is the number of dTDI stages selected for spectral band k,
S is the hardware limit, taken from Figure 3-1 for a given orbital height

Equation 1 states the maximum dTDI stages per band is limited to 8. Equation 2 ensures the sum of all the dTDI stages (across all the enabled bands) is within the hardware limit, S, set by the line scan rate as shown in Figure 3-1. The line scan rate vs orbit altitude for various FMC rates are provided in Figure 3-2.

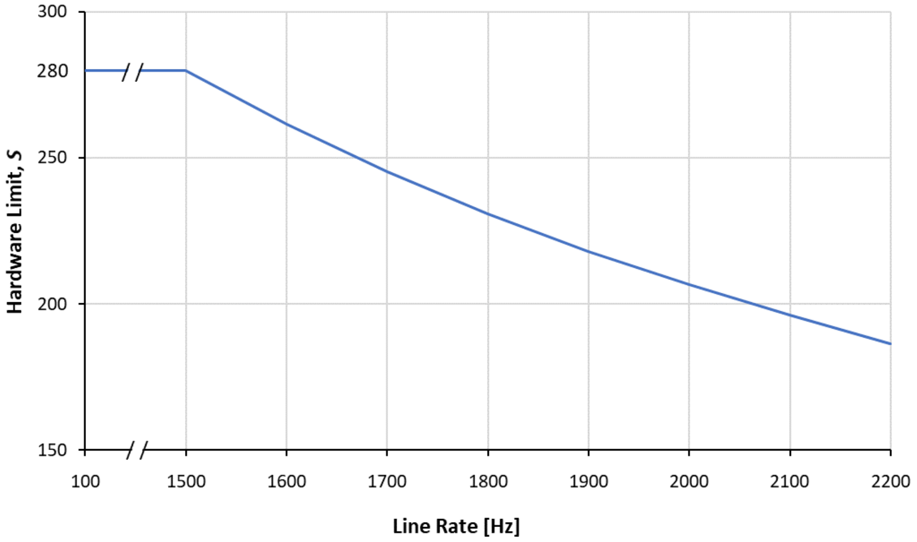

Figure 3-1: Hardware Limit vs Line Rate

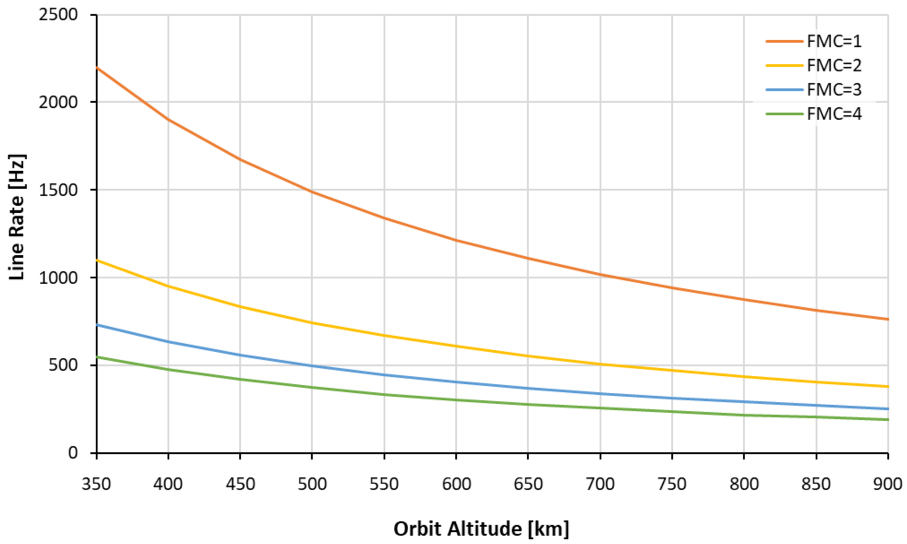

Figure 3-2: Line Rate vs Orbit Altitude

The signal-to-noise ratio with a selection of TDI stages, at an orbit height of 500 km is shown below. A radiance function of 100 $W \cdot m^{-2} \cdot sr^{-1} \cdot \mu m^{-1}$ is assumed across the spectral range.

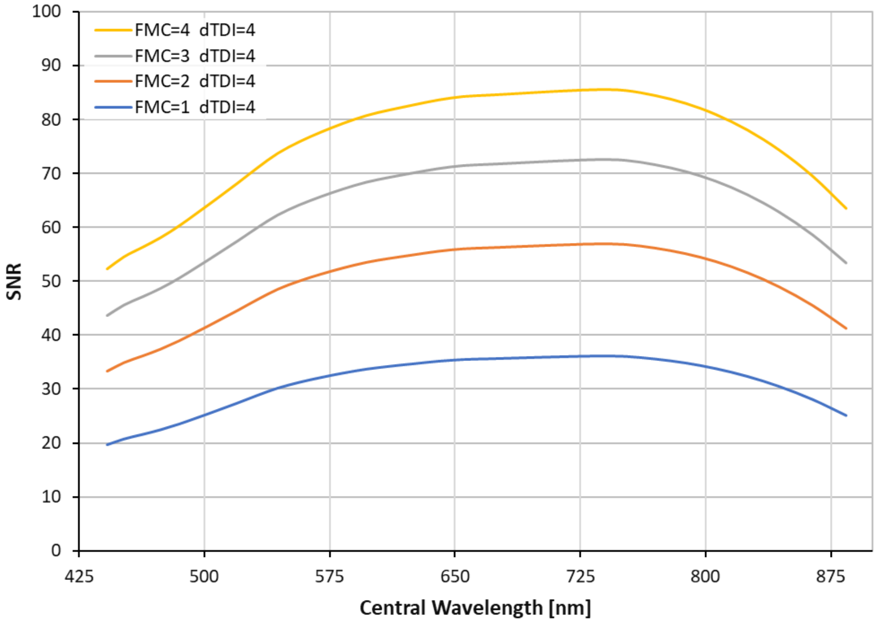

Figure 3-3: SNR for Hyperspectral Bands vs Central Wavelength

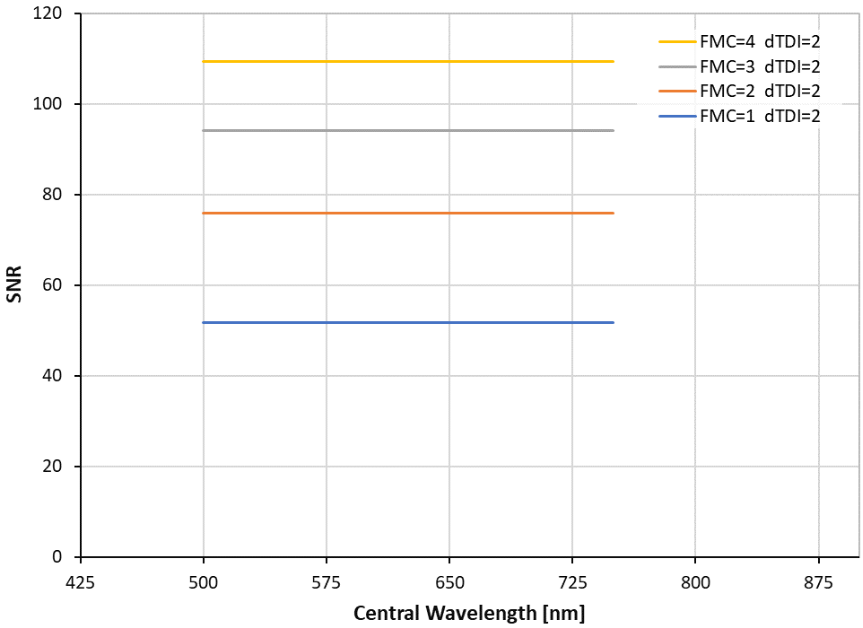

Figure 3-4: SNR for Panchromatic Band

3.3 Control Electronics

The Control Electronics (CE) is a single PCB with a standard PC-104 form factor. It interfaces to the Front-End Electronics (FEE) of the HyperScape100 Sensor Unit as well as the external satellite bus. The functionality of the CE is largely based on a high-performance FPGA, which allows image data to be captured at high data rates, processed on-board, and delivered via a high-speed interface. The CE is highly configurable, with several standard selections and options available, which allows for flexible integration into existing systems.

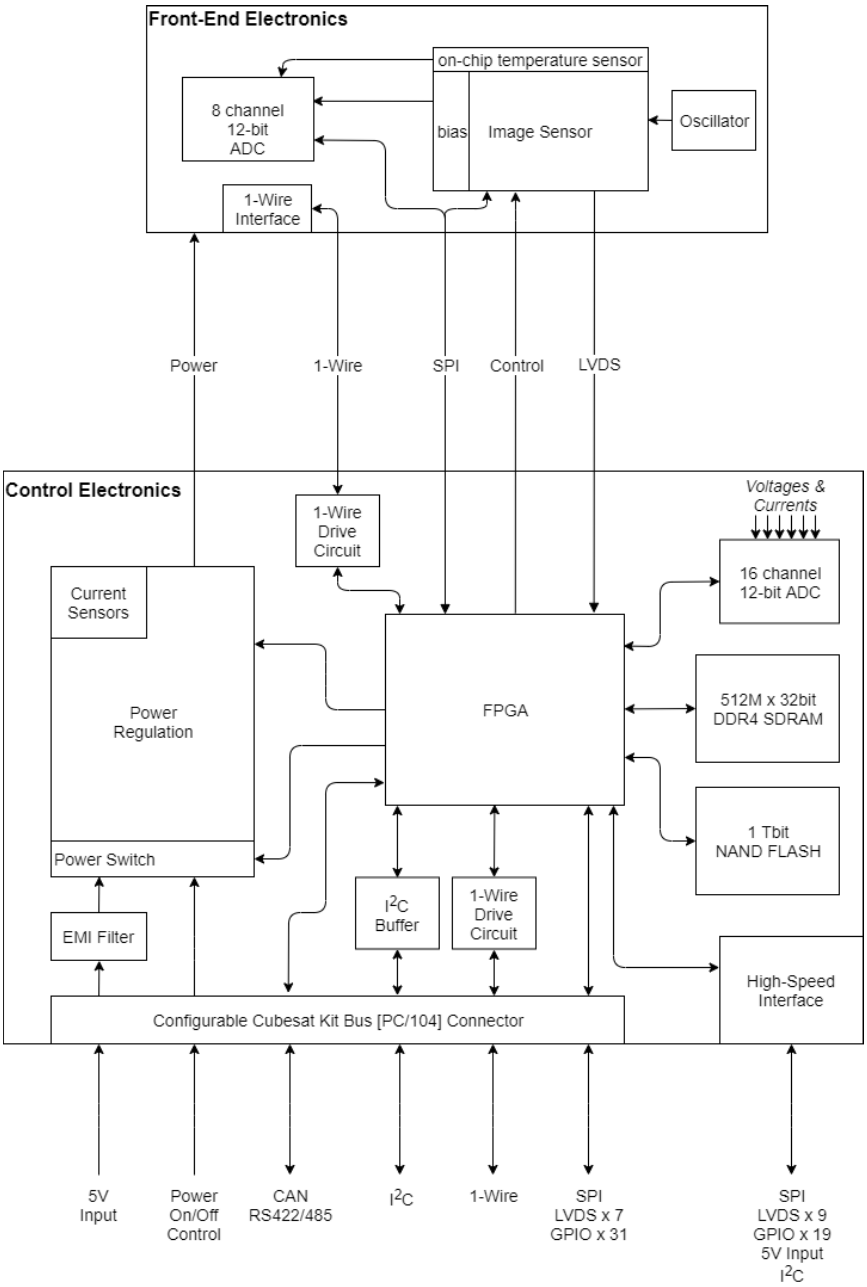

Figure 3-5: Control Electronics Block Diagram

3.3.1 Power Supply

The Imager requires a direct current (DC) power supply regulated at 5 V ± 5% with a current rating of at least 1.5 A. Typically, the satellite bus supplies a switched power supply to the CE. In cases where the power supplied to the CE is not switched, user control of an on-board power switch is available. The CE monitors the current consumption of various sub-circuits and can initiate a full power-down or power-cycle if an over-current event occurs. This serves to protect against radiation-induced single-event latch-up (SEL). The different power switching possibilities are shown in Table 3-3

Table 3-3: Power Switching Alternatives

Power Mode	Description	Over-current
Bus Switched	External 5 V supply is switched.	Power-cycle
User-Controlled Switch (Direct)	External 5 V supply stays ON. Switch ON – Power Control line is driven high Switch OFF – Power Control line is driven low	Power-cycle
User-Controlled Switch (Latched)	External 5 V supply stays ON. Switch ON – Power Control line is driven high Switch OFF – Control command to CE	Power-cycle or Power-down (1)

(1) Drive the Power Control line low for over-current power-down, or high for power-cycle.

3.3.2 Control Interface

The CE implements an I^2C slave which is used as a control interface for commands and telemetry. It supports standard-mode (100 kHz) and fast-mode (400 kHz), as well as 3.3 V (default) or 5 V signal levels. The 7-bit slave address is configurable, as well as the optional pull-up resistors.

The CE also provides a Serial-Peripheral Interface (SPI), which may be accessed via any available GPIO pin (see section 3.3.4). Optionally, the control electronics can make provision for RS-422/RS-485, and/or SpaceWire. The SpaceWire link conforms to the ECSS-E-ST-50-12C standard and can operate at up to 100 Mbps in either direction. A single SpaceWire node is implemented having two services (end-points): a Data Service and a Control Service. Provision is made for up to 7 SpaceWire routing bytes and protocols can be customized.

Table 3-4: Control Interface Options

Interface	Details
I^2C	Standard
SPI	Standard
SpaceWire	Optional
RS-422 or RS-485	Optional
CAN 2.0B	Under Development

3.3.3 Data Interface

The data interface is used for dedicated high-speed transfers, where image data is read out to a payload processor or downlink transmitter. The interface uses an in-house streaming protocol and supports the Simera Sense Standard LVDS link, SpaceWire or USART.

3.3.3.1 Link Options

The standard high-speed link consists of a minimum of 4 LVDS pairs to provide a data output with bit rates from 100 to 800 Mbit/s per data lane, as shown in Table 3-5. By default the link operates at 100 MHz and uses two data lanes for a total of 5 LVDS pairs.

Table 3-5: High-Speed Data Output Interface Characteristics

Characteristic	Value
LVDS Pairs	4 to 7
Clock Frequency	100 to 400 MHz
Data Lanes	1 to 4
Data Lane Rate	SDR or DDR

The source-synchronous clock is centre or bit aligned to the double data rate data lanes. In single data rate the clock is rising or falling edge aligned. The data lanes are synchronised to the free-running clock using a dedicated synchronisation signal. Data is transferred in bytes of 8 bits, most significant bit (MSB) first. Optional flow control is also available in cases where the receiver needs to throttle the incoming data stream. Table 3-6 describes the role of the LVDS pairs in more detail. The pin assignment of the interface is shown in section 4.2.

Table 3-6: Standard LVDS Link Description

LVDS Pair	Description	Direction
HS_Clk	Clock to which HS_D[n] and HS_Ctrl is synchronised	Output
HS_D[0-3]	The Data Lanes	Output
HS_Ctrl	Synchronisation and other out-of-band status	Output
HS_RR	Optional Flow Control signal returned from the data sink	Input

The most basic one byte transfer cycle using a single data lane at SDR is shown in Figure 3-6.

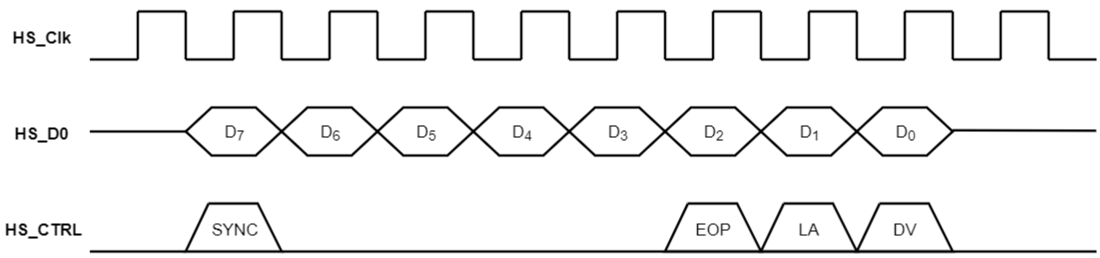

Figure 3-6: Standard LVDS Link Byte Transfer Cycle Waveform

The USART Link consists of four LVDS pairs: a clock, data, clear-to-send, and end-of-frame; as shown in Table 3-7. The clock is free running and falling-edge aligned to the data. Data is transmitted in 10-bit transfers (8-N-1) similar to a UART, but synchronised to the clock.

Table 3-7: USART Signal Description

LVDS Pair	Description	Direction
US_Clk	Clock to which US_TxData and US_EOF is synchronised	Output
US_TxData	The Data Line. Driven high (‘1’) when idle.	Output
US_nCTS	Active Low “clear to send” signal driven by the data sink	Input
US_EOF	“End of frame” signal pulsed high at the end of transmission	Output

The SpaceWire link conforms to the ESCC-E-ST-50-12C standard and can operate at up to 100 Mbps in either direction. A single SpaceWire node is implemented having two services (end-points): a Data Service and a Control Service. Provision is made for up to 7 SpaceWire routing bytes plus an additional byte for the logical address of the destination node.

3.3.3.2 Data Format

Image data is packet based which is read out as a continuous stream. Pixel data is formatted into packets and time stamped. Additional packets, like platform time, imager and user ancillary data, are injected to make the exact imager settings and satellite attitude available for processing. Each packet includes a header, payload and a footer as shown in Figure 3-7. The header is used to identify the packet and extract the variable length payload. The footer is in the form of a CRC-32 applied to the full packet.

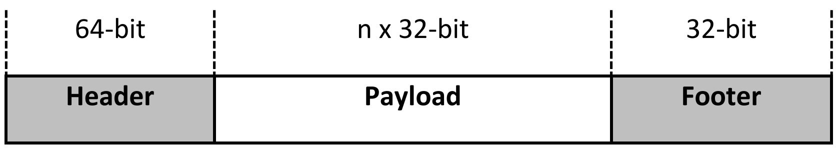

Figure 3-7: Imager Data Packet Description

3.3.4 General Purpose and High-Speed Digital I/Os

The CE includes a total of 50 I/O lines at a 3.3 V signal level, which may be used as part of the standard configuration or customer-specific interfaces (optional). These are essentially pins that are directly connected to the FPGA. All of these I/Os may be configured as single-ended general-purpose I/Os (GPIOs), while select I/Os maybe be configured as LVDS (differential) pairs for use as High-Speed I/Os (HSIOs). A total of 16 LVDS pairs are available to allow for customer-specific interfaces to be implemented. The available I/Os are summarised in Table 3-8. They are all located on the CubeSat Kit Bus (CSKB) and High-Speed connectors, with pin assignments described in Sections 4.1 and 4.2.

Table 3-8: GPIOs and HSIOs

Description	Number
Total I/Os	50
GPIOs	Up to 50 (1)
HSIOs (LVDS pairs)	16

(1) The number of GPIOs available is reduced by 2 for each HSIO pair used.

When the SPI interface is selected, 4 GPIO lines must be reserved for this interface. GPIOs can be used as input for PPS (optional). GPIOs can also be used as outputs to indicate a specific status or event (optional), or as input to trigger imaging or to provide pulse per second input.

3.3.5 Telemetry and Health Monitoring

The CE provides comprehensive telemetry and health monitoring, with 32 unique measurement channels available, as shown in Table 3-9. This allows for thorough analysis and fault-detection of the electronics while in-flight.

Table 3-9: Telemetry Measurement Channels

Sub-Circuit	Channel Description	Number of Channels
FEE	Supply Voltages	2
	Bias Voltages	8
	Sensor Temperature	1
CE Power Regulation	Supply Voltages	10
	Supply Currents	8
CE FPGA	Chip Temperature	1
	Supply Voltages	3
TOTAL		**33**

3.4 Parts and Materials Selection

Parts and materials are carefully selected to survive the harsh space environment. The entrance lens (the first optical element of the OFE) is made from fused silica, which is naturally radiation resistant. Samples of other optical materials have been tested for TID radiation effects. COTS EEE parts are selected for radiation tolerance using available radiation test data. In some cases, where little to no radiation test data is available, radiation effects as seen on similar devices and technologies are mitigated through a best practice approach. Memories used for medium to long term storage are EDAC protected, the FPGA configuration is SEU immune, and all subcircuits are protected for SEL through eight current sensors which are continuously monitored. COTS EEE components are always derated, taking the effects of radiation (both TID and displacement damage) and temperature into account. COTS EEE parts having commercial temperature grade is not used.

4. Electrical Interfaces

The HyperScape100 Control Electronics features two connectors for external interfacing – a standard CubeSat Kit Bus (CSKB) PC-104 connector pair (H1 and H2) and a custom high-density connector (P5) for high-speed data transfers. The pin assignment of the PC-104 connectors are not completely fixed, and many configuration selections are available to ease integration with existing systems. It is typically used for power supply and a control interface. High-speed data transfers (of image data) are recommended via connector P5. Connectors P2, P3 and P4 provide an internal interface to the FEE.

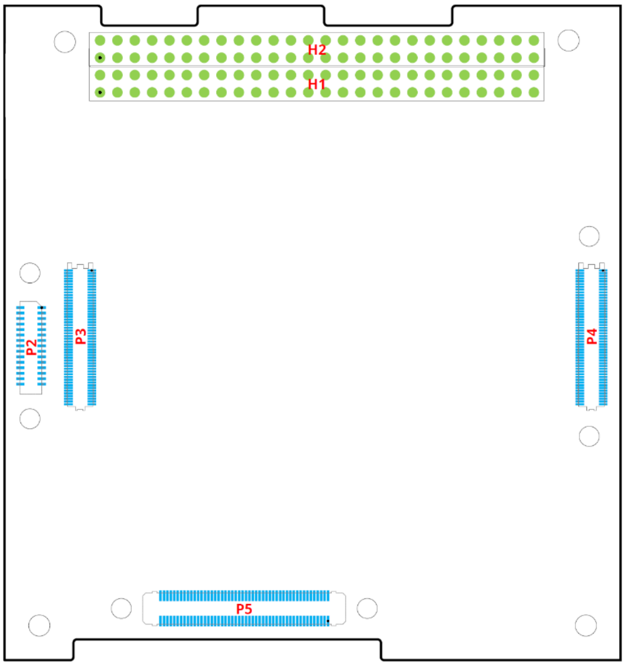

Figure 4-1: CE Connector Locations

4.1 CSKB PC-104 Connector H1 and H2

The standard CubeSat Kit Bus Connectors (H1 and H2) have a pin assignment as shown in Table 4-1 and Table 4-2. It should be noted that due to the diverse configuration selections, several pins appear in the table more than once, according to their configured role.

Table 4-1: Connector H1 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
47, 49, 51	5V_IN	Power	5 V Input Power supply (1)
4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16	PowerCtrl	3.3 V Input (3)	Power switch user control. High for on, low for off. (4)
1	CANL	CAN	Low level CAN bus line (6)
3	CANH	CAN	High level CAN bus line (6)
23, 41	SDA	3.3 V I/O (5)	I^2C serial data

Pin Number(s)	Pin Name	Signal Type	Description
21, 43	SCL	3.3 V Input (5)	I^2C serial clock
1, 2, 3, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 30, 31, 33, 40	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 29, 32, 35, 39	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 5 pairs)
12, 25, 26, 27, 28, 34, 36, 37, 38, 42, 44, 45, 46, 48, 50, 52	NC	N/A	Not connected.

Table 4-2: Connector H2 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
13, 15, 16, 25, 26	5V_IN	Power	5 V Input Power supply (1)
29, 30, 32	5V_RETURN	Power	5 V Power return (2)
17, 18, 19, 20	PowerCtrl	3.3 V Input (3)	Power switch user control. High for on, low for off (4)
47	RS422_RX_A	RS-422	RS-422 Receiver A line (6)
49	RS422_RX_B	RS-422	RS-422 Receiver B line (6)
48	RS422_TX_A	RS-422	RS-422 Transmitter A line (6)
50	RS422_TX_B	RS-422	RS-422 Transmitter B line (6)
47, 48	RS485_A	RS-485	RS-485 A line (5)
49, 50	RS485_B	RS-485	RS-485 B line (5)
21, 22, 47, 48, 49, 50	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
17, 18, 19, 20, 47, 50	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 2 pairs)
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 23, 24, 27, 28, 31, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 51, 52	NC	N/A	Not connected.

(1) At least two 5V_IN supply pins must be used
(2) At least two 5V_RETURN supply pins must be used
(3) PowerCtrl input is 5 V tolerant.
(4) Only one of these pins may be selected (as per the product configuration).
(5) I^2C interface may be configured for 5 V signal levels (as per the product configuration).
(6) Only available as an option

4.2 High-Speed Connector P5

The primary purpose of the high-density connector P5 is to provide an interface suitable for high-speed data transfers. A total of 9 LVDS pairs are available. These LVDS pairs may also be used to implement a customer-specific interface if required, as a custom option. The High-Speed Connector also provides an alternate power and control interface that includes I^2C. Harwin G125, Omnetics BiLobe as wel as Harwin Datamate wirable connector breakout options are available.

Table 4-3: Connector P5 Pin Assignment

Pin Number(s)	Pin Name	Signal Type	Description
1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 49, 50, 55, 56, 61, 62, 67, 68, 73, 74, 79, 80, 85	GND	Power	Digital Ground
95, 96, 97, 98, 99, 100	5V_IN	Power	5 V Input Power supply (1)
86, 89, 90, 91, 93, 94	5V_RETURN	Power	5 V Power return (2)
87	PowerCtrl	3.3 V Input (3)	Power switch user control. High for on, low for off.
59	CE_On	3.3 V Output	Power Status. High when CE is on, low when off.
88	SDA	3.3 V I/O (4)	I^2C serial data
92	SCL	3.3 V Input (4)	I^2C serial clock
57	GPIOx	3.3 V I/O	General Purpose Input/Output. Use for SPI or customer specific options
58, 60, 63, 64, 65, 66, 69, 70, 71, 72, 75, 76, 77, 78, 81, 82, 83, 84	HSIOx	3.3 V I/O or LVDS	High-speed capable Input/Output. Each pin be used as a general-purpose single-ended I/O, or two pins together as a high-speed differential pair (maximum of 9 pairs)
3, 4, 5, 6, 9, 10, 11, 12, 15, 16, 17, 21, 22, 23, 24, 27, 28, 29, 30, 33, 34, 35, 36, 39, 40, 41, 42, 45, 46, 47, 48, 51, 52, 53, 54	Reserved	N/A	Reserved

(1) At least two 5V_IN supply pins must be used
(2) At least two 5V_RETURN supply pins must be used
(3) PowerCtrl input is 5 V tolerant
(4) I^2C interface may be configured for 5 V signal levels (as per the product configuration sheet)

5. Electrical Specifications

5.1 Absolute Maximum Ratings

The absolute maximum ratings of the electrical interfaces are shown in Table 5-1. Use of the HyperScape100 beyond the absolute maximum ratings may cause permanent damage.

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
Power Supply				
V_{in}	5 V Input Supply	- 0.3	5.5	V
GPIOs (1)				
V_{GPIO}	Voltage on input/output pin	- 0.5	3.8	V
I^2C				
V_{I2C}	Voltage on I^2C pin	- 0.5	7	V
LVDS (2)				
V_{ICM}	Common-mode input voltage	0.6		V
V_{ID}	Differential input voltage	0.1		V
Power Control				
V_{PC}	High-level input voltage	0	5.5	V

(1) GPIOs include the SPI interface
(2) LVDS signals include the HSIOs and High-Speed Data Interface

5.2 Electrical Characteristics

The recommended signal levels for the Control Electronics interfaces are given in Table 5-2

Table 5-2: DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Power Supply					
V_{in}	5 V Input Supply	4.75	5.0	5.25	V
GPIOs (1)					
V_{IH}	High-level input voltage	2.0	-	3.45	V
V_{IL}	Low-level input voltage	- 0.3	-	0.8	V
V_{OH}	High-level output voltage	2.9	-	-	V
V_{OL}	Low-level output voltage	-	-	0.4	V
I_{SINK}, I_{SOURCE}	Current sink or source per pin	-	-	±10	mA
I^2C					
$V_{IH\ (5.0\ V)}$	High-level input voltage @ 5.0 V (3)	2.31	-	5.5	V
$V_{IH\ (3.3\ V)}$	High-level input voltage @ 3.3 V (3)	2.31	-	3.45	V
V_{IL}	Low-level input voltage	-0.5	-	0.99	V
V_{OL}	Low-level output voltage	-	0.1	0.2	V
LVDS (2)					
V_{ICM}	Common-mode input voltage	0.6	1.25	2.35	V
V_{ID}	Differential input voltage	0.1	0.35	0.6	V
V_{OCM}	Common-mode output voltage	1.125	1.2	1.375	V

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{OD}	Differential output voltage	0.25	0.35	0.45	V
Power Control					
V_{IH}	High-level input voltage	2.5	3.3	5.0	V
V_{IL}	Low-level input voltage	0.0	-	0.5	V
I_{IH}	High-level input current	-	0.9	2.0	mA
I_{IL}	Low-Level input current	-	-0.1	-0.3	mA

(1) GPIOs include the SPI interface
(2) LVDS signals include the HSIOs and High-Speed Data Interface
(3) The maximum input voltage depends on the selected I²C voltage (3.3 V or 5.0 V)

The AC characteristics of the interfaces are summarised in Table 5-3.

Table 5-3: AC Characteristics

Symbol	Parameter	Min.	Max.	Units
SPI				
f_{SPI}	SPI frequency	0.5	1	MHz
I²C				
f_{I2C}	I²C frequency	100	400	kHz
RS422/485				
f_{RS4xx}	RS4xx baud rate	9.6	460.8	kbps
Standard LVDS Link				
f_{LVDS}	LVDS frequency	100	400	MHz
USART Link				
f_{USART}	USART baud rate	0.4	25	Mbps
SpaceWire Link				
f_{SpW}	SpaceWire baud rate	10	200	Mbps
Power Control				
t_{ON}	Input turn-on pulse width	100	-	ms
t_{OFF}	Input turn-off pulse width	20	-	ms

5.3 Power Consumption

The typical power consumption of the HyperSpace100, with a power supply of 5.0 V, is given below, for the beginning of life (BOL) as well as after exposure to radiation (total ionising dose of 25 krad).

Table 5-4: Power Consumption (BOL)

Operational Mode	Current (Typ.)	Power Consumption (Typ.)
Idle Mode (1)	700 mA	3.5 W
Imaging Mode (2)	1400 mA	7.0 W
Readout Mode (3)	700 mA	3.5 W

Table 5-5: Power Consumption (after 25 krad TID)

Operational Mode	Current (Typ.)	Power Consumption (Typ.)
Idle Mode (1)	745 mA	3.7 W
Imaging Mode (2)	1480 mA	7.4 W
Readout Mode (3)	745 mA	3.7 W

(1) CE is powered on, but the FEE is off. Control and High-Speed Data interfaces are static.
(2) CE and FEE are powered on, and an image is being captured.
(3) CE is powered on, but the FEE is off. Control and High-Speed Data interfaces are active.

6. Environmental Ratings

The HyperScape100 is designed for use in LEO orbit space applications, within the environmental conditions described in Table 6-1.

Table 6-1: Environmental Absolute Maximum Ratings

Description	Value
Operating Temperature	-10 to +50 °C
Survivable Temperature	-25 to +65 °C
Vibration	14.1 g_{rms} (all directions) (1)
Radiation (Total Ionizing Dose)	Performance guaranteed to 15 krad (2)

(1) Based on GSFC-STD-7000
(2) Imager tested to 25 krad, without shielding, using a ^{60}Co source.
Functional beyond 15 krad, but performance may be degraded.

7. Physical Characteristics

The physical characteristics of the HyperScape100 are shown in Table 7-1.

Table 7-1: Physical Characteristics

Description	Value
Mass	1.18 kg ± 5%
Dimensions	98 x 98 x 176 mm

The mechanical drawing in Figure 7-1 belowpresents the envelope dimensions of the HyperScape100 and indicates the position of the centre of mass relative to the OFE's mounting points. All dimensions are in millimetres (mm).

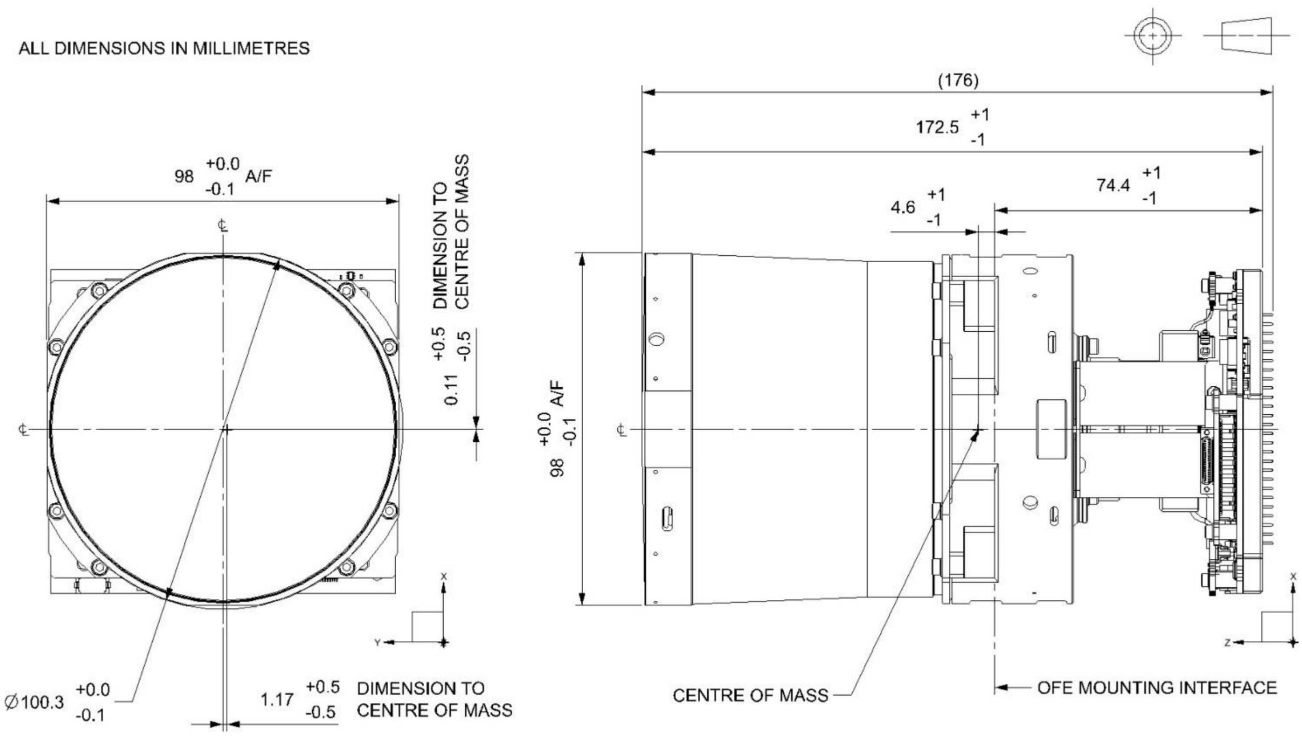

Figure 7-1: Mechanical Drawing

The mounting points on the OFE are shown in Figure 7-2 below. These mounting points, along with the mounting points on the CE (see Figure 7-3), are used to secure the HyperScape100 to the satellite bus structure.

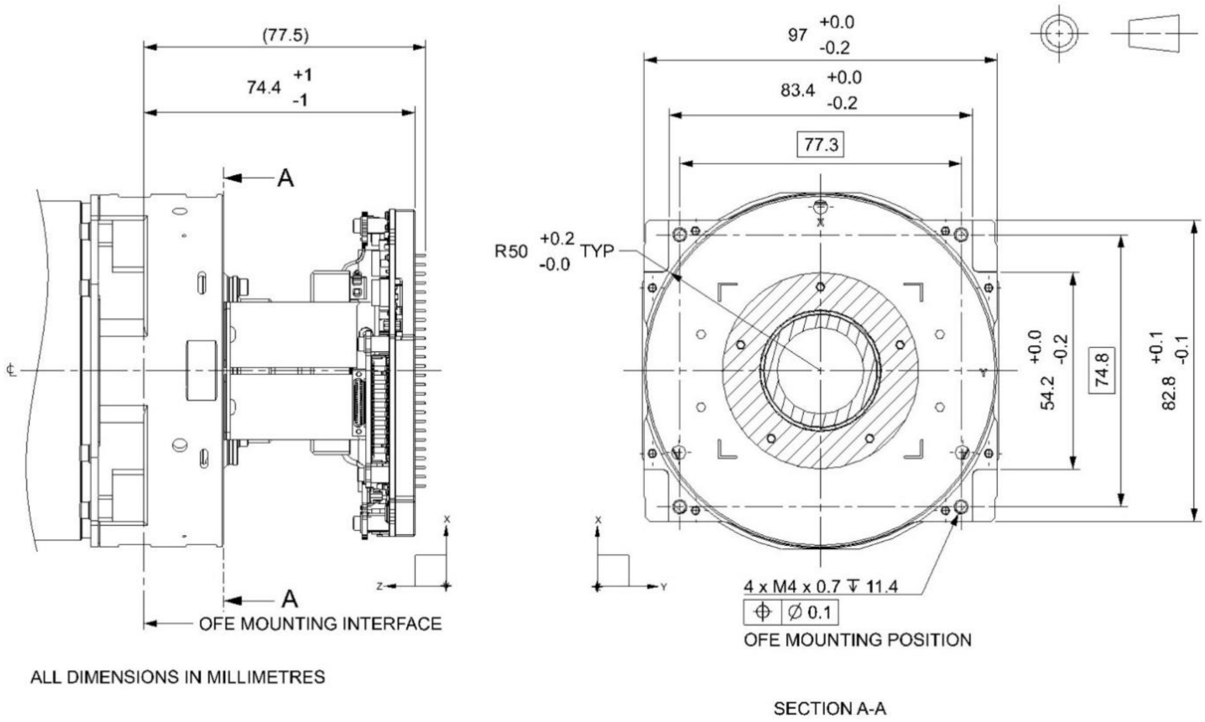

Figure 7-2: OFE Mounting Interface Dimensions

Figure 7-3 shows the standard PC-104 PCB mounting points of the control electronics.

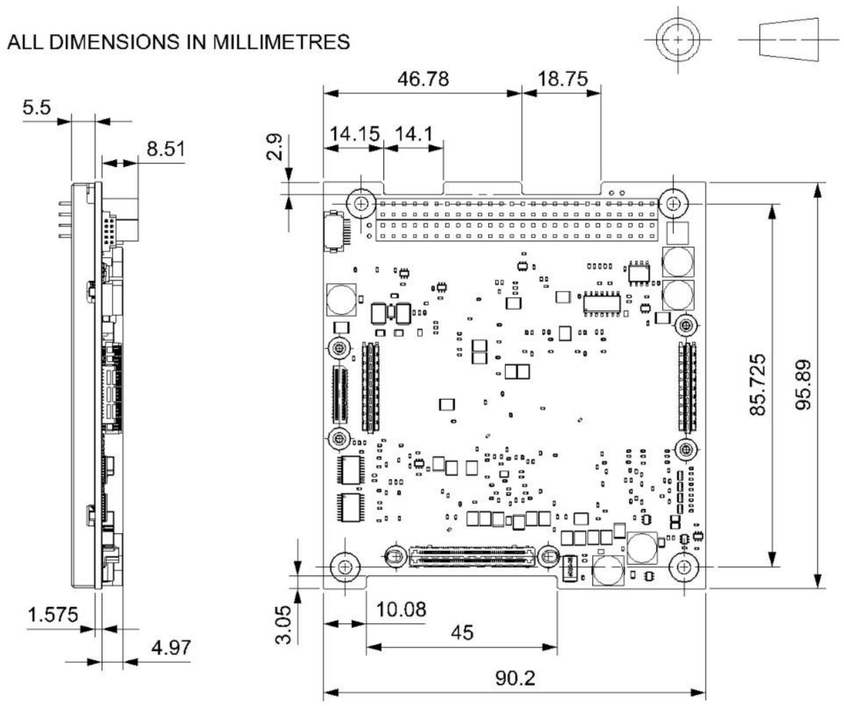

Figure 7-3: CE Mechanical Drawing

There are three breakout adapter options available for the high-speed interface on the CE (see section 4.2 for more details). Figure 7-4 shows the CE with the Harwin G125 Gecko Breakout Adapter option.

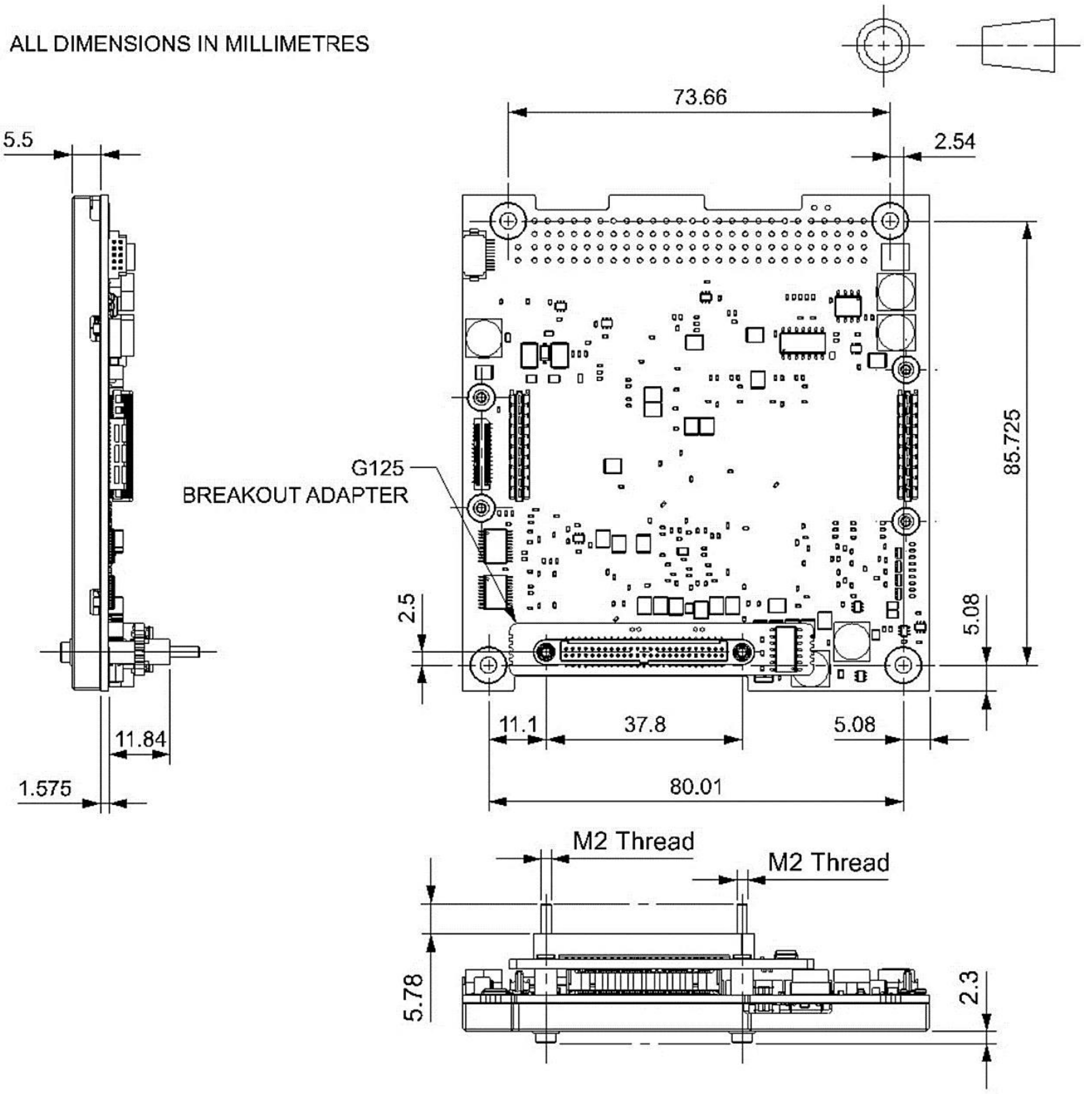

Figure 7-4: CE with Harwin G125 Gecko Breakout Adapter

Figure 7-5 shows the CE with the Bi-Lobe Breakout Adapter option.

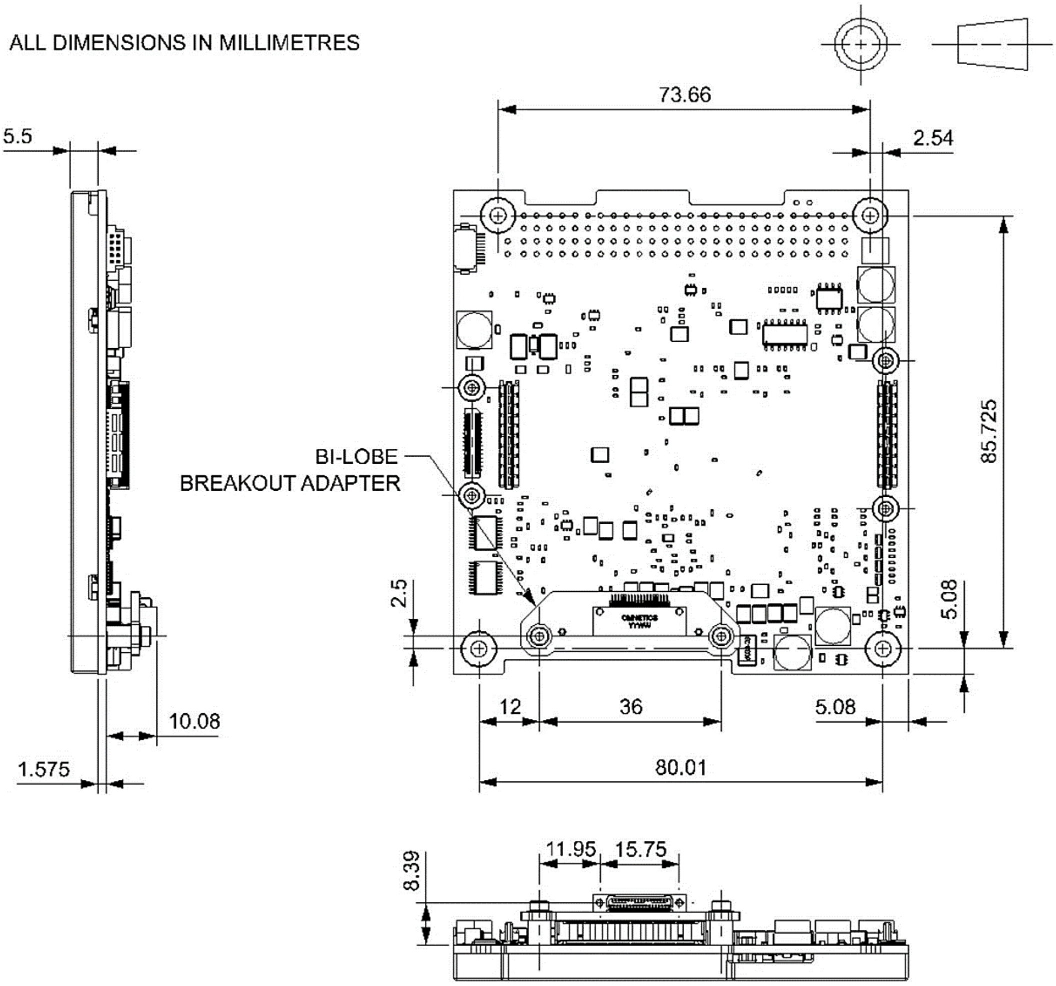

Figure 7-5: CE with Omnetics Bi-Lobe Breakout Adapter

Figure 7-6 shows the CE with the Harwin M80 Datamate Breakout Adapter option.

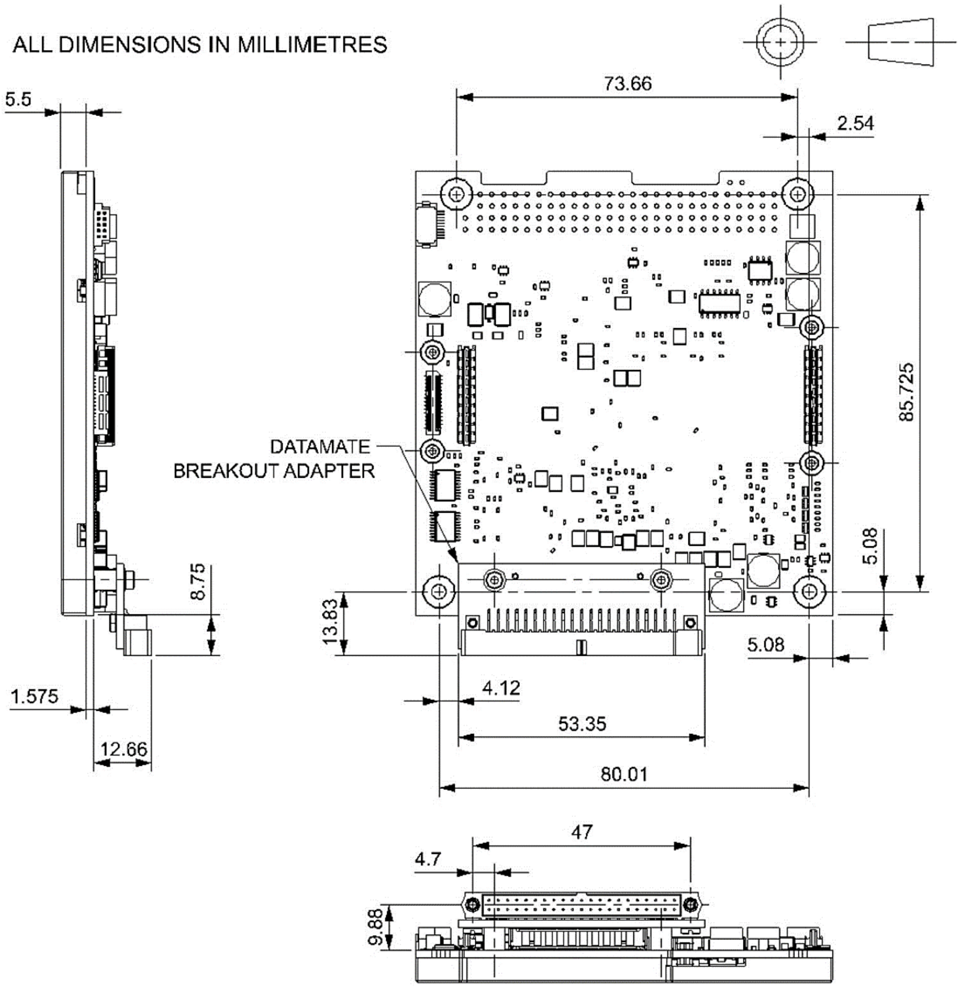

Figure 7-6: CE with Harwin M80 Datamate Breakout Adapter

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