GOPAL KRISHNA COLLEGE OF ENGINEERING AND TECHNOLOGY

GOURAHARI VIHAR, PO: RANIPUT, JEYPORE – 764 005

LESSON PLAN

Name of the Subject: VLSI DESIGN
Name of the Faculty: Suvendu Swain
Semester: 6th Semester **Branch:** ETC
Semester From:January to April **No. of Weeks:** 15 Weeks

Week	Day	Theory/ Practical Topics	Classes
1		**UNIT 1-Introduction to VLSI Design & CMOS Technology**	**6**
	1.	Introduction to VLSI design, abstraction levels, VLSI system hierarchy	1
	2.	regularity, modularity, and locality. Overview of VLSI design styles	1
	3.	quality metrics such as area, delay, power, and reliability	1
	4.	Basic CMOS technology concepts	1
2	5.	n-wel/p-wel processes	1
	6.	layout fundamentals including stick diagrams and design rules	1
		UNIT 2-MOS Transistor Fundamentals & CMOS Inverter	**6**
	7.	MOSFET structure and operation, threshold voltage concepts, MOS I–V characteristics (conceptual)	1
	8.	body effect and channel length modulation (introductory)	1
3	9.	CMOS inverter principles, voltage transfer characteristics (VTC)	1
	10.	noise margins, power dissipation components	1
	11.	Dynamic behavior of the CMOS inverter including rise/fal times	1
	12.	propagation delays, and capacitive loading	1
4		**UNIT 3-CMOS Logic Design**	**6**
	13.	Design of static CMOS logic gates such as NAND, NOR, XOR, and complex logic structures	1
	14.	Transmission gate logic and pass-transistor logic for efficient combinational circuit realization	1
	15.	Implementation of multiplexers, adders, and basic arithmetic circuits.	1
	16.	Sequential logic circuit fundamentals including latches, flip-flops, registers	1
5	17.	timing constraints. Concepts of setup time, hold time	1
	18.	clock skew, jitter, and their impact on synchronous system performance.	1
		UNIT 4-Verilog HDL Programming	**6**
	19.	Introduction to Verilog HDL: modules, ports, data types	1
6	20.	nets, and registers. Behavioral, dataflow, and structural modeling styles	1
	21.	Combinational circuit design using continuous assignment and procedural blocks	1
	22.	s. Sequential logic implementation using always blocks, blocking/non-	1

		blocking assignments	
	23.	event control. Writing Verilog testbenches for simulation	
7	24.	waveform analysis, and verification of functionality	1
		UNIT 5-RTL Design & Synthesis Flow	**6**
	25.	RTL-level digital system design, synthesizable Verilog constructs	1
	26.	FSM design using Verilog (Moore and Mealy models)	1
	27.	Design examples such as counters, shift registers	1
8	28.	ALU components, and control FSMs	1
	29.	Introduction to logic synthesis	1
	30.	, technology mapping, resource utilization, and timing reports.	1
	31.		1

Books Recommended:

1. Jan M. Rabaey, Digital Integrated Circuits: A Design Perspective, Pearson.
2. Neil H. E. Weste & David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson.
3. Kang & Leblebici, CMOS Digital Integrated Circuits, McGraw-Hi l.