GOAPAL KRISHNA COLLEGE OF ENGINEERING AND TECHNOLOGY
GOURAHARI VIHAR, PO: RANIPUT, JEYPORE – 764 005

LESSON PLAN

Name of the Subject: CSPC2005 COMPUTER ORGANIZATION AND ARCHITECTURE
Session : 2025-26
Name of the Faculty: Amod Kumar Bagh
Semester: 4th **Branch:** Computer Sc.&Engg.
Semester From: February **No. of Weeks:** 16 Weeks

Week	Day	Theory Topics	Classes
Module-I:			**8**
1	1	Functional blocks of a computer: CPU, memory, input-output subsystems, control Unit,	1
	2	Overview of Computer Architecture and Organization: Fundamentals of computer architecture, Organization of Von Neumann machine,	1
	3		1
	4	Basic operation concepts, Performance andHistorical perspective,	1
2	5	Instruction set architecture of a CPU–registers,	1
	6	instruction execution cycle,	1
	7	RTL interpretation of instructions,	1
	8	addressing modes, instruction set.	1
Module-II:			**8**
3	9	Data representation: signed number representation, fixed and floating pointrepresentations,	1
	10	character representation. Computer arithmetic – integer addition andsubtraction,	1
	11	ripple carry adder, carry look-ahead adder, etc.	2
	12		
4	13	multiplication – shiftand add, Booth multiplier, carry save multiplier, etc.	2
	14		
	15	Division restoring and non-restoring techniques, floating point arithmetic.	2
	16		
Module-III:			**12**
5	17	CPU control unit design: hardwired and micro-programmed design approaches,	2
	18		
	19	Memory system design: semiconductor memory technologies,	1
	20	Memory Organization- Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.	2
6	21		
	22	Peripheral devices and their characteristics: I/O subsystems,	1
	23	I/O device interface, I/O transfers–program controlled,	2
	24		
7	25	Asynchronous data transfer, Modes of Transfer, interrupt driven and DMA,	2
	26		

	27	Privileged and non-privileged instructions, software interrupts and exceptions.	1
	28	Programs andprocesses–role of interrupts in process state transitions, I/O device interfaces – SCII,USB	1
Module-IV: (07 Hrs.)			**7**
9	29	**Reduced Instruction Set Computer:** CISC Characteristics, RISC Characteristics.	1
	30	**Pipeline and Vector Processing:** Pipelining: Basic concepts of pipelining, throughput and speedup,	3
	31		
	32		
10	33	pipeline hazards. Vector Processing, Array Processor. **Multi Processors:** Characteristics of Multiprocessors,	1
	34	Interconnection Structures, Inter-processor arbitration, Inter-processor communication and synchronization	1
	35	Cores, and Hyper-Threading ,Cache Coherence.	1
	32	Revision of Previous Modules	1
Module-V: (08 Hrs.)			
11	33	**Memory organization:** Memory interleaving, concept of hierarchical memoryorganization,	4
	34		
	35		
	36		
12	37	cache memory, cache size vs. block size,	2
	38		
	39	mapping functions,	1
	40	replacement algorithms, write policies.	1