

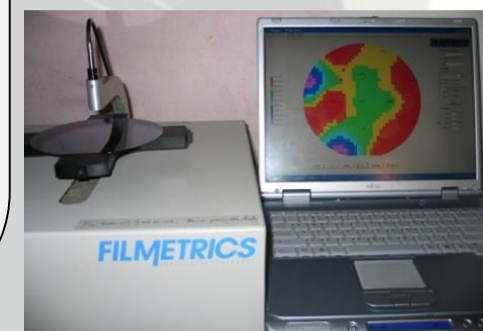
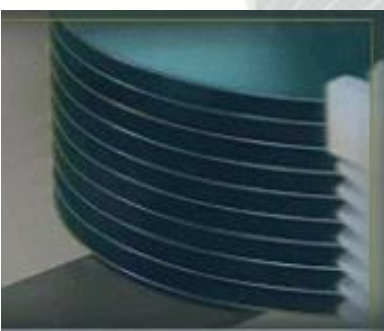


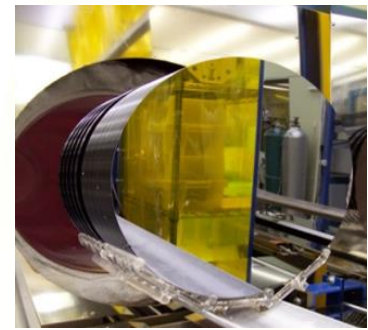
QSS is working with a Dedicated US Supplier that has Developed a Propriety Process Flow for Manufacturing SOI Wafers for the MEMS and Semiconductor Industry. QSS has Achieved Noteworthy Business Growth with many MEMS Design Houses and Companies.

Through our Proprietary Technologies in Wafer Bonding, Thinning and Surface Modification, we can provide the following products and services:

- 1. Thick SOI wafers (**device thickness > 1.0 micron**) with broad resistivity range (0.001~10,000 ohm.cm), thick buried oxide or nitride (up to 20 micron) and up to +/-0.15 micron device uniformity by grinding/polishing and EPI transfer*
- 2. Thin SOI wafers (**device thickness < 1.0 micron**) with device thickness down to 0.15 micron by implant exfoliation (150 Nanometer)*
- 3. Lowest SOI wafer stress on the market*
- 4. De-bondable SOI wafers for forming membrane by direct transferring*
- 5. New engineering substrate (GaAs/Si, glass/glass, etc.) by low temperature fusion bonding*
- 6. Ultra thin double side polished silicon wafer with thickness uniformity less than 1 micron (as thin as 30 micron)*

QSS (617) 899-0917

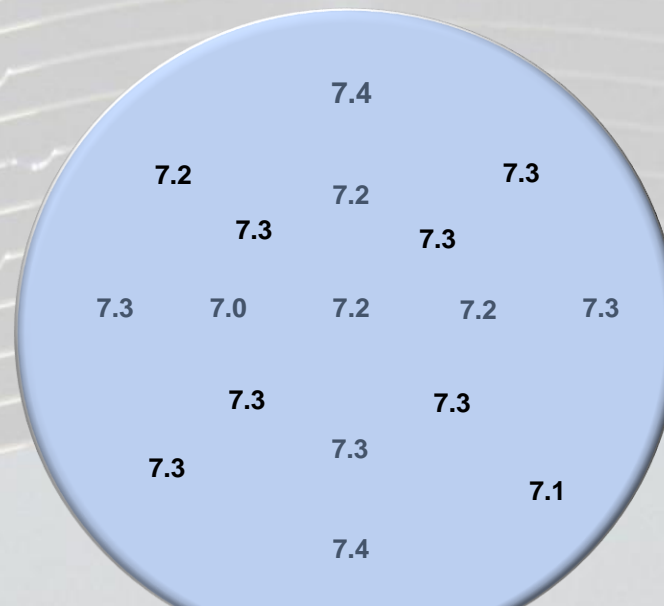




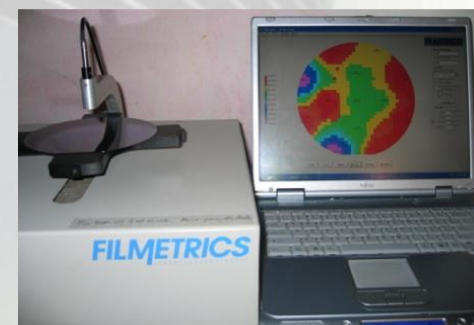
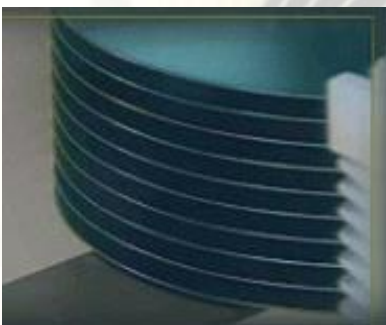
SOI Wafers with Industry Leading Device Thickness Uniformity Using Grind & Polishing processes

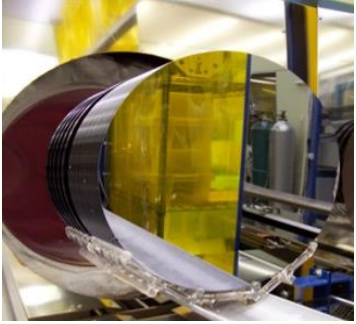


In MEMS applications, device layer is often used as sensing element. The thickness and uniformity are the most critical parameters in determining device performance. After many years of development, we have achieved +/-0.25 micron uniformity through the grinding/polishing process.



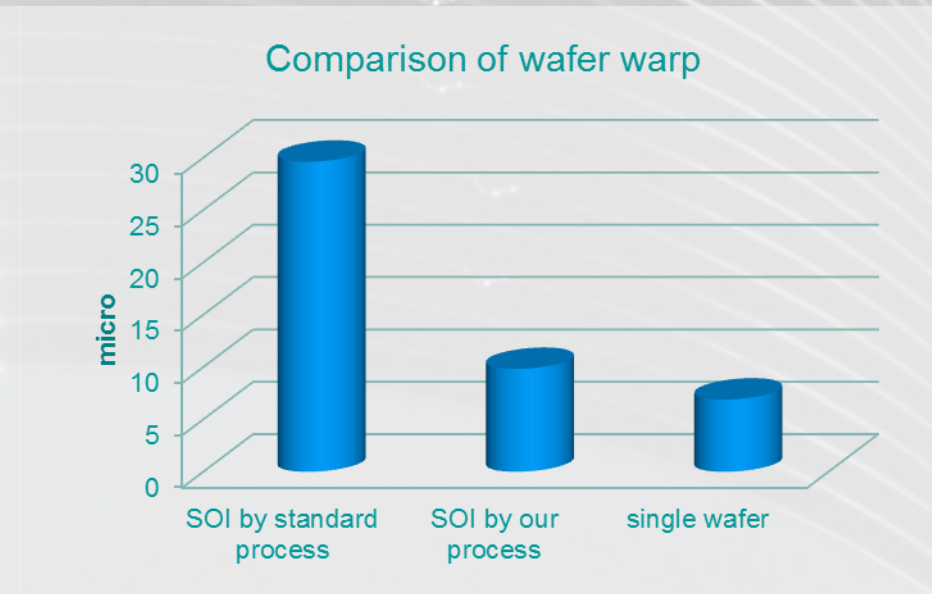
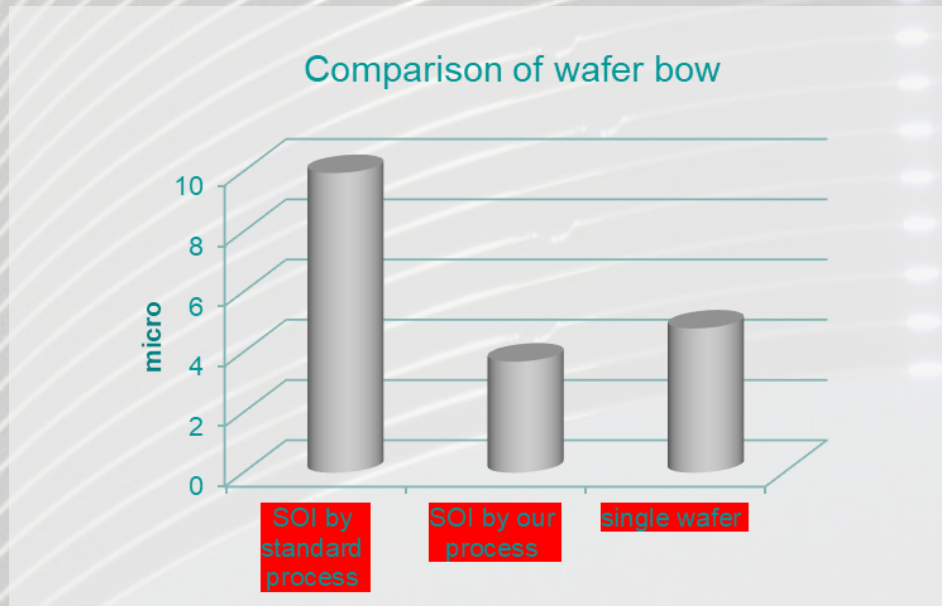
SOI Thickness Distribution
SOI Spec: 150mm , device: 7.2 um, oxide: 1um , handle: 500 um



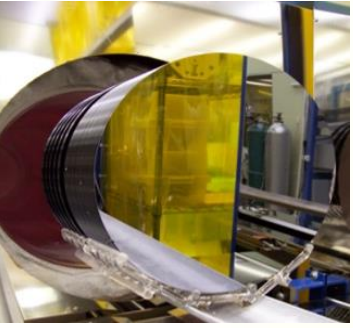


SOI wafers with the lowest stress in the market place

SOI wafers usually have higher stress than single wafers, due to physical deformation during the wafer bonding process. Form many applications it is desirable to have as low stress as possible on SOI wafers. We have developed a proprietary process to make low stress SOI wafers. The stress of our SOI wafers is close to single silicon wafers, as shown in the following graphs.



SOI wafer: Handle 650 micron, Oxide: 2 micron, Device: 25 micron



SOI WAFER PREPARATION BY GRINDING/POLISHING

Device Wafer

Handle Wafers

