SASKO ZAREV

5550 Sample Way **719-238-8765**
Colorado Springs, CO 80919 **sasko.zarev@gmail.com**

SUMMARY

Versatile and resourceful R&D engineer with 20 years of hardware and software design and integration experience for design and test of high-speed analog, digital and mixed-signal integrated circuits. Expert skills in ATE prototype and production test development and "rack-and-stack" test system design and implementation. In-depth knowledge and understanding of high-speed RF/microwave PCB and ceramic package design/fabrication and silicon qualification processes and principles. Extensive experience with wide variety of test and measurement instrumentation.

• RF/Microwave Design and Simulation – Agilent ADS, Mentor HyperLynx , ANSYS HFSS	• PCB and Electronic Circuit Design – Mentor Graphics PowerLogic, PowerPCB, Cadence OrCAD • Analog IC Design – Cadence Virtuoso IC6
• Software Design – C/C++, Microsoft Visual Basic, LabVIEW, Perl	• Thermal and Fluid Mechanics Modeling and Simulation – ESI-CFD Software
• Statistical Analysis Tools – PADB, SAS-JMP, Microsoft Excel	• Material Failure Analysis – Scanning Electron Microscope (SEM)
• T&M Instrumentation – Network Analyzer, TDR Oscilloscope, Parametric Analyzer, High-Performance 12.5 Gbps J-BERT	• Automated Test Equipment (ATE) – Agilent 93000 series SOC test system, Teradyne Tiger Catalyst test system

PROFESSIONAL EXPERIENCE

Aeroflex Colorado Springs, Inc, Colorado Springs, CO **2010 – Present**
Commercial and Aerospace/Defense Hi-Rel RadHard Integrated Circuits Premier Supplier

Applications Engineer, Sr. 2013 – Present
Designed and procured characterization test solution for 90nm high-speed serial full-custom analog IP block, consisting of a quad-lane full-duplex SERDES macro for up to 3.125Gbps serial data rate per full-duplex lane.

- Designed and implemented a die-level laboratory prototype high-speed characterization test solution, consisting of a silicon die high-frequency test socket and a PCB, integrated with a N4903B serial J-BERT and a wide-bandwidth oscilloscope, centrally controlled and automated using the National Instruments LabVIEW development environment. Directly enabled revenue of US$ 1,000,000 for FY2017.
- Presented the test solution as a customer evaluation demo unit, during customer visits, program reviews and renowned industry conferences such as the 2013 and 2015 IEEE NSREC conference and 2014 GOMAC conference.
- Designed and implemented an RF characterization test fixture for accurate measurement and design verification of a high-speed ceramic package solution. Confirmed HFSS design modeling methodology up to 12GHz bandwidth, providing prospective customers with high level of confidence in the custom-designed ASIC packaging solution.
- Produced a design verification solution for an IBIS-AMI high-speed TX buffer model, using the Mentor HyperLynx EDA solution. Achieved TX eye diagram simulation-to-measurement correlation of better than 90%.
- Performed pre- and post-layout IC design verification of full-custom analog Power-On Reset IP block for a radiation-hardened microcontroller application.
- Performed extensive SEU/SET and SEL radiation effects testing at the Texas A&M University Cyclotron Institute of the SERDES IP implemented on custom-designed multi-purpose high-speed PCB substrate and application board.

Mixed Signal Test Engineer, Sr. **2010 – 2012**
Produced and implemented comprehensive prototype and production test applications, for Aeroflex's next generation mixed signal ASIC's for commercial and aerospace/defense applications.

- Implemented package-level prototype and production test applications in C programming language for commercial and aerospace/defense mixed-signal ASIC's with emphasis on high quality and reliability, while enabling over US$ 4.5 million in orders and revenue for FY2010 and FY2011.
- Developed Tiger Catalyst tests system PCB load-boards with emphasis on low analog input noise applications to meet the most stringent design specifications and requirements. Conducted post-test FFT frequency domain analysis to confirm the low input noise performance of the analog input DUT circuit.
- Designed and implemented wafer-level automated test applications for production testing of a high-density channel, low-noise mixed-signal ADC ASIC for a ground-braking innovative DNA sampling technology application, enabling rapid development as well as a short time-to-market cycle for the targeted application.

Hewlett-Packard and Agilent Technologies, Inc, Colorado Springs, CO **1998 – 2009**
Premier Test and Measurement Company

Hardware Design Engineer – Test Development Engineer, **2001 – 2009**
Produced and implemented detailed test plans from investigation phase to production phase, for Agilent's next generation Product Life-Cycle development program.

- Specified and implemented package-level prototype and production 93000 series automated test applications in C/C++ for a highly-complex mixed-signal ASIC's with an aggressive development schedule, enabling US$ 4.5 million in orders and revenue for FY2008.
- Developed automated test PCB load-boards incorporating high-speed design and simulation software (Agilent ADS and Ansoft HFSS), saving on average of US$ 35,000 Non-Recurring Engineering costs (NRE expenses) per design.
- Designed and implemented wafer-level automated test applications for eliminating the failed parts before the start of the packaging process, in order to reduce the production cost and maximize the yield of the packaged ASICs, while saving close to US$ 20,000 per production lot.
- Conducted statistical limits analysis of test results, to maximize yields, quality and eliminate false-pass part delivery to the customers, providing incremental cost savings of approx. US$ 100,000 per quarter by eliminating production reworks in the internal and the external manufacturing chain.
- Engineered a custom "rack-and-stack" test system using the common GPIB instrument platform and Visual Basic test application, enabling a fast development of a high-frequency MEMS RF switch to be used in a wide variety of Agilent's next generation T&M instruments.
- Reduced the MEMS switch development cost by designing and producing high frequency characterization modules for fast customer access and evaluation, as well as providing in-house MEMS multi-physics design and simulation capabilities.
- Conducted extensive MEMS device characterization and measurements for IP2, IP3 (linearity), power carrying, TDR and RF/Microwave performance.

Regional Sales Engineer – Network Systems Monitoring, **1998 – 2000**
Supported a sales force of twelve representatives for US, Canada and Latin America for Hewlett-Packard's NetMetrix TCP/IP network monitoring solution.

- Developed a scaling methodology for customer-specific implementation of the network monitoring solution while maximizing the sales force efficiency and improving the customer experience, significantly contributing to over US$ 200 million in sales for FY2000 and accomplishing a sales quota of 220%.
- Developed and implemented a time-critical Y2K compliance test and evaluation of an OEM network monitoring solution, for a major installed-base customer (Eli Lily), saving the company several million in potential legal liabilities.

- Conducted training courses, tradeshows and seminars of the network monitoring solution, to improve the sales force technical knowledge and understanding of the product and maximize their chances for winning profitable deals.

EDUCATION

MSEE, Analog/Digital IC Design and Micro-fabrication
University of Colorado, Colorado Springs, CO
BSEE, Electronics and Telecommunications
University of Sts. Cyril and Methodius, Republic of Macedonia

PROFESSIONAL DEVELOPMENT COURSES

Project Management Principles – Aeroflex Colorado Springs, Inc.
Project Management Essentials – Agilent Technologies
Critical Conversations – Communications Course – Agilent Technologies
Total Quality Control (TQC) process – Agilent Technologies
Microsoft C++ Foundation Classes Programming – Batky-Howell
Teledyne-LeCroy Dr. Eric Bogatin Si Academy – Essential Principles of Signal Integrity

PATENTS AND PUBLICATIONS

U.S. patent number 6,559,420:
"Micro-switch heater with varying gas sub-channel cross-section"
U.S. patent number 7,119,294:
"Switch with concentric curvilinear heater resistor"

IEEE NSREC 2015 Conference Poster Presentation:
"Radiation Characterization of 3.125Gbps SERDES Macro IP"

GOMAC 2014 Conference Paper Presentation:
"High-Speed Characterization Testing of 3.125Gbps Quad SERDES Macro"

ESI – CFD North America User Conference 2006 publication:
"Use of VOF plus Heat Transfer Simulation Capabilities in ESI-CFD for Accurate Modeling of Thermally Actuated Micro-fluidics based MEMS"

Application Notes:

"UT90nHBD 3.125Gbps SERDES IBIS-AMI Model"
http://ams.aeroflex.com/pagesproduct/appnotes/AppNote-90nm-SERDES-IBIS-AMI.pdf

"UT54LVDS, UT200SpW 3.3V Fault Propagation Tolerance"
http://ams.aeroflex.com/pagesproduct/appnotes/AppNote_UT54LVDS_UT200SpW_Fault_Propagation.pdf

"Power-up Sequencing of UT54LVDS217/218"
http://ams.aeroflex.com/pagesproduct/appnotes/AppNote_LVDS_SERDES_Powerup_Sequence.pdf