SET-01/Hpc

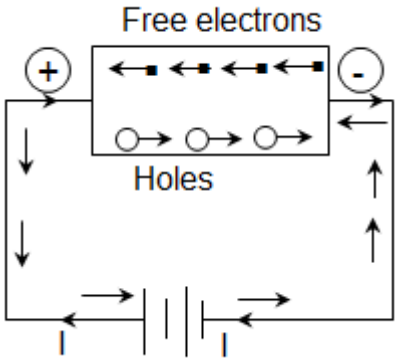
*This **Set-01** contains notes on semiconductor devices ,photoelectric effect & logic gates of class 12th. PAGE-1*

Semiconductor:

The Semiconductor are material whose temperature coefficient of resistance is negative $\alpha = \delta R/R\delta T$ = -ve The resistance decreases with increases in temperature. The semiconductors are materials having almost filled. Valence band and imply conduction band. Separated by small energy gap (forbidden gap)

Intrinsic/ Pure semiconductor:

(a.) Semiconductors in an extremely pure form is known as intrinsic semiconductor.
(b). In pure semiconductors breakdown of bonds due to thermal agitation (increases in temp.) causing formation of positively charged vacancy in V-band and free electron in conduction band.
(c). When external pot diff is applied the randomly drifting electrons gets attracted towards the positive terminals and holes gets shifted towards the negative terminal.



(d). The conducing ability gets limited by the availability of free electrons in band. The availability depends upon break down of bonds which depends upon temperature.

Extrinsic/Impure semiconductor

When an impurity atom is introduced by in the pure semiconductor crystalline structure such that energy level of impurity atom lie inside the forbidden gap of pure semiconductor and divides the gap into two parts. This makes transfer of electrons more easier from valence band to conduction band. Such as semiconductors are called extrinsic semiconductors and the process is called doping. [Generally one impurity atom is introduced out of 10^8 pure semiconductor atoms.]
Depending of impurity atom the impure semiconductors are classified into two types.
(a). N-type
(b). P-type

N-type semiconductors:

(a). When pentavalent impurity atoms are introduced in the crystalline structure of tetravalent impurely material four electrons gets engaged in to bonding and lie in valence band but fifth electron has its energy level above valence band and below conduction bond.
(b). This energy level associated with fifth electron of impurity atom is called donor energy level
(c). The bonds breakdown due to temperature creates electrons- holes pair which free electrons provided by fifth electron impurity atoms exceeds therefore number of electrons exceeds number of holes.
Therefore it is called N-type semiconductor
(d). When free electron is created due to breakdown of bonds a positive hole is created in valence band But when fifth electron of impurity atom gets free a positively charged ion gets formed in forbidden gap.

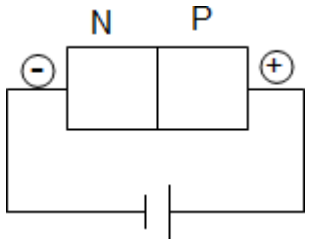
P-type semiconductors:

When a trivalent semiconductor atom is introduced in crystalline structure of pure tetravalent semiconductor material the three electrons get engaged in bonding and lie in valence atom ,a neutral vacancy gets created whose energy level lie forbidden gap. When any free electron occupy this level a stationary negative ion attached with lattice structure .Thus total number of holes exceeds number of electrons ,therefore majority charge careers are holes . That is why such semiconductors are called Positive type semiconductors /P-type .

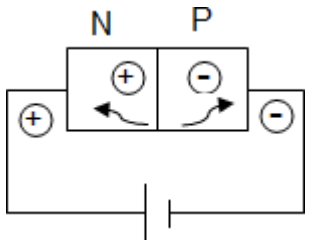
SET-01/Hpc -01

When p-type semiconductors is suitably joined to n-type semiconductor the contact surface is called P-N junction . The free electrons in N-Region diffuses into p-type In N-Region there is stationary positively charged layer near the junction. The electrons of n-region enters into p-region and occupy acceptor energy level and forms a positively charged layer near junction. These two charged layer opposes drift of majority charge careers of each region towards the junction and form junction potential barrier.Due to junction potential barrier PN junction is connected to the circuit in two different ways.

(a). **Forward biasing :** connecting N-region with negative and p-region with positive terminal is called forward biasing. *PAGE-2*

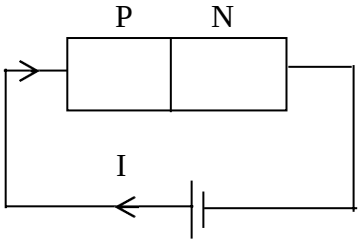


(b). Reverse biasing :

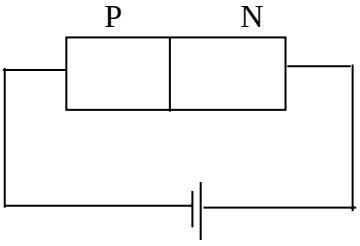


1. Describe P-N junction semiconductor rectifier.

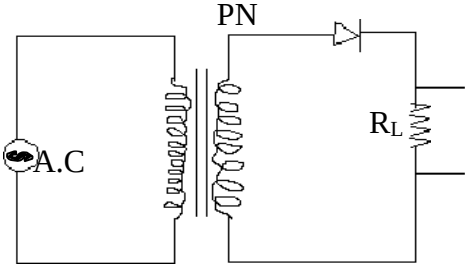
Ans: The P-N junction has unidirectional current flow property. When PN junction is forward biased it conducts current.



But when the PN junction is reverse biased it does not conducts current.



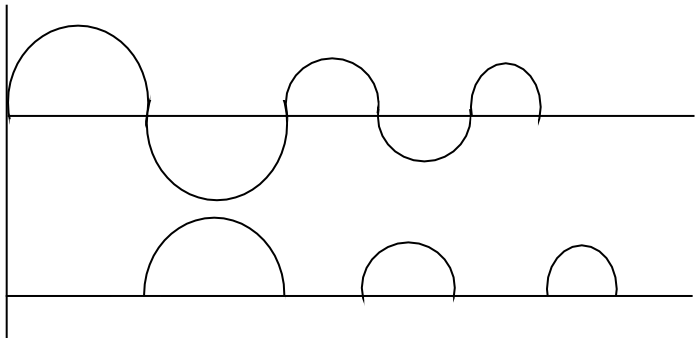
Due to this undirectional current conducting ability the PN junction is used converting A.C. into d.c. and this process is called rectification. The device is called rectifier.

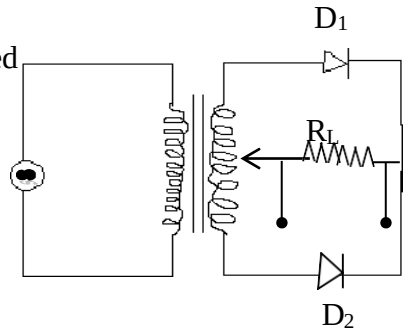


Half Wave rectifier :- In half wave rectifier the a.c. source is connected across a primary coil of transformer, A PN junction diode in series with a resistance is connected with secondary coil of the transformer.

In first (positive) half cycle the PN junction remains reverse biased no current flows through resistance. In next half cycle the PN junction becomes forward biased and current flows resistance. Thus alternate half cycle appears in the output. The output is pulsating unidirectional and d.c.

SET-01/Hpc -01

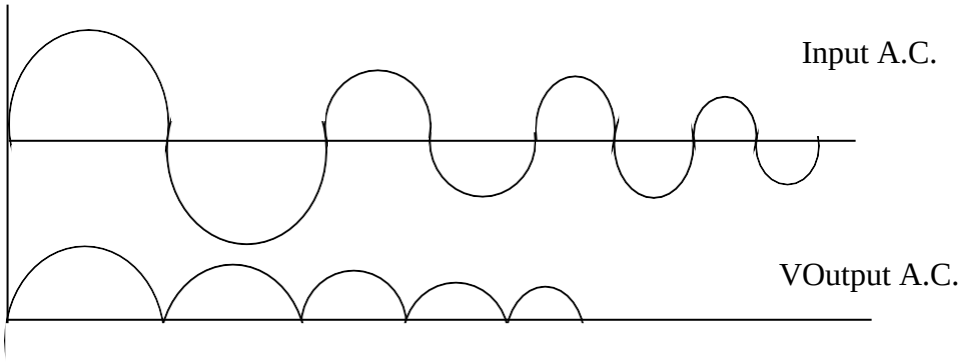




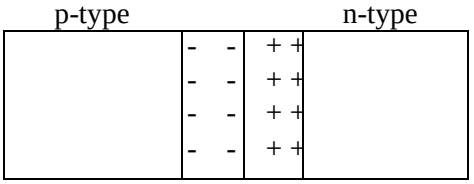
Full Wave rectifier :- In full wave rectifier two PN junction are connected across secondary coil of transformer. The loads resistance is connected in center tap with the secondary coil. In the first half cycle D_1 remains half cycle D_2 becomes forward biased while D_2 remains reverse biased. Thus both half cycle appears across load resistance R_L.

The out put is continuous, variable and unidirectional.

The full wave rectifier is more efficient than half wave rectifier.



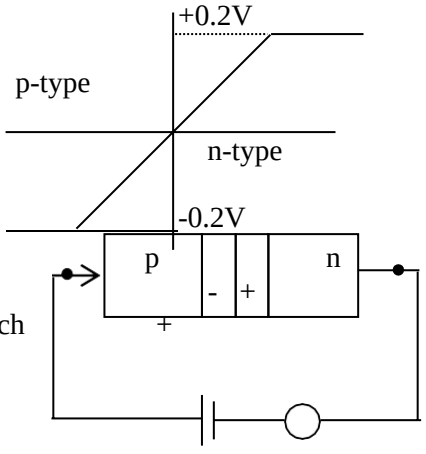
2. **P - N junction.**



When a p-type semiconductor material is suitably joined to n-type semiconductor the contact surface is called P - N junction. The n – type material contains high concentration of free electrons than p – type material therefore electrons diffuses from n – type to p – type material. This causes positively charged layer in n – region and negative charge layer in p – region.

The negatively charged layer in p – type semiconductor repell electrons and prevent electrons and prevent electron n – type from entering. Similarly the positively charged layer in n – region prevents deft of holes of p – region from entering into n – region. Thus PN junction behaves like barrier for majority charge carriers of each region and is called potential difference.

In the region of potential barrier the density of charge carriers is low therefore it is called depletion layer.



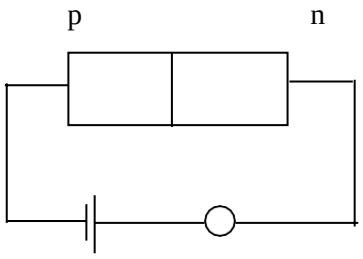
3. Mode of operating a P – N junction in any electric circuit:

(a) Forward biasing: When external voltage is applied across the junction, such that it cancel out the potential barrier permitting flow of majority charge carriers across the junction is called forward biasing.

(i) Potential barrier gets reduced.

(ii) Junction offers low resistance to the current flow (Forward resistance R_f)

(b) Reverse biasing: Connecting p – type with negative terminal and n – type with positive terminals is called reverse biasing. Under reverse biasing the majority



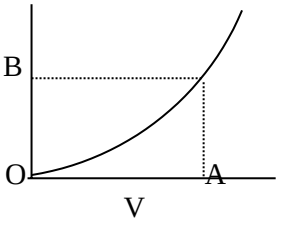
charge carriers of each region gets attracted towards the terminal away from the junction. This increases barriers voltage. Under reverse bias the minority charge carrier of each region cross the junction and forms a weak current called leakage current or reverse or minority current. *PAGE-4*

4. <u>P- N junction as element of electric circuit</u>:

(a) Forward resistance : Under forward bias it conducts current therefore it is assigned a resistance value called forward resistance.

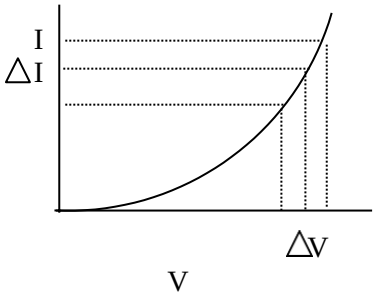
d.c. forward Resistance

$R_f = OA/OB = V_f/I_f$

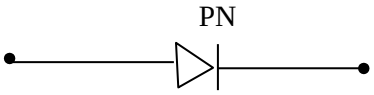


a.c. forward Resistance

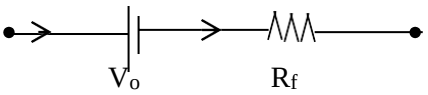
$R_f = \triangle V/\triangle I$ = Change in voltage across diode/Change in current through diode.



PAGE-3



$V_f = V_o + I_f R_f$



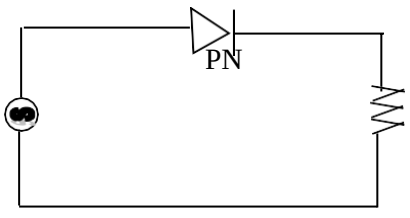
V_o = Potential barrier (PN junction)

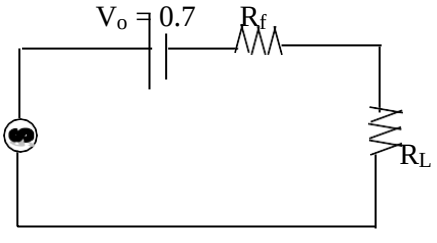
R_f = Forward Resistence.

<u>Problem</u> : An ac voltage of peak value of 20Volt is connected in series with a silicon diode and load Resistance of 500. If forwarding Resistance is 10 and potential barrier is of 0.7 volt. Find

(a) Peak current (b) Peak output voltage.

<u>Solution</u>





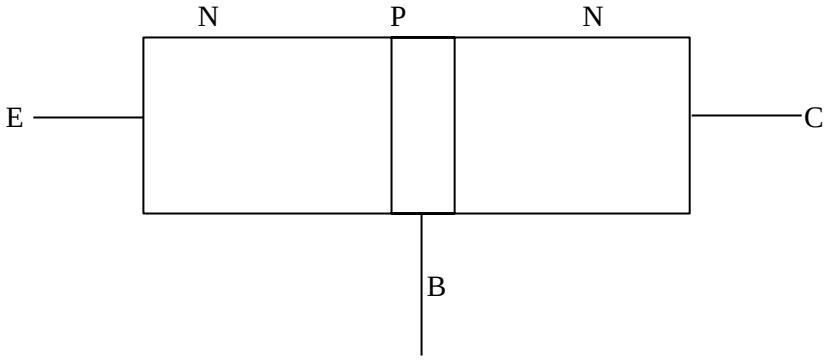
(a) Applying loop Rule for peak value.

$V_{AC} - V_o - I_f R_f - I_f R_L = 0$ $I_f = V_{AC} - V_o/R_f + R_L = 37.8$ mA

Peak load voltage = $I_f R_L = 18.9$ Volt.

Transistor: It consists of two PN – junction back to back and is obtained by either p-type or n-type sandwichting between two pair of opposite type semiconductors.

(a) PNP transistor (b) NPN transistor



The transistor consists of three regions.

(a) Emitter: It is of moderate size and heavily doped semiconductor region. It supplies a large number of majority carriers.

(b) Base: It is thin and lightly doped semiconductor region.

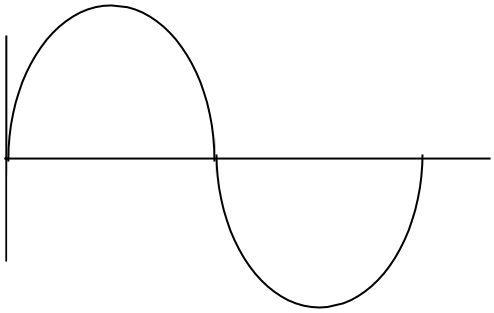
(c) Collector: This region is moderately doped and larger in size.

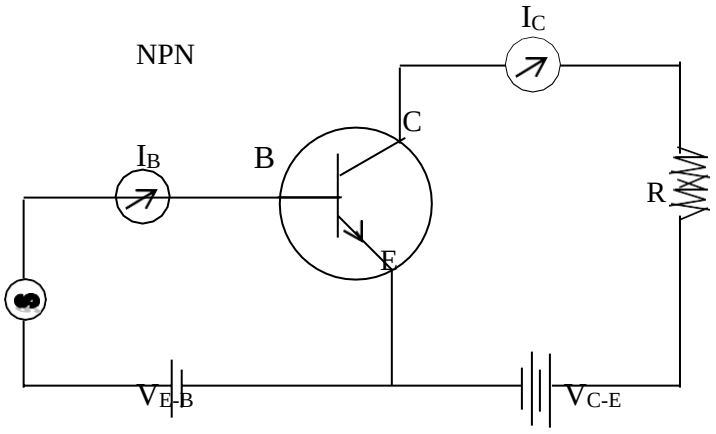
PAGE-5

Basic transistor circuit configuration: - The transistor has three terminals. Emitter (E), Base (B) and Collector (C)

(a) Common Emitter (CE)
(b) Common Base (CB)
(c) Common Collector (CC)

Common Emitter configuration: -

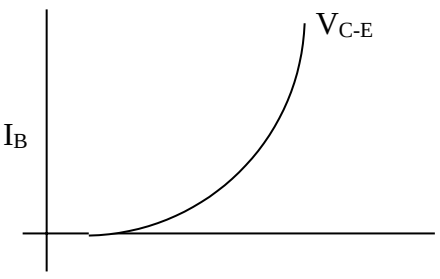




During positive half cycle of the signal forward bias the emitter-base junction is increased. More electrons flow from emitter region to collector region.

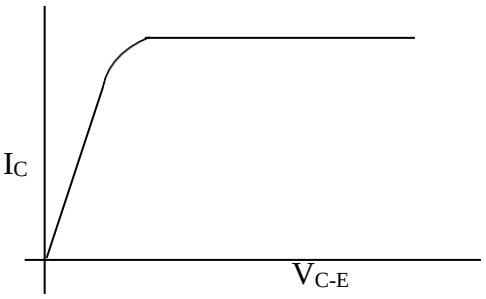
During negative half cycle forward biasing of e-base junction decreases collector current.

Input Characteristic curve (I_B - V_{B-E}): -



SET-01/Hpc -01

Output Characteristic curve ($I_C - V_{C-E}$): - V_{E-B}

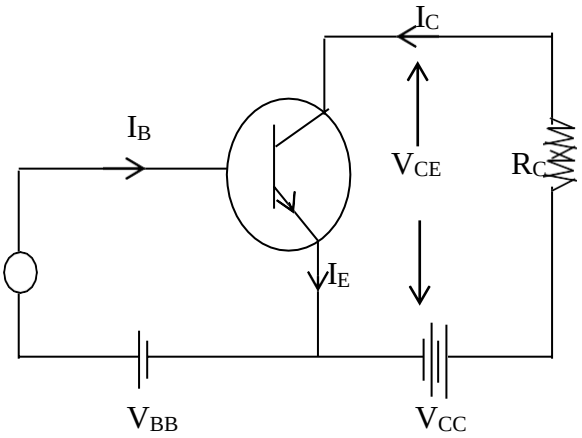


The collector current remains always constant with increase in collector – emitter voltage.

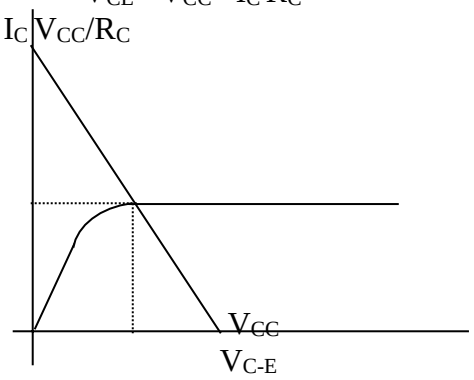
Transistor Parameters: -

(a) Input Resistance	$r_i = (\Delta V_{BE}/\Delta I_B)\ V_{CE}$ = Constant	Kilo ohm
(b) Output Resistance	$r_o = (\Delta V_{CE}/\Delta I_c)$	
(c) Current amplification factor	$\beta = \Delta I_C/\Delta I_B$	
(d) Voltage gain	$A_V = \Delta V_{CE}/\Delta V_{B-E}$	

Transistor load line analysis: -



$V_{CE} = V_{CC} - I_C R_C$



When collector current $I_C = 0$ $V_{C-E} = V_{CC}$

When collector current I_C is max $V_{EE} = 0$ $I_C = V_{CC}/R_C$

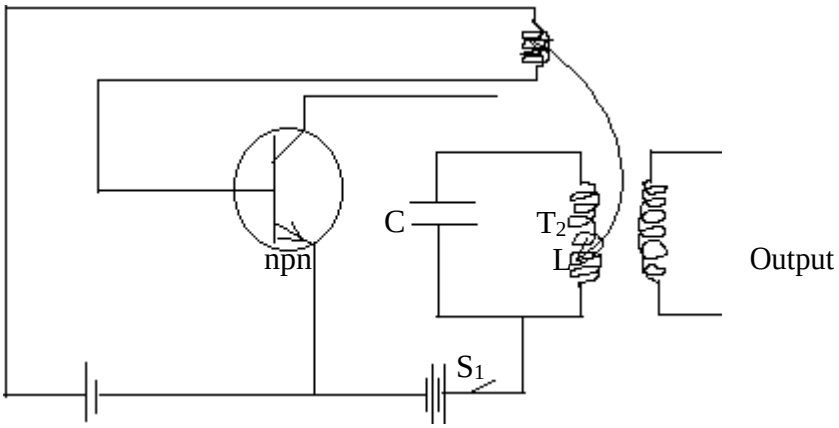
The curve drawn on output characteristics is called load line. The point where load line intersect output characteristic curve is called operating point. The zero value signal of I_C and V_{CE} is called operating point. The collector load R_C is in parallel.

Transistor as an oscillator: -

In an amplified signal output given which appears as an amplified signal output. Thus external input is necessary to sustain. A.C signal in output for an amplifier.

In oscillator sinusoidal output is generated without any external input signal. Thus oscillator is self-sustained.

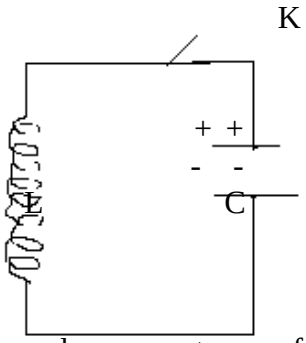
For form an oscillator some of the output power is returned back to input in phase with starting power. This process is called positive feedback.



SET-01/Hpc -01

The switch S_1 is put on to apply proper bias a surge of collector current flows through coil T_2.

Sinusoidal Oscillator :



An electronic device that generates sinusoidal oscillation of desired frequency is known as a sinusoidal oscillator. An oscillator circuit consist of a capacitor (C) and inductance coil (L) in parallel.

Initially the capacitor is fully charged using a source. Then the capacitor has electrostatic potential energy.

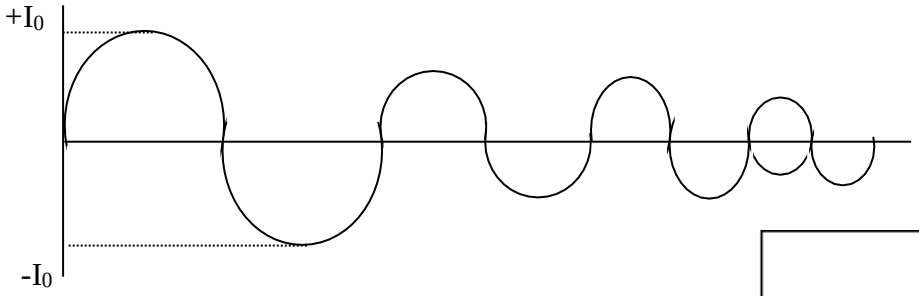
(a) When the switch S is closed the capacitor discharges through inductance. The current in the inductance through inductance establishes magnetic field around the coil.

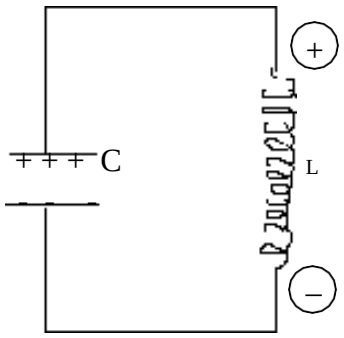
(b) Once the capacitor is discharges magnetic field begin to collapse and produces counter e.m.f. which charges the capacitor with opposite polirity.

The sequence of repeated charge and discharge results in to production of oscillation. In each cycle there is loss of energy due to resistive and radiation loss.

$$fr = 1/2\pi\sqrt{LC}$$

Due to loss the amplitude continue to decrease with amplitude. *PAGE-7*





This loss is compensated by feed back circuit.

$Q_t/C - LdI/dt = 0$ $\qquad$ $d^2Q_t/dt^2 = -1/LC.Q_t$

$dI/dt = 1/LC.Q_t$ $\qquad$ $d^2Q_t/dt^2 \propto Q_t$

as $-dQ/dt = I$

$d^2Q_t/dt^2 = -\omega_f^2\,\omega_f$ $\qquad$ $\omega_f = 2\pi V = 1/\sqrt{LC}$

$$V = 1/2\pi\sqrt{LC}$$

$Q_t = Q_o\cos(\omega t + \phi)$ $\quad$ at $\quad t = 0$ $\quad Q_t = Q_o$ $\quad \phi = 0^o$

$Q_t = Q_o\cos\omega_f t$

$I_t = I_o\sin\omega t = \omega Q_o \sin\omega t$ $\qquad$ $I_o = \omega Q_o$

Photo Electric Effect

1.(*Additional)* ***Obtain expression for magnetic field at point due to a bar magnet at its equatorial position.***

Ans: Ab is a var magnet having length 2l, pole strength m and magnetic moment M. P is a point at equilateral bisector at distance r.

Magnetic field due to north pole at P. $\qquad B_N = \mu_o/4\pi[m/r^2 + l^2]$

Magnetic field due to south pole at P $\qquad B_S = \mu_o/4\pi[m/r^2 + l^2]$

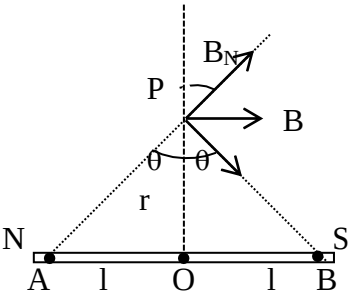
Taking vector sum of B_N and B_S

$$B_P = B_N\sin\theta + B_S\sin\theta$$

$$= 2.\,\mu_o/4\pi(m/r^2 + l^2)(l/\sqrt{r^2 + l^2})$$

$$B_P = \mu_o/4\pi(2lm/r^2 + l^2)^{3/2}$$

$$= \mu_o/4\pi(M/r^2 + l^2)^{3/2}$$

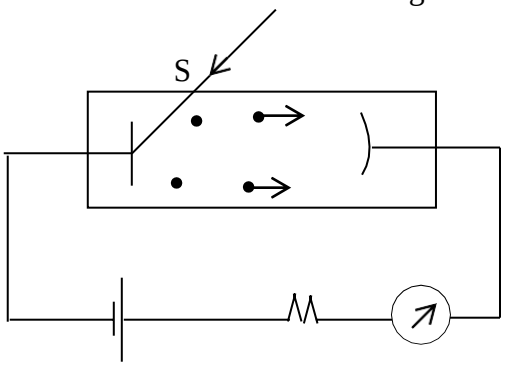


2. What is Photo electric effect? How it was explained by Einstein? Also describe a Photo Cell.

Ans: The phenomenon of emission of electrons from metal surface when it is exposed to light radiation is called Photo-electric effect. According to Einstein's theory of Photo-electric effect the energy of incident photon is partially used in liberating electrons and partially imparting kinetic energy to electrons.

The minimum amount of energy used for liberating an electrons is called Work function. According to Einstein's Theory

$$h\nu = \phi + 1/2mu_o^2$$



When ν = Frequency of incident photons.

ϕ = Work function of the metal surface.

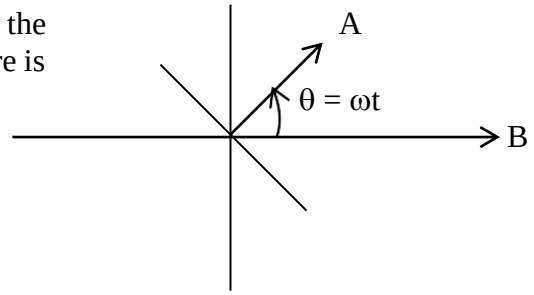
m = mass of the electrons.

u_o = speed of the ejected electrons.

A photo electric cell is a device to convert light energy into electric energy. A photo emissive photocell consists of a photo sensetive coated cathode inside a vacuum tube having an anode. The terminals are connected to terminals when light gets incident on cathode electrons are emitted and forms a current in the circuit.

3.(**Additional**) Deduce an expression for induced e.m.f. in a coil rotating uniformly in uniform magnetic field. Discuss the nature of e.m.f.

Ans: When a rectangular coil is rotated about its axis of symmetry in the space where magnetic field is normal to the axis of rotation there is change in flux this causes induced e.m.f. in the coil.



Instanteneous flux intercepted by the coil.

$$\phi = NBA \cos \omega t$$

Where N = no. of turns of the coil.

B = Magnetic field.

A = Area of the coil.

ω = angular speed of rotation.

According to Faraday's law of electromagnetic induction.

$$e = -d\phi/dt = NBA \sin \omega t$$

$$= e_o \sin \omega t$$

Where e_o = NBAω is called peak value of e.m.f.

The e.m.f. varies with time under sinusoidal function.

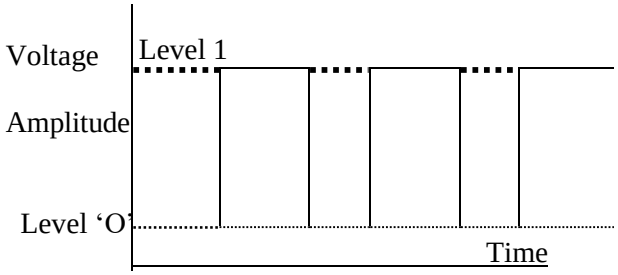
Such e.m.f. is called alternating current e.m.f

PAGE-8

Logic Gates

Digital electronics & Logic gates : - A Logic gate is an electric circuit which make logical decisions by relating input and output. It contains semiconductor devices like PN junction, transistor. These devices function in two status supposed to be yes or no, true or false, high and low, open or closed. These functional states are represented as level 0 and 1.

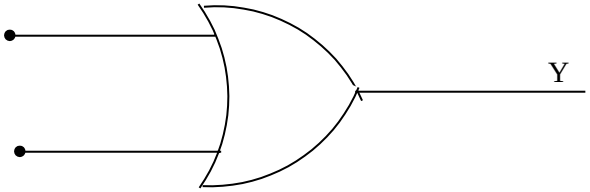
Usually 0 stands for before barrier and 1 for above barrier in which PN junction operates.



The graph shows discrete values of voltages. The values of voltages are classified into two levels. High level is termed as '1' while low level is called 'O'.

Logic Gate or Gate :- It has two inputs with one output.

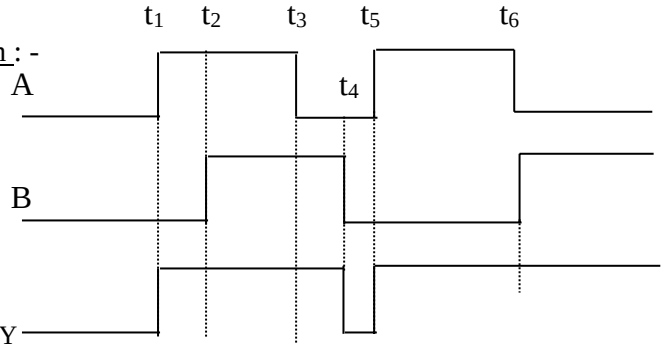
Y = A + B



Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

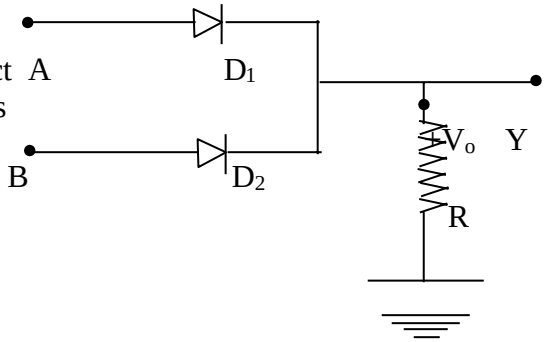
OR Gate Wave form : -



	A	B	Y
(i) $t<t_1$	Low(o)	Low(o)	Low(o)
(ii) $t_1<t<t_2$	High(l)	Low(o)	High(l)
(iii) $t_2<t<t_3$	High(l)	High(l)	High(l)
(iv) $t_3<t<t_4$	Low(o)	High(l)	High(l)
(v) $t_4<t<t_5$	Low(o)	Low(o)	Low(o)
(vi) $t_5<t<t_6$	High(l)	Low(o)	High(l)

PAGE-9

Diode OR Gate :-



(a) When voltage of A and B both are zero none of two D_1 & D_2 conduct and there is no current through R. There is no potential difference across R and potential at Y is zero.

A	B	Y
0	0	0

(b) When potential at A is V_o and at B is zero D_1 is forward biased. D_1 conducts through R causing potential difference across R then potential at Y is V_o positive.

A	B	Y
1	0	1

(c) When potential at A is zero but at B is V_o D_2 is forward biased and conducts through R causing potential difference across R and potential at Y to be positive.

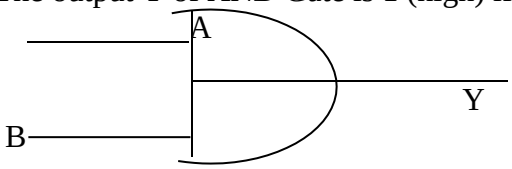
A	B	Y

When A and B both are positive potential both conducts through R. Y is at positive potential.

A	B	Y
1	1	1

AND Gate :-

The logic gate has two inputs and one output. The output Y of AND Gate is 1 (high) if all the inputs simultan ously have the state 1 (high).



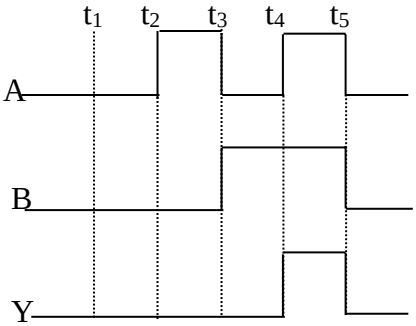
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

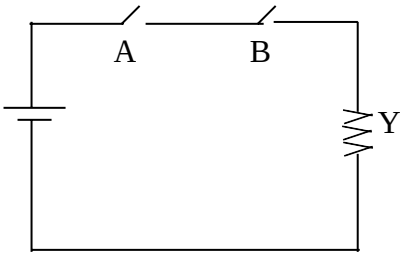
$t_1<t<t_2$
$A \rightarrow$ Low(o)
$B \rightarrow$ Low(o)
$Y \rightarrow$ Low(o)

$t_3<t<t_4$
$A \rightarrow$ Low(o)
$B \rightarrow$ High(l)
$Y \rightarrow$ Low(o)

$t_2<t<t_3$
$A \rightarrow$ High(l)
$B \rightarrow$ Low(o)
$Y \rightarrow$ Low(o)

$t_4<t<t_5$
$A \rightarrow$ High(l)
$B \rightarrow$ High(l)
$Y \rightarrow$ High(l)





Diode AND Gate :-

(a) When A and B both are zero, D_1 and D_2 both conducts through R the potential at Y drops to low level.

A	B	Y
0	0	0

(b) A is positive B is zero D_2 conducts through R Y is zero.

A	B	Y
1	0	0

(c) A is zero B is positive D_1 conducts through R.

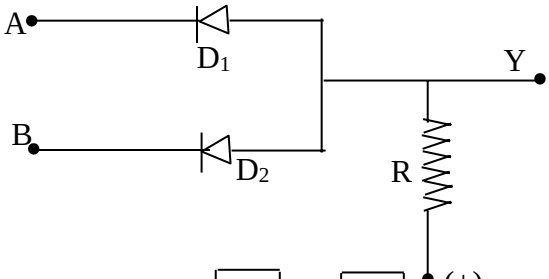
A	B	Y
0	1	0

(d) A and B both are positive no current flows Y is at positive.

A	B	Y
1	1	1

Y = A.B

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

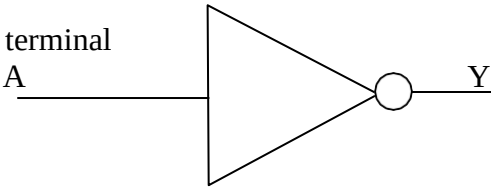


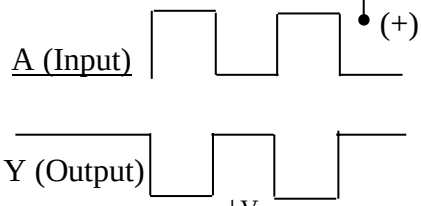
NOT Gate :-

It has a single input and output terminal

Truth table

A	Y
0	1
1	0

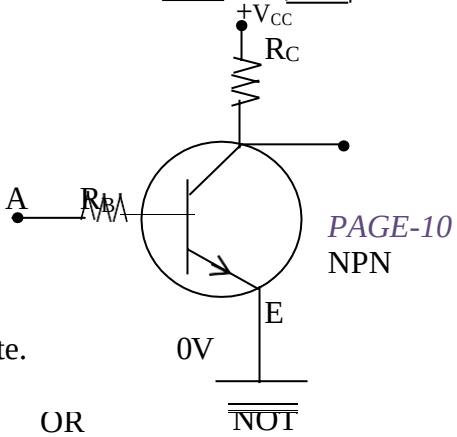




Transistor Not Gate :-

A	Y
0	1

When A is at positive potential E-B junction is forward biased current flows through R_C then Y is at low potential. When A is at zero E-B junction is unbiased and no current flows through R_C therefore y lie at high potential.



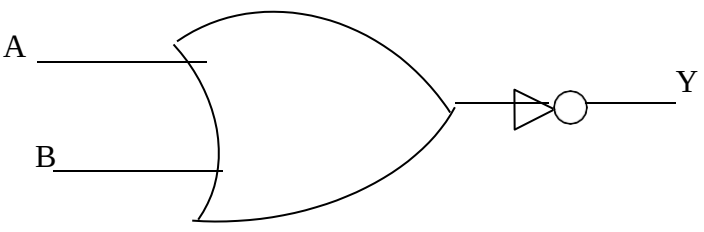
NOR Gate :-

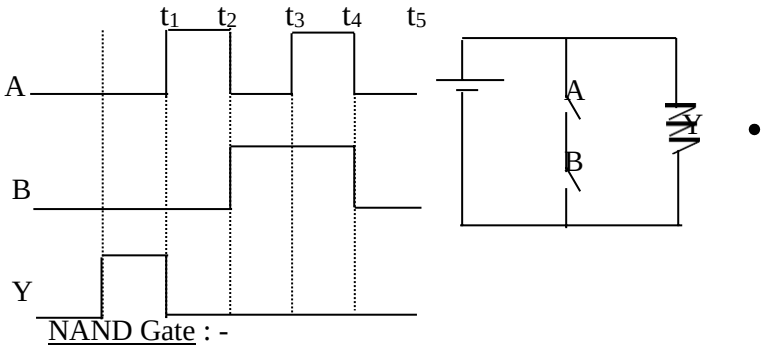
It has two input and one output. The OR Gate is followed by a NOT Gate.

$Y = (A+B)$

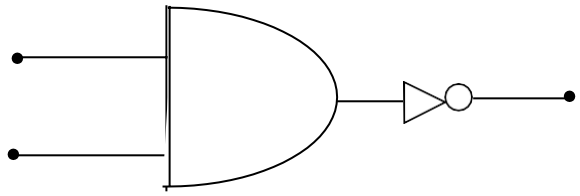
A	B	A+B	$\overline{A+B}$
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0
	A	B	Y

OR NOT



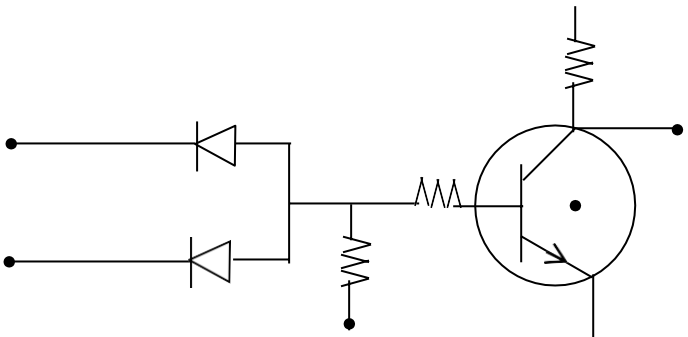


NAND Gate : -

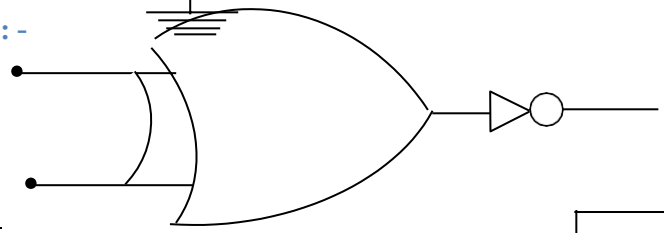


$\overline{Y = AB}$

A	B	AB	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0



Exclusive OR Gate (X OR Gate) : -



$Y = A \overline{O} B$

$= AB + BA$

A	B	$\overline{B}$	$\overline{A}$	Y
0	0	1	1	1
1	0	1	0	1
0	1	0	1	1
1	1	0	0	0