GV & ASSOCIATES, INC.

Hardware Interface Control Rev A Document

CubeSat DSP Processing System

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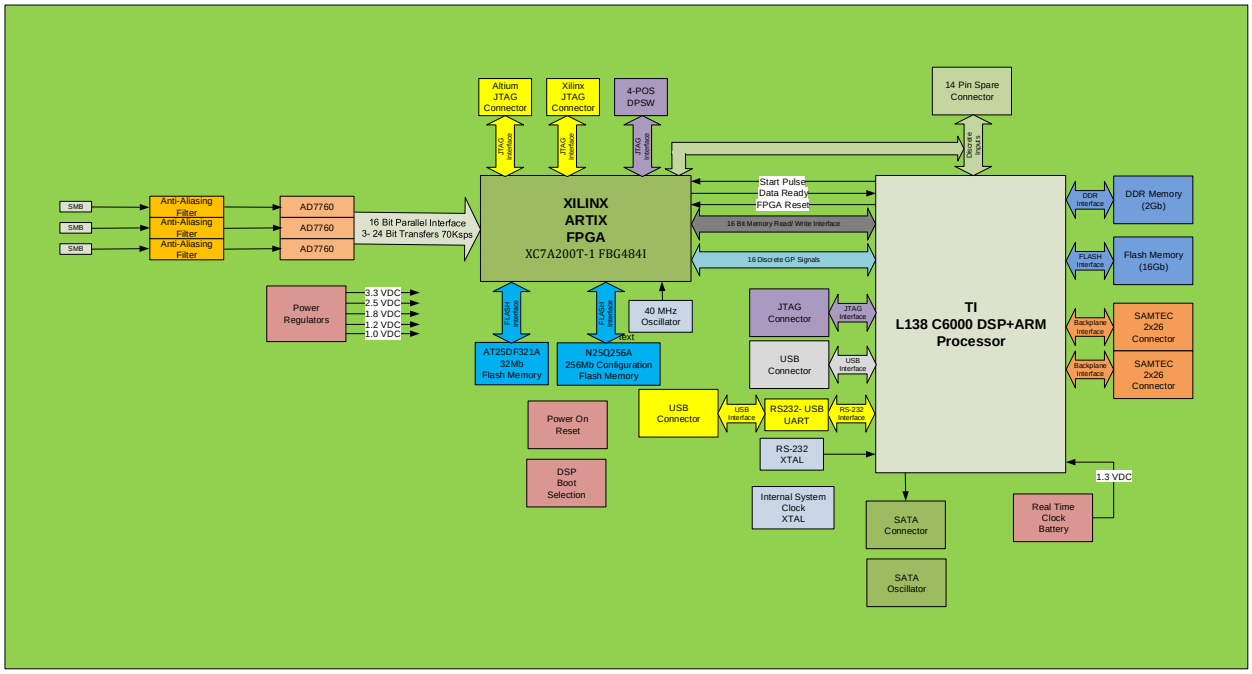
Table of Contents

1 Introduction

The purpose of this document is to describe the various components and the use of these components on the PCB and the FPGA. The first section of this document will focus on the PCB and the following sections will focus on the internal design of the FPGA.

2 CubeSat DSP Processing System V1.1 PCB Description

The CubeSat DSP Processing System PCB is divided into two main sections: Analog and Digital sections. The Analog section is comprised of the three AD7760s along with their associated Anti-Aliasing-Diff Amps and Precision Voltage References. The Digital section is comprised of all of the remaining components on the PCB. Please refer to the following block diagram for the remaining discussion of this section.



2.1.1.1 CubeSat DSP Processing System PCB Block Diagram

3 CubeSat DSP Processing System PCB Analog Section Discussion

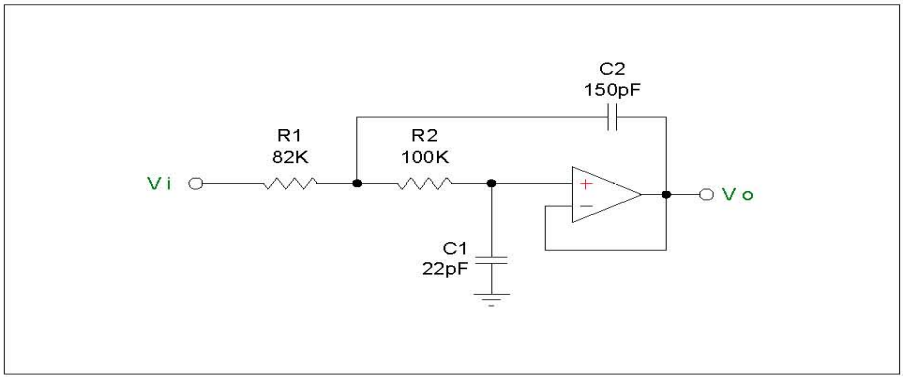
The Analog Section of the CubeSat DSP Processing System PCB is comprised of the SMB connector, the Analog Anti-Aliasing filter, the Differential Amplifier, and the AD7760 Analog to Digital Converter. The input to the analog SMB is expected to be a +- 2Vpp signal between 0-30 KHz.

3.1.1 Anti-Aliasing Filter

Each of the AD7760 Analog to Digital Converters has a 4th order Butterworth Low Pass Anti-Aliasing filter which has a passband of 30 KHz and a stopband frequency of 80 KHz with 30dB attenuation. The following diagrams show the schematic for the filter and the filter characteristics.

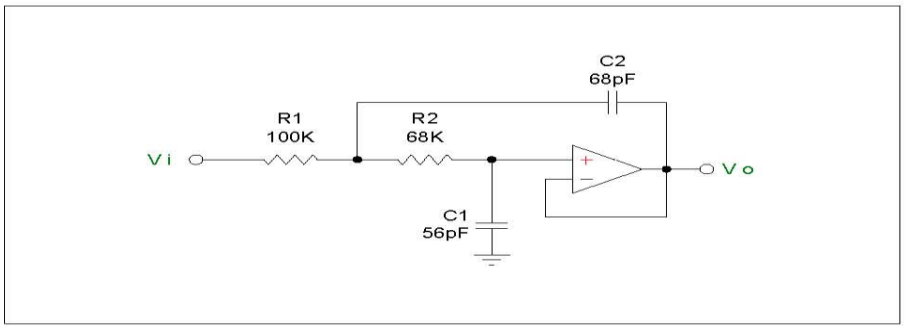
Butterworth Lowpass Filter N=4

Stage 1 of 2: Sallen-Key (SK) Second Order Lowpass I



3.1.1.1 Butterworth Lowpass Anti-Aliasing Filter Stage 1

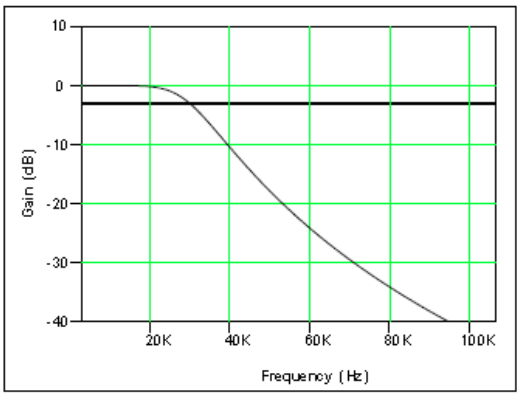
Stage 2 of 2: Sallen-Key (SK) Second Order Lowpass I

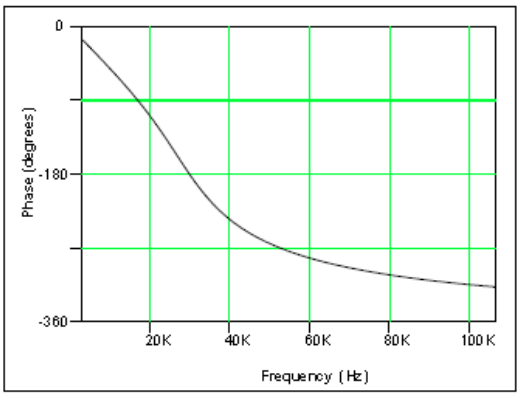


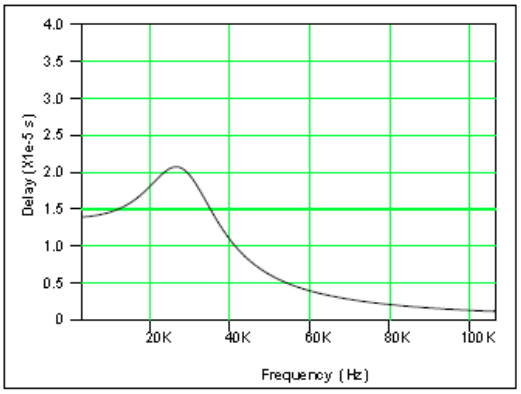
3.1.1.2 Butterworth Lowpass Anti-Aliasing Filter Stage 2

Butterworth Lowpass Filter N=4 Ideal Response

Passband attenuation:	3.000 dB	Stopband attenuation:	30.000 dB
Passband edge frequency:	33 KHz	Stopband edge frequency:	88 KHz



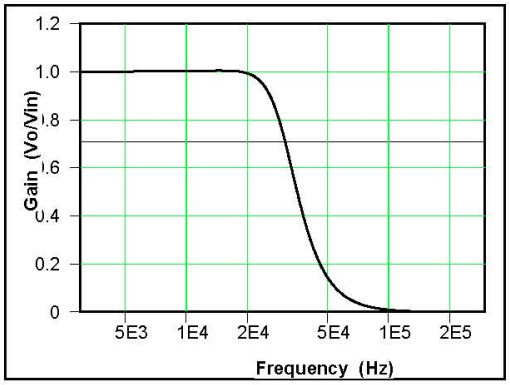


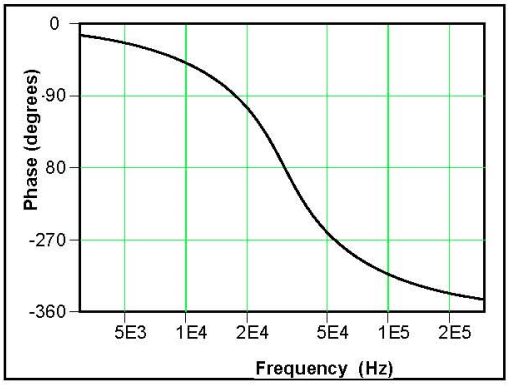


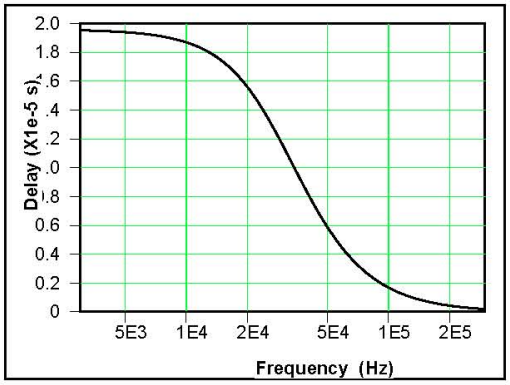
3.1.1.3 Butterworth Lowpass Anti-Aliasing Filter Ideal Frequency Response

Butterworth Lowpass Filter N=4 Final Response

Passband attenuation:	3.000 dB	Stopband attenuation:	30.000 dB
Passband edge frequency:	33 KHz	Stopband edge frequency:	88 KHz







3.1.1.4 Butterworth Lowpass Anti-Aliasing Filter Final Frequency Response

3.1.2 AD7760 Analog to Digital Converter Differential Amplifier Input Stage

It recommend by Analog Devices that a single end to differential conversion using an AD8021 opamp be use to drive the differential input of the AD7760. The recommended design as shown below in Figure 2.2.2.1

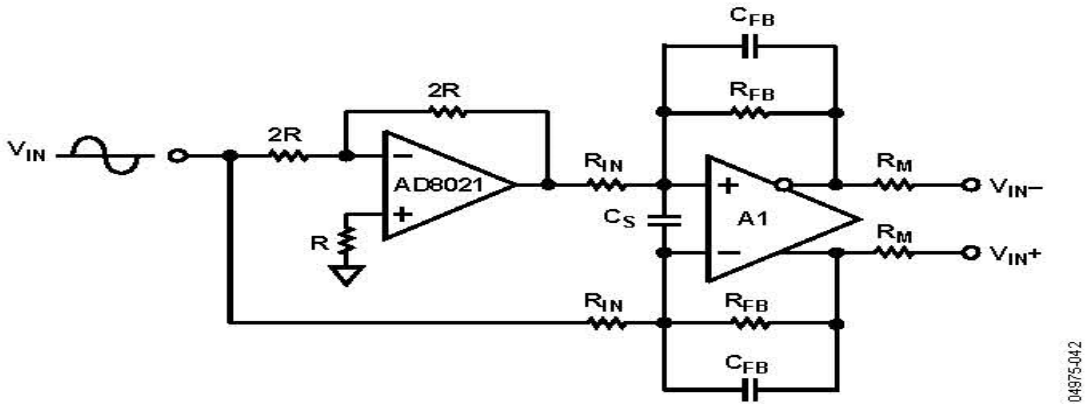


Figure 53. Single-Ended-to-Differential Conversion

3.1.2.1 AD7760 Differential Input Drive Diagram

3.1.3 AD7760 Analog to Digital Converter

The AD7760 is a high performance, 24-bit Σ-Δ analog-to-digital converter (ADC). It combines wide input bandwidth and high speed with the benefits of Σ-Δ conversion to achieve a performance of 100 dB SNR at 2.5 MSPS, making it ideal for high speed data acquisition. The differential input is sampled at up to 40 MSPS by an analog modulator. The modulator output is processed by a series of low pass filters, with the final filter having default or user-programmable coefficients. The sample rate, filter corner frequencies, and output word rate are set by a combination of the external clock frequency and the configuration registers of the AD7760. These configuration parameters are shown in the Table below. The boxed selection is the configuration used by the CubeSat DSP Processing System.

Table 6. Configuration with Default Filter

ICLK Frequency	Filter 1	Filter 2	Filter 3	Data State	Computation Delay	Filter Delay	Pass-Band Bandwidth	Output Data Rate (ODR)
20 MHz	Bypassed	Bypassed	Bypassed	Unfiltered	0	0	10 MHz	20 MHz
20 MHz	4×	Bypassed	Bypassed	Partially filtered	0.325 µs	1.2 µs	1.35 MHz	5 MHz
20 MHz	4×	Bypassed	2×	Fully filtered	1.075 µs	10.8 µs	1 MHz	2.5 MHz
20 MHz	4×	2×	Bypassed	Partially filtered	1.35 µs	3.6 µs	562.5 kHz	2.5 MHz
20 MHz	4×	2×	2×	Fully filtered	1.625 µs	22.8 µs	500 kHz	1.25 MHz
20 MHz	4×	4×	Bypassed	Partially filtered	1.725 µs	6 µs	281.25 kHz	1.25 MHz
20 MHz	4×	4×	2×	Fully filtered	1.775 µs	44.4 µs	250 kHz	625 kHz
20 MHz	4×	8x	Bypassed	Partially filtered	2.6 µs	10.8 µs	140.625 kHz	625 kHz
20 MHz	4×	8×	2×	Fully filtered	2.25 µs	87.6 µs	125 kHz	312.5 kHz
20 MHz	4×	16×	Bypassed	Partially filtered	4.175 µs	20.4 µs	70.3125 kHz	312.5 kHz
20 MHz	4×	16×	2×	Fully filtered	3.1 µs	174 µs	62.5 kHz	156.25 kHz
20 MHz	4×	32×	Bypassed	Partially filtered	7.325 µs	39.6 µs	35.156 kHz	156.25 kHz
20 MHz	4×	32×	2×	Fully filtered	4.65 µs	346.8 µs	31.25 kHz	78.125 kHz
12.288 MHz	4×	8×	2×	Fully filtered	3.66 µs	142.6 µs	76.8 kHz	192 kHz
12.288 MHz	4×	16×	2×	Fully filtered	5.05 µs	283.2 µs	38.4 kHz	96 kHz
12.288 MHz	4×	32×	Bypassed	Partially filtered	11.92 µs	64.45 µs	21.6 kHz	96 kHz
12.288 MHz	4×	32×	2×	Fully filtered	7.57 µs	564.5 µs	19.2 kHz	48 kHz

3.1.3.1 AD7760 Digital Filter Configuration Table

The SYNC input to the AD7760 provides a synchronization function that allows the user to begin gathering samples of the analog front-end input from a known point in time. The SYNC function allows multiple AD7760s, operated from the same MCLK, RESET, and SYNC signals, to be synchronized so that each ADC simultaneously updates its output register. The distribution of the signals that are common to each of the devices that are to be synchronized is extremely important in insuring that the timing of each of the AD7760 devices is correct, that is, that each AD7760 device sees the same digital edges synchronously. The timing of the SYNC signal is shown in the diagram show below.

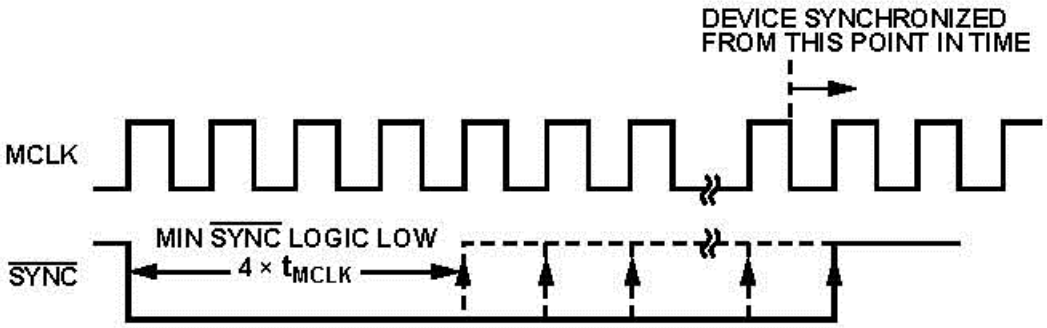


Figure 46. Recommended SYNC Timing

3.1.3.2 AD7760 SYNC Timing Diagram

To read a conversion result from the AD7760, two 16-bit read operations are performed. The DRDY pulse indicates that a new conversion result is available. Both RD/WR and CS go low to perform the first read operation. Shortly after both lines go low, the data bus becomes active and the 16 most significant bits (MSBs) of the conversion result are output. The RD/WR and CS lines must return high for a full ICLK period before the second read is performed. This second read contains the eight least significant bits (LSBs) of the conversion result along with six status bits. The read/write timing diagram and Status Register is shown below.

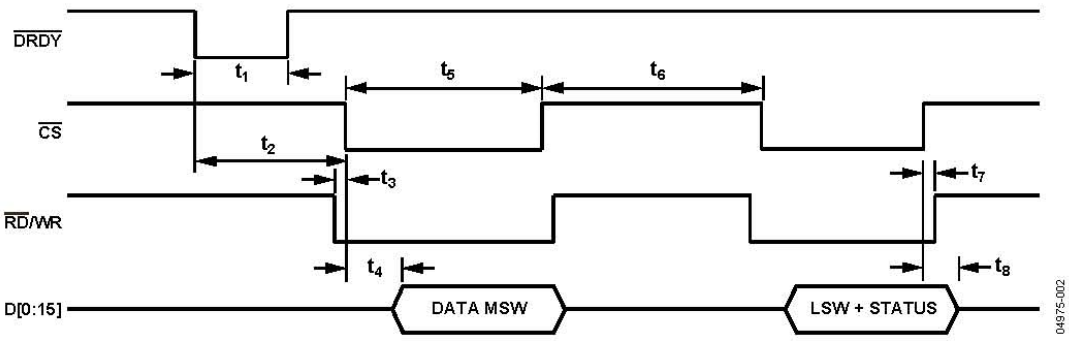


Figure 2. Filtered Output—Parallel Interface Timing Diagram

3.1.3.3 AD7760 Read/Write Timing Diagram

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
DVALID	OVR	UFILT	LPWR	FILTOK	DLOK	0	0

3.1.3.4 AD7760 Status Register

The AD7760 has a number of user-programmable registers. The control registers are used to set the decimation rate, the filter configuration, the clock divider, and so on. There are also digital gain, offset, and over-range threshold registers. Writing to these registers involves writing the register address first, then a 16-bit data-word. Control Register 1 is loaded with 1DH and Control Register 2 is loaded with 02H by the FPGA firmware.

CONTROL REGISTER 1—ADDRESS 0x0001

Default Value 0x001A

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DL_ FILT	RD OVR	RD GAIN	RD OFF	RD STAT	0	SYNC	FLEN3	FLEN2	FLEN1	FLEN0	$\overline{\text{BYP F3}}$	$\overline{\text{BYP F1}}$	DEC2	DEC1	DEC0

Table 15. Bit Descriptions of Control Register 1

Bit	Mnemonic	Description
15	DL_FILT[1]	Download Filter. Before downloading a user-defined filter, this bit must be set. The filter length bits must also be set at this time. The write operations that follow are interpreted as the user coefficients for the FIR filter until all the coefficients and the checksum have been written.
14	RD OVR[1, 2]	Read Overrange. If this bit has been set, the next read operation outputs the contents of the overrange threshold register instead of a conversion result.
13	RD GAIN[1, 2]	Read Gain. If this bit has been set, the next read operation outputs the contents of the digital gain register.
12	RD OFF[1, 2]	Read Offset. If this bit has been set, the next read operation outputs the contents of the digital offset register.
11	RD STAT[1, 2]	Read Status. If this bit has been set, the next read operation outputs the contents of the status register.
10	0	0 must be written to this bit.
9	SYNC[1]	Synchronize. Setting this bit initiates an internal synchronization routine. Setting this bit simultaneously on multiple devices synchronizes all filters.
8 to 5	FLEN [3:0]	Filter Length Bits. These bits must be set when the DL_FILT bit is set before a user-defined filter is downloaded.
4	$\overline{\text{BYP F3}}$	Bypass Filter 3. If this bit is 0, Filter 3 (programmable FIR) is bypassed.
3	$\overline{\text{BYP F1}}$	Bypass Filter 1. If this bit is 0, Filter 1 is bypassed. This should only occur when the user requires unfiltered modulator data to be output.
2 to 0	DEC [2:0]	Decimation Rate. These bits set the decimation rate of Filter 2. All 0s implies that the filter is bypassed. A value of 1 corresponds to 2× decimation, a value of 2 corresponds to 4× decimation, and so on, up to the maximum value of 5, corresponding to 32× decimation.

[1] Bit 15 to Bit 9 are self-clearing bits.
[2] Only one of the bits from Bit 14 to Bit 11 can be set in any write operation because it determines the contents of the next read operation.

CONTROL REGISTER 2—ADDRESS 0x0002

Default Value After $\overline{\text{RESET}}$: 0x009B

Recommended register setting for power-up and normal operation using clock divide-by-2 ($\overline{\text{CDIV}}$ = 0) mode: 0x0002

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	$\overline{\text{CDIV}}$	0	PD	LPWR	1	D1PD

Table 16. Bit Descriptions of Control Register 2

Bit	Mnemonic	Description
5	$\overline{\text{CDIV}}$	Clock Divider Bit. This sets the divide ratio of the MCLK signal to produce the internal ICLK. Setting $\overline{\text{CDIV}}$ = 0 divides the MCLK by 2. If $\overline{\text{CDIV}}$ = 1, the ICLK frequency is equal to the MCLK.
3	PD	Power Down. Setting this bit powers down the AD7760, reducing the power consumption to 6.35 mW.
2	LPWR	Low Power. If this bit is set, the AD7760 is operating in a low power mode. The power consumption is reduced for a 6 dB reduction in noise performance.
1	1	Write 1 to this bit.
0	D1PD	Differential Amplifier Power Down. Setting this bit powers down the on-chip differential amplifier.

4 CubeSat DSP Processing System FPGA Section Discussion

This section will discuss the use of the FPGA and its associated peripherals devices. The main purpose of the FPGA is to interface the three AD7760 Analog to Digital Converters, process the data gathered from the AD7760s and transfer the processed data to the L138 DSP Processor for further processing.

4.1 FPGA to AD7760 Interface

The FPGA uses a standard 16 bit microprocessor memory interface to communicate with the three AD7760. The FPGA shares the data bus, reset, sync, read/write, and data ready signal with the three AD7760s. Each AD7760 has its own individual CS signal so that the FPGA can select the AD7760 to which it wishes to communicate.

4.2 FGPA to L138 DSP Processor Interface

The FPGA uses a standard 16 bit microprocessor memory interface to communicate with the L138 DSP Processor. The L138 will use this interface to read the processed data from the FPGA as well as communicate future command and status. There is a 13 bit address bus along with two CS (CS0 and CS2). Additionally, the WE, OE, WAIT and the DSP Clock are routed to the FPGA.

4.3 General Purpose Discrete Signals

There are 16 Discrete I/O signals that are shared between the FPGA and the L138 for strobes, resets and other I/O purposes. These I/O signals and the associated pins for the L138 and FPGA are shown in the table below. The first SIX signals (L138_GP0-L138_GP5) are connected to on-board LEDs for visibility purposes.

Signal Name	L138 Port	L138 Pin No.	FPGA Pin No.	LED (active low)
L138_GP0	GP8[15]	G1	AB1	D2
L138_GP1	GP1[9]	E1	AA1	D3
L138_GP2	GP1[12]	D1	Y1	D4
L138_GP3	GP1[14]	C1	W1	D5
L138_GP4	GP0[14]	B1	U1	D6
L138_GP5	GP0[15]	A1	T1	D7
L138_GP6	GP8[7]	F3	AB2	
L138_GP7	GP1[11]	E3	Y2	
L138_GP8	GP1[13]	D3	W2	
L138_GP9	GP0[1]	C3	V2	
L138_GP10	GP0[5]	B3	U2	
L138_GP11	GP0[0]	E4	R2	
L138_GP12	GP0[6]	B4	AB3	
L138_GP13	GP0[4]	C4	V3	
L138_GP14	GP0[2]	D4	U3	
L138_GP15	GP0[3]	C5	R3	

4.3.1.1 FPGA to L138 DSP Processor General Purpose Discrete Signal Table

4.4 FPGA Peripheral Components

This section discusses the peripherals that are connected to just the FPGA.

4.4.1 256 Mb Configuration EEPROM (U22)

This is the non-volatile memory device used to hold the FPGA configuration file that will be used to program the FPGA after power is applied to the CubeSat DSP Processing System PCB.

4.4.2 32 Mb EEPROM (U23)

This is an accessary device which would allow for future use to storage information or data by the FPGA in a non-volatile device. It could be used to record errors, diagnostic issues, or other data.

4.4.3 4 Position Dip Switch (SW1)

This switch allow for the user of the CubeSat DSP Processing System PCB to set discreet inputs directly into the FPGA for such as the following: allowing a pre-set test data set to be used instead of real AD data, allowing for the internal generation of the sweep input signal or other diagnostic or operational configurations.

4.5 FPGA Connectors

This section will describe the CubeSat DSP Processing System PCB connectors that are used only by the FPGA

4.5.1 Xilinx JTAG Connector (JP1)

This connector is used to allow access to the internal design of the FPGA for programming, debugging and simulation via the Xilinx development platform. It allows for the ability to directly program the FPGA Configuration EEPROM (U22) via a Xilinx USB POD which is connected to a laptop computer running the Xilinx development software.

Signal Name	JP1 Pin No.	FPGA Pin No.
TDI	5	R13
TDO	2	U13
TCK	4	V12
TMS	3	T13
+3.3VDC	1	
DGND	6	

4.5.1.1 Xilinx JTAG Connector (JP1) Table

4.5.2 Altium JTAG Connector (JP2)

This connector is used to allow access to the internal design of the FPGA for programming, debugging and simulation via the Altium development platform. It allows for the embedding of logic analyzers, discreet signal input and output along with the ability to directly program the FPGA via an Altium USB POD which is connected to a laptop computer running the Altium development software.

Signal Name	JP2 Pin No.	FPGA Pin No.
TDI	1	R13
TDO	2	U13
TCK	3	V12
TMS	4	T13
SOFT_TDI	5	K19
SOFT_TDO	6	K18
SOFT_TCK	7	K16
SOFT_TMS	8	K17
DGND	9	

4.5.2.1 Altium JTAG Connector (JP2) Table

4.5.3 FPGA Configuration Jumper (JP3)

This jumper is used to allow for two different methods for the programming of the FPGA. If the jumper is installed, the FPGA is configured for JTAG programming and expects that either the Xilinx or Altium USB pod will be used to program the FPGA. If the jumper is removed, the FPGA will be programmed with the configuration file stored in the configuration EEPROM (U22).

5 CubeSat DSP Processing System DSP Processor (L138) Section Discussion

This section will discuss the use of the DSP Processor (L138) and its associated peripherals devices. The main purpose of the DSP Processor is to process data transferred from the FPGA and store the resulting data on a SATA SSD for downlinking to an Earth station.

5.1 FPGA Peripheral Components

This section discusses the peripherals that are connected to just the DSP Processor (L138).

5.1.1 Double Data Rate SDRAM (U32A)

The DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. DDR SDRAM is the DSP Processor (L138) primary working memory, storing program instructions and data. It is a 8M deep x 16 bits x 8 banks architecture.

5.1.2 NAND FLASH Memory (U33)

The NAND FLASH memory is the primary storage memory for the program that runs the DSP Processor (L138). This a 4Gb device with a 4096 blocks by 16 bit architecture.

5.1.3 RS-232 to USB UART (U31)

This device allows the DSP Processor to communicate via the on-chip RS-232 ports (UART2_RXD and UART2_TXD) to a USB device connected to connector J1.

5.1.4 RS-232 Dual Transceiver (U6)

This RS-232 transceiver is used to connect the DSP Processor RS-232 ports UART0_TXD and UART0_RXD to the SATCOM_TXD and SATCOM_RXD respectfully. The SATCOM signals come on-board via the H1 connector pin 2 and 3.

Additionally, the second half of the transceiver is used to connect the DSP Processor RS-232 ports UART1_TXD and UART1_RXD to the SYNTH_TXD and SYNTH_RXD respectfully. The SYNTH signals come on-board via the H2 connector pin 2 and 3.

5.1.5 SATA Oscillator (U30)

This component is used to generate the 25MHz clock for the internal SATA controller.

5.2 DSP Processor Connectors

This section will describe the CubeSat DSP Processing System PCB connectors that are used only by the DSP Processor (L138)

5.2.1 USB Mini Type A Connector (P5)

This connector allows the DSP Processor to access a USB device via USB1_DM and USB1_DP.

5.2.2 SATA Connector (J2)

This connector is used to interface the DSP Processor with the SATA Solid State Drive (SSD) which is being used to store processed data for downlinking to an Earth station.

Signal Name	J2 Pin No.	L138 Pin No.
SATA_TX_P	2	J1
SATA_TX_N	3	J2
SATA_RX_N	5	L2
SATA_RX_P	6	L1
DGND	1	
DGND	4	
DGND	7	

5.2.2.1 DSP SATA Connector (J2) Table

5.2.3 DSP Processor (L138) Boot Jumpers (JP6 and JP7)

These two jumpers are used to select which device the DSP Processor will use to boot from upon power-up.

JP6	JP7	Boot Selection
Removed	Removed	EEPROM
Installed	Removed	UART2 Boot
Removed	Installed	SD Boot

5.2.3.1 DSP Processor Boot Jumper (JP6 and JP7) Table

6 CubeSat DSP Processing System Shared Connectors

6.1 PC104 Connector (H1)

These are the pins used on the PC104 H1 connector.

Signal Name	H1 Pin No.	L138 Port	L138 Pin No.	FPGA Pin No.
H1_SPARE1	1	GP8[5]	C18	G17
SATCOM_TXD	2	UARTO_TXD	D18	
SATCOM_RXD	3	UART0_RXD	C19	
H1_SPARE2	4	GP8[6]	C16	G18
H1_SPARE4	30	GP1[6]	D17	J22
H1_SPARE5	34	GP8[1]	D16	J19
H1_SPARE6	33	GP8[2]	E17	J20
H1_SPARE7	36	GP1[7]	E16	H18
H1_SPARE8	35	GP2[3]	G19	H22
H1_SPARE9	38	GP1[4]	G18	H17
H1_SPARE10	37	GP2[10]	G17	L20
H1_SPARE11	40	GP1[5]	G16	M20
H1_SPARE12	39	GP2[11]	H17	L21
H1_SPARE13	44	GP2[12]	H16	M21

6.1.1.1 PC104 Connector (H1) Table

6.2 PC104 Connector (H2)

These are the pins used on the PC104 H2 connector.

Signal Name	H1 Pin No.	L138 Port	L138 Pin No.	FPGA Pin No.
SATCOM_TXD	2	UARTO_TXD	D18	
SATCOM_RXD	3	UART0_RXD	C19	
H1_SPARE2	4	GP8[6]	C16	G18
H1_SPARE4	30	GP1[6]	D17	J22
H1_SPARE5	34	GP8[1]	D16	J19
H1_SPARE6	33	GP8[2]	E17	J20
H1_SPARE7	36	GP1[7]	E16	H18
H1_SPARE8	35	GP2[3]	G19	H22
H1_SPARE9	38	GP1[4]	G18	H17
H1_SPARE10	37	GP2[10]	G17	L20
H1_SPARE11	40	GP1[5]	G16	M20
H1_SPARE12	39	GP2[11]	H17	L21
H1_SPARE13	44	GP2[12]	H16	M21

6.2.1.1 PC104 Connector (H1) Table

6.3 Spare Connector (JP4)

JP4 is a spare connector added for use with proposed daughter PCBs such as a SD card reader PCB. These SPARE signals are shared with the L138 DSP Processor.

Signal Name	JP4 Pin No.	L138 Port	L138 Pin No.	FPGA Pin No.
SP_HDR0	4	MMCSD0_CMD	A10	V17
SP_HDR1	5	MMCSD0_D1	A11	R19
SP_HDR2	6	MMCSD0_D7	A12	T18
SP_HDR3	7	MMCSD0_D0	B10	V20
SP_HDR4	8	MMCSD0_D4	B11	W17
SP_HDR5	9	MMCSD0_D2	C10	W21
SP_HDR6	10	MMCSD0_D6	C11	AA18
SP_HDR7	11	MMCSD0_CLK	E9	AB18
SP_HDR8	12	MMCSD0_D3	E11	P19
SP_HDR9	13	MMCSD0_D5	E12	AB20
-5VDC	1			
+5VDC	2			
+3.3VDC	3			
DGND	14			

6.3.1.1 FPGA SPARE Connector (JP4) Table

6.4 Spare Input Power Connector (JP5)

This connector can be used as an auxiliary power input connector in case the PC-104 power inputs will not supply sufficient input power.

Signal Name	JP5 Pin No.	Signal Name	JP5 Pin No.
+3.3V	1	-5V	7
+3.3V	2	-5V	8
+3.3V	3	DGND	9
+3.3V	4	DGND	10
+5V	5	DGND	11
+5V	6	DGND	12

6.4.1.1 Spare Input Power Connector (JP5) Table

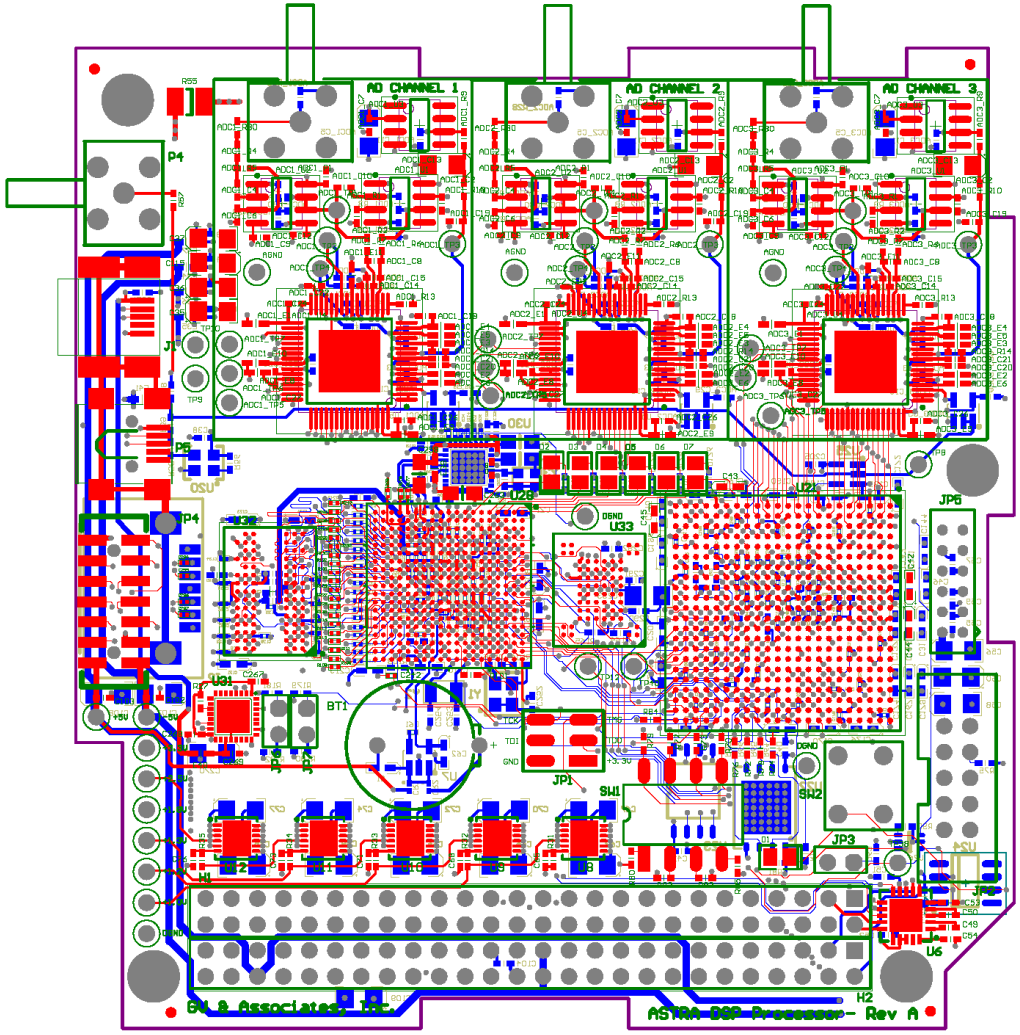
6.5 External Clock Connector (P4)

This connector can be used to bring an external clock to be used instead of the on-board 40 MHz clock. R57 and R58 (0 ohm) would need to be installed and R59 would need to be removed in order to use this feature.

7 Revision A Notes

This revision represents the hardware changes between the Rev 1.1 and Rev A PCB Hardware changes.

1. Removal of the DSP Emulator Connector.
2. Move the Xilinx JTAG connector to former location of the DSP Emulator Connector
3. Add an auxiliary power input connector JP5 in the former location of the Xilinx JTAG Connector
4. Replaced the Voltage regulators with Linear Tech components
5. Redesign and added a voltage regulator and diodes for L138 Real Time Clock Power.


AD CHANNEL 1
AD CHANNEL 2
AD CHANNEL 3
P4
P5
P6
JP1
JP3
JP6
SW1
SW2
U6
U31
U33
BT1
H2
ASTRA DSP Processor- Rev A