GVA-395

Virtex-II Hardware Accelerator
User's Manual

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1.0 GVA-395 Introduction and General Description

The GVA-395 Modular DSP Development Platform consists of three Xilinx FPGAs. Two Virtex-II FPGAs are used for Analog Control (ACX and AC) and two Virtex-II FPGAs are used for Data Processing (DP and DPX) respectively. The DPX FPGA also serves as the primary FPGA for external communication. A Spartan-II FPGA (EI) is used for interfacing to provide a 5V tolerant external interface. An additional Spartan-II FPGA is used to assist in programming the bit stream into the Flash EPROM and the configuration of the other FPGAs.

The platform's general configuration consists of 12 interchangeable daughter PCBs that allow for a wide range of I/O capability. Eight of the daughter PCBs are dedicated to the ACX FPGA. Two daughter PCBs are dedicated to the AC FPGA and an additional two daughter PCBs are dedicated to the DP FPGA. Daughter PCB modules are to be as follows:

- 100 MSPS 12 bit A/D (GVA-AD9432)
- 170 MSPS 12 bit A/D (GVA-AD9430)
- 100 MSPS 14 bit A/D (GVA-AD6645)
- 100 MSPS 12 bit D/A (GVA-AD9762)
- 160 MSPS 14 bit D/A (GVA-AD9772)
- Customer specific designs may be implemented.

The digitized data from the daughter PCB may be processed by the ACX FPGA and passed to the other FPGPs for further processing. The processed data may also be sent to the external LVDS data port via the DPX Virtex-II FPGA. A data file may also be uploaded via a USB or Parallel Port interface and may be imported into MatLab for additional analysis. A data file may also be downloaded to the on-board SDRAM via two USBs interface for processing by the GVA-395.

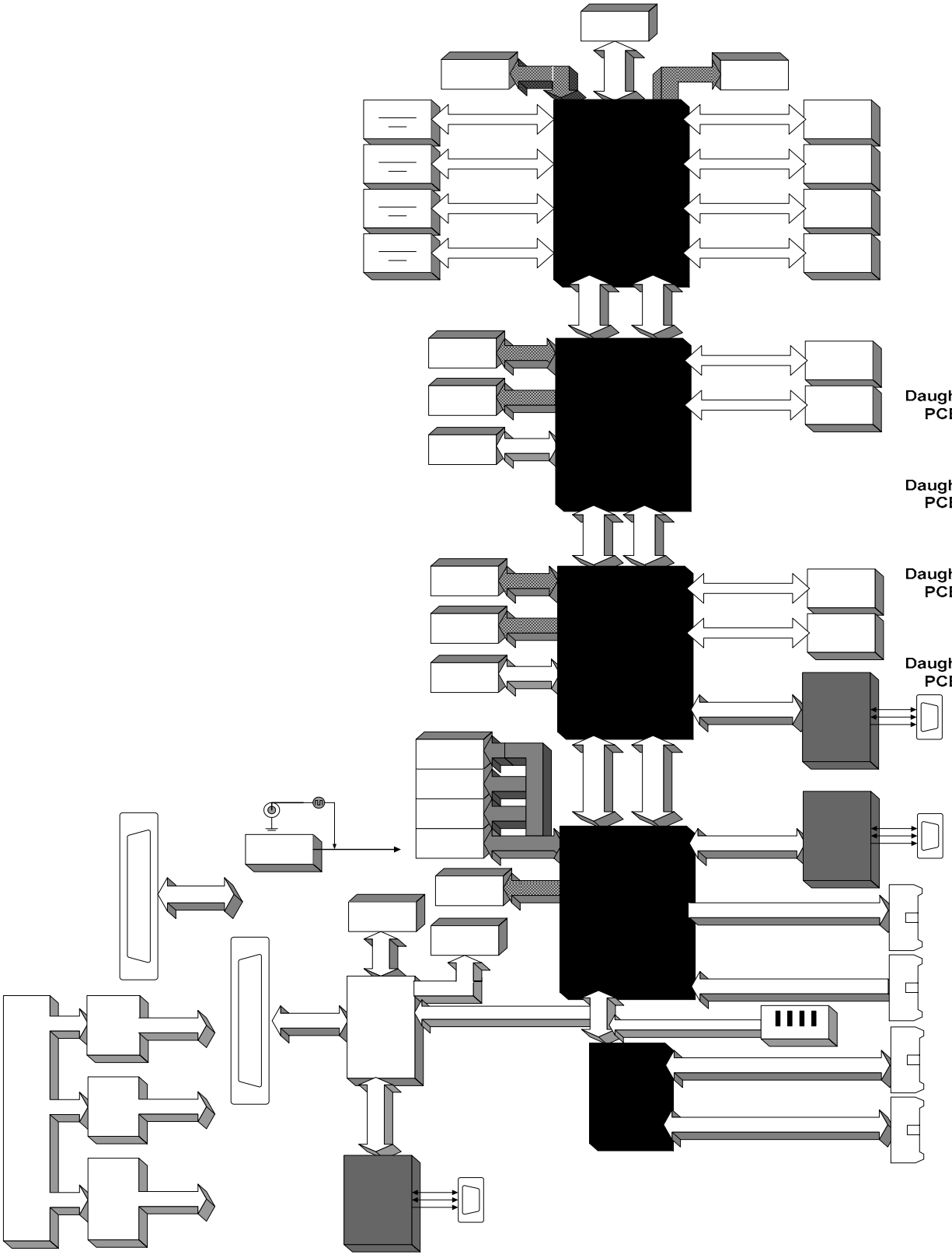
The ACX and AC FPGAs have access to an external 256K x 18 ZBT SRAM, the DP FPGAS has access to an external 1M x 18 ZBT SRAM, and the DPX has access to four external 1M x 18 ZBT SRAMs that can be used for temporary data storage. Each Virtex-II FPGA also has up to 1,728,000 bits of internal Block SelectRAM. There individual 100 bit dedicated local buses connecting the ACX, AC, DP and the DPX FPGAs. Additionally, there is a shared 43 bit local buses between the ACX, AC, DP, DPX and the EI FPGAs.

The external interface Spartan II FPGA (EI) is used to provide a +5V CMOS tolerant interface between the Virtex-II FPGAs and other external devices. However, this FPGA could be used for additional processing as determined by the user.

Using the 48-bit external bus interface, the GVA-395 could be configured to have an off-board interface to an external processor such as a TMS320C31 or other Digital Signal Processors. Additionally, the GVA-395 can be configured either by the Multilinx JTAG cable or by the on-board FLASH EPROM. The on-board FLASH EPROM can be programmed through the use of the Multilinx Slave Serial configuration connector. The Xilinx FPGAs may also access unused address space in the configuration EPROM by interfacing to the Spartan-II configuration FPGA via either the FPGA local bus or the dedicated 32 bit Spartan-II external interface bus. For non-specific clock requirements, an external clock source is available.

Additional features are listed below and will be explained in detail in Section 2.0.

- **4 Virtex™-II FPGAs for Signal Processing**
- **1 Spartan™-II FPGA for External Interface**
- **1 Spartan™-II FPGA for Configuration Control**
- **3 USB interfaces**
- **Supports Xilinx ChipScope-ILA**
- **12 Interchangable I/O Daughter PCB capability**
- **Dedicated external communication FPGA for analog control**
- **Eight Digital Clock Managers per Virtex-II FPGA**
- **Up to 168 18x18 Multipliers per Virtex-II FPGA**
- **+5 V tolerant 48 bit external I/O**
- **32 Bit LVDS interface**
- **FPGA logic expansion (1.5M to 3M gates)**
- **Each Virtex-II FPGA has at least a dedicated 256K x 18 ZBT SRAM**
- **Up to 3,024,000 bits of internal Block SelectRAM™**
- **100 bit local bus between the each of Virtex-II FPGAs**
- **43 bit shared local bus between Virtex-II and Spartan-II FPGAs**
- **JTAG download configurable**
- **On-board 16M x 8 FLASH EPROM**
- **On-board FLASH EPROM programming**
- **On-board 20 Amp 1.5V Core Power supply**
- **Programmable A/D and D/A sample clocks**
- **On-board 50 MHz clock oscillator (which can be doubled by the Virtex-II DLL).**
- **External high stability clock Input**
- **Four bit DIP Switch for internal use by FPGAs**



1.1.1 GVA-395 DSP Demonstration Platform Block Diagram

2.0 GVA-395 Power Configuration

The GVA-395 Hardware Accelerator was delivered with Molex power connector. Care should be taken to insure that the proper power levels are applied to this power connector. The power configuration is shown in Table 2.1.1.

Power Connector Pin No.	Power	Connector Wire Color
1	Ground	Black
2	Ground	Black
3	Ground	Black
4	Ground	Black
5	+5V	Red
6	+5V	Red
7	+5V	Red
8	+5V	Red

2.1.1 GVA-395 Power Configuration Table

The GVA-395 Hardware Accelerator comes configured for a single supply mode (+5V).

3.0 Initial GVA-395 Diagnostic Check-out

In order to verify proper operation of the GVA-395, the customer should perform the following tests upon receipt of the unit. The GVA-395 on-board Flash EEPROM when delivered is configured with the diagnostic program for all of the tests. Additionally, the GVA-395 is setup to configure the FPGAs for the diagnostic routine.

1. Insure that a jumper block is on the jumper block at JP5 and JP9.
2. Connect the power cable to at least a 3 A +5V regulated power supply as describe in Section 2.0.
3. Attach a 34-wire ribbon cable to J1 and J2 for the LVDS loop back test.
4. Attach a 34-wire ribbon cable to J4 and J5 for the LVTTL loop back test.
5. Apply power to the GVA-395.
6. Verify that the proper voltages are present: +5V->TP8, +3.3V->TP9, +2.5V->TP10, 1.5V->TP11.
7. The LEDS of AR3 will toggle while the FPGA are being programmed
8. Once the tests which are described in Section 16 are run, all of the LEDs (D1 thru D40) should be lite. This indicates that the tests have been successfully completed.
9. Using a function generator, an analog signal should be connected to P1 thru P4. The same waveform may then be viewed with either an oscilloscope or spectrum analyzer at P7 thru P10. It should be noted that the customer should use an anti-aliasing filter such as SLP-30 (Mini-Circuits) on each input channel and a similar smoothing filter on each output channel. Without the filters, excessive noise may be present.
10. The diagnostic tests may be re-initiated by pressing the reset button SW1.

4.0 Xilinx FPGA Configuration

The three Xilinx FPGAs may be configured three ways.

4.1 JTAG Cable Configuration

To use the JTAG download cable, the jumper block must be installed on JP1 and jumper block on JP9 must be removed. The Virtex-II FGPA at U10 will be configured first, then the Virtex-II FPGA at U12, then the Virtex-II FPGA at U14, then the Virtex-II FPGA at U16, and finally the Spartan II FPGA at U18. Attach the JTAP Cable to JP10 as follows: VCC ->1, GND->2, TDO -> 3, TDI -> 4, TCK ->5, TMS ->6. Pin 1 will be the pin closest to SW1.

4.2 Slave Serial Cable Configuration

To use the Slave Serial download cable, a jumper block must be installed on JP1 and JP9. The Virtex-II FGPA at U10 will be configured first, then the Virtex-II FPGA at U12, then the Virtex-II FPGA at U14, then the Virtex-II FPGA at U16, and finally the Spartan II FPGA at U18. Attach the Slave Serial Cable to JP5 as follows: VCC -> 1, GND -> 2, CCLK -> 4, DONE -> 5, DIN -> 6, PROG -> 7, INIT -> 8, RST -> 9. Pin 1 will be the pin closest to U13.

4.3 Parallel Down-Load Configuration

To use the parallel Flash EPROM (U2) to configure the Xilinx FPGAs, the jumper block at JP3 and JP9 must be installed and the jumper block on JP2 must be removed. The EPROM file must be programmed from the ***bottom up***. This file must then be uploaded to the FLASH EPROM (U37) using the Slave Serial configuration mode. This is further described in the section below. The Virtex-II FGPA at U10 will be configured first, then the Virtex-II FPGA at U12, then the Virtex-II FPGA at U14, then the Virtex-II FPGA at U16, and finally the Spartan II FPGA at U18.

4.4 Slave Serial Programming of On-Board EEPROM (U2)

1. Install the jumper blocks on JP1, JP2 and JP9.
2. Remove the jumper blocks from JP3.
3. Using the Parallel Cable IV Programming Adapter, connect the Slave Serial cable to the JP5 of the GVA-395 as shown in the table below.
4. Apply power to the GVA-395.
5. Press the reset button SW1.
6. LED D41 will be lited for approximately 10 seconds while the Flash Memory is being erased.
7. Wait for the LED D41 to extinguish.
8. It is necessary to use the serial cable connection for the Programming Adapter in order to use a the slower 57 Kbps serial transfer rate.
9. From the Xilinx Foundation Project Manager, select the Programming icon.
10. Select the Hardware Debugger.
11. From the Hardware Debugger, select the desire exo file to be programmed into the EEPROM. Please note that the FPGA will also be programmed as the data is being written into the EEPROM.
12. While the data is being written into the EEPROM, the LEDs D42 thru D44 will be toggling
13. When all of the LED D41 thru D44 are lite, the program function has been completed.
14. Remove power from the GVA-395 and remove the Slave Serial cable. Install that jumper blocks are install on JP3 and JP9 with the jumper block on JP2 is removed. When power is reapplied, the GVA-395 will configured from the EEPROM.

Slave Serial Signal	JP5 Connection
VCC	1
GND	2
CCLK	4
DONE	5
DIN	6
PROG	7
INIT	8

4.4.1.1 EEPROM Slave Serial Programming Configuration Table

5.0 Flash EEPROM Configuration FPGA (U1)

Normally, this FPGA will be configured by the serial prom (U3) which is programmed at the factory to perform the configurations operations described in Section 4. However, this FPGA maybe reprogrammed by installing a jumper block on JP4. The FPGA may now be reprogrammed by connecting the JTAG download cable to JP7 as follows: VCC ->1, GND->2, TDO -> 3, TDI -> 4, TCK ->5, TMS ->6. This is not recommended but it would have no adverse effects on the GVA-395 as long as the configuration pins for the other FPGAs are not used. Please refer to the schematic for additional information.

6.0 On-Board System Clock Configuration

The GVA-395 uses an 50 MHz oscillator to generate the on-board system clock. which has a SG-615 form factor such as those found in the Digi-Key catalog. The System clock is on pin AF18 for Virtex-II FPGAs and on pin 15 of the Spartan-II FPGAs. To select the on-board oscillator as the system clock connect a jumper block between pins1 and 2 of JP8

6.1 External Clock Configuration

An exterior clock source (P1) may be selected as the system clock by installing a jumper block between pins 2 and 3 of JP8. Insure that this clock source meet the TTL minimum value (V_{ih} = 2.4V and V_{il} = 0.4V) and does not exceed 7V in reference to Ground before attaching the source to P1.

7.0 Xilinx FPGA Power-On Reset and Manual Reset Push Button Switch

The power-on reset may be used for initialization purposes. There is also a manual reset push button switch (SW1) which will reactive the reset signal. It should be noted that if the +3.3V supply voltage drops below +3.00V the power-on reset will trigger.

Signal Name	ACX FPGA (U10) Pin No.	AC FPGA (U12) Pin No.	DP FPGA (U14) Pin No.	DPX FPGA (U16) Pin No.	E1 FPGA (U18) Pin No.
RESETL	AG18	AG18	AG18	AG18	18

7.1.1 Power-on Reset Interconnect Table

8.0 ACX FPGA (U10)

8.1 ACX FPGA (U10) to Daughter I/O PCB Interface.

. The data is then transferred to the Xilinx ACX FPGA (U10). The data may then be processed by the FPGA.

Signal	PC1 Pin No.	ACX FPGA Pin	Signal	PC2 Pin No.	ACX FPGA Pin
AD0_DN0	1	E1	AD1_DN0	1	M1
AD0_DP0	2	D1	AD1_DP0	2	L1
AD0_DN1	3	E2	AD1_DN1	3	M2
AD0_DP1	4	D2	AD1_DP1	4	L2
AD0_DN2	5	E3	AD1_DN2	5	M3
AD0_DP2	6	D3	AD1_DP2	6	L3
AD0_DN3	7	G1	AD1_DN3	7	L4
AD0_DP3	8	F1	AD1_DP3	8	K4
AD0_DN4	9	G2	AD1_DN4	9	P2
AD0_DP4	10	F2	AD1_DP4	10	N2
AD0_DN5	11	G3	AD1_DN5	11	N4
AD0_DP5	12	F3	AD1_DP5	12	M4
AD0_DN6	13	F4	AD1_DN6	13	P3
AD0_DP6	14	E4	AD1_DP6	14	N3
AD0_DN7	15	F5	AD1_DN7	15	P5
AD0_DP7	16	G5	AD1_DP7	16	N5
AD0_DN8	17	J1	AD1_DN8	17	N6
AD0_DP8	18	H2	AD1_DP8	18	P6
AD0_DN9	19	J3	AD1_DN9	19	T2
AD0_DP9	20	H3	AD1_DP9	20	R1
AD0_DN10	21	J4	AD1_DN10	21	T3
AD0_DP10	22	H4	AD1_DP10	22	R3
AD0_DN11	23	J5	AD1_DN11	23	R4
AD0_DP11	24	H5	AD1_DP11	24	P4
AD0_CLKN	25	U1	AD1_CLKN	25	U3
ADO_CLK	26	U2	AD1_CLK	26	V4
+3.3V	27	No. Connect	+3.3V	27	No. Connect
+3.3V	28	No. Connect	+3.3V	28	No. Connect
+5V	29	No. Connect	+5V	29	No. Connect
+5V	30	No. Connect	+5V	30	No. Connect
AD0_DN12	31	E19 (GCLKP)	AD1_DN12	31	K18 (GCLKP)
AD0_DP12	32	E18 (GCLKS)	AD1_DP12	32	J18 (GCLKS)
AD0_DN13	33	K2	AD1_DN13	33	L6
AD0_DP13	34	J2	AD1_DP13	34	M6
AD0_DN14	35	L5	AD1_DN14	35	N7
AD0_DP14	36	K5	AD1_DP14	36	M7
AD0_DN15	37	J6	AD1_DN15	37	N8
AD0_DP15	38	K6	AD1_DP15	38	P8
DGND	39	No. Connect	DGND	39	No. Connect
DGND	40	No. Connect	DGND	40	No. Connect
DGND	41	No. Connect	DGND	41	No. Connect
DGND	42	No. Connect	DGND	42	No. Connect
DGND	43	No. Connect	DGND	43	No. Connect

8.1.1.1 ACX FPGA (U10) to PC1 and PC2 Interconnection Table

Signal	PC3 Pin No.	ACX FPGA Pin	Signal	PC4 Pin No.	ACX FPGA Pin
AD2_DN0	1	AA1	AD3_DN0	1	AE2
AD2_DP0	2	AB1	AD3_DP0	2	AF1
AD2_DN1	3	AA2	AD3_DN1	3	AF2
AD2_DP1	4	AB2	AD3_DP1	4	AG2
AD2_DN2	5	AA4	AD3_DN2	5	AF3
AD2_DP2	6	AB4	AD3_DP2	6	AG3
AD2_DN3	7	AA5	AD3_DN3	7	AH1
AD2_DP3	8	AB5	AD3_DP3	8	AJ1
AD2_DN4	9	AD1	AD3_DN4	9	AH2
AD2_DP4	10	AC1	AD3_DP4	10	AJ2
AD2_DN5	11	AC2	AD3_DN5	11	AH3
AD2_DP5	12	AD2	AD3_DP5	12	AJ3
AD2_DN6	13	AC3	AD3_DN6	13	AK2
AD2_DP6	14	AD3	AD3_DP6	14	AL2
AD2_DN7	15	AC4	AD3_DN7	15	AL1
AD2_DP7	16	AD4	AD3_DP7	16	AK1
AD2_DN8	17	AB6	AD3_DN8	17	AH6
AD2_DP8	18	AC6	AD3_DP8	18	AJ5
AD2_DN9	19	AD5	AD3_DN9	19	AJ4
AD2_DP9	20	AE5	AD3_DP9	20	AK4
AD2_DN10	21	AE4	AD3_DN10	21	AF5
AD2_DP10	22	AF4	AD3_DP10	22	AG5
AD2_DN11	23	V5	AD3_DN11	23	AF6
AD2_DP11	24	W5	AD3_DP11	24	AG6
AD2_CLKN	25	V1	AD3_CLKN	25	W3
AD2_CLK	26	V2	AD3_CLK	26	Y3
+3.3V	27	No. Connect	+3.3V	27	No. Connect
+3.3V	28	No. Connect	+3.3V	28	No. Connect
+5V	29	No. Connect	+5V	29	No. Connect
+5V	30	No. Connect	+5V	30	No. Connect
AD2_DN12	31	E17 (GCLKP)	AD3_DN12	31	H17 (GCLKP)
AD2_DP12	32	E16 (GCLKS)	AD3_DP12	32	H16 (GCLKS)
AD2_DN13	33	V6	AD3_DN13	33	AG4
AD2_DP13	34	W6	AD3_DP13	34	AH5
AD2_DN14	35	V7	AD3_DN14	35	AD6
AD2_DP14	36	W7	AD3_DP14	36	AE6
AD2_DN15	37	Y7	AD3_DN15	37	AD7
AD2_DP15	38	AA8	AD3_DP15	38	AE7
DGND	39	No. Connect	DGND	39	No. Connect
DGND	40	No. Connect	DGND	40	No. Connect
DGND	41	No. Connect	DGND	41	No. Connect
DGND	42	No. Connect	DGND	42	No. Connect
DGND	43	No. Connect	DGND	43	No. Connect

8.1.1.2 ACX FPGA (U10) to PC3 and PC4 Interconnection Table

Signal	PC5 Pin No.	ACX FPGA Pin	Signal	PC6 Pin No.	ACX FPGA Pin
DA0_DN0	1	E34	DA1_DN0	1	K31
DA0_DP0	2	D34	DA1_DP0	2	K30
DA0_DN1	3	E33	DA1_DN1	3	M34
DA0_DP1	4	D33	DA1_DP1	4	L34
DA0_DN2	5	E32	DA1_DN2	5	M33
DA0_DP2	6	D32	DA1_DP2	6	L33
DA0_DN3	7	F31	DA1_DN3	7	M32
DA0_DP3	8	E31	DA1_DP3	8	L32
DA0_DN4	9	G34	DA1_DN4	9	M31
DA0_DP4	10	F34	DA1_DP4	10	L31
DA0_DN5	11	G33	DA1_DN5	11	L30
DA0_DP5	12	F33	DA1_DP5	12	K29
DA0_DN6	13	G32	DA1_DN6	13	L29
DA0_DP6	14	F32	DA1_DP6	14	M29
DA0_DN7	15	F30	DA1_DN7	15	P33
DA0_DP7	16	G30	DA1_DP7	16	N33
DA0_DN8	17	J34	DA1_DN8	17	P32
DA0_DP8	18	H33	DA1_DP8	18	N32
DA0_DN9	19	J31	DA1_DN9	19	P31
DA0_DP9	20	H31	DA1_DP9	20	N31
DA0_DN10	21	H29	DA1_DN10	21	P30
DA0_DP10	22	G29	DA1_DP10	22	N30
DA0_DN11	23	J29	DA1_DN11	23	N29
DA0_DP11	24	H28	DA1_DP11	24	P29
DA0_CLKN	25	V31	DA1_CLKN	25	U34
DA0_CLK	26	U31	DA1_CLK	26	U33
+3.3V	27	No. Connect	+3.3V	27	No. Connect
+3.3V	28	No. Connect	+3.3V	28	No. Connect
+5V	29	No. Connect	+5V	29	No. Connect
+5V	30	No. Connect	+5V	30	No. Connect
DA0_DN12	31	K33	DA1_DN12	31	R28
DA0_DP12	32	J33	DA1_DP12	32	R29
DA0_DN13	33	J32	DA1_DN13	33	U30
DA0_DP13	34	H32	DA1_DP13	34	T30
DA0_DN14	35	H30	DA1_DN14	35	T29
DA0_DP14	36	J30	DA1_DP14	36	U29
DA0_DN15	37	L28	DA1_DN15	37	U28
DA0_DP15	38	K28	DA1_DP15	38	T28
DGND	39	No. Connect	DGND	39	No. Connect
DGND	40	No. Connect	DGND	40	No. Connect
DGND	41	No. Connect	DGND	41	No. Connect
DGND	42	No. Connect	DGND	42	No. Connect
DGND	43	No. Connect	DGND	43	No. Connect

8.1.1.3 ACX FPGA (U10) to PC6 and PC7 Interconnection Table

Signal	PC8 Pin No.	ACX FPGA Pin	Signal	PC9 Pin No.	ACX FPGA Pin
DA2_DN0	1	V34	DA3_DN0	1	AD26
DA2_DP0	2	V33	DA3_DP0	2	AE26
DA2_DN1	3	V27	DA3_DN1	3	AD28
DA2_DP1	4	V26	DA3_DP1	4	AE28
DA2_DN2	5	V28	DA3_DN2	5	AE25
DA2_DP2	6	W28	DA3_DP2	6	AF25
DA2_DN3	7	W31	DA3_DN3	7	AE27
DA2_DP3	8	Y31	DA3_DP3	8	AF27
DA2_DN4	9	Y29	DA3_DN4	9	AE29
DA2_DP4	10	Y28	DA3_DP4	10	AF29
DA2_DN5	11	W27	DA3_DN5	11	AF26
DA2_DP5	12	Y27	DA3_DP5	12	AG26
DA2_DN6	13	AB30	DA3_DN6	13	AF28
DA2_DP6	14	AA30	DA3_DP6	14	AG28
DA2_DN7	15	AA33	DA3_DN7	15	AF30
DA2_DP7	16	AB33	DA3_DP7	16	AG30
DA2_DN8	17	AA31	DA3_DN8	17	AG31
DA2_DP8	18	AB31	DA3_DP8	18	AF31
DA2_DN9	19	AA29	DA3_DN9	19	AG32
DA2_DP9	20	AB29	DA3_DP9	20	AF32
DA2_DN10	21	AB32	DA3_DN10	21	AG29
DA2_DP10	22	AC32	DA3_DP10	22	AH29
DA2_DN11	23	AD31	DA3_DN11	23	AH32
DA2_DP11	24	AC31	DA3_DP11	24	AJ32
DA2_CLKN	25	W32	DA3_CLKN	25	V30
DA2_CLK	26	V32	DA3_CLK	26	W30
+3.3V	27	No. Connect	+3.3V	27	No. Connect
+3.3V	28	No. Connect	+3.3V	28	No. Connect
+5V	29	No. Connect	+5V	29	No. Connect
+5V	30	No. Connect	+5V	30	No. Connect
DA2_DN12	31	AC34	DA3_DN12	31	AK31
DA2_DP12	32	AD34	DA3_DP12	32	AJ31
DA2_DN13	33	AC33	DA3_DN13	33	AK32
DA2_DP13	34	AD33	DA3_DP13	34	AL32
DA2_DN14	35	Y26	DA3_DN14	35	AK33
DA2_DP14	36	AA26	DA3_DP14	36	AL33
DA2_DN15	37	Y25	DA3_DN15	37	AK34
DA2_DP15	38	AA25	DA3_DP15	38	AL34
DGND	39	No. Connect	DGND	39	No. Connect
DGND	40	No. Connect	DGND	40	No. Connect
DGND	41	No. Connect	DGND	41	No. Connect
DGND	42	No. Connect	DGND	42	No. Connect
DGND	43	No. Connect	DGND	43	No. Connect

8.1.1.4 ACX FPGA (U10) to PC8 and PC9 Interconnection Table

8.2 ACX FPGA HP Logic Analyzer Mictor Connector

Signal	HC1 Pin No.	ACX FPGA Pin No.
No Connection	1	
No Connection	2	
No Connection	3	
No Connection	4	
HP0_SIG0	5	C7
HP0_SIG1	6	C8
HP0_SIG2	7	C13
HP0_SIG3	8	C14
HP0_SIG4	9	C16
HP0_SIG5	10	C15
HP0_SIG6	11	D9
HP0_SIG7	12	C9
HP0_SIG8	13	C11
HP0_SIG9	14	C12
HP0_SIG10	15	D12
HP0_SIG11	16	D13
HP0_SIG12	17	D10
HP0_SIG13	18	D11
HP0_SIG14	19	E8
HP0_SIG15	20	E9
HP0_SIG16	21	E13
HP0_SIG17	22	E14
HP0_SIG18	23	F14
HP0_SIG19	24	F13
HP0_SIG20	25	G12
HP0_SIG21	26	G13
HP0_SIG22	27	F15
HP0_SIG23	28	G15
HP0_SIG24	29	G16
HP0_SIG25	30	G17
HP0_SIG26	31	F16
HP0_SIG27	32	F17
HP0_SIG28	33	E11
HP0_SIG29	34	E10
HP0_SIG30	35	F10
HP0_SIG31	36	G9
HP0_SIG32	37	G10
HP0_SIG33	38	G11
DGND	39	No Connection
DGND	40	No Connection
DGND	41	No Connection
DGND	42	No Connection
DGND	43	No Connection

8.2.1.1 ACX FPGA (U10) to HC1 Interconnection Table

8.3 ACX FPGA 256K X 16 ZBT RAM

Each Virtex-II FPGA has access to a 256K x 18 ZBT RAM. The access time for each Static RAM is 7.5 nanoseconds. Refer to the data sheet for the IDT71V3558 for more detailed information. The interconnection is shown in the table below.

Description	Signal	Pin No.	Description	Signal	Pin No.
Address Bit 0	ZBT0_A0	A31	Data Bit 0	ZBT0_D0	A12
Address Bit 1	ZBT0_A1	A30	Data Bit 1	ZBT0_D1	A11
Address Bit 2	ZBT0_A2	A28	Data Bit 2	ZBT0_D2	A9
Address Bit 3	ZBT0_A3	A29	Data Bit 3	ZBT0_D3	A7
Address Bit 4	ZBT0_A4	A26	Data Bit 4	ZBT0_D4	A6
Address Bit 5	ZBT0_A5	A24	Data Bit 5	ZBT0_D5	A5
Address Bit 6	ZBT0_A6	A23	Data Bit 6	ZBT0_D6	A4
Address Bit 7	ZBT0_A7	B32	Data Bit 7	ZBT0_D7	B12
Address Bit 8	ZBT0_A8	B31	Data Bit 8	ZBT0_D8	B11
Address Bit 9	ZBT0_A9	B30	Data Bit 9	ZBT0_D9	B10
Address Bit 10	ZBT0_A10	B28	Data Bit 10	ZBT0_D10	B9
Address Bit 11	ZBT0_A11	B29	Data Bit 11	ZBT0_D11	B8
Address Bit 12	ZBT0_A12	B27	Data Bit 12	ZBT0_D12	B7
Address Bit 13	ZBT0_A13	B24	Data Bit 13	ZBT0_D13	B6
Address Bit 14	ZBT0_A14	B23	Data Bit 14	ZBT0_D14	B5
Address Bit 15	ZBT0_A15	B22	Data Bit 15	ZBT0_D15	B4
Address Bit 16	ZBT0_A16	B21	Data Bit 16	ZBT0_D16	B3
Address Bit 17	ZBT0_A17	C33	Data Bit 17	ZBT0_D17	C2
Address Bit 18	ZBT0_A18	C28	RAM ReDA / Write	ZBT0_RW	B13
Address Bit 19	ZBT0_A19	C27	RAM Byte Write Enable 1	ZBT0_BW1	D18
RAM Clock	ZBT0_CLK	B14	RAM Byte Write Enable 2	ZBT0_BW2	D19
RAM Clock Enable	ZBT0_CEN	C19	RAM Linear Burst Order	ZBT0_LBO	D6
RAM Chip Enable	ZBT0_CE	C18	RAM Internal Register LoDA	ZBT0_ALD	D8
			RAM Output Enable	ZBT0_OE	C6

8.3.1 ACX FPGA (U10) ZBT RAM Pin Configuration Table

8.4 ACX FPGA LED Configuration.

The each Virtex-II FPGA has 10 amber LEDs for general purpose use.

Signal	LED	ACX FPGA Pin No.
ACXLED0	D1	K21
ACXLED1	D2	K20
ACXLED2	D3	C22
ACXLED3	D4	C23
ACXLED4	D5	E21
ACXLED5	D6	E22
ACXLED6	D7	H21
ACXLED7	D8	H20
ACXLED8	D9	G20
ACXLED9	D10	F20

8.4.1 ACX FPGA (U10) LED Configuration Table

8.5 ACX FPGA- AC FPGA XBUS Configuration.

Signal	ACX Pin No.	AC Pin No.	Signal	ACX Pin No.	AC Pin No.
XBUS0	AH11	AH11	XBUS50	AL12	AL12
XBUS1	AL6	AL6	XBUS51	AF14	AF14
XBUS2	AM6	AM6	XBUS52	AF15	AF15
XBUS3	AK6	AK6	XBUS53	AM13	AM13
XBUS4	AJ8	AJ8	XBUS54	AM12	AM12
XBUS5	AM8	AM8	XBUS55	AP12	AP12
XBUS6	AM7	AM7	XBUS56	AP11	AP11
XBUS7	AN3	AN3	XBUS57	AG15	AG15
XBUS8	AM2	AM2	XBUS58	AG16	AG16
XBUS9	AJ10	AJ10	XBUS59	AN14	AN14
XBUS10	AJ9	AJ9	XBUS60	AN13	AN13
XBUS11	AH9	AH9	XBUS61	AP14	AP14
XBUS12	AH10	AH10	XBUS62	AP13	AP13
XBUS13	AN5	AN5	XBUS63	AD16	AD16
XBUS14	AN4	AN4	XBUS64	AD17	AD17
XBUS15	AE12	AE12	XBUS65	AK14	AK14
XBUS16	AE13	AE13	XBUS66	AK13	AK13
XBUS17	AM9	AM9	XBUS67	AL16	AL16
XBUS18	AL8	AL8	XBUS68	AL17	AL17
XBUS19	AP5	AP5	XBUS69	AJ17	AJ17
XBUS20	AP4	AP4	XBUS70	AJ16	AJ16
XBUS21	AG11	AG11	XBUS71	AM15	AM15
XBUS22	AG12	AG12	XBUS72	AM14	AM14
XBUS23	AN7	AN7	XBUS73	AM16	AM16
XBUS24	AN6	AN6	XBUS74	AM17	AM17
XBUS25	AL10	AL10	XBUS75	AF17	AF17
XBUS26	AL9	AL9	XBUS76	AG17	AG17
XBUS27	AF12	AF12	XBUS77	AK16	AK16
XBUS28	AF13	AF13	XBUS78	AK17	AK17
XBUS29	AK10	AK10	XBUS79	AL30	AL30
XBUS30	AK11	AK11	XBUS80	AM31	AM31
XBUS31	AP7	AP7	XBUS81	AG24	AG24
XBUS32	AP6	AP6	XBUS82	AG25	AG25
XBUS33	AH13	AH13	XBUS83	AK28	AK28
XBUS34	AH12	AH12	XBUS84	AL29	AL29
XBUS35	AJ11	AJ11	XBUS85	AM28	AM28
XBUS36	AJ12	AJ12	XBUS86	AM29	AM29
XBUS37	AP9	AP9	XBUS87	AJ27	AJ27
XBUS38	AN8	AN8	XBUS88	AJ26	AJ26
XBUS39	AG13	AG13	XBUS89	AM33	AM33
XBUS40	AG14	AG14	XBUS90	AN32	AN32
XBUS41	AM11	AM11	XBUS91	AG23	AG23
XBUS42	AL11	AL11	XBUS92	AF24	AF24
XBUS43	AN12	AN12	XBUS93	AK26	AK26
XBUS44	AN11	AN11	XBUS94	AK27	AK27
XBUS45	AE14	AE14	XBUS95	AN31	AN31
XBUS46	AE15	AE15	XBUS96	AN30	AN30
XBUS47	AJ13	AJ13	XBUS97	AH26	AH26
XBUS48	AJ14	AJ14	XBUS98	AJ25	AJ25
XBUS49	AL13	AL13	XBUS99	AL27	AL27

8.5.1 ACX FPGA (U10) to AC FPGA (U12) XBUS Configuration Table

9.0 AC FPGA (U12)

9.1 AC FPGA (U12) to Daughter I/O PCB Interface.

. The data is then transferred to the Xilinx AC FPGA (U12). The data may then be processed by the FPGA.

Signal	PC9 Pin No.	AC FPGA Pin	Signal	PC10 Pin No.	AC FPGA Pin
AD4_DN0	1	M1	DA4_DN0	1	K31
AD4_DP0	2	L1	DA4_DP0	2	K30
AD4_DN1	3	M2	DA4_DN1	3	M34
AD4_DP1	4	L2	DA4_DP1	4	L34
AD4_DN2	5	M3	DA4_DN2	5	M33
AD4_DP2	6	L3	DA4_DP2	6	L33
AD4_DN3	7	L4	DA4_DN3	7	M32
AD4_DP3	8	K4	DA4_DP3	8	L32
AD4_DN4	9	P2	DA4_DN4	9	M31
AD4_DP4	10	N2	DA4_DP4	10	L31
AD4_DN5	11	N4	DA4_DN5	11	L30
AD4_DP5	12	M4	DA4_DP5	12	K29
AD4_DN6	13	P3	DA4_DN6	13	L29
AD4_DP6	14	N3	DA4_DP6	14	M29
AD4_DN7	15	P5	DA4_DN7	15	P33
AD4_DP7	16	N5	DA4_DP7	16	N33
AD4_DN8	17	N6	DA4_DN8	17	P32
AD4_DP8	18	P6	DA4_DP8	18	N32
AD4_DN9	19	T2	DA4_DN9	19	P31
AD4_DP9	20	R1	DA4_DP9	20	N31
AD4_DN10	21	T3	DA4_DN10	21	P30
AD4_DP10	22	R3	DA4_DP10	22	N30
AD4_DN11	23	R4	DA4_DN11	23	N29
AD4_DP11	24	P4	DA4_DP11	24	P29
AD4_CLKN	25	U3	DA4_CLKN	25	U34
AD4_CLK	26	V4	DA4_CLK	26	U33
+3.3V	27	No. Connect	+3.3V	27	No. Connect
+3.3V	28	No. Connect	+3.3V	28	No. Connect
+5V	29	No. Connect	+5V	29	No. Connect
+5V	30	No. Connect	+5V	30	No. Connect
AD4_DN12	31	K18 (GCLKP)	DA4_DN12	31	R28
AD4_DP12	32	J18 (GCLKS)	DA4_DP12	32	R29
AD4_DN13	33	L6	DA4_DN13	33	U30
AD4_DP13	34	M6	DA4_DP13	34	T30
AD4_DN14	35	N7	DA4_DN14	35	T29
AD4_DP14	36	M7	DA4_DP14	36	U29
AD4_DN15	37	N8	DA4_DN15	37	U28
AD4_DP15	38	P8	DA4_DP15	38	T28
DGND	39	No. Connect	DGND	39	No. Connect
DGND	40	No. Connect	DGND	40	No. Connect
DGND	41	No. Connect	DGND	41	No. Connect
DGND	42	No. Connect	DGND	42	No. Connect
DGND	43	No. Connect	DGND	43	No. Connect

9.1.1.1 AC FPGA (U12) to PC9 and PC10 Interconnection Table

9.2 AC FPGA HP Logic Analyzer Mictor Connector

Signal	HC1 Pin No.	AC FPGA Pin No.
No Connection	1	
No Connection	2	
No Connection	3	
No Connection	4	
HP1_SIG0	5	C7
HP1_SIG1	6	C8
HP1_SIG2	7	C13
HP1_SIG3	8	C14
HP1_SIG4	9	C16
HP1_SIG5	10	C15
HP1_SIG6	11	D9
HP1_SIG7	12	C9
HP1_SIG8	13	C11
HP1_SIG9	14	C12
HP1_SIG10	15	D12
HP1_SIG11	16	D13
HP1_SIG12	17	D10
HP1_SIG13	18	D11
HP1_SIG14	19	E8
HP1_SIG15	20	E9
HP1_SIG16	21	E13
HP1_SIG17	22	E14
HP1_SIG18	23	F14
HP1_SIG19	24	F13
HP1_SIG20	25	G12
HP1_SIG21	26	G13
HP1_SIG22	27	F15
HP1_SIG23	28	G15
HP1_SIG24	29	G16
HP1_SIG25	30	G17
HP1_SIG26	31	F16
HP1_SIG27	32	F17
HP1_SIG28	33	E11
HP1_SIG29	34	E10
HP1_SIG30	35	F10
HP1_SIG31	36	G9
HP1_SIG32	37	G10
HP1_SIG33	38	G11
DGND	39	No Connection
DGND	40	No Connection
DGND	41	No Connection
DGND	42	No Connection
DGND	43	No Connection

9.2.1.1 AC FPGA (U12) to HC1 Interconnection Table

9.3 AC FPGA 256K X 16 ZBT RAM

Each Virtex-II FPGA has access to a 256K x 18 ZBT RAM. The access time for each Static RAM is 7.5 nanoseconds. Refer to the data sheet for the IDT71V3558 for more detailed information. The interconnection is shown in the table below.

Description	Signal	Pin No.	Description	Signal	Pin No.
Address Bit 0	ZBT1_A0	A31	Data Bit 0	ZBT1_D0	A12
Address Bit 1	ZBT1_A1	A30	Data Bit 1	ZBT1_D1	A11
Address Bit 2	ZBT1_A2	A28	Data Bit 2	ZBT1_D2	A9
Address Bit 3	ZBT1_A3	A29	Data Bit 3	ZBT1_D3	A7
Address Bit 4	ZBT1_A4	A26	Data Bit 4	ZBT1_D4	A6
Address Bit 5	ZBT1_A5	A24	Data Bit 5	ZBT1_D5	A5
Address Bit 6	ZBT1_A6	A23	Data Bit 6	ZBT1_D6	A4
Address Bit 7	ZBT1_A7	B32	Data Bit 7	ZBT1_D7	B12
Address Bit 8	ZBT1_A8	B31	Data Bit 8	ZBT1_D8	B11
Address Bit 9	ZBT1_A9	B30	Data Bit 9	ZBT1_D9	B10
Address Bit 10	ZBT1_A10	B28	Data Bit 10	ZBT1_D10	B9
Address Bit 11	ZBT1_A11	B29	Data Bit 11	ZBT1_D11	B8
Address Bit 12	ZBT1_A12	B27	Data Bit 12	ZBT1_D12	B7
Address Bit 13	ZBT1_A13	B24	Data Bit 13	ZBT1_D13	B6
Address Bit 14	ZBT1_A14	B23	Data Bit 14	ZBT1_D14	B5
Address Bit 15	ZBT1_A15	B22	Data Bit 15	ZBT1_D15	B4
Address Bit 16	ZBT1_A16	B21	Data Bit 16	ZBT1_D16	B3
Address Bit 17	ZBT1_A17	C33	Data Bit 17	ZBT1_D17	C2
Address Bit 18	ZBT1_A18	C28	RAM ReDA / Write	ZBT1_RW	B13
Address Bit 19	ZBT1_A19	C27	RAM Byte Write Enable 1	ZBT1_BW1	D18
RAM Clock	ZBT1_CLK	B14	RAM Byte Write Enable 2	ZBT1_BW2	D19
RAM Clock Enable	ZBT1_CEN	C19	RAM Linear Burst Order	ZBT1_LBO	D6
RAM Chip Enable	ZBT1_CE	C18	RAM Internal Register LoDA	ZBT1_ALD	D8
			RAM Output Enable	ZBT1_OE	C6

9.3.1 AC FPGA (U12) ZBT RAM Pin Configuration Table

9.4 AC FPGA LED Configuration.

The each Virtex-II FPGA has 10 amber LEDs for general purpose use.

Signal	LED	AC FPGA Pin No.
ACLED0	D11	K21
ACLED1	D12	K20
ACLED2	D13	C22
ACLED3	D14	C23
ACLED4	D15	E21
ACLED5	D16	E22
ACLED6	D17	H21
ACLED7	D18	H20
ACLED8	D19	G20
ACLED9	D20	F20

9.4.1 AC FPGA (U12) LED Configuration Table

9.5 AC FPGA - DP FPGA XBUS_A Configuration.

Signal	AC Pin No.	DP Pin No.	Signal	AC Pin No.	DP Pin No.
XBUS_A0	AD25	E2	XBUS_A50	AG33	L6
XBUS_A1	AE24	D2	XBUS_A51	AF33	M6
XBUS_A2	AK32	F5	XBUS_A52	AB28	M3
XBUS_A3	AL32	G5	XBUS_A53	AC28	L3
XBUS_A4	AE25	E3	XBUS_A54	AE33	L4
XBUS_A5	AF25	D3	XBUS_A55	AF34	K4
XBUS_A6	AK31	J9	XBUS_A56	AA27	N4
XBUS_A7	AJ31	K9	XBUS_A57	AB27	M4
XBUS_A8	AG29	F4	XBUS_A58	Y25	M2
XBUS_A9	AH29	E4	XBUS_A59	AA25	L2
XBUS_A10	AF26	E1	XBUS_A60	AC33	N8
XBUS_A11	AG26	D1	XBUS_A61	AD33	P8
XBUS_A12	AK33	J8	XBUS_A62	AB32	N6
XBUS_A13	AL33	K8	XBUS_A63	AC32	P6
XBUS_A14	AH32	H7	XBUS_A64	Y26	P5
XBUS_A15	AJ32	J7	XBUS_A65	AA26	N5
XBUS_A16	AF28	H6	XBUS_A66	AC34	P10
XBUS_A17	AG28	G6	XBUS_A67	AD34	R10
XBUS_A18	AF30	L10	XBUS_A68	AD31	P3
XBUS_A19	AG30	L9	XBUS_A69	AC31	N3
XBUS_A20	AE29	G3	XBUS_A70	W27	M1
XBUS_A21	AF29	F3	XBUS_A71	Y27	L1
XBUS_A22	AE27	G2	XBUS_A72	AA29	P9
XBUS_A23	AF27	F2	XBUS_A73	AB29	R9
XBUS_A24	AK34	M10	XBUS_A74	AA31	P2
XBUS_A25	AL34	N10	XBUS_A75	AB31	N2
XBUS_A26	AD28	J6	XBUS_A76	Y29	R4
XBUS_A27	AE28	K6	XBUS_A77	Y28	P4
XBUS_A28	AD26	J5	XBUS_A78	AA33	R8
XBUS_A29	AE26	H5	XBUS_A79	AB33	T8
XBUS_A30	AG31	L7	XBUS_A80	AB30	T3
XBUS_A31	AF31	K7	XBUS_A81	AA30	R3
XBUS_A32	AG32	J4	XBUS_A82	V28	T2
XBUS_A33	AF32	H4	XBUS_A83	W28	R1
XBUS_A34	AB25	G1	XBUS_A84	V34	U7
XBUS_A35	AC25	F1	XBUS_A85	V33	T7
XBUS_A36	AH33	L8	XBUS_A86	W31	T6
XBUS_A37	AJ33	M8	XBUS_A87	Y31	U6
XBUS_A38	AD32	J1	XBUS_A88	V27	U1
XBUS_A39	AE31	H2	XBUS_A89	V26	U2
XBUS_A40	AC27	J3	XBUS_A90	V30	U9
XBUS_A41	AD27	H3	XBUS_A91	W30	U8
XBUS_A42	AH34	M9	XBUS_A92	W32	U3
XBUS_A43	AJ34	N9	XBUS_A93	V32	V4
XBUS_A44	AD30	L5	XBUS_A94	H32	AC9
XBUS_A45	AE30	K5	XBUS_A95	J32	AB9
XBUS_A46	AB26	K2	XBUS_A96	N26	AF1
XBUS_A47	AC26	J2	XBUS_A97	M26	AE2
XBUS_A48	AC29	N7	XBUS_A98	J33	AE6
XBUS_A49	AD29	M7	XBUS_A99	K33	AD6

9.5.1 AC FPGA (U12) to DP FPGA (U14) XBUS_A Configuration Table

10.0 DP FPGA (U14)

10.1 DP FPGA (U14) to Daughter I/O PCB Interface.

. The data is then transferred to the Xilinx DP FPGA (U14). The data may then be processed by the FPGA.

Signal	PC11 Pin No.	DP FPGA Pin	Signal	PC12 Pin No.	DP FPGA Pin
AD5_DN0	1	F31	DA5_DN0	1	K31
AD5_DP0	2	E31	DA5_DP0	2	K30
AD5_DN1	3	G32	DA5_DN1	3	M34
AD5_DP1	4	F32	DA5_DP1	4	L34
AD5_DN2	5	K33	DA5_DN2	5	M33
AD5_DP2	6	J33	DA5_DP2	6	L33
AD5_DN3	7	L27	DA5_DN3	7	M32
AD5_DP3	8	M27	DA5_DP3	8	L32
AD5_DN4	9	E32	DA5_DN4	9	M31
AD5_DP4	10	D32	DA5_DP4	10	L31
AD5_DN5	11	J31	DA5_DN5	11	L30
AD5_DP5	12	H31	DA5_DP5	12	K29
AD5_DN6	13	J29	DA5_DN6	13	N28
AD5_DP6	14	H28	DA5_DP6	14	M28
AD5_DN7	15	L28	DA5_DN7	15	P32
AD5_DP7	16	K28	DA5_DP7	16	N32
AD5_DN8	17	G34	DA5_DN8	17	U30
AD5_DP8	18	F34	DA5_DP8	18	T30
AD5_DN9	19	J26	DA5_DN9	19	P31
AD5_DP9	20	K27	DA5_DP9	20	N31
AD5_DN10	21	E34	DA5_DN10	21	P30
AD5_DP10	22	D34	DA5_DP10	22	N30
AD5_DN11	23	G33	DA5_DN11	23	N27
AD5_DP11	24	F33	DA5_DP11	24	P27
AD5_CLKN	25	E33	DA5_CLKN	25	U28
AD5_CLK	26	D33	DA5_CLK	26	T28
+3.3V	27	No. Connect	+3.3V	27	No. Connect
+3.3V	28	No. Connect	+3.3V	28	No. Connect
+5V	29	No. Connect	+5V	29	No. Connect
+5V	30	No. Connect	+5V	30	No. Connect
AD5_DN12	31	M25	DA5_DN12	31	P33
AD5_DP12	32	N25	DA5_DP12	32	N33
AD5_DN13	33	M26	DA5_DN13	33	U26
AD5_DP13	34	N26	DA5_DP13	34	U27
AD5_DN14	35	J32	DA5_DN14	35	U34
AD5_DP14	36	H32	DA5_DP14	36	U33
AD5_DN15	37	H29	DA5_DN15	37	V31
AD5_DP15	38	G29	DA5_DP15	38	U31
DGND	39	No. Connect	DGND	39	No. Connect
DGND	40	No. Connect	DGND	40	No. Connect
DGND	41	No. Connect	DGND	41	No. Connect
DGND	42	No. Connect	DGND	42	No. Connect
DGND	43	No. Connect	DGND	43	No. Connect

10.1.1.1 DP FPGA (U14) to PC11 and PC12 Interconnection Table

10.2 DP FPGA HP Logic Analyzer Mictor Connector

Signal	HC1 Pin No.	DP FPGA Pin No.
No Connection	1	
No Connection	2	
No Connection	3	
No Connection	4	
HP2_SIG0	5	C7
HP2_SIG1	6	C8
HP2_SIG2	7	C13
HP2_SIG3	8	C14
HP2_SIG4	9	C16
HP2_SIG5	10	C15
HP2_SIG6	11	D9
HP2_SIG7	12	C9
HP2_SIG8	13	C11
HP2_SIG9	14	C12
HP2_SIG10	15	D12
HP2_SIG11	16	D13
HP2_SIG12	17	D10
HP2_SIG13	18	D11
HP2_SIG14	19	E8
HP2_SIG15	20	E9
HP2_SIG16	21	E13
HP2_SIG17	22	E14
HP2_SIG18	23	F14
HP2_SIG19	24	F13
HP2_SIG20	25	G12
HP2_SIG21	26	G13
HP2_SIG22	27	F15
HP2_SIG23	28	G15
HP2_SIG24	29	G16
HP2_SIG25	30	G17
HP2_SIG26	31	F16
HP2_SIG27	32	F17
HP2_SIG28	33	E11
HP2_SIG29	34	E10
HP2_SIG30	35	F10
HP2_SIG31	36	G9
HP2_SIG32	37	G10
HP2_SIG33	38	G11
DGND	39	No Connection
DGND	40	No Connection
DGND	41	No Connection
DGND	42	No Connection
DGND	43	No Connection

10.2.1.1 DP FPGA (U14) to HC2 Interconnection Table

10.3 DP FPGA 1M X 16 ZBT RAM

EDPh Virtex-II FPGA has Access to a 1M x 18 ZBT RAM. The Access time for DP Static RAM is 10 nanoseconds. Refer to the data sheet for the IDT71T75802 for more detailed information. The interconnection is shown in the table below.

Description	Signal	Pin No.	Description	Signal	Pin No.
Address Bit 0	ZBT2_A0	A31	Data Bit 0	ZBT2_D0	A12
Address Bit 1	ZBT2_A1	A30	Data Bit 1	ZBT2_D1	A11
Address Bit 2	ZBT2_A2	A28	Data Bit 2	ZBT2_D2	A9
Address Bit 3	ZBT2_A3	A29	Data Bit 3	ZBT2_D3	A7
Address Bit 4	ZBT2_A4	A26	Data Bit 4	ZBT2_D4	A6
Address Bit 5	ZBT2_A5	A24	Data Bit 5	ZBT2_D5	A5
Address Bit 6	ZBT2_A6	A23	Data Bit 6	ZBT2_D6	A4
Address Bit 7	ZBT2_A7	B32	Data Bit 7	ZBT2_D7	B12
Address Bit 8	ZBT2_A8	B31	Data Bit 8	ZBT2_D8	B11
Address Bit 9	ZBT2_A9	B30	Data Bit 9	ZBT2_D9	B10
Address Bit 10	ZBT2_A10	B28	Data Bit 10	ZBT2_D10	B9
Address Bit 11	ZBT2_A11	B29	Data Bit 11	ZBT2_D11	B8
Address Bit 12	ZBT2_A12	B27	Data Bit 12	ZBT2_D12	B7
Address Bit 13	ZBT2_A13	B24	Data Bit 13	ZBT2_D13	B6
Address Bit 14	ZBT2_A14	B23	Data Bit 14	ZBT2_D14	B5
Address Bit 15	ZBT2_A15	B22	Data Bit 15	ZBT2_D15	B4
Address Bit 16	ZBT2_A16	B21	Data Bit 16	ZBT2_D16	B3
Address Bit 17	ZBT2_A17	C33	Data Bit 17	ZBT2_D17	C2
Address Bit 18	ZBT2_A18	C28	RAM ReDA / Write	ZBT2_RW	B13
Address Bit 19	ZBT2_A19	C27	RAM Byte Write Enable 1	ZBT2_BW1	D18
RAM Clock	ZBT2_CLK	B14	RAM Byte Write Enable 2	ZBT2_BW2	D19
RAM Clock Enable	ZBT2_CEN	C19	RAM Linear Burst Order	ZBT2_LBO	D6
RAM Chip Enable	ZBT2_CE	C18	RAM Internal Register LoDA	ZBT2_ALD	D8
			RAM Output Enable	ZBT2_OE	C6

10.3.1 DP FPGA (U14) ZBT RAM Pin Configuration Table

10.4 DP FPGA LED Configuration.

The DP Virtex-II FPGA has 10 amber LEDs for general purpose use.

Signal	LED	DP FPGA Pin No.
DPLED0	D21	K21
DPLED1	D22	K20
DPLED2	D23	C22
DPLED3	D24	C23
DPLED4	D25	E21
DPLED5	D26	E22
DPLED6	D27	H21
DPLED7	D28	H20
DPLED8	D29	G20
DPLED9	D30	F20

10.4.1 DP FPGA (U14) LED Configuration Table

10.5 DP USB Interface

The Cypress CY7C68001 USB Controller (U19) is connected to both Virtex-II FPGAs (U14). An software and firmware interface design is available. The link to the design on our web site is (http://www.gvassociates.com/software.asp?prod=12). Additional documentation is also available.

Signal Name	Signal Description	DP FPGA (U14) Pin No.
USB0_SLRD	read strobe for the slave FIFOs connected to FDI[15..0]	AK34
USB0_SLWR	write strobe for the slave FIFOs connected to FDI[15..0]	AF27
USB0_SLOE	output enable for the slave FIFOs connected to FD[15..0]	AG28
USB0_READY	ready that gates external command reads andwrites. Active High.	
USB0_INT	external interrupt signal. Active Low.	
USB0_FIFOADR2	address bus select for the slave FIFOs connected to FD[15..0]	AF30
USB0_FIFOADR1	address bus select for the slave FIFOs connected to FD[15..0]	AG30
USB0_FIFOADR0	address bus select for the slave FIFOs connected to FD[15..0]	AE29
USB0_PKTEND	packet end signal for the slave FIFOs connected to FD[15..0]	AF29
USB0_CS#	master chip select (active low)	AE27
USB0_FD15	Bidirectional FIFO/Command Data Bit 15	AG31
USB0_FD14	Bidirectional FIFO/Command Data Bit 14	AF31
USB0_FD13	Bidirectional FIFO/Command Data Bit 13	AG32
USB0_FD12	Bidirectional FIFO/Command Data Bit 12	AF32
USB0_FD11	Bidirectional FIFO/Command Data Bit 11	AB25
USB0_FD10	Bidirectional FIFO/Command Data Bit 10	AC25
USB0_FD9	Bidirectional FIFO/Command Data Bit 9	AH33
USB0_FD8	Bidirectional FIFO/Command Data Bit 8	AJ33
USB0_FD7	Bidirectional FIFO/Command Data Bit 7	AD32
USB0_FD6	Bidirectional FIFO/Command Data Bit 6	AE31
USB0_FD5	Bidirectional FIFO/Command Data Bit 5	AC27
USB0_FD4	Bidirectional FIFO/Command Data Bit 4	AD27
USB0_FD3	Bidirectional FIFO/Command Data Bit 3	AH34
USB0_FD2	Bidirectional FIFO/Command Data Bit 2	AJ34
USB0_FD1	Bidirectional FIFO/Command Data Bit 1	AD30
USB0_FD0	Bidirectional FIFO/Command Data Bit 0	AE30
USB0_FLAGA	a programmable slave-FIFO output status flag signal. Defaults to PRGFLAG for the FIFO selected by the FIFOADR[1:0] pins	AE26
USB0_FLAGB	a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[2:0] pins.	AD26
USB0_FLAGC	a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[2:0] pins.	AE28

10.5.1 USB Interface for DP FPGA Interconnection Table

10.6 DP FPGA - DPX FPGA XBUS_B Configuration.

Signal	DP Pin No.	DPX Pin No.	Signal	DP Pin No.	DPX Pin No.
XBUS_B0	AH11	AH11	XBUS_B50	AL12	AL12
XBUS_B1	AL6	AL6	XBUS_B51	AF14	AF14
XBUS_B2	AM6	AM6	XBUS_B52	AF15	AF15
XBUS_B3	AK9	AK9	XBUS_B53	AM13	AM13
XBUS_B4	AJ8	AJ8	XBUS_B54	AM12	AM12
XBUS_B5	AM8	AM8	XBUS_B55	AP12	AP12
XBUS_B6	AM7	AM7	XBUS_B56	AP11	AP11
XBUS_B7	AN3	AN3	XBUS_B57	AG15	AG15
XBUS_B8	AM2	AM2	XBUS_B58	AG16	AG16
XBUS_B9	AJ10	AJ10	XBUS_B59	AN14	AN14
XBUS_B10	AJ9	AJ9	XBUS_B60	AN13	AN13
XBUS_B11	AH9	AH9	XBUS_B61	AP14	AP14
XBUS_B12	AH10	AH10	XBUS_B62	AP13	AP13
XBUS_B13	AN5	AN5	XBUS_B63	AD16	AD16
XBUS_B14	AN4	AN4	XBUS_B64	AD17	AD17
XBUS_B15	AE12	AE12	XBUS_B65	AK14	AK14
XBUS_B16	AE13	AE13	XBUS_B66	AK13	AK13
XBUS_B17	AM9	AM9	XBUS_B67	AL16	AL16
XBUS_B18	AL8	AL8	XBUS_B68	AL17	AL17
XBUS_B19	AP5	AP5	XBUS_B69	AJ17	AJ17
XBUS_B20	AP4	AP4	XBUS_B70	AJ16	AJ16
XBUS_B21	AG11	AG11	XBUS_B71	AM15	AM15
XBUS_B22	AG12	AG12	XBUS_B72	AM14	AM14
XBUS_B23	AN7	AN7	XBUS_B73	AM16	AM16
XBUS_B24	AN6	AN6	XBUS_B74	AM17	AM17
XBUS_B25	AL10	AL10	XBUS_B75	AF17	AF17
XBUS_B26	AL9	AL9	XBUS_B76	AG17	AG17
XBUS_B27	AF12	AF12	XBUS_B77	AK16	AK16
XBUS_B28	AF13	AF13	XBUS_B78	AK17	AK17
XBUS_B29	AK10	AK10	XBUS_B79	AL30	AL30
XBUS_B30	AK11	AK11	XBUS_B80	AM31	AM31
XBUS_B31	AP7	AP7	XBUS_B81	AG24	AG24
XBUS_B32	AP6	AP6	XBUS_B82	AG25	AG25
XBUS_B33	AH13	AH13	XBUS_B83	AK28	AK28
XBUS_B34	AH12	AH12	XBUS_B84	AL29	AL29
XBUS_B35	AJ11	AJ11	XBUS_B85	AM28	AM28
XBUS_B36	AJ12	AJ12	XBUS_B86	AM29	AM29
XBUS_B37	AP9	AP9	XBUS_B87	AJ27	AJ27
XBUS_B38	AN8	AN8	XBUS_B88	AJ26	AJ26
XBUS_B39	AG13	AG13	XBUS_B89	AM33	AM33
XBUS_B40	AG14	AG14	XBUS_B90	AN32	AN32
XBUS_B41	AM11	AM11	XBUS_B91	AG23	AG23
XBUS_B42	AL11	AL11	XBUS_B92	AF24	AF24
XBUS_B43	AN12	AN12	XBUS_B93	AK26	AK26
XBUS_B44	AN11	AN11	XBUS_B94	AK27	AK27
XBUS_B45	AE14	AE14	XBUS_B95	AN31	AN31
XBUS_B46	AE15	AE15	XBUS_B96	AN30	AN30
XBUS_B47	AJ13	AJ13	XBUS_B97	AH26	AH26
XBUS_B48	AJ14	AJ14	XBUS_B98	AJ25	AJ25
XBUS_B49	AL13	AL13	XBUS_B99	AL27	AL27

10.6.1 DP FPGA (U14) to DPX FPGA (U16) XBUS_B Configuration Table

11.0 DPX FPGA (U16)

11.1 DPX FPGA 4 X 1M X 16 ZBT RAM

DPX Virtex-II FPGA has access to four 1M x 18 ZBT RAMs. The access time for DPX Static RAM is 10 nanoseconds. Refer to the data sheet for the IDT71T75802 for more detailed information. The interconnection is shown in the table below.

Description	Signal	Pin No.	Description	Signal	Pin No.
Address Bit 0	ZBTM_A0	A31	Data Bit 0	ZBTM_D0	A12
Address Bit 1	ZBTM_A1	A30	Data Bit 1	ZBTM_D1	A11
Address Bit 2	ZBTM_A2	A28	Data Bit 2	ZBTM_D2	A9
Address Bit 3	ZBTM_A3	A29	Data Bit 3	ZBTM_D3	A7
Address Bit 4	ZBTM_A4	A26	Data Bit 4	ZBTM_D4	A6
Address Bit 5	ZBTM_A5	A24	Data Bit 5	ZBTM_D5	A5
Address Bit 6	ZBTM_A6	A23	Data Bit 6	ZBTM_D6	A4
Address Bit 7	ZBTM_A7	B32	Data Bit 7	ZBTM_D7	B12
Address Bit 8	ZBTM_A8	B31	Data Bit 8	ZBTM_D8	B11
Address Bit 9	ZBTM_A9	B30	Data Bit 9	ZBTM_D9	B10
Address Bit 10	ZBTM_A10	B28	Data Bit 10	ZBTM_D10	B9
Address Bit 11	ZBTM_A11	B29	Data Bit 11	ZBTM_D11	B8
Address Bit 12	ZBTM_A12	B27	Data Bit 12	ZBTM_D12	B7
Address Bit 13	ZBTM_A13	B24	Data Bit 13	ZBTM_D13	B6
Address Bit 14	ZBTM_A14	B23	Data Bit 14	ZBTM_D14	B5
Address Bit 15	ZBTM_A15	B22	Data Bit 15	ZBTM_D15	B4
Address Bit 16	ZBTM_A16	B21	Data Bit 16	ZBTM_D16	B3
Address Bit 17	ZBTM_A17	C33	Data Bit 17	ZBTM_D17	C2
Address Bit 18	ZBTM_A18	C28	RAM ReDA / Write	ZBTM_RW	B13
Address Bit 19	ZBTM_A19	C27	RAM Byte Write Enable 1	ZBTM_BW1	D18
RAM Clock	ZBTM_CLK	B14	RAM Byte Write Enable 2	ZBTM_BW2	D19
RAM Clock Enable	ZBTM_CEN	C19	RAM Linear Burst Order	ZBTM_LBO	D6
RAM Chip Enable 0	ZBTM_CE0	C18	RAM Internal Register LoDA	ZBTM_ALD	D8
RAM Chip Enable 1	ZBTM_CE1	F19	RAM Output Enable	ZBTM_OE	C6
RAM Chip Enable 2	ZBTM_CE2	E18	RAM Chip Enable 3	ZBTM_CE3	E19

11.1.1 DPX FPGA (U16) ZBT RAM Pin Configuration Table

11.2 DPX FPGA LED Configuration.

The DP Virtex-II FPGA has 10 amber LEDs for general purpose use.

Signal	LED	DP FPGA Pin No.
DPXLED0	D31	K21
DPXLED1	D32	K20
DPXLED2	D33	C22
DPXLED3	D34	C23
DPXLED4	D35	E21
DPXLED5	D36	E22
DPXLED6	D37	H21
DPXLED7	D38	H20
DPXLED8	D39	G20
DPXLED9	D40	F20

11.2.1 DPX FPGA (U16) LED Configuration Table

11.3 DPX USB Interface

The Cypress CY7C68001 USB Controller (U21) is connected to both Virtex-II FPGAs (U14). An software and firmware interface design is available. The link to the design on our web site is (http://www.gvassociates.com/software.asp?prod=12). Additional documentation is also available.

Signal Name	Signal Description	DP FPGA (U14) Pin No.
USB1_SLRD	read strobe for the slave FIFOs connected to FDI[15..0]	AK34
USB1_SLWR	write strobe for the slave FIFOs connected to FDI[15..0]	AF27
USB1_SLOE	output enable for the slave FIFOs connected to FD[15..0]	AG28
USB1_READY	ready that gates external command reads andwrites. Active High.	
USB1_INT	external interrupt signal. Active Low.	
USB1_FIFOADR2	address bus select for the slave FIFOs connected to FD[15..0]	AF30
USB1_FIFOADR1	address bus select for the slave FIFOs connected to FD[15..0]	AG30
USB1_FIFOADR0	address bus select for the slave FIFOs connected to FD[15..0]	AE29
USB1_PKTEND	packet end signal for the slave FIFOs connected to FD[15..0]	AF29
USB1_CS#	master chip select (active low)	AE27
USB1_FD15	Bidirectional FIFO/Command Data Bit 15	AG31
USB1_FD14	Bidirectional FIFO/Command Data Bit 14	AF31
USB1_FD13	Bidirectional FIFO/Command Data Bit 13	AG32
USB1_FD12	Bidirectional FIFO/Command Data Bit 12	AF32
USB1_FD11	Bidirectional FIFO/Command Data Bit 11	AB25
USB1_FD10	Bidirectional FIFO/Command Data Bit 10	AC25
USB1_FD9	Bidirectional FIFO/Command Data Bit 9	AH33
USB1_FD8	Bidirectional FIFO/Command Data Bit 8	AJ33
USB1_FD7	Bidirectional FIFO/Command Data Bit 7	AD32
USB1_FD6	Bidirectional FIFO/Command Data Bit 6	AE31
USB1_FD5	Bidirectional FIFO/Command Data Bit 5	AC27
USB1_FD4	Bidirectional FIFO/Command Data Bit 4	AD27
USB1_FD3	Bidirectional FIFO/Command Data Bit 3	AH34
USB1_FD2	Bidirectional FIFO/Command Data Bit 2	AJ34
USB1_FD1	Bidirectional FIFO/Command Data Bit 1	AD30
USB1_FD0	Bidirectional FIFO/Command Data Bit 0	AE30
USB1_FLAGA	a programmable slave-FIFO output status flag signal. Defaults to PRGFLAG for the FIFO selected by the FIFOADR[1:0] pins	AE26
USB1_FLAGB	a programmable slave-FIFO output status flag signal. Defaults to FULL for the FIFO selected by the FIFOADR[2:0] pins.	AD26
USB1_FLAGC	a programmable slave-FIFO output status flag signal. Defaults to EMPTY for the FIFO selected by the FIFOADR[2:0] pins.	AE28

11.3.1 USB Interface for DPX FPGA Interconnection Table

11.4 DPX FPGA LVDS Interface

This is a 32 bit LVDS bus can be used to transfer data and control between the Virtex-II FGPA (U16) and two external connectors. The 32-bit bus is broken into a 16-bit receiver bus and a 16-bit transmitter bus. Each of these two buses has the appropriate termination resistors for the LVDS interface. LVDS_R designates a LVDS receiver and LVDS_D designates a LVDS driver. The pin numbering does alternate rows.

Signal	DCX FPGA (U16) Pin No.	J4 No.	Signal	DCX FPGA (U16) Pin No.	J4 No.
LVDS_RN0	AB9	1	DGND		18
LVDS_RP0	AC9	2	LVDS_RN8	AF7	19
LVDS_RN1	AD6	3	LVDS_RP8	AG7	20
LVDS_RP1	AE6	4	LVDS_RN9	AL1	21
LVDS_RN2	AF2	5	LVDS_RP9	AK1	22
LVDS_RP2	AG2	6	LVDS_RN10	AH2	23
LVDS_RN3	AF3	7	LVDS_RP10	AJ2	24
LVDS_RP3	AG3	8	LVDS_RN11	AJ4	25
LVDS_RN4	AF5	9	LVDS_RP11	AK4	26
LVDS_RP4	AG5	10	LVDS_RN12	AK2	27
LVDS_RN5	AE8	11	LVDS_RP12	AL2	28
LVDS_RP5	AD8	12	LVDS_RN13	AH6	29
LVDS_RN6	AH1	13	LVDS_RP13	AJ5	30
LVDS_RP6	AJ1	14	LVDS_RN14	AE11	31
LVDS_RN7	AG4	15	LVDS_RP14	AF11	32
LVDS_RP7	AH5	16	LVDS_RN15	AF10	33
DGND		17	LVDS_RP15	AG9	34

11.4.1 DPX FPGA LVDS Bus Interconnection Table for J6

Signal	DCX FPGA (U16) Pin No.	J5 No.	Signal	DCX FPGA (U16) Pin No.	J5 No.
LVDS_DN0	AE4	1	DGND		18
LVDS_DP0	AF4	2	LVDS_DN8	AA5	19
LVDS_DN1	AD5	3	LVDS_DP8	AB5	20
LVDS_DP1	AE5	4	LVDS_DN9	AA1	21
LVDS_DN2	AB10	5	LVDS_DP9	AB1	22
LVDS_DP2	AC10	6	LVDS_DN10	Y7	23
LVDS_DN3	AC8	7	LVDS_DP10	AA8	24
LVDS_DP3	AB8	8	LVDS_DN11	AA4	25
LVDS_DN4	AC4	9	LVDS_DP11	AB4	26
LVDS_DP4	AD4	10	LVDS_DN12	W3	27
LVDS_DN5	AC3	11	LVDS_DP12	Y3	28
LVDS_DP5	AD3	12	LVDS_DN13	V1	29
LVDS_DN6	AB6	13	LVDS_DP13	V2	30
LVDS_DP6	AC6	14	LVDS_DN14	V7	31
LVDS_DN7	AA2	15	LVDS_DP14	W7	32
LVDS_DP7	AB2	16	LVDS_DN15	V5	33
DGND		17	LVDS_DP15	W5	34

11.4.2 DPX FPGA LVDS Bus Interconnection Table for J7

12.0 EI FPGA (U18)

12.1 EI FPGA XE_BUS Configuration.

There is a 43 bit local bus that can be used to transfer data and control between the two Virtex-II Xilinx FPGAs (U10, U12, U14, U16 & U18) and the Spartan II FPGAS (U18 & U20). This bus can be configured for LVTTL or PCI.

Signal	ACX FPGA (U10) Pin No.	AC FPGA (U12) Pin No.	DP FPGA (U14) Pin No	DPX FPGA (U16) Pin No	EI FPGA (U18) Pin No.	EP FPGA (U1) Pin No.
XE_BUS0	D29	D29	D29	D29	30	23
XE_BUS1	C29	C29	C29	C29	31	26
XE_BUS2	H26	H26	H26	H26	44	27
XE_BUS3	G26	G26	G26	G26	46	28
XE_BUS4	F25	F25	F25	F25	49	29
XE_BUS5	F26	F26	F26	F26	57	40
XE_BUS6	H25	H25	H25	H25	60	41
XE_BUS7	H24	H24	H24	H24	62	42
XE_BUS8	E26	E26	E26	E26	67	43
XE_BUS9	F27	F27	F27	F27	3	47
XE_BUS10	J24	J24	J24	J24	4	86
XE_BUS11	J23	J23	J23	J23	5	87
XE_BUS12	K23	K23	K23	K23	6	93
XE_BUS13	K22	K22	K22	K22	7	94
XE_BUS14	C26	C26	C26	C26	10	95
XE_BUS15	D27	D27	D27	D27	11	96
XE_BUS16	G24	G24	G24	G24	12	NC
XE_BUS17	G25	G25	G25	G25	13	NC
XE_BUS18	E25	E25	E25	E25	19	NC
XE_BUS19	E24	E24	E24	E24	20	NC
XE_BUS20	D25	D25	D25	D25	21	NC
XE_BUS21	D26	D26	D26	D26	22	NC
XE_BUS22	H23	H23	H23	H23	23	NC
XE_BUS23	H22	H22	H22	H22	26	NC
XE_BUS24	F23	F23	F23	F23	27	NC
XE_BUS25	F24	F24	F24	F24	28	NC
XE_BUS26	J22	J22	J22	J22	29	NC
XE_BUS27	J21	J21	J21	J21	40	NC
XE_BUS28	C24	C24	C24	C24	41	NC
XE_BUS29	D24	D24	D24	D24	42	NC
XE_BUS30	D22	D22	D22	D22	43	NC
XE_BUS31	D23	D23	D23	D23	47	NC
XE_BUS32	G22	G22	G22	G22	48	NC
XE_BUS33	G23	G23	G23	G23	50	NC
XE_BUS34	F22	F22	F22	F22	51	NC
XE_BUS35	F21	F21	F21	F21	54	NC
XE_BUS36	J20	J20	J20	J20	56	NC
XE_BUS37	K19	K19	K19	K19	58	NC
XE_BUS38	D20	D20	D20	D20	59	NC
XE_BUS39	D21	D21	D21	D21	63	NC
XE_BUS40	G18	G18	G18	G18	64	NC
XE_BUS41	G19	G19	G19	G19	88 (GCLK)	NC
XE_BUS42	F18	F18	F18	F18	91 (GCLK)	NC

12.1.1 XE_BUS Interconnection Table

12.2 External Spartan Interface FPGA Connectors

This is a 48 bit bus can be used to transfer data and control between the External Interface Spartan II FGPA and three external connectors. This bus can be configured for LVTTL and provides a +5V tolerant I/O capability for the GVA-395. The pin numbering does alternate rows.

Signal	EI FPGA (U20) Pin No.	J1 No.	Signal	EI FPGA (U20) Pin No.	J1 No.
DGND		1	DGND		18
DGND		2	EBUS12	86	19
EBUS0	65	3	EBUS13	87	20
EBUS1	66	4	DGND		21
EBUS2	74	5	DGND		22
EBUS3	75	6	EBUS14	93	23
EBUS4	76	7	EBUS15	94	24
EBUS5	77	8	EBUS16	95	25
EBUS6	78	9	EBUS17	96	26
EBUS7	79	10	EBUS18	99	27
EBUS8	80	11	EBUS19	100	28
EBUS9	83	12	EBUS20	101	29
DGND		13	EBUS21	102	30
DGND		14	EBUS22	103	31
EBUS10	84	15	EBUS23	112	32
EBUS11	85	16	DGND		33
DGND		17	DGND		34

12.2.1 External Interface FPGA Bus Interconnection Table for J1

Signal	EI FPGA (U14) Pin No.	J2 No.	Signal	EI FPGA (U20) Pin No.	J2 No.
DGND		1	DGND		18
DGND		2	EBUS36	129	19
EBUS24	113	3	EBUS37	130	20
EBUS25	114	4	DGND		21
EBUS26	115	5	DGND		22
EBUS27	116	6	EBUS38	131	23
EBUS28	117	7	EBUS39	132	24
EBUS29	118	8	EBUS40	133	25
EBUS30	120	9	EBUS41	134	26
EBUS31	121	10	EBUS42	136	27
EBUS32	122	11	EBUS43	137	28
EBUS33	123	12	EBUS44	138	29
DGND		13	EBUS45	139	30
DGND		14	EBUS46	140	31
EBUS34	124	15	EBUS47	141	32
EBUS35	126	16	DGND		33
DGND		17	DGND		34

12.2.2 External Interface FPGA Bus Interconnection Table for J2

12.3 EI FPGA LED

There is one Green LED, which is recommended to be used as a FPGA Configuration OK indication. This would give the user a visual indication that all of the Xilinx FPGAs have been configured. The Configuration Done LED may be lite by connecting ground to pin 38 of U20.

13.0 Optional Daughter I/O PCBs for Analog Control FPGA (U14) Descriptions

13.1 GVA-AD9430 170 MSPS 12 Bit A/D

The analog input is injected via a 50-ohm SMA connector (P1). The analog input voltage should not exceed 1.5 Vp-p. The input Analog – Digital Converter (AD9430) is protected against accidental application of an over-voltage input up to 3.8 Vp-p by a protection diodes. The analog signals are each sampled by a 100 MSPS analog to digital converter (AD9432). The input sample clock (AD0_CLK) can be set to a maximum frequency of 170 MHz via the Analog Control FPGA (U14). The sample clock may be generated either the 50 MHz system clock or from the External Clock Input (P6). The LVTTL clock signal is coupled with a differential receiver (MC10EL16). The output of this differential receiver drive the ENC_CLK+ and ENC_CLK- inputs of the converter and provides the sub-nanosecond rise times for optimum performance.

13.1.1 AC Coupled Analog Input Path

The analog input is AC coupled into two Mini-Circuits T1:1 transformer, which has a high pass corner at 50 KHz. These transformers are used to generate a differential input to the AD9430.

13.1.2 GVA-AD9430 Output Configuration

Signal Name	Signal Description	PC Pin No.	Signal Name	Signal Description	PC Pin No.
D11-	LVDS Output Data Bit 11 Complement	1	D1+	LVDS Output Data Bit 1	22
D11+	LVDS Output Data Bit 11	2	D0-	LVDS Output Data Bit 0 Complement	23
D10-	LVDS Output Data Bit 10 Complement	3	D0+	LVDS Output Data Bit 0	24
D10+	LVDS Output Data Bit 10	4	AD_CLK-	LVDS Input Clock Complement	25
D9-	LVDS Output Data Bit 9 Complement	5	AD_CLK	LVDS Input Clock	26
D9+	LVDS Output Data Bit 9	6	+3.3V	+3.3 VDC Input	27
D8-	LVDS Output Data Bit 8 Complement	7	+5V	+5 VDC Input	28
D8+	LVDS Output Data Bit 8	8	+3.3V	+3.3 VDC Input	29
D7-	LVDS Output Data Bit 7 Complement	9	+5V	+5 VDC Input	30
D7+	LVDS Output Data Bit 7	10	DCO-	LVDS Output (JP5) Data Clock Complement	31
D6-	LVDS Output Data Bit 6 Complement	11	DCO+	LVDS Output (JP6) Data Clock	32
D6+	LVDS Output Data Bit 6	12	OR-	LVDS Output Data (JP7) Over Range Complement	33
D5-	LVDS Output Data Bit 5 Complement	13	OR+	LVDS Output Data (JP8) Over Range	34
D5+	LVDS Output Data Bit 5	14	TP5	Test Point 5	35
D4-	LVDS Output Data Bit 4 Complement	15	TP8	Test Point 8	36
D4+	LVDS Output Data Bit 4	16	TP6	Test Point 6	37
D3-	LVDS Output Data Bit 3 Complement	17	TP7	Test Point 7	38
D3+	LVDS Output Data Bit 3	18	DGND	Digital Ground	39
D2-	LVDS Output Data Bit 2 Complement	19	DGND	Digital Ground	40
D2+	LVDS Output Data Bit 2	20	DGND	Digital Ground	41
D1-	LVDS Output Data	21	DGND	Digital Ground	42

	Bit 1 Complement				

13.1.2.1 GVA-AD9430 to GVA-395 PC Connection Interface Table

Signal Name	PC Pin No.	AC FPGA PC #2 Pin No.	AC FPGA PC #3 Pin No.	AC FPGA PC #4 Pin No.	AC FPGA PC #5 Pin No.
D11-	1	E1	M1	AA1	AE2
D11+	2	D1	L1	AB1	AF1
D10-	3	E2	M2	AA2	AF2
D10+	4	D2	L2	AB2	AG2
D9-	5	E3	M3	AA4	AF3
D9+	6	D3	L3	AB4	AG3
D8-	7	G1	L4	AA5	AH1
D8+	8	F1	K4	AB5	AJ1
D7-	9	G2	P2	AD1	AH2
D7+	10	F2	N2	AC1	AJ2
D6-	11	G3	N4	AC2	AH3
D6+	12	F3	M4	AD2	AJ3
D5-	13	F4	P3	AC3	AK2
D5+	14	E4	N3	AD3	AL2
D4-	15	F5	P5	AC4	AL1
D4+	16	G5	N5	AD4	AK1
D3-	17	J1	N6	AB6	AH6
D3+	18	H2	P6	AC6	AJ5
D2-	19	J3	T2	AD5	AJ4
D2+	20	H3	R1	AE5	AK4
D1-	21	J4	T3	AE4	AF5
D1+	22	H4	R3	AF4	AG5
D0-	23	J5	R4	V5	AF6
D0+	24	H5	P4	W5	AG6
AD_CLK-	25	U1	U3	V1	W3
AD_CLK	26	U2	U4	V2	Y3
DCO-	31	E19	K18	E17	H17
DCO+	32	E18	J18	E16	H16
OR-	33	K2	L6	V6	AG4
OR+	34	J2	M6	W6	AH5
TP5	35	L5	N7	V7	AD6
TP8	36	K5	M7	W7	AE6
TP6	37	J6	N8	Y7	AD7
TP7	38	K6	P9	AA8	AE7

13.1.2.2 GVA-AD9430 to GVA-395 AC FPGA PC No. 2-5 Connection Table

Signal Name	PC Pin No.	AC FPGA PC #6 Pin No.	AC FPGA PC #7 Pin No.	AC FPGA PC #8 Pin No.	AC FPGA PC #9 Pin No.
D11-	1	E34	K31	V34	AD26
D11+	2	D34	K30	V33	AE26
D10-	3	E33	M34	V27	AD28
D10+	4	D33	L34	V26	AE28
D9-	5	E32	M33	V28	AE25
D9+	6	D32	L33	W28	AF25
D8-	7	F31	M32	W31	AE27
D8+	8	E31	L32	Y31	AF27
D7-	9	G34	M31	Y29	AE29
D7+	10	F34	L31	Y28	AF29
D6-	11	G33	L30	W27	AF26
D6+	12	F33	K29	Y27	AG26
D5-	13	G32	L29	AB30	AF28
D5+	14	F32	M29	AA30	AG28
D4-	15	F30	P33	AA33	AF30
D4+	16	G30	N33	AB33	AG30
D3-	17	J34	P32	AA31	AG31
D3+	18	H33	N32	AB31	AF31
D2-	19	J31	P31	AA29	AG32
D2+	20	H31	N31	AB29	AF32
D1-	21	H29	P30	AB32	AG29
D1+	22	G29	N30	AC32	AH29
D0-	23	J29	N29	AD31	AH32
D0+	24	H28	P29	AC31	AJ32
AD_CLK-	25	V31	U34	W32	V30
AD_CLK	26	U31	U33	V32	W30
DCO-	31	K33	R28	AC34	AK31
DCO+	32	J33	R29	AD34	AJ31
OR-	33	J32	U30	AC33	AK32
OR+	34	H32	T30	AD33	AL32
TP5	35	H30	T29	Y26	AK33
TP8	36	J30	U29	AA26	AL33
TP6	37	L28	U28	Y25	AK34
TP7	38	K28	T28	AA25	AL34

13.1.3 GVA-AD9430 to GVA-395 AC FPGA PC No. 6-9 Connection Table

Output Configuration	JP4
Offset Binary	Jumper on pin 1 and pin 2
Twos-Complement	Jumper on pin 2 and pin 3

13.1.3.1 GVA-AD9430 Digital Output Format Jumper Configuration Table

13.2 GVA-AD9432 100 MSPS 12 Bit A/D

The analog input is injected via a 50-ohm SMA connector (P1). The analog input voltage should not exceed 2 Vp-p. The input Analog – Digital Converter (AD9432) is protected against accidental application of an over-voltage input by a protection diodes. The digital data generated by the Analog to Digital Converters is buffered by 74ALVCH16374 (a 16 bit D register). This buffer incurs a one-clock delay between the A/D and the FPGA. This was necessary to insure proper data setup time for the FPGA. The analog signals are each sampled by a 100 MSPS analog to digital converter (AD9432). The input sample clock (AD0_CLK) can be set to a maximum frequency of 100 MHz via the Analog Control FPGA (U14). The sample clock may be generated either the 100 MHz system clock or from the External Clock Input (P6). The LVTTL clock signal is coupled with a differential receiver (MC10EL16). The output of this differential receiver drive the ENCODE and ENCODE- inputs of the converter and provides the sub-nanosecond rise times for optimum performance.

13.2.1 AC Coupled Analog Input Path

The analog input is AC coupled into two Mini-Circuits T1:1 transformer, which has a high pass corner at 50 KHz. These transformers are used to generate a differential input to the AD9432. To reduce the second harmonic distortion two T1-1T transformers are connected in series. A 3 dB to 4 dB improvement can be realized. Additionally, an external anti-aliasing filter may be needed to limit the input bandwidth of the A/D.

13.2.2 DC Coupled Analog Input Path

A differential output op amp (AD8138) is used to drive the AD9432 in the dc-coupled configuration. The AD8138 was specifically designed for ADC driver applications and has superior SNR performance in analog frequencies from 0 thru 30 MHz.

13.2.3 GVA-AD9432 Analog Input Configuration

Input Configuration	JP1	JP2	JP3
AC-Coupled Analog Input	**Jumper on pin 1 and pin 2**	**Jumper on pin 1 and pin 2**	**Jumper on pin 1 and pin 2**
DC-Coupled Analog Input	**Jumper on pin 2 and pin 3**	**Jumper on pin 2 and pin 3**	**Jumper on pin 2 and pin 3**

13.2.3.1 GVA-AD9432 Analog Input Jumper Configuration Table

* Pin 1 is the closest pin to GV & Associates logo on the PCB.

Signal Name	Signal Description	PC Pin No.	Signal Name	Signal Description	PC Pin No.
AD0_D0	AD Output Bit 0	1	DGND	Digital Ground	22
DGND	Digital Ground	2	AD0_D11	AD Output Bit 11	23
AD0_D1	AD Output Bit 1	3	DGND	Digital Ground	24
DGND	Digital Ground	4	AD0_CLK	AD Input Sample Clock	25
AD0_D2	AD Output Bit 2	5			26
DGND	Digital Ground	6	+3.3V	+3.3 VDC Input	27
AD0_D3	AD Output Bit 3	7	+5V	+5 VDC Input	28
DGND	Digital Ground	8	+3.3V	+3.3 VDC Input	29
AD0_D4	AD Output Bit 4	9	+5V	+5 VDC Input	30
DGND	Digital Ground	10	AD0_OR	AD Overflow Bit	31
AD0_D5	AD Output Bit 5	11	D_BUS1	Daughter PC Data Bus 1	32
DGND	Digital Ground	12	D_BUS2	Daughter PC Data Bus 2	33
AD0_D6	AD Output Bit 6	13	D_BUS3	Daughter PC Data Bus 3	34
DGND	Digital Ground	14	D_BUS4	Daughter PC Data Bus 4	35
AD0_D7	AD Output Bit 7	15	D_BUS5	Daughter PC Data Bus 5	36
DGND	Digital Ground	16	D_BUS6	Daughter PC Data Bus 6	37
AD0_D8	AD Output Bit 8	17	D_BUS7	Daughter PC Data Bus 7	38
DGND	Digital Ground	18	DGND	Digital Ground	39
AD0_D9	AD Output Bit 9	19	DGND	Digital Ground	40
DGND	Digital Ground	20	DGND	Digital Ground	41
AD0_D10	AD Output Bit 10	21	DGND	Digital Ground	42

13.2.3.2 GVA-AD9432 to GVA-395 PC Connection Interface Table

Signal Name	PC Pin No.	AC FPGA PC #2 Pin No.	AC FPGA PC #3 Pin No.	AC FPGA PC #4 Pin No.	AC FPGA PC #5 Pin No.
AD0_D0	1	E1	M1	AA1	AE2
AD0_D1	3	E2	M2	AA2	AF2
AD0_D2	5	E3	M3	AA4	AF3
AD0_D3	7	G1	L4	AA5	AH1
AD0_D4	9	G2	P2	AD1	AH2
AD0_D5	11	G3	N4	AC2	AH3
AD0_D6	13	F4	P3	AC3	AK2
AD0_D7	15	F5	P5	AC4	AL1
AD0_D8	17	J1	N6	AB6	AH6
AD0_D9	19	J3	T2	AD5	AJ4
AD0_D10	21	J4	T3	AE4	AF5
AD0_D11	23	J5	R4	V5	AF6
AD0_CLK	25	U1	U3	V1	W4

13.2.3.3 GVA-AD9432 to GVA-395 AC FPGA PC No. 2-5 Connection Table

Signal Name	PC Pin No.	AC FPGA PC #6 Pin No.	AC FPGA PC #7 Pin No.	AC FPGA PC #8 Pin No.	AC FPGA PC #9 Pin No.
AD0_D0	1	E34	K31	V34	AD26
AD0_D1	3	E33	M34	V27	AD28
AD0_D2	5	E32	M33	V28	AE25
AD0_D3	7	F31	M32	W31	AE27
AD0_D4	9	G34	M31	Y29	AE29
AD0_D5	11	G33	L30	W27	AF26
AD0_D6	13	G32	L29	AB30	AF28
AD0_D7	15	F30	P33	AA33	AF30
AD0_D8	17	J34	P32	AA31	AG31
AD0_D9	19	J31	P31	AA29	AG32
AD0_D10	21	H29	P30	AB32	AG29
AD0_D11	23	J29	N29	AD31	AH32
AD0_CLK	25	V31	U34	W32	V30

13.2.3.4 GVA-DA9432 to GVA-395 AC FPGA PC No. 6-9 Connection Table

13.3 GVA-DA6645 100 MSPS 14 Bit A/D

The analog input is injected via a 50-ohm SMA connector (P1). The analog input voltage should not exceed 2 Vp-p. The input Analog – Digital Converter (DA6645) is protected against accidental application of an over-voltage input by a protection diodes. The digital data generated by the Analog to Digital Converters is buffered by 74ALVCH16374 (a 16 bit D register). This buffer incurs a one-clock delay between the A/D and the FPGA. This was necessary to insure proper data setup time for the FPGA. The analog signals are each sampled by a 100 MSPS analog to digital converter (DA6645). The input sample clock (DA_CLK) can be set to a maximum frequency of 100 MHz via the Analog Control FPGA (U14). The sample clock may be generated either the 100 MHz system clock or from the External Clock Input (P6). The LVTTL clock signal is coupled with a differential receiver (MC10EL16). The output of this differential receiver drive the ENCODE and ENCODE- inputs of the converter and provides the sub-nanosecond rise times for optimum performance.

13.3.1 AC Coupled Analog Input Path

The analog input is AC coupled into two Mini-Circuits T1:1 transformer, which has a high pass corner at 50 KHz. These transformers are used to generate a differential input to the DA6645. To reduce the second harmonic distortion two T1-1T transformers are connected in series. A 3 dB to 4 dB improvement can be realized. DAditionally, an external anti-aliasing filter may be needed to limit the input bandwidth of the A/D.

13.3.2 DC Coupled Analog Input Path

A differential output op amp (DA8138) is used to drive the DA6645 in the dc-coupled configuration. The DA8138 was specifically designed for DAC driver applications and has superior SNR performance in analog frequencies from 0 thru 30 MHz.

13.3.3 GVA-DA6645 Analog Input Configuration

Input Configuration	JP1	JP2	JP3
AC-Coupled Analog Input	**Jumper on pin 1 and pin 2**	**Jumper on pin 1 and pin 2**	**Jumper on pin 1 and pin 2**
DC-Coupled Analog Input	**Jumper on pin 2 and pin 3**	**Jumper on pin 2 and pin 3**	**Jumper on pin 2 and pin 3**

13.3.3.1 GVA-AD6645 Analog Input Jumper Configuration Table

* Pin 1 is the closest pin to GV & Associates logo on the PCB.

Signal Name	Signal Description	PC Pin No.	Signal Name	Signal Description	PC Pin No.
AD_OVR	AD Overflow Bit	1			
AD13	AD Output Bit 13	2			
AD_DRY	AD Output Data Ready	3			
AD11	AD Output Bit 11	4	AD_CLK	AD Input Sample Clock	25
AD12	AD Output Bit 12	5			26
AD9	AD Output Bit 9	6	+3.3V	+3.3 VDC Input	27
AD10	AD Output Bit 10	7	+5V	+5 VDC Input	28
AD7	AD Output Bit 7	8	+3.3V	+3.3 VDC Input	29
AD8	AD Output Bit 8	9	+5V	+5 VDC Input	30
AD5	AD Output Bit 5	10	AD0_OR	AD Overflow Bit	31
AD6	AD Output Bit 6	11	D_BUS1	DAughter PC DAta Bus 1	32
AD3	AD Output Bit 3	12	D_BUS2	DAughter PC DAta Bus 2	33
AD4	AD Output Bit 4	13	D_BUS3	DAughter PC DAta Bus 3	34
AD1	AD Output Bit 1	14	D_BUS4	DAughter PC DAta Bus 4	35
AD2	AD Output Bit 2	15	D_BUS5	DAughter PC DAta Bus 5	36
		16	D_BUS6	DAughter PC DAta Bus 6	37
AD0	AD Output Bit 0	17	D_BUS7	DAughter PC DAta Bus 7	38
		18	DGND	Digital Ground	39
		19	DGND	Digital Ground	40
		20	DGND	Digital Ground	41
		21	DGND	Digital Ground	42

13.3.3.2 GVA-DA6645 to GVA-395 Interface Table

Signal Name	PC Pin No.	AC FPGA PC #2 Pin No.	AC FPGA PC #3 Pin No.	AC FPGA PC #4 Pin No.	AC FPGA PC #5 Pin No.
AD_D0	17	J1	N6	AB6	AH6
AD_D1	14	E4	N3	AD3	AL2
AD_D2	15	F5	P5	AC4	AL1
AD_D3	12	F3	M4	AD2	AJ3
AD_D4	13	F4	P3	AC3	AK2
AD_D5	10	F2	N2	AC1	AJ2
AD_D6	11	G3	N4	AC2	AH3
AD_D7	8	F1	K4	AB5	AJ1
AD_D8	9	G2	P2	AD1	AH2
AD_D9	6	D3	L3	AB4	AG3
AD_D10	7	G1	L4	AA5	AH1
AD_D11	4	D2	L2	AB2	AG2
AD_D12	5	E3	M3	AA4	AF3
AD_D13	2	D1	L1	AB1	AF1
AD_OVR	1	E1	M1	AA1	AE2
AD_DRY	3	E2	M2	AA2	AF2
AD_CLK	25	U1	U3	V1	W3

13.3.3.3 GVA-AD6645 to GVA-395 AC FPGA PC No. 2-5 Connection Table

Signal Name	PC Pin No.	AC FPGA PC #6 Pin No. (* = 0)	AC FPGA PC #7 Pin No. (* = 1)	AC FPGA PC #8 Pin No. \(* = 2)	AC FPGA PC #9 Pin No. (* = 3)
AD_D0	17	J34	P32	AA31	AG31
AD_D1	14	F32	M29	AA30	AG28
AD_D2	15	F30	P33	AA33	AF30
AD_D3	12	F33	K29	Y27	AG26
AD_D4	13	G32	L29	AB30	AF28
AD_D5	10	F34	L31	Y28	AF29
AD_D6	11	G33	L30	W27	AF26
AD_D7	8	E31	L32	Y31	AF27
AD_D8	9	G34	M31	Y29	AE29
AD_D9	6	D32	L33	W28	AF25
AD_D10	7	F31	M32	W31	AE27
AD_D11	4	D33	L34	V26	AE28
AD_D12	5	E32	M33	V28	AE25
AD_D13	2	D34	K30	V33	AE26
AD_OVR	1	E34	K31	V34	AD26
AD_DRY	3	E33	M34	V33	AE26
AD_CLK	25	V31	U34	W32	V30

13.3.3.4 GVA-DA6645 to GVA-395 AC FPGA PC No. 6-9 Connection Table

13.4 GVA-DA9762 125 MSPS 12 Bit D/A

The DA9762 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 k output impedance support update rates up to 125 MSPS. Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

13.4.1 Single-Ended Output Path

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an appropriately sized loDA resistor, 51-ohm, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. The DA9762 can be configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 cable since the nominal full-scale current 20 mA flows through the equivalent RLODA of 25 ohm . In this case, RLODA represents the equivalent loDA resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching 25-ohm resistor.

13.4.2 Differential Coupled Analog Output Path

An RF transformer is be used to perform a differential-to-single-ended signal conversion. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the loDA. Note that the transformer provides ac coupling only.

13.4.3 GVA-DA9762 Analog Output Configuration

Output Configuration	JP1	JP2	Output Connector
Singled-Ended Analog Output	Jumper on pin 1 and pin 2	Jumper on pin 1 and pin 2	P1
Differential Coupled Analog Output	Jumper on pin 2 and pin 3	Jumper on pin 2 and pin 3	P2

13.4.3.1 GVA-DA9762 Analog Output Jumper Configuration Table

* Pin 1 is the closest pin to GV & Associates logo on the PCB.

Signal Name	Signal Description	PC Pin No.	Signal Name	Signal Description	PC Pin No.
DA0_D0	DA Output Bit 0	1	DGND	Digital Ground	22
DGND	Digital Ground	2	DA0_D11	DA Output Bit 11	23
DA0_D1	DA Output Bit 1	3	DGND	Digital Ground	24
DGND	Digital Ground	4	DA0_CLK	DA Input Sample Clock	25
DA0_D2	DA Output Bit 2	5			26
DGND	Digital Ground	6	+3.3V	+3.3 VDC Input	27
DA0_D3	DA Output Bit 3	7	+5V	+5 VDC Input	28
DGND	Digital Ground	8	+3.3V	+3.3 VDC Input	29
DA0_D4	DA Output Bit 4	9	+5V	+5 VDC Input	30
DGND	Digital Ground	10			31
DA0_D5	DA Output Bit 5	11	D_BUS1	Daughter PC Data Bus 1	32
DGND	Digital Ground	12	D_BUS2	Daughter PC Data Bus 2	33
DA0_D6	DA Output Bit 6	13	D_BUS3	Daughter PC Data Bus 3	34
DGND	Digital Ground	14	D_BUS4	Daughter PC Data Bus 4	35
DA0_D7	DA Output Bit 7	15	D_BUS5	Daughter PC Data Bus 5	36
DGND	Digital Ground	16	D_BUS6	Daughter PC Data Bus 6	37
DA0_D8	DA Output Bit 8	17	D_BUS7	Daughter PC Data Bus 7	38
DGND	Digital Ground	18	DGND	Digital Ground	39
DA0_D9	DA Output Bit 9	19	DGND	Digital Ground	40
DGND	Digital Ground	20	DGND	Digital Ground	41
DA0_D10	DA Output Bit 10	21	DGND	Digital Ground	42

13.4.3.2 GVA-DA9762 to GVA-395 Interface Table

Signal Name	PC Pin No.	AC FPGA PC #2 Pin No.	AC FPGA PC #3 Pin No.	AC FPGA PC #4 Pin No.	AC FPGA PC #5 Pin No.
DA0_D0	1	E1	M1	AA1	AE2
DA0_D1	3	E2	M2	AA2	AF2
DA0_D2	5	E3	M3	AA4	AF3
DA0_D3	7	G1	L4	AA5	AH1
DA0_D4	9	G2	P2	AD1	AH2
DA0_D5	11	G3	N4	AC2	AH3
DA0_D6	13	F4	P3	AC3	AK2
DA0_D7	15	F5	P5	AC4	AL1
DA0_D8	17	J1	N6	AB6	AH6
DA0_D9	19	J3	T2	AD5	AJ4
DA0_D10	21	J4	T3	AE4	AF5
DA0_D11	23	J5	R4	V5	AF6
DA0_CLK	25	U1	U3	V1	W4

13.4.3.3 GVA-DA9762 to GVA-395 AC FPGA PC No. 2-5 Connection Table

Signal Name	PC Pin No.	AC FPGA PC #6 Pin No.	AC FPGA PC #7 Pin No.	AC FPGA PC #8 Pin No.	AC FPGA PC #9 Pin No.
DA0_D0	1	E34	K31	V34	AD26
DA0_D1	3	E33	M34	V27	AD28
DA0_D2	5	E32	M33	V28	AE25
DA0_D3	7	F31	M32	W31	AE27
DA0_D4	9	G34	M31	Y29	AE29
DA0_D5	11	G33	L30	W27	AF26
DA0_D6	13	G32	L29	AB30	AF28
DA0_D7	15	F30	P33	AA33	AF30
DA0_D8	17	J34	P32	AA31	AG31
DA0_D9	19	J31	P31	AA29	AG32
DA0_D10	21	H29	P30	AB32	AG29
DA0_D11	23	J29	N29	AD31	AH32
DA0_CLK	25	V31	U34	W32	V30

13.4.3.4 GVA-DA9762 to GVA-395 AC FPGA PC No. 6-9 Connection Table

13.5 GVA-DA9772 125 MSPS 14 Bit D/A

The DA9772 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 k output impedance support update rates up to 125 MSPS. Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

13.5.1 Single-Ended Output Path

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an appropriately sized loDA resistor, 51-ohm, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. The DA9772 can be configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 cable since the nominal full-scale current 20 mA flows through the equivalent RLODA of 25 ohm . In this case, RLODA represents the equivalent loDA resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching 25-ohm resistor.

13.5.2 Differential Coupled Analog Output Path

An RF transformer is be used to perform a differential-to-single-ended signal conversion. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the loDA. Note that the transformer provides ac coupling only.

13.5.3 GVA-DA9772 Analog Output Configuration

Output Configuration	JP2	JP3	Output Connector
Singled-Ended Analog Output	Jumper on pin 1 and pin 2	Jumper on pin 1 and pin 2	P1
Differential Coupled Analog Output	Jumper on pin 2 and pin 3	Jumper on pin 2 and pin 3	P2

13.5.3.1 GVA-DA9772 Analog Output Jumper Configuration Table

* Pin 1 is the closest pin to GV & Associates logo on the PCB.

13.5.4 GVA-DA9772 PLL Configuration

Applications requiring input data rates below 6 MSPS must disable the PLL clock multiplier and provide an external reference clock . To disable the PLL Clock Multiplier, connect PLLVDD to PLLCOM by DAding a jumper between pins 2 and 3 of JP1. Please refer to the DA9772 Data sheet for DAditional information.

Signal Name	Signal Description	PC Pin No.	Signal Name	Signal Description	PC Pin No.
DA_D0	DA Output Bit 0	1			22
DA_D1	DA Output Bit 1	2			23
DA_D2	DA Output Bit 2	3			24
DA_D3	DA Output Bit 3	4	DA_CLK	DA Input Sample Clock	25
DA_D4	DA Output Bit 4	5			26
DA_D5	DA Output Bit 5	6	+3.3V	+3.3 VDC Input	27
DA_D6	DA Output Bit 6	7	+5V	+5 VDC Input	28
DA_D7	DA Output Bit 7	8	+3.3V	+3.3 VDC Input	29
DA_D8	DA Output Bit 8	9	+5V	+5 VDC Input	30
DA_D9	DA Output Bit 9	10			31
DA_D10	DA Output Bit 10	11	D_BUS1	Daughter PC Data Bus 1	32
DA_D11	DA Output Bit 11	12	D_BUS2	Daughter PC Data Bus 2	33
DA_D12	DA Output Bit 12	13	D_BUS3	Daughter PC Data Bus 3	34
DA_D13	DA Output Bit 13	14	D_BUS4	Daughter PC Data Bus 4	35
DIV1	Div Bit 1	15	D_BUS5	Daughter PC Data Bus 5	36
MOD1	“zero-stuffing” option	16	D_BUS6	Daughter PC Data Bus 6	37
DIV0	Div Bit 0	17	D_BUS7	Daughter PC Data Bus 7	38
MOD0	2x digital filter’s response	18	DGND	Digital Ground	39
SLEEP	Power Down	19	DGND	Digital Ground	40
PLLLOCK	PLL Lock	20	DGND	Digital Ground	41
RESET	Reset Internal Divider	21	DGND	Digital Ground	42

13.5.4.1 GVA-DA9772 to GVA-395 Interface Table

Signal Name	PC Pin No.	AC FPGA PC #2 Pin No.	AC FPGA PC #3 Pin No.	AC FPGA PC #4 Pin No.	AC FPGA PC #5 Pin No.
DA_D0	1	E1	M1	AA1	AE2
DA_D1	2	D1	L1	AB1	AF1
DA_D2	3	E2	M2	AA2	AF2
DA_D3	4	D2	L2	AB2	AG2
DA_D4	5	E3	M3	AA4	AF3
DA_D5	6	D3	L3	AB4	AG3
DA_D6	7	G1	L4	AA5	AH1
DA_D7	8	F1	K4	AB5	AJ1
DA_D8	9	G2	P2	AD1	AH2
DA_D9	10	F2	N2	AC1	AJ2
DA_D10	11	G3	N4	AC2	AH3
DA_D11	12	F3	M4	AD2	AJ3
DA_D12	13	F4	P3	AC3	AK2
DA_D13	14	E4	N3	AD3	AL2
DIV1	15	F5	P5	AC4	AL1
MOD1	16	G5	N5	AD4	AK1
DIV0	17	J1	N6	AB6	AH6
MOD0	18	H2	P6	AC6	AJ5
SLEEP	19	J3	T2	AD5	AJ4
PLLLOCK	20	H3	R1	AE5	AK4
RESET	21	J4	T3	AE4	AF5
DA_CLK	25	U1	U3	V1	W4

13.5.4.2 GVA-DA9772 to GVA-395 AC FPGA PC No. 2-5 Connection Table

Signal Name	PC Pin No.	AC FPGA PC #6 Pin No.	AC FPGA PC #7 Pin No.	AC FPGA PC #8 Pin No.	AC FPGA PC #9 Pin No.
DA_D0	1	E34	K31	V34	AD26
DA_D1	2	D34	K30	V33	AE26
DA_D2	3	E33	M34	V27	AD28
DA_D3	4	D33	L34	V26	AE28
DA_D4	5	E32	M33	V28	AE25
DA_D5	6	D32	L33	W28	AF25
DA_D6	7	F31	M32	W31	AE27
DA_D7	8	E31	L32	Y31	AF27
DA_D8	9	G34	M31	Y29	AE29
DA_D9	10	F34	L31	Y28	AF29
DA_D10	11	G33	L30	W27	AF26
DA_D11	12	F33	K29	Y27	AG26
DA_D12	13	G32	L29	AB30	AF28
DA_D13	14	F32	M29	AA30	AG28
DIV1	15	F30	P33	AA33	AF30
MOD1	16	G30	N33	AB33	AG30
DIV0	17	J34	P32	AA31	AG31
MOD0	18	H33	N32	AB31	AF31
SLEEP	19	J31	P31	AA29	AG32
PLLLOCK	20	H31	N31	AB29	AF32
RESET	21	H29	P30	AB32	AG29
DA_CLK	25	V31	U34	W32	V30

13.5.4.3 GVA-DA9772 to GVA-395 AC FPGA PC No. 6-9 Connection Table

14.0 GVA-395 Configuration Jumper Settings

The table below describes the various setup configuration for the GVA-395

JP5	JP6	JP9	JP10	
Not Installed	Not Installed	Not Installed	Install	Enables the configuration of the FPGAs via the JTAG Connector JP3.
Installed	Not Installed	Not Installed	Installed	Enables the configuration of the FPGAs via the Slave Serial Connector JP7.
Installed	Not Installed	Installed	Not Installed	Enables the configuration of the FPGAs via the on-board FLASH EEPROM.
Installed	Installed	Not Installed	Installed	Enables the configuration of the FPGAs via the Slave Serial Connector JP7 and program the on-board EEPROM

14.1.1 GVA-395 Jumper Configuration Table

15.0 GVA-395 Test Point Description

TP	Description
2	Flash EEPROM Write Enable
3	Flash EEPROM Chip Enable
4	Flash EEPROM Output Enable
5	Flash EEPROM Reset
6	Flash EEPROM Ready
7	Ground
8	VCC
9	+3.3V
10	+2.5V
11	+1.5V
12	PT7711 Sync
13	PT7711 Standby
18	Additional Clock Output
19	System Clock
20	DPX ZBTM Chip Enable 0
21	DPX ZBTM Read / Write
22	DPX ZBTM Output Enable
23	DPX ZBTM Clock
24	DPX ZBTM Chip Enable 1
28	DPX ZBTM Chip Enable 2
32	DPX ZBTM Chip Enable 3
38	AD0 Clock
96	VREF
97	VCCO

16.0 Appendix A: GVA-395 Hardware Accelerator Schematic

17.0 Appendix B: GVA-395 Self Test FGPA Schematic

18.0 Appendix C: GVA-395 Flash EEPROM Download and System Clock Configuration Spartan-II Schematic