Five Innovative Radiation-Tolerant Semiconductor Device Patents Created For Avionics, Space, Military, Automotive and Consumer Applications

Inventor: Jeffrey Titus

Assignment: United States of America as represented by the Secretary of the Navy

Joining Forces

Technology Transfer

Crane's Technology Transfer program allows the Navy the ability to share our federally developed technology with state and local government and private industry. We work with businesses, entrepreneurs, and start-ups. Our objective is to create partnerships with various industry and academia, license technologies, and encourage and assist with the transfer of new technologies to the private sector.

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Need some help? Contact us today to speak with a Tech Transfer representative to help you find the right technology for you. We can also assist you with the licensing process or give you an opportunity to learn more about our program.

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Patented Structures (Compatibility and Operation)

Patented structures can be fabricated as either N-channel or P-channel (or both). Structures are normally planar (and self aligned although other variations are possible). Structures can be fabricated using different semiconductor base materials (e.g., silicon, silicon carbide, gallium arsenide, or other base materials). By adjusting doping and thickness profiles, structures produce different blocking voltages from a few volts to several thousand volts (e.g., blocking voltages using silicon can range from a few volts up to 1000V while blocking voltages using silicon carbide can range from 100V to over 3000V). By adjusting overall structure area (e.g., by changing the number of cells placed in parallel), structures can produce a range of current handling capabilities. Using those variations, a family of devices with different electrical capabilities and performance can be fabricated and marketed.

Device design should allow easy integration into existing fabrication processes with minimal effort and costs. Structure can be fabricated as a discrete power device or fabricated into more complex integrated circuits such as a linear or analog type circuits.

Patent Summary

Patent #	Date	Patent Description
US 9,425,187	08/23/2016	Lateral metal-oxide semiconductor field-effect transistor (LMOSFET) layout integrated with a junction field-effect transistor (JFET) gate mitigating catastrophic radiation effects
US 9,425,303	08/23/2016	Vertical metal-oxide semiconductor field-effect transistor (VMOSFET) layout integrated with a junction field-effect transistor (JFET) gate mitigating catastrophic radiation effects
US 9,455,701	09/27/2016	Lateral metal-oxide semiconductor field-effect transistor (LMOSFET) layout integrated with a metal-semiconductor field-effect transistor (MEFET) gate mitigating catastrophic radiation effects
US 9,595,519	03/14/2017	Lateral metal-oxide semiconductor field-effect transistor (LMOSFET) layout integrated with a buried junction field-effect transistor (JFET) gate mitigating catastrophic radiation effects
US 9,735,769	08/15/2017	Vertical metal-oxide semiconductor field-effect transistor (VMOSFET) layout integrated with a metal-semiconductor field-effect transistor (MEFET) gate mitigating catastrophic radiation effects

Manufacturability

Fabrication & Manufacturing Steps

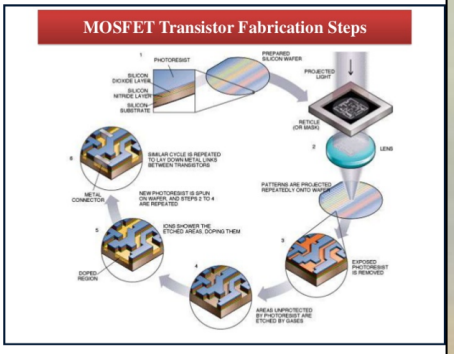
Fabrication processes compatible with standard commercial foundry processing steps

Patented structures employ two independent gates (depending on layout may require 2nd metal layer or 2nd polysilicon layer)

Topology compatible with stripe, rectangular, hexagonal or square cell design layouts

Compatible with different semiconductor base materials such as silicon (Si), silicon Carbide (SiC), and Gallium Arsenide (GaAs)

Compatible with Standard Commercial and Rad-Hard Foundry Steps



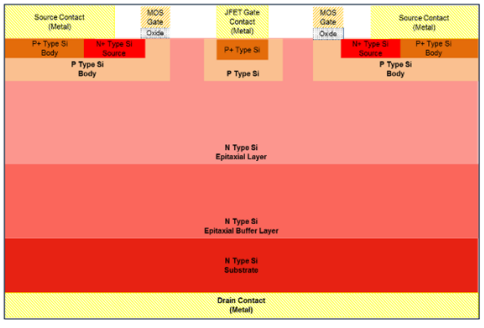
NSWC Crane performed limited simulations using SILVACO to verify structures exhibited suitable electrical performance. Simulations indicated that electrical responses of patented structures were comparable to their conventional MOSFET responses.

Electrical Parameter	Response Compared to Conventional MOSFET
RDSON	Slight Increase
IDSON	Slight Decrease
VTH	Similar (1st Gate)
IDSS	Similar
IGSS	Similar (1st Gate)
	2nd Gate Current Added
BVDSS	Similar

Second Gate Response

AC Modulation of IDS (Excellent)
DC Control of IDS (Excellent)
Injected TID Oxide Damage (No Affect)

Example of Patented Structure Layout Used in Simulations



Patented Structures (Compatibility and Operation)

Radiation Performance

- Conventional structures can exhibit low radiation performance
- Patent embodiments can exhibit better radiation performance

Expected Radiation Enhancements

Total Ionizing Dose (TID)
- Reduce Drain Leakage (Idss)
- Reduce Channel Inversion (Vth)

Heavy Ions
- Reduce Burnout
- Reduce Gate Rupture

Prompt Dose
- Reduce Burnout
- Reduce Channel Inversion (Vth)

Radiation is high concern for space, avionics, and military applications (e.g., satellites, space station, missiles)

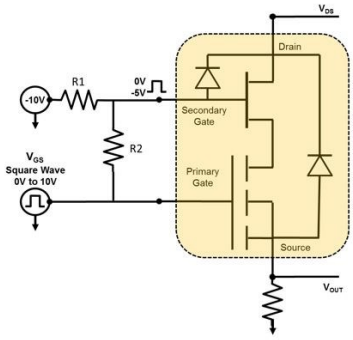
Patented structures are radiation-hardened by design (RHBD) offering enhanced radiation performance. The commercially available LDMOSFET and VDMOSFET constructs are prone to degraded radiation performance, but that degraded radiation performance is negated by using a second gate hardened by design construct, which is not prone to radiation degradation. Additional radiation performance can be achieved by fabricating patented structures using proven radiation-hardened process techniques (e.g., dual epitaxial layers).

Single-Gate Control Configuration

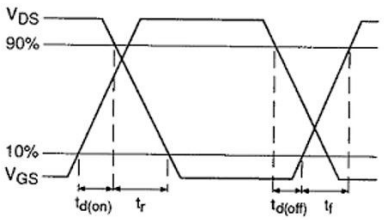
Example of Embodiment Configuration Using Single-Gate Control With Second Gate Under Static Bias

Simulation Exhibited Higher TID Performance Compared to Conventional Device

Embodiment Concept Using Single-Gate Control



Switching Characteristic Illustration

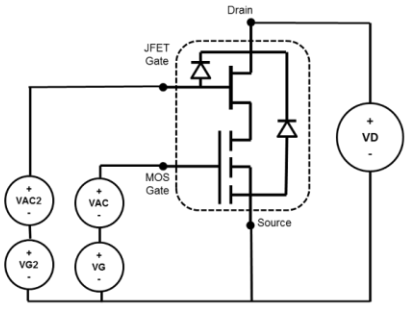


Patented structures can be configured to function under a single-gate control configuration. Under this configuration, its electrical and switching characteristics are comparable to its commercially-equivalent MOS device transistor. Limited simulation showed negligible difference.

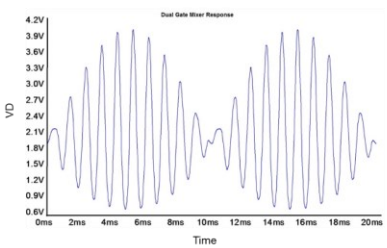
Dual-Gate Control Configuration

Example of Embodiment Configuration Using Dual-Gate Control For AC Modulation and RF Type Applications

Embodiment Concept Using Dual-Gate Control (RF Mixer)



Mixer Output Illustration



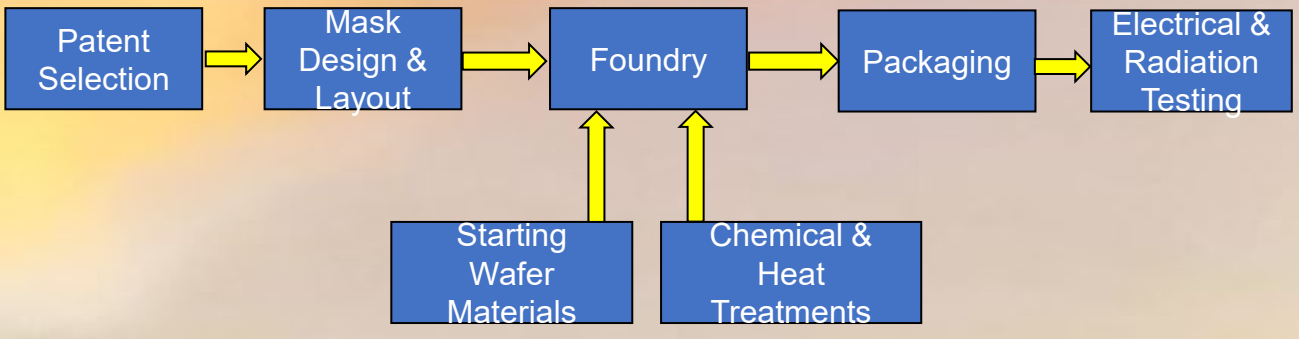
Patented structures can be configured to function under a dual-gate control configuration. Under this configuration, its switching characteristics are comparable to placing two commercially-equivalent transistors in series. The patented structure designs are smaller in size and are matched for better performance.

Radiation-Hard by Design (RHBD) Patent Embodiments Can Be Merged With Other Radiation-Hard by Processing (RHBP) Techniques To Achieve Even Higher Radiation Performance

Patented embodiments offer RHBD attributes. Those patented RHBD embodiments can be further enhanced by utilizing RHBP techniques to increase overall radiation tolerance and performance.

Additional Design and Processing Enhancements Are Compatible with Patented Embodiments Increasing Their Overall Radiation Tolerance to Higher Performance Levels

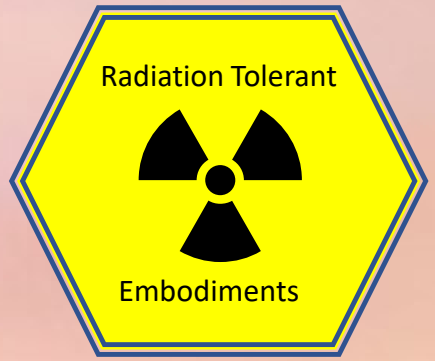
- Total Ionizing Dose (TID)
  - ❑ In-House Process Treatment
  - ❑ Gate Oxide Treatment
  - ❑ Field Oxide Treatment
- Single Event Burnout (SEB)
  - ❑ Buffer Layer
  - ❑ MOS Cell Layout and Design
  - ❑ Dielectric Isolated Substrate
- Single Event Gate Rupture (SEGR)
  - ❑ Buffer Layer
  - ❑ MOS Cell-to-Cell Layout and Design
- Survivability
  - ❑ Buffer Layer
  - ❑ MOS Cell Layout and Design
  - ❑ MOS Cell-to-Cell Layout and Design
  - ❑ Dielectric Isolated Substrate



Potential Applications and Advantages (Different Patent Embodiments)

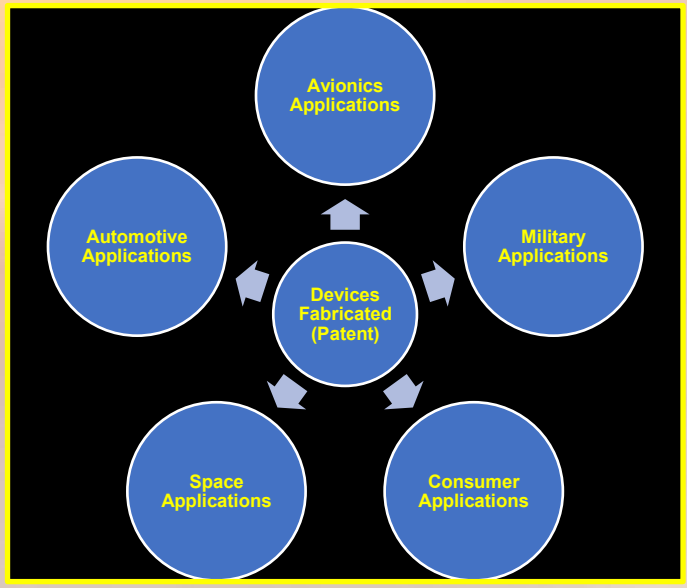
Patented embodiments offer RHBD attributes. Those patented RHBD embodiments can be further enhanced by utilizing RHBP techniques to increase overall radiation tolerance and performance.

Advantages



- Radiation-Tolerant Power Structures
  - High-Voltage Capabilities
  - High Current Capabilities
- Package (Not a Hybrid)
  - Discrete Packages
- Lower Costs
  - Compatible with Existing Foundry Processes
  - Compatible with Existing Design Tools
- Smaller Size
  - Smaller than Two Discrete Transistors

Potential Applications



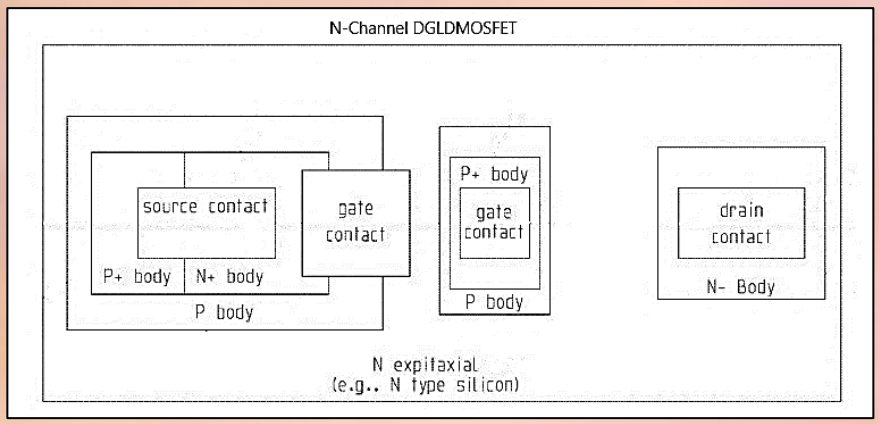
- High Power RF Mixer
  - High Current
  - High Voltage
- High Power Amplifier
  - High Current
  - High Voltage
- High Power Switches
- Power Modulators
- Power Converters
  - DC-to-DC Converters
  - AC-to-DC Converters
- Motor Controllers
- Power Controllers

Integrated Lateral MOSFET/JFET: 9,425,187

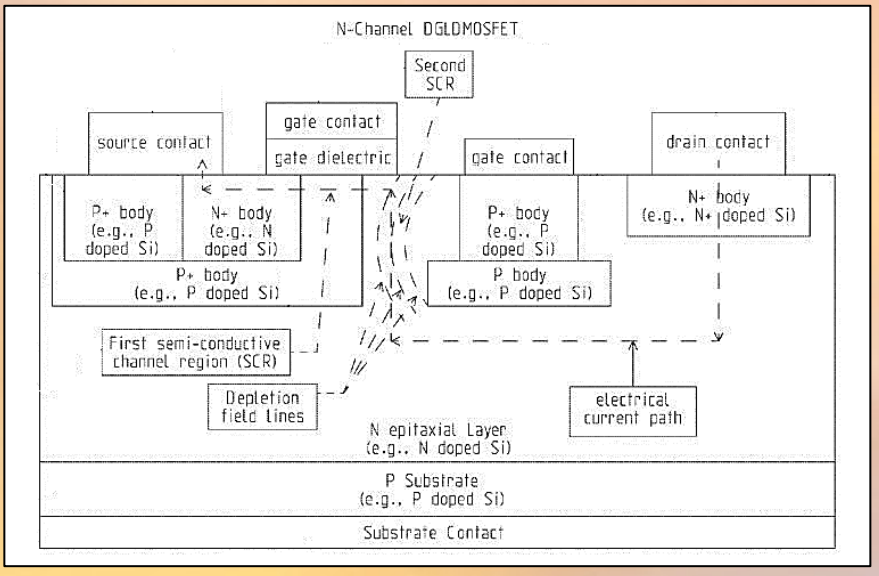
Abstract

Apparatuses and methods for modulating current/voltage response using multiple semi-conductive channel regions (SCR) produced from different integrated semiconductor structures are provided. In particular, embodiments include systems and methods for controlling current or mitigating electromagnetic or radiation interference effects using combined integrated functions of a lateral double-diffused metal-oxide semiconductor field effect transistor (LDMOSFET) and junction field effect transistor (JFET) disposed in proximity of a LDMOSFET's SCR within a certain orientation forming a second SCR.

Top Cross-Sectional View



Side Cross-Sectional View



Embodiments can be fabricated using different semiconductor type base materials (e.g., Si, SiC, and GaAs). Structure implementation using a Si base material could produce blocking voltages from a few volts up to 150 volts (n- or p–channel).

This Lateral Dual-Gate structure should allow easy integration into existing fabrication processes with minimal effort and costs. The LDMOSFET structure portion is prone to radiation degradation but is compensated by the JFET gated portion.

Expected Radiation Enhancements

Total Ionizing Dose (TID)
- Reduce Drain Leakage (Idss)
- Reduce Channel Inversion (Vth)

Heavy Ions
- Reduce Burnout
- Reduce Gate Rupture

Prompt Dose
- Reduce Burnout
- Reduce Channel Inversion (Vth)

Fabricated structures can be externally configured (circuit configuration) using either single-gate or dual-gate control. Configuration under dual-gate control allows AC modulation and RF-type applications (e.g., RF Mixer).

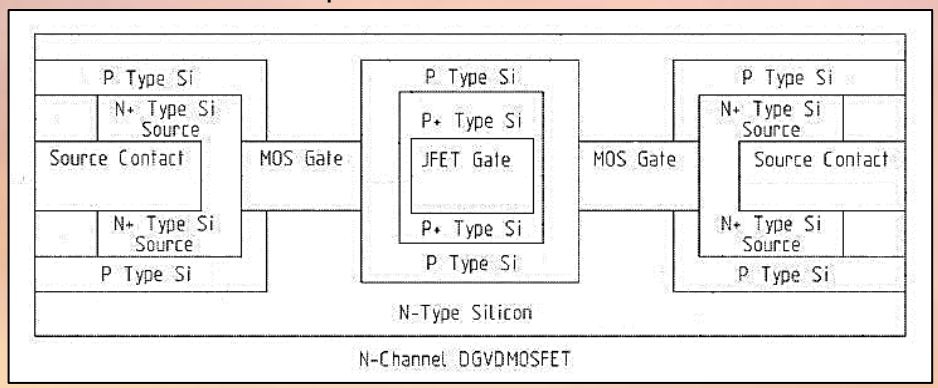
Patent details are available via the US patent and trademark office website: https://www.uspto.gov/patents

Integrated Vertical MOSFET/JFET: 9,425,303

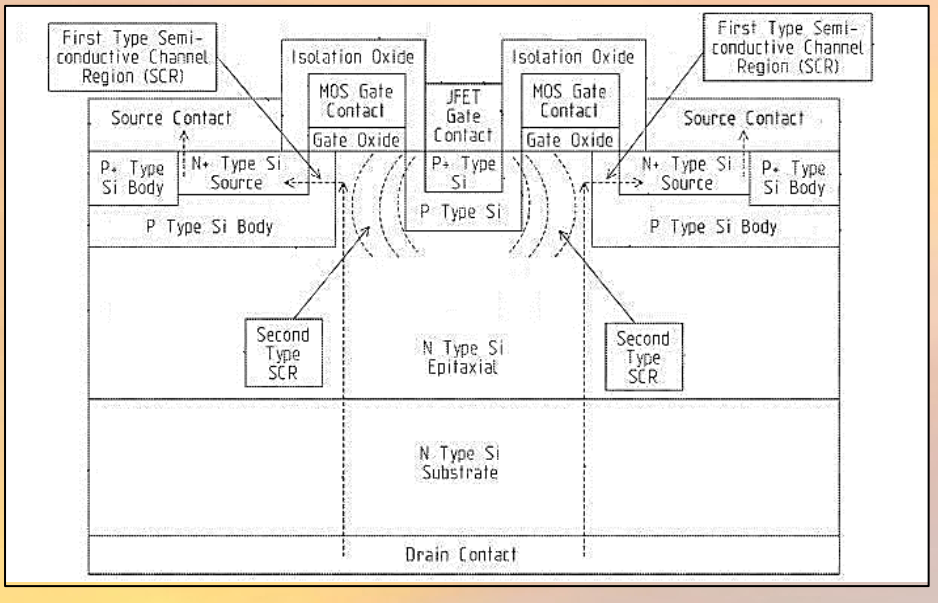
Abstract

Systems and methods for controlling current or mitigating electromagnetic or radiation interference effects using multiple different semi-conductive channel regions generating structures formed by multiple different semi-conductive electrical current or voltage control structures. One embodiment includes providing a first and second metal oxide semiconductor field effect transistor (MOSFET) sections formed on opposite sides of a junction field effect transistor (JFET) such that operation of the JFET modulates or controls current otherwise controlled by an electrical path of the MOSFET sections. A control system for determining when an embodiment of the invention is to be operated is also provided to include automated systems including sensors as well as manually operated systems. Automated systems can include radiation sensors as well as other control systems such as high-voltage radio frequency transmitter or receiver systems. Methods of operation for a variety of modes are also provided.

Top Cross-Sectional View



Side Cross-Sectional View



Embodiments can be fabricated using different semiconductor type base materials (e.g., Si, SiC, and GaAs). Structures fabricated using a silicon base material could produce blocking voltages from a few volts to 1000 volts depending upon the doping and thickness of epitaxial layer; and structures fabricated using a SiC base material could produce blocking voltages from a few volts to 2400 volts depending upon the doping and thickness of epitaxial layer (n-channel or p-channel). This Vertical Dual-Gate structure can be integrated using existing fabrication processes.

Expected Radiation Enhancements

Total Ionizing Dose (TID)
- Reduce Drain Leakage (Idss)
- Reduce Channel Inversion (Vth)

Heavy Ions
- Reduce Burnout
- Reduce Gate Rupture

Prompt Dose
- Reduce Burnout
- Reduce Channel Inversion (Vth)

The VDMOSFET portion of this structure is prone to radiation degradation; but that degradation is compensated by the radiation-tolerant JFET gated structure.

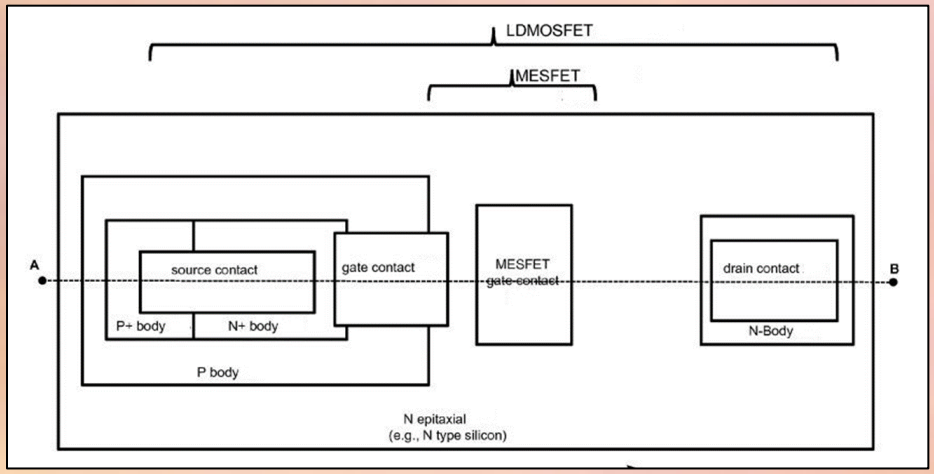
Patent details are available via the US patent and trademark office website: https://www.uspto.gov/patents

Integrated Lateral MOSFET/MESFET: 9,455,701

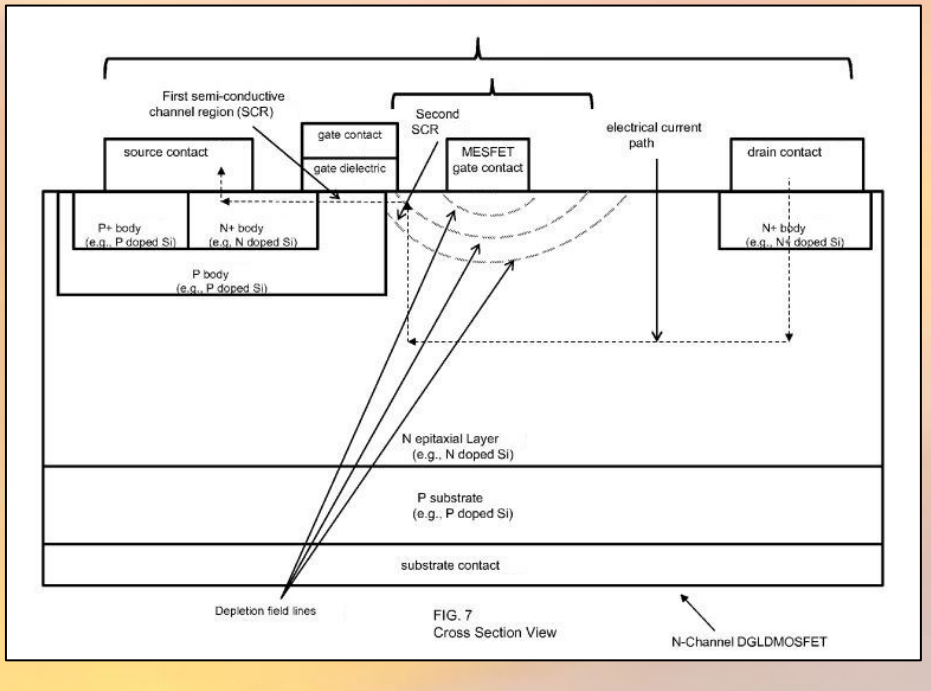
Abstract

Apparatuses and methods for modulating current/voltage response using multiple semi-conductive channel regions (SCR) produced from different integrated semiconductor structures are provided. In particular, embodiments include systems and methods for controlling current or mitigating electromagnetic or radiation interference effects using combined integrated functions of a lateral double-diffused metal-oxide semiconductor field effect transistor (LDMOSFET) and metal-semiconductor field effect transistor (MESFET) disposed in proximity of a LDMOSFET's SCR within a certain orientation forming a second SCR.

Top Cross-Sectional View



Side Cross-Sectional View



Embodiments can be fabricated using different semiconductor type base materials (e.g., Si, SiC, and GaAs). Structures fabricated using a silicon base material could produce blocking voltages from a few volts to 150 volts depending upon the doping and thickness of epitaxial layer; and structures fabricated using a SiC base material could produce blocking voltages from a few volts to 1000 volts depending upon the doping and thickness of epitaxial layer (n-channel or p-channel). This Lateral Dual-Gate structure can be integrated using existing fabrication processes.

Expected Radiation Enhancements

Total Ionizing Dose (TID)
- Reduce Drain Leakage (Idss)
- Reduce Channel Inversion (Vth)

Heavy Ions
- Reduce Burnout
- Reduce Gate Rupture

Prompt Dose
- Reduce Burnout
- Reduce Channel Inversion (Vth)

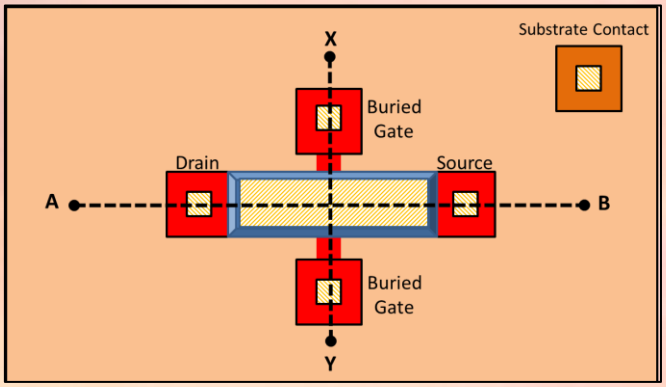
The LDMOSFET portion of this structure is prone to radiation degradation; but that degradation is compensated by the radiation tolerant MESFET gated structure.

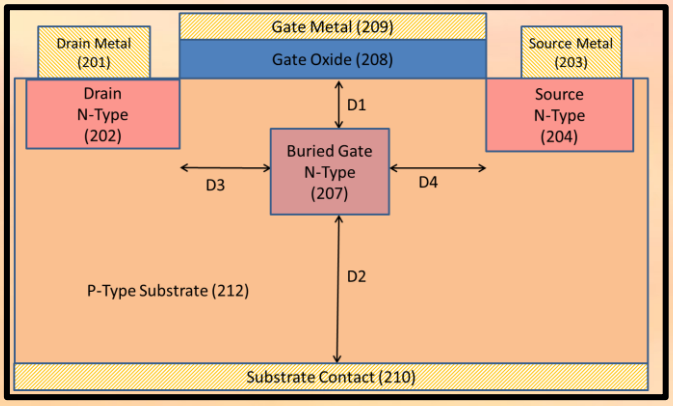
Patent details are available via the US patent and trademark office website: https://www.uspto.gov/patents

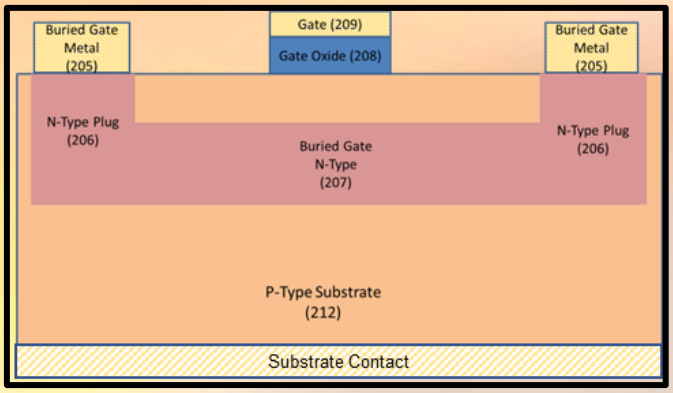
Integrated Lateral MOSFET/Buried JFET: 9,595,519

Abstract

Systems and methods for controlling current or mitigating electromagnetic or radiation interference effects using a combination of a metal-oxide semiconductor field effect transistor (MOSFET) and junction field effect transistor (JFET) disposed perpendicularly and within a certain orientation to each other. An embodiment of the invention can be formed and operable for modulating current and/or voltage response or mitigating electromagnetic or radiation interference effects on the MOSFET by controlling a semi-conductive channel region (SCR) using an additional gate, e.g., JFET, disposed perpendicularly with respect to the MOSFET configured to generate an electromagnetic field into the MOSFET's semi-SCR. A control system for controlling operation is also provided to include automated systems including sensors as well as manually operated systems. Automated systems can include radiation sensors as well as other control systems such as radio frequency transmitter or receiver systems. Methods of operation for a variety of modes are also provided.







Embodiments can be fabricated using different semiconductor type base materials (e.g., Si, SiC, and GaAs). Structures fabricated using a silicon base material could produce blocking voltages from a few volts to 150 volts depending upon the doping and thickness of epitaxial layer; and structures fabricated using a SiC base material could produce blocking voltages from a few volts to 1000 volts depending upon the doping and thickness of epitaxial layer (n-channel or p-channel). This Lateral Dual-Gate structure can be integrated using existing fabrication processes.

Expected Radiation Enhancements

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- Reduce Drain Leakage (Idss)
- Reduce Channel Inversion (Vth)

Heavy Ions
- Reduce Burnout
- Reduce Gate Rupture

Prompt Dose
- Reduce Burnout
- Reduce Channel Inversion (Vth)

The LDMOSFET portion of this structure is prone to radiation degradation; but that degradation is compensated by the radiation tolerant buried JFET structure.

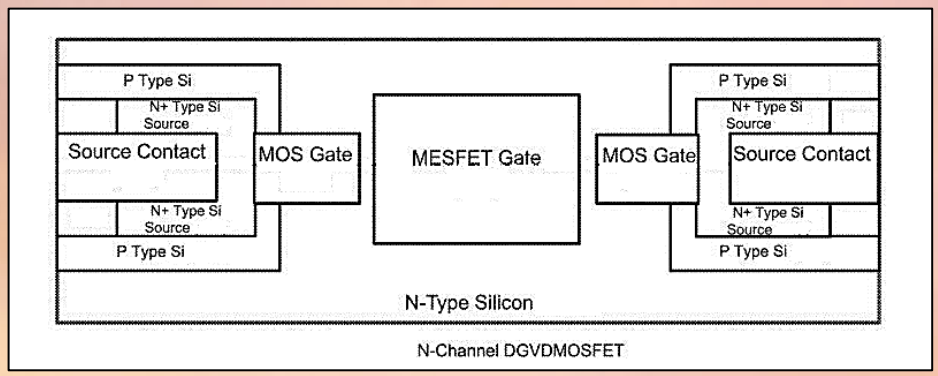
Patent details are available via the US patent and trademark office website: https://www.uspto.gov/patents

Integrated Vertical MOSFET/MESFET: 9,735,769

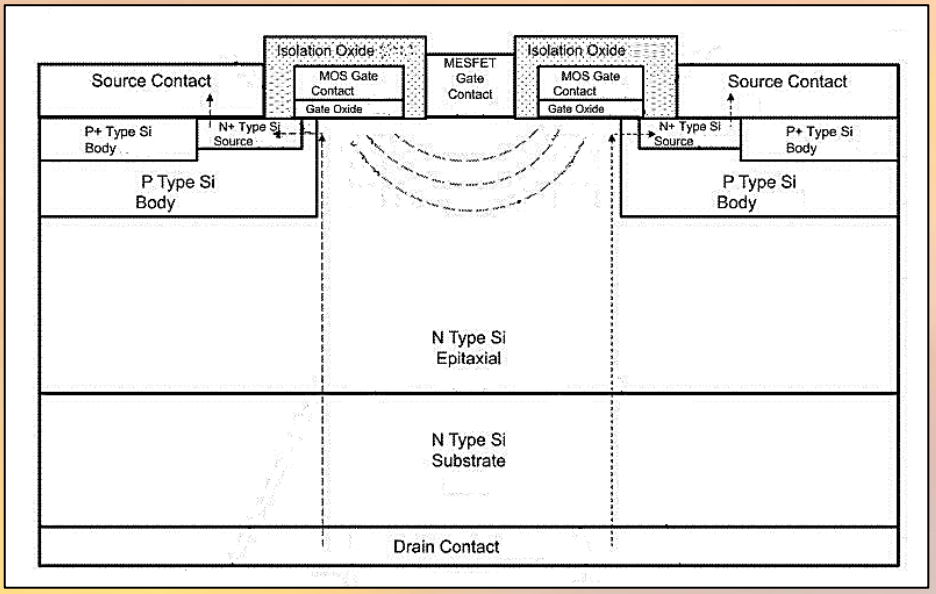
Abstract

Systems and methods for controlling current or mitigating electromagnetic or radiation interference effects using multiple different semi-conductive channel regions generating structures formed by multiple different semi-conductive electrical current or voltage control structures. One embodiment includes providing a first and second metal oxide semiconductor field effect transistor (MOSFET) sections formed on opposite sides of a metal-semiconductor field effect transistor (MESFET) such that operation of the MESFET modulates or controls current otherwise controlled by an electrical path of the MOSFET sections. A control system for determining when an embodiment of the invention is to be operated is also provided to include automated systems including sensors as well as manually operated systems. Automated systems can include radiation sensors as well as other control systems such as high voltage radio frequency transmitter or receiver systems. Methods of operation for a variety of modes are also provided.

Top Cross-Sectional View



Side Cross-Sectional View



Embodiments can be fabricated using different semiconductor type base materials (e.g., Si, SiC, and GaAs). Structures fabricated using a silicon base material could produce blocking voltages from a few volts to 1000 volts depending upon the doping and thickness of epitaxial layer; and structures fabricated using a SiC base material could produce blocking voltages from a few volts to 4800 volts depending upon the doping and thickness of epitaxial layer (n-channel or p-channel). This Vertical Dual-Gate structure can be integrated using existing fabrication processes.

Expected Radiation Enhancements

Total Ionizing Dose (TID)
- Reduce Drain Leakage (Idss)
- Reduce Channel Inversion (Vth)

Heavy Ions
- Reduce Burnout
- Reduce Gate Rupture

Prompt Dose
- Reduce Burnout
- Reduce Channel Inversion (Vth)

The VDMOSFET portion structure is prone to radiation degradation; but that degradation is compensated by the radiation-tolerant MESFET gate structure.

Patent details are available via the US patent and trademark office website: https://www.uspto.gov/patents

Patent Opportunities

Licensing Agreements

Cooperative Research & Development Agreement (CRADA)

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