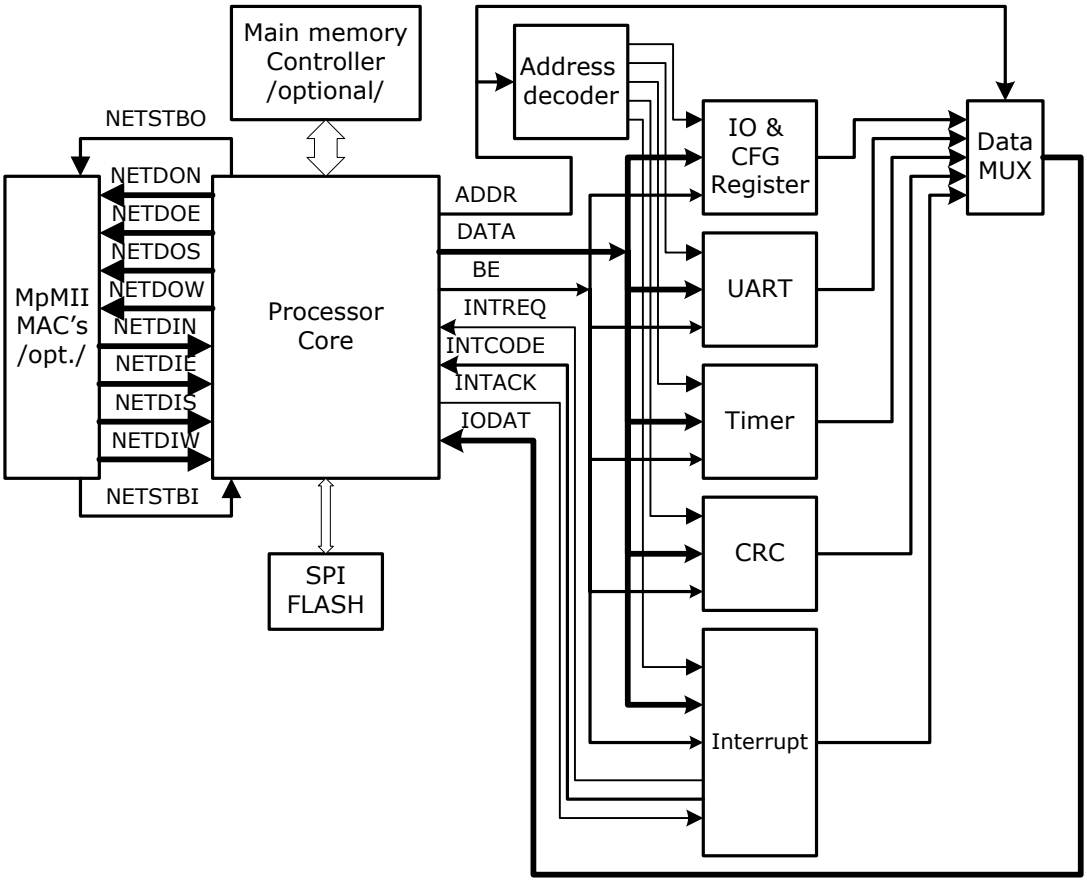
Contents

Basic Processor System Architecture

In the basic configuration, the processor system contains six main components:

1. The actual processor core.Core of any type: X32Carrier/X32/X16/X16E/X16DT/X16x2/X16x4/T2X16T2X32
2. Processor module configuration register.
3. System UART required for downloading and debugging software.
4. System timer.
5. CRC calculator.
6. Interrupt controller.



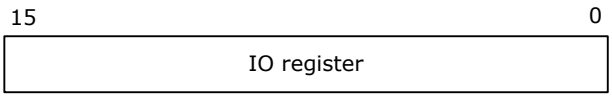
Board registers

To access system registers, an object with the 02h selector is used. This object is available only at privilege level zero. Kernel has a number of functions available from processes with privilege levels 1,2 and 3. These functions allow you to indirectly access the IO registers and configure the interrupt controller for the application hardware.

LED &| Keys

Offset: 00h /read and write/

Format:



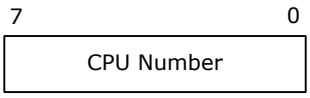
Description:

This register can be used for LED indication or to enter the status of any buttons or switches. The Kernel only uses bit 0 of this register to indicate activity.

CPU Number

Offset: 02h /read only/

Format:

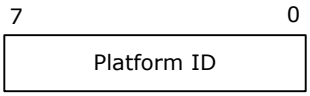


Description:

This register is used to set the value of the core number in a multi-core system, or to determine the base for core numbers for multi-core variants like X16x2 and X16x4.

FPGA platform identifier
Offset: 03h /read only/

Format:



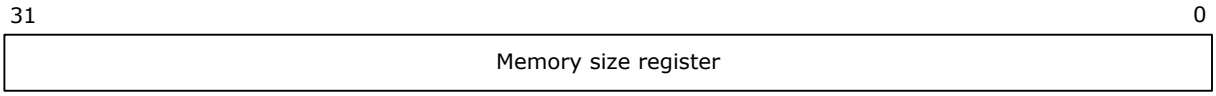
Description:

This register displays the type of platform the processor is running on.

Platform ID	***Description***
0	Arria II, EP2AGX125EF29I3
1	Arria V, 5AGTFC7H3F35I3
2	Kintex 7, XC7K420TIFFG901-2L
3	Stratix IV, EP4SGX530KH40C2
4	Stratix V, 5SGXEA7N2F45C2
5..255	Reserved

Memory size register
Offset: 04h /read only/

Format:

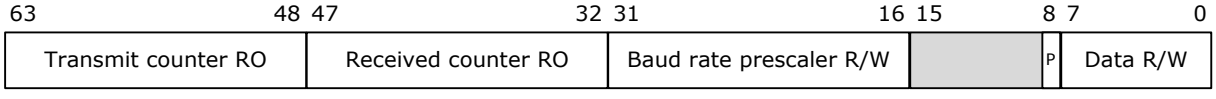


Description:

This register describes the size of the implemented system memory expressed in 64KB paragraphs. For example, if the system has a 2 GB memory module, then the register should contain the value 32768, and the value 4 would indicate a total of 256 KB. The value for the register is given by a constant in the top-level source code of the FPGA project.

UART registers
Offset: 08h

Format:



Description:

The low byte of the register is the output of the UART receive queue and the input of the transmit queue.

Bit 8 is read-only and indicates the validity of the read byte if P=1.

Bits 16 to 31 represent the divisor register used to set the desired baud rate. The UART is clocked by the same clock signal as the processor core and the divider expresses the number of clocks, which is one bit interval. Kernel uses 921600 baud to communicate with the computer.

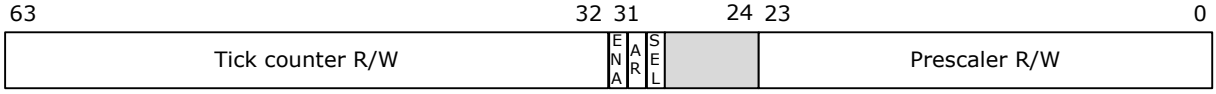
Bits [47:32] contain the value of the counter of bytes in the receive queue. Data reception from the UART can be controlled in two ways.

1. By parsing the P bit as each byte is read, all 16 bits must be read to correctly determine the validity of the byte read.
2. Using the counter of received bytes. It is necessary to read the value of the counter and if it is not equal to 0, then read the specified number of bytes from the FIFO.

Bits [63:48] contain a counter of bytes in the UART transmit queue and allow control over the transfer of data arrays to avoid queue overflows and data loss due to overflow.

Timer's register
Offset: 10h /read & write/

Format:



Description:

Prescaler is used to generate ticks from the main main clock of the processor core. In particular, Kernel programs the Prescaler to generate 1/128 second ticks.

The SEL bit is used to select the value read from bits [23:0] of the timer. When SEL=0, the current value of the Prescaler counter is read, and when SEL=1, the programmed counter recalculation value is read, upon reaching which the Prescaler is reset to zero.

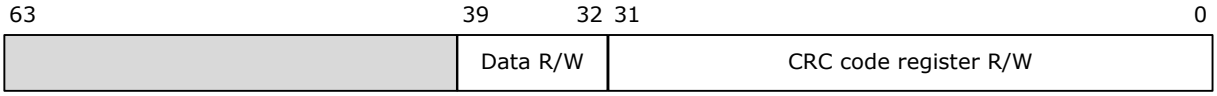
The AR bit controls the autoload mode. If AR=0, then when the programmed value is reached, the Prescaler stops counting. If AR=1, then when the recalculation value is reached, the Prescaler is reset to zero and the counting starts again.

The ENA bit enables the timer if it is set to 1.

The tick counter is incremented by 1 each time the Prescaler reaches the programmed value. It usually counts 7.8125 ms intervals. The timer can generate an interrupt request every 128th tick. But this interrupt is not used by Kernel yet.

CRC Generator
Offset: 18h /read & write/

Format:



Description:

CRC code generated in accordance with the IEEE 802 polynomial. The CRC register can be preset to any value. Before counting starts, it is usually initialized to 0FFFFFFFFh. The

calculation of the CRC for the data block is performed by sequential writing of bytes to bits [39:32] of the register. With each write, the CRC value is recalculated.

Interrupt index table
Offset: 40h /read and write/

Format:

63 48	47 32	31 16	15 0
Index IRQ15	Index IRQ14	Index IRQ13	Index IRQ12
Index IRQ11	Index IRQ10	Index IRQ9	Index IRQ8
Index IRQ7	Index IRQ6	Index IRQ5	Index IRQ4
Index IRQ3	Index IRQ2	Index IRQ1	Index IRQ0

Description:

This table contains 16 interrupt indexes for 16 interrupt controller inputs.

Interrupt Mask Register
Offset: 60h /read and write/

Format:

31 16	15 0
Mask Set WO	Mask & Mask Clear R/W

Description:

The lower 16 bits of the register, when read, return the interrupt mask. An interrupt is enabled if the corresponding mask bit is set to 1. Writing to the lower 16 bits of the register allows you to reset to 0 the mask bits for which the corresponding bits of the written word are set to 1. For example, if the current contents of the mask register is 0087h, then writing a 16-bit reset mask code 0080h will disable the IRQ7 interrupt and the mask register will have code 0007h.

The upper 16 bits of the mask register are write-only. To enable the interrupt, write a 1 to the corresponding bit of the mask setting code.

The interrupt is masked automatically when it is latched. Those. a bit in the mask register is cleared when the corresponding input interrupt is latched. Therefore, at the end of the interrupt processing, it is necessary to reset the desired bit in the mask register to enable a new interrupt.

After a system reset, the mask register is set to 0, which disables all 16 interrupts.