Board registers.

Registers of the LED/Key, system UART, system timer, CRC-generator and interrupt controller. This hardware is the minimum that required for the properly work of the kernel.

Object selector is 02h.

Offset	Bytes	Description
00h	2 r/w	LED's and Keys register.
02h	1 r	CPU number in the multicore network.
03h	1 r	Platform identifier. 0 – Arria II EP2AGX125EF29I3, 1 – Arria V 5AGTFC7H3F35I3, 2 – Kintex 7 XC7K420, 3 – Stratix IV /not implemented, 4 – Stratix V 5SGXEA7N2F45C2.
04h	4 r	Implemented system memory size in 64Kbyte paragraphs.
08h	1 r/w	UART data register.
09h	1 r	Bit 0 contains the flag of the presence of data in the UART receive queue /if 1/.
0Ah	2 r/w	Baud rate prescaler. Programmed for 921600 baud.
0Ch	2 r	Number of bytes in the receive queue.
0Eh	2 r	Number of bytes in the transmit queue.
10h	3 r/w	Prescaler register. Used to generate 1/128 sec. time slices.
13h	1 r/w	Timer control register. Bit 29 controls the output of the current value of the counter /at 0/, or the divider factor /at 1/ from the register at offset 14h. Bit 30 controls the autoreload of the counter when it reaches the divisor value /at 1/. Bit 31 enables timer operation if 1.
14h	4 r/w	Time slices counter.
18h	4 r/w	Register CRC code generated in accordance with the IEEE 802 polynomial
1Ch	1 w	A register for writing a byte to be added into a CRC code.
40h	32 r/w	16 16-bit words of the interrupt indexes for 16 interrupt channels.
60h	2 r/w	Read interrupt mask register /0 after reset/ and write mask clear code if bit Data[15:0] is set to 1.
62h	2 w	Write mask set code. Mask bit set to 1 if data bit Data[31:16] is set to 1.