A Few of Ted Hollinger Patents:

- **Patent number: 4895810**
  Abstract: A dopant-opaque layer of polysilicon is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop the substrate. A trench is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The trench sidewall is profile tailored using a novel O.sub.2 -- SF.sub.6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarizing layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer.
  Type: **Grant**
  Filed: May 17, 1988
  Date of Patent: January 23, 1990
  Assignee: Advanced Power Technology, Inc.
  Inventors: Theodore O. Meyer, John W. Mosier, II, Douglas A. Pike, Jr., Theodore G. Hollinger

- Topographic pattern delineated power MOSFET with profile tailored recessed source

Patent number: 5045903

Abstract: A dopant-opaque layer of polysilicon is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop the substrate. A trench is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The trench sidewall is profile tailored using a novel O.sub.2 -SF.sub.6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarizing layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer.

Type: **Grant**
Filed: November 16, 1989
Date of Patent: September 3, 1991
Assignee: Advanced Power Technology, Inc.
Inventors: Theodore O. Meyer, John W. Mosier, II, Douglas A. Pike, Jr., Theodore G. Hollinger, Dah W.

Tsang

- Method of making topographic pattern delineated power MOSFET with profile tailored recessed source

Patent number: 5019522

Abstract: A dopant-opaque layer of polysilicon is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop the substrate. A trench is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The trench sidewall is profile tailored using a novel O.sub.2 -SF.sub.6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structure, before depositing the conductive material. A planarizing layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer.

Type: **Grant**
Filed: January 2, 1990
Date of Patent: May 28, 1991
Assignee: Advanced Power Technology, Inc.
Inventors: Theodore O. Meyer, John W. Mosier, II,

Douglas A. Pike, Jr., Theodore G. Hollinger, Dah W. Tsang

- Semiconductor doping process

Patent number: 4766094
Abstract: A method for making a semiconductor device, such as a power-MOS transistor, wherein dopant is introduced into the structure underlying a lead contact pad to create a conducting subregion which minimizes electrical conductive breakdown.
Type: **Grant**
Filed: March 21, 1986
Date of Patent: August 23, 1988
Inventor: Theodore G. Hollinger

- Method for controlling electrical breakdown in semiconductor power devices

Patent number: 5434095
Abstract: A field-effect, power-MOS transistor wherein a region under the gate contact pad is specially doped with a dopant that is electrically compatible with that in the transistor's channel to obviate problems of electrical breakdown in that region.
Type: **Grant**
Filed: March 12, 1993
Date of Patent: July 18, 1995
Assignee: Sundstrand Corporation

- Semiconductor device with doped electrical breakdown control region

  Patent number: 5231474
  Abstract: A field-effect, power-MOS transistor wherein a region under the gate contact pad is specially doped with a dopant that is electrically compatible with that in the transistor's channel to obviate problems of electrical breakdown in that region.
  Type: **Grant**
  Filed: July 17, 1992
  Date of Patent: July 27, 1993
  Assignee: Advanced Power Technology, Inc.
  Inventor: Theodore G. Hollinger

- Frequency-dependent single-phase to three-phase AC power conversion

  Patent number: 4899268
  Abstract: Apparatus for supplying from a single-phase, known-frequency AC source, three-phase AC power at the same frequency. The apparatus features circuitry which employs high-speed power switching with respect to only one phase of a three-phase load, with the result that only two high-speed power-switching devices (transistors) are required.

- Type: **Grant**
  Filed: May 10, 1989
  Date of Patent: February 6, 1990
  Assignee: APC-Onsite, Inc.
  Inventor: Theodore G. Hollinger

- Mask-surrogate semiconductor process employing dopant protective region

  Patent number: 4748103
  Abstract: A mask-defect-immune process for making MOS semiconductor devices. The process features the creation of a surrogate mask in semiconductor wafer material per se, thus to eliminate the requirement that plural masks be used, and that plural mask alignments be performed. In all ways of practicing the invention, a surrogate mask is created in a dopant protective region.
  Type: **Grant**
  Filed: March 21, 1986
  Date of Patent: May 31, 1988
  Assignee: Advanced Power Technology
  Inventor: Theodore G. Hollinger

- Frequency-independent single-phase to three-phase AC power conversion

  Patent number: 4908744
  Abstract: Three-phase power-conversion wherein the

frequency output voltage is independent of the frequency of input voltage. One of three input terminals in a load powered by the apparatus is directly grounded. Each of the other two input terminals is supplied a sinusoidal voltage artifact from an appropriate transform circuit which is driven by a microprocessor, with one of these artifacts having a form 1.73.alpha.SinA, and the other having the form of 1.73.alpha.Sin(A+60.degree.), where .alpha. is the nominal amplitude of the source voltage and the Expressions A and (A+60.degree.) are the respective phase angles. Operation of the microprocessor controls output frequency.
Type: **Grant**
Filed: May 10, 1989
Date of Patent: March 13, 1990
Assignee: APC-Onsite, Inc.
Inventor: Theodore G. Hollinger

- Mask surrogate semiconductor process employing dopant-opaque region

Patent number: 5089434
Abstract: A dopant-opaque layer of polysilicon is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive

structure formed atop the substrate. A trench is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The trench sidewall is profile tailored using a novel O.sub.2 -SF.sub.6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarizing layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer.
Type: **Grant**
Filed: January 22, 1990
Date of Patent: February 18, 1992
Assignee: Advanced Power Technology, Inc.
Inventor: Theodore G. Hollinger

- Mask surrogate semiconductor process with polysilicon gate protection

Patent number: 5256583
Abstract: A dopant-opaque layer of polysilicon is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop the substrate. A trench is

formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The trench sidewall is profile tailored using a novel O.sub.2 -SF.sub.6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarizing layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer.

Type: **Grant**
Filed: January 7, 1992
Date of Patent: October 26, 1993
Assignee: Advanced Power Technology, Inc.
Inventor: Theodore G. Hollinger

Some of Ted Hollinger's Recent Patents:

Patent number: 7411310
Abstract: A distributed generator system is provided having an alignment hub to assist in the alignment and securement of an engine and a generator of the system. The system comprises a distributed generator system having an engine and a single bearing generator, and an alignment hub for defining an alignment position between the engine and the generator and maintaining the

alignment within a predetermined tolerance.
Type: **Grant**
Filed: April 7, 2005
Date of Patent: August 12, 2008
Assignee: Hydrogen Engine Center, Inc.
Inventor: Ted Hollinger

- Pigtailed stator windings for electrical generator

  Patent number: 7687960
  Abstract: A modified armature winding for a stator of an electrical generator having a pigtail shape to promote cooling of the stator. At least one turn of the windings is extended outside the circumferential periphery of the stator, preferably forming a loop. An electrical short is created near the circumferential periphery of the stator between the winding segments to prevent current from flowing through the pigtail winding segment.
  Type: **Grant**
  Filed: December 28, 2007
  Date of Patent: March 30, 2010
  Assignee: Hydrogen Engine Center
  Inventor: Ted Hollinger

- Devices, Systems and Methods for Closed Loop Energy Production

Patent number: 11371609

Abstract: Certain exemplary embodiments can provide a piston comprising a piston head, a connecting rod coupled to the piston head, a stabilizer bar, a retaining ring, and a stabilizer bar collar. The stabilizer bar collar defines one or more apertures. The one or more apertures are constructed to receive the stabilizer bar. The piston is constructed to reduce energy losses in an engine comprising the piston.

Type: **Grant**

Filed: September 30, 2019

Date of Patent: June 28, 2022

Inventor: Ted Hollinger

Patent number: 8025033

Abstract: Disclosed is a method of operating an internal combustion engine simultaneously with ammonia and another fuel. The other fuel may be hydrogen, ethanol, propane, natural gas, liquefied petroleum gas, or the like. In a preferred embodiment, the other fuel is hydrogen and the engine has zero carbon emissions. A control system is

programmable to adjust the proportion of ammonia and the other, catalyst fuel as selected by the operator.

Type: **Grant**

Filed: May 29, 2008

Date of Patent: September 27, 2011

Assignee: Hydrogen Engine Center, Inc.

Inventors: Mike Schiltz, Ted Hollinger, Don Vanderbrook