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ACCELERATING THE SOLDER PASTE EVALUATION PROCESS

Chrys Shea
Shea Engineering Services
East Greenwich, RI, USA
Chrys@sheaengineering.com

ABSTRACT

Solder paste can make or break the profitability of SMT processes. Using the proper chemistry is critical to a successful operation. Because solder pastes have so many different characteristics that affect their assembly line performance, they can be cumbersome and costly to evaluate. As a result, many assemblers are using mature formulations that have since been improved upon, simply because they don't have the resources to properly evaluate new, more process- or product-friendly materials.

This paper proposes a new solder paste evaluation regimen that helps engineers assess up to 25 solder paste properties on their assembly line in 5 hours or less.

KEY WORDS: solder paste, solder paste evaluation, solder paste qualification, SMTA test board, SMTA test vehicle, solder paste test kit.

INTRODUCTION

Why change solder pastes?

Because defects like solder balls, tombstones, skews, bridges, and voids can all be caused by the paste formulation. Process engineers and specialists can try changing stencil designs, padstacks and reflow profiles to mitigate defects, but if the solder paste is not a good match to the process or board design, their opportunities for improvement are severely limited. Upgrading to newer formulations has been shown to instantly reduce paste formulation-related defects.[1]

Why not change solder pastes?

The costs of line time, test assemblies, and technical resources add up fast. There's also the risk of overlooking a critical property of the paste and choosing the wrong one for the job, especially because there are no accepted industry test methods to determine paste performance on an actual assembly line.[2]

The SMTA Test Kit project was developed specifically to address paste-related cost concerns. It is a comprehensive standardized test which gathers information in a time efficient manner and enables customized, data-driven decisions on the best product for a given process.

Figure 1 shows the vision of the turnkey test kit.

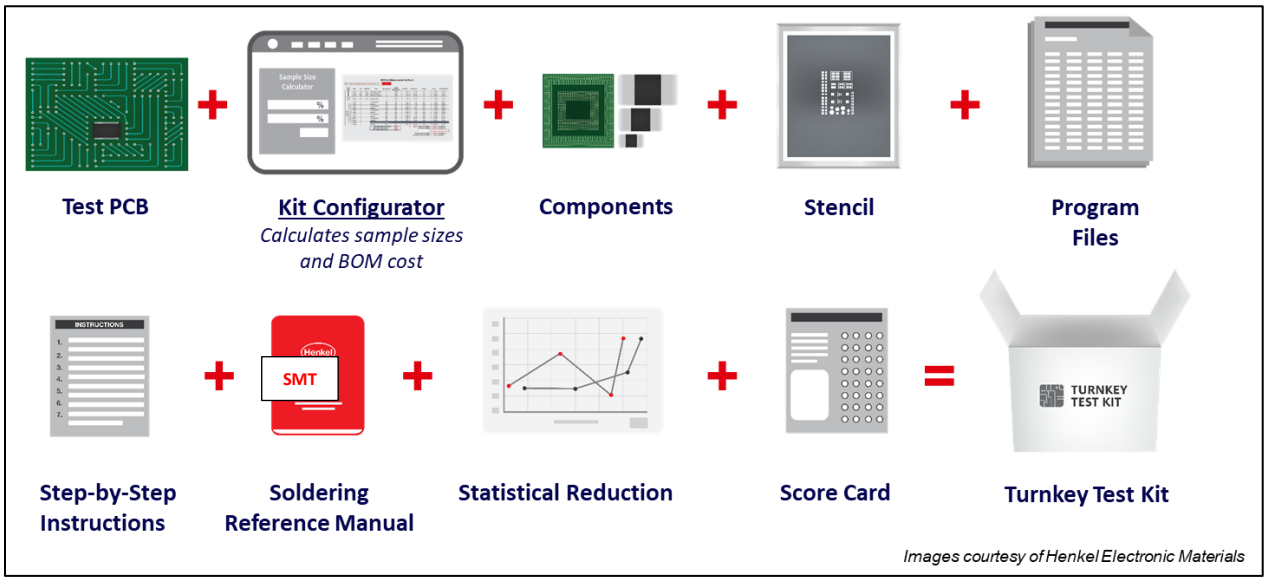

Figure 1. Solder Paste Evaluation Test Kit contents

TEST VEHICLE DESIGN

The SMTA Miniaturization Test Vehicle (MTV) is shown in Figure 2. The top side, or populated side, contains numerous miniaturized components:

- Eight 0.3 mm BGAs
- Nine 0.4 mm BGAs
- Ten 0.5 mm BGAs
- Four blocks of 008004 (0201M) components (100 each)
- Eight blocks of 01005 (0402M) components
- Eight blocks of 0201 (0603M) components
- Ten 0.4mm MLF components
- Additional 0402s, 0603s, and 1206s

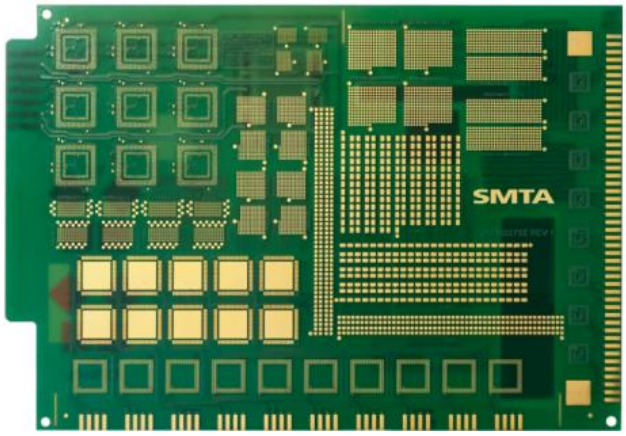

Figure 2. Test PCB Top Side

The bottom side, or unpopulated side shown in Figure 3, contains numerous paste property tests:

- Wetting
- Spread
- Slump
- Bridging
- Fine feature Printability (PTF or Print-To-Fail)

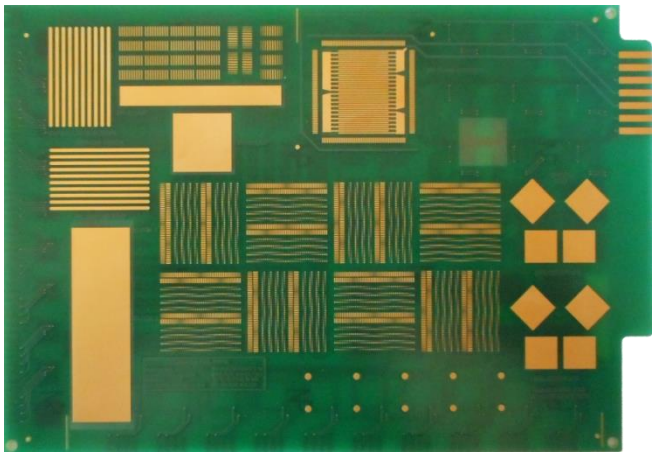

Figure 3. Test PCB Bottom Side

SOLDER PASTE PROPERTIES TESTED

Combining the layout of the PCB and a prescribed, nested test method enables the user to determine any of the following solder paste characteristics:

1. Transfer efficiency (Cpk)
2. Volume repeatability (Cpk)
3. Process capability (Cpk)
4. Peaking or dog-earring – visual, and heights
5. Response to abandon time (Cpk)
6. Response to Stencil life (Cpk)
7. Wipe sensitivity (under wipe between prints) (Cpk)
8. Hot and cold slump (SPI) - areas
9. Tack - visual
10. Voiding – BGA and QFN, Chip resistors (Visual/Xray)
11. Head-in-Pillow – BGA, CSP (Visual/Xray)
12. Tombstoning – Chip capacitor
13. Skewing – Chip capacitor
14. Solder balling and beading - Chip resistor (Visual/Xray)
15. Wetting to components (Visual)
16. Wetting to board surface finish (Visual)
17. Spread on board surface finish (IPC test)
18. Coalescence – small components (Visual)
19. Reliability (SIR, off-line, ICT)
20. Reflow residue cosmetics (Test Engineering, off-line)
21. Cleanability/Reliability (Ion Chromatography, off-line)
22. Post-reflow materials compatibility (off-line)
23. Material compatibility (Underfills, Conformal Coatings)

The 20+ solder paste characteristics that can be evaluated in the test regimen represent the needs of most assemblers. However, special needs can be addressed by modifying the test plan, or even the PCB layout itself.

The chart in Figure 4 show how the characteristics are grouped into similar property categories.

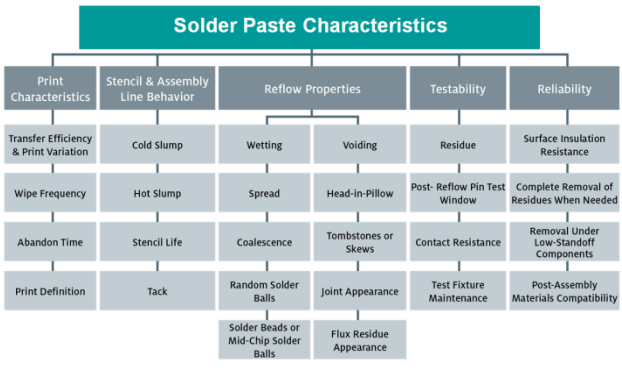

Figure 4. Solder paste characteristics chart

Figures 5 and 6 show the CAD images of the test board, and highlight each section of component footprints

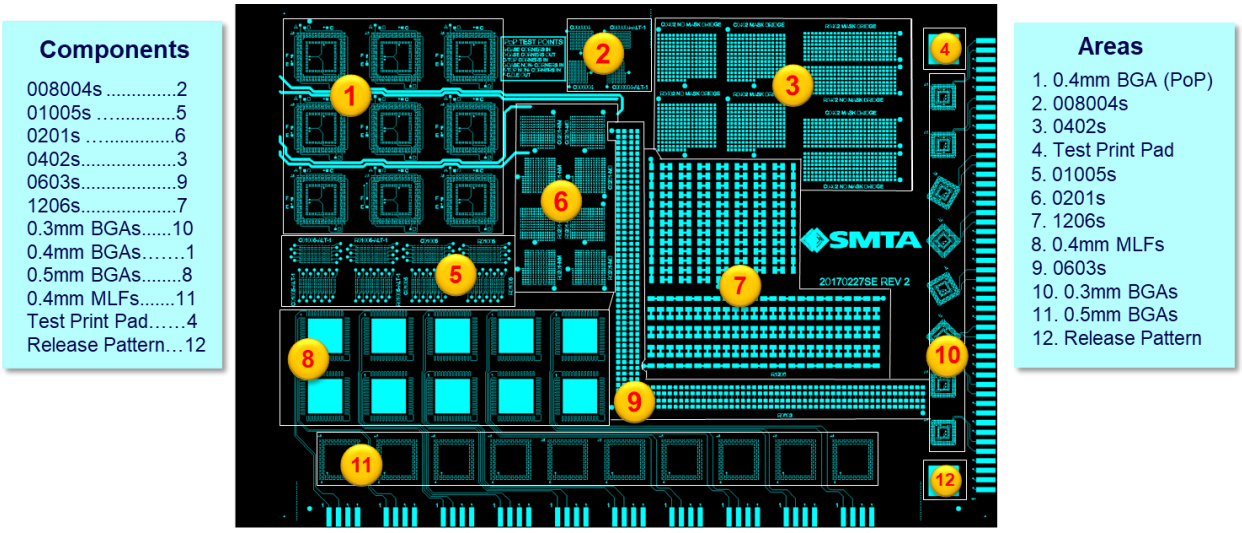

Figure 5. Top (populated) side layout

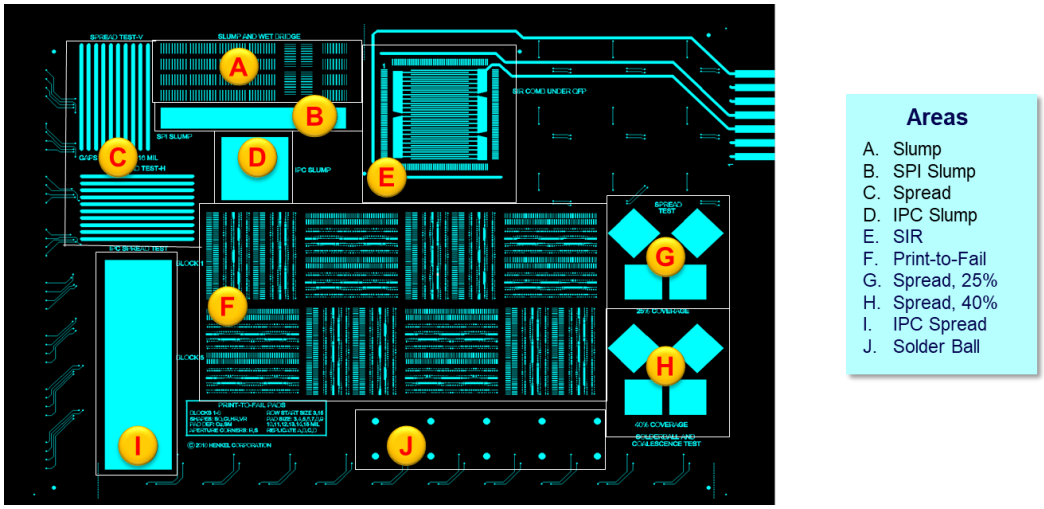

Figure 6. Bottom (unpopulated) side layout

For users specifically interested in transfer efficiency, the chart shown in Table 1 illustrates the area ratios for each land pattern at different stencil foil thicknesses.

Table 1. Area Ratios for PCB land patterns at various stencil foil thicknesses

Component Size		Type	Pad Size		Stencil Aperture Size		Area Ratios *Stencil Thickness - mil (µm)*				
Imperial	Metric		mil	µm	mil	µm	2 (50)	2.5 (68)	3 (75)	3.5 (88)	4 (100)
008004- ALT-1	0201M	Chip	4.7 x 5.7	120 x 145	4.7 x 5.7	120 x 145	0.64	0.52	0.43	0.37	0.32
008004- ALT-1 Rev 1.0	0201M	Chip	5.1 x 6.3	130 x 160	5.1 x 6.3	130 x 160	0.70	0.56	0.47	0.40	0.35
12 mil or 0.3mm pitch		BGA	6 - round	150 - round	6 x 6[1]	150 x 150[1]	0.75	0.60	0.50	0.43	0.38
16 mil or 0.4mm pitch		BGA	7.5 - round	190 - round	7.5 x 7.5[1]	190 x 190[1]	0.94	0.75	0.63	0.54	0.47
01005	0402M	Chip	8x8 (7 mil gap)	200 x 200	8 x 8	200 x 200	1.00	0.80	0.67	0.57	0.50
01005- ALT-1	0402M	Chip	8x8 (8 mil gap)	200 x 200	8 x 8	200 x 200	1.00	0.80	0.67	0.57	0.50
20 mil or 0.5mm pitch		BGA	10- round	250 - round	10 x 10[1]	250 x 250[1]	1.25	1.00	0.83	0.71	0.63

[1] - Square apertures with radiused corners

EASY SETUP

The documentation package for the test kit includes:

- ODB++ file
- BOM and sample size calculator spreadsheet
- Stencil Gerbers
- Step-by-step instructions for 30 print DOE
- Scorecard
- SPI and AOI programs as they become available

The test board should be no more difficult to program and set up as any new product; perhaps even easier due to the small amount of part numbers.

BOM and Sample Size calculator

An Excel spreadsheet displays component numbers and costs from a commercial dummy component provider[3]. The actual costs and the name of the provider have been omitted from Figure 7 to comply with anti-commercialism policies, but the actual web download will have the complete cost and provider information.

The calculator provides sample sizes based on the I/O of each component and displays them at the bottom of the sheet. Seeing the sample size and cost together can help make the tradeoffs between test materials cost and data quantity more transparent.

Kit Configurator for Miniaturization Test Board

Enter number of boards to populate in each of 10 print runs: 3

Comp Type	Pitch	I/O	Body Size	Type	Qty per board	# paste deposits/print	# of components	Unit	Cost Each	Cost/board	Reflow Qty	Set up Qty	# Components or Reels	Kit Cost	Item #	Description/ Component Name in ODB++ BOM
BGA/LGA	0.3mm	368	8mm	ChipArray - Very Thin	8	2944	24	Tray			3	12	36		31610	A-CVBGA368-.3MM-8MM-DC-LF-305
	0.4mm	620	14mm	Thru Mold Via PoP	9	5580	27	Tray			3	12	39		31558	A-TMV620-.4mm-14mm-DC-LF-125
	0.5mm	228	12mm	ChipArray - Very Thin	10	2280	30	Tray			3	12	42		31329	A-CTBGA228-.5mm-12mm-DC-LF-305
MLF/ QFN	0.4mm	100	12mm	Single Row MLF	10	1000	30	Tray			3	12	42		32202	A-MLF100-12mm-.4mm-DC-Sn-T
Discretes For overall defect rate, use capacitors For solderball analysis use resistors	1206	2		0 Ohm Resistor	50	100	150	T&R			3	reel	#DIV/0!		16047	1206SMR-PA-5K-Sn-0
	1206	2		Capacitor	50	100	150	T&R			3	reel	#DIV/0!		16604	1206SMC-PL-4K-LF
	0603	2		0 Ohm Resistor	50	100	150	T&R			3	reel	#DIV/0!		16070	0603-SMR-PA-5K-Sn-0
	0603	2		Capacitor	50	100	150	T&R			3	reel	#DIV/0!		16602	0603SMC-PA-4K-LF
	0402	2		0 Ohm Resistor	400	800	1200	T&R			3	reel	#DIV/0!		16069	0402SMR-PA-10K-Sn-0
	0402	2		Capacitor	400	800	1200	T&R			3	reel	#DIV/0!		16601	0402SMC-PA-10K-LF
	0201	2		0 Ohm Resistor	400	800	1200	T&R			3	reel	#DIV/0!		19865	0201SMR-PA-15K-Sn-0-P
	0201	2		Capacitor	400	800	1200	T&R			3	reel	#DIV/0!		11710	0201SMC-PA-15K-LF-M
	01005	2		0 Ohm Resistor	400	800	1200	T&R			3	reel	#DIV/0!		19921	01005SMR-PA-TRB-LF-0
	01005	2		Capacitor	400	800	1200	T&R			3	reel	#DIV/0!		19481	01005SMC-PL-TRB-LF
	008004	2		*Resistor is not available at this time*												
	008004	2		Capacitor	400	800	1200	T&R			3	reel	1200		19220	008004SMC-5K-LF

Total Paste Deposits per board	17804
Total Solder Joints per run	53412
Total Opportunities per run	62524

Kit Cost with 008004 *per run*
Kit Cost w/o 008004 *per run*

* Reels of 01005s are $500 for 5K parts
Reels of 008004s are $2,000 for 5K parts

Kit excl 01005 and 008004 *per run*
Board excl 01005 and 008004 *per board*

Figure 7. Configurator, or BOM and sample size calculator

TEST EXECUTION

Designed-In Experiments

The PCB's topside layout has several DOEs embedded in it:

QFN Center Pad Voiding
- 5 aperture designs
- 2 replicates (10 components) + overprint on toes, as seen in Figure 8.

1206, 0603
- 1 variable – vertical or horizontal mounting, user chooses components
- 100 replicates (200 components)

0402, 0201
- 3 variables – resistor or capacitor, vertical or horizontal mounting, solder mask bridge or no solder mask bridge between pads.
- 100 replicates (800 components)

01005
- 3 variables – resistor or capacitor, vertical or horizontal, different pad spacings (no room for solder mask bridges)
- 100 replicates (800 components)

008004
- 2 variables – capacitors only, vertical or horizontal mounting, different pad sizes
- 100 replicates (400 components)

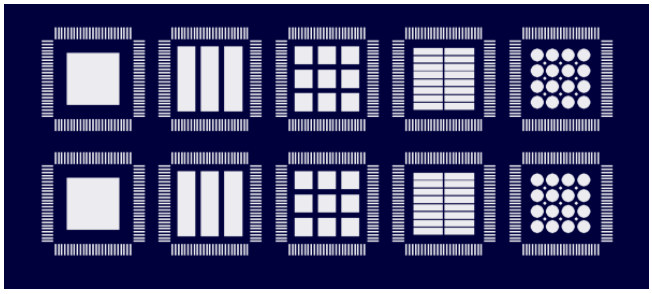

Figure 8. MLF aperture designs

The unpopulated side offers both standardized and original test patterns with the following sample sizes[4]:

- Slump:
  - Industry standard test pattern, n=1
  - Internally developed for visual inspection, n=240
  - Internally developed for automated solder paste inspection, n=60
- Solder Ball:
  - Industry standard test patterns, n=10
- Spread:
  - Industry standard test patterns, n=10
  - Internally developed, n=8
  - Internally developed, n=20
- SIR:
  - Industry standard test patterns, n=1
- Fine Feature Printing, also known as PTF (Print-To-Fail) Patterns

The eight PTF test cells produce 64 mask- or copper-defined circles and squares, and 32 copper-defined rectangles in each direction, with apertures at 1:1 and the same shape as the pad.

Each cell repeats the pattern twice. The top portion prints "squircles," or radially cornered apertures. The bottom portion prints apertures the same shape as the pads: square, circular or rectangular. This design is meant to demonstrate the effect of aperture design on deposition quality. Solder mask defined rectangles were intentionally omitted to utilize the space for better process-indicating features. An example of the test cell is shown in Figure 9.

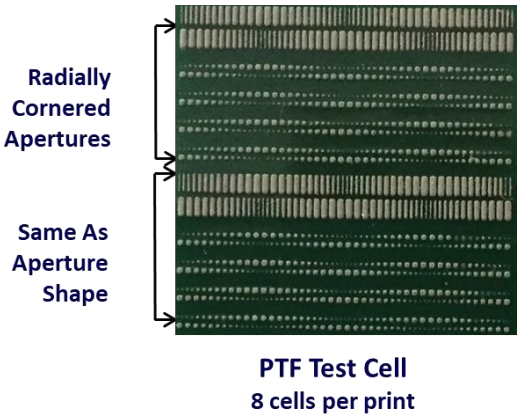

Figure 9. Print-to-Fail (PTF) test cell

The radially cornered apertures more than 8 mils (200 µm) wide have corner radii of 2 mils; apertures less than 8 mils wide have corner radii 25% of their width. The area ratios for apertures range from 3 to 15 mils is 0.19 to 0.94.

The majority of production facilities will be most interested in the feature ranges of 7 -10 mils, or area ratio ranges of 0.44 to 0.63, which represent the demands of the near term on the low end, and a baseline of well-controlled printing on the high end.

More documentation slump, solder ball, wetting and spread tests analysis will be included in the next technical paper on this topic.

Maximizing Test Efficiency

To gather the most data with the least resource expenditures, the tests have been nested, enabling the concurrent execution of multiple assessments.

First, the populated side is printed, placed and reflowed. The stencil is then set aside to introduce abandon time tests, and the unpopulated side is loaded up. Boards are printed and reflowed; then the paste gets kneaded to shear it for a fixed period of time. It is then printed and reflowed again to evaluate its stencil and production line life. After the post-shear run on the unpopulated side, the populated side is reinstalled and the solder paste's response to abandon time – or how many prints it takes to return to a steady state and if

it reflows as well – are measured. Figure 10 shows a flowchart of the test process.

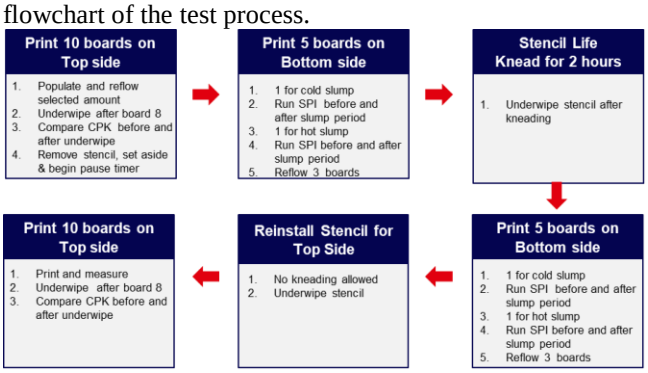

Figure 10. Nested test order

A copy of the DOE spreadsheet can be seen in Appendix A.

DATA ANALYSIS

The Scorecard

A scorecard helps the users customize their paste selection to fit their specific process or product needs.

Prior to executing the tests, the user reviews the solder paste characteristics tested on the PCB and determines each one's relative importance to their operation. For example, if an assembler runs high-volume production, then recovery from abandon time is far less important than it is to a low-volume operation that has many stops and starts.

After running the tests and compiling the data, the user then ranks each solder paste's characteristics relative to each other. The poorest performing product receiving a score of 1 and the best performing product receives the highest score, equal to the number of products in the trial. Typically four or five pastes are compared at a time. The rest are ranked in ascending order based on their performance. The relative ranking achieves three goals:

1. Smoothly blend objective data, like Cpk, with subjective data, such as solder joint appearance.
2. Easily compare tradeoffs between different formulations.
3. Provide a baseline with the current product and provides insight on what the assembler can expect when introducing a new selection.

The basic categories of solder paste performance include:

- Printability
- Reflow
- Testability
- Reliability
- Supplier Support and Value

The scorecard shown in Figure 11 breaks each major category into subcategories. Relative solder paste performance for each major category is judged by viewing their weighted subtotals at the bottom line of each section.

Complete weighted totals are shown at the bottom of the sheet. Typically, the best performer is the solder paste with the highest overall score. Sometimes, however, the runner up takes the prize. The highest scorer may have a disappointing flaw – such as high voiding, solder balling, graping, peaking, or low wipe frequency – that can't be tolerated.

It is not uncommon for a solder paste's performance to be great in one category yet mediocre, or even weak in another. Solder paste characteristics are balanced during formulation where often a particular characteristic is optimized. There are always performance tradeoffs, even in the most successful products.

SMT operations also have their strengths and weaknesses; therefore, finding the optimum solder paste for a specific process requires investigation of the properties most critical to the operation. The scorecard provides a data–driven method for examining and comparing such properties.

Weighting key:
10- critical
7.5-Very Important
5-Important
2.5-Less Critical/ Important
1-not Critical

Ranking:
4 - Best
1 - Worst
In case of tie both get equal rank and next one drops (eg. 4,3,3,1)

Solder Paste Score Card - Rank Order for Each Solder Paste Characteristic

Note: the numbers in red are examples of user input

Weight		Category	Paste A	Paste B	Paste C	Paste D	Criteria	Comments
		PRINTABILITY/PRODUCTION WORTHINESS						
33.5	10	Transfer Efficiency and Variation - Cpk					Cpk - goal is >2.0; >1.66 is also acceptable	Volumes of 8-12 mil features (AR 0.50 to 0.75)
	5	Wipe frequency requirements					Compare Cpks before and after wipe	8 prints before wipe; 2 (or 12) prints after
	2.5	Recovery from Abandon Time					Compare Cpks before and after abandon	Cpk post-abandon ***and*** number of prints required to return to steady state
	2.5	Print Definition (peaking or dog ears)					Average heights or visual scale	Heights on QFN I/Os at comparable Transfer Efficiencies or Visual Scale if no SPI
	1	Cold Slump					IPC or alternate patterns	Visual or SPI 20 minutes after printing (ambient)
	2.5	Hot Slump					IPC or alternate patterns	Visual or SPI 20 minutes after printing (182 C)
	5	Stencil Life					Cpk before and after 2 hour shear down	Cpk post-shear, also visual assessment of print definition
	5	Tack					Part locations on board held prior to placement	Needed for XY movement and transport of PCBs, pre-reflow AOI is helpful
		Weighted Category Results	*0*	*0*	*0*	*0*		
		REFLOW						
77.5	7.5	Wetting					Wetting test on copper pad or wetting to components	Wetting and spread are different
	2.5	Spread					Spread test on copper traces	A component can wet but not spread, however, it will not spread if it doesn't wet
	5	Coalescence/graping					Assessment of joint surface, solder ball test	Smaller features more likely to grape, larger overprints less likely to coalesce
	7.5	Random solder balls					Total quantity violating solder ball criteria	IPC - not large enough to bridge the smallest I/O conductor gap on the PCB
	5	Solder beads or mid-chip solder balls					Total quantity violating solder ball criteria	*or* alternate criteria set by assembler or OEM
	10	Voiding					Void % (typically <30%) and total number of voids	Usually, more smaller voids are preferable to fewer larger voids for any overall %
	10	Head-In-Pillow					# of defects found at X-Ray	Multi-chip packages show non-traditional warpage and HiP locations
	10	Tombstones/skews/positional errors					IPC Class 1, 2 or 3 defects or alternate criteria	Product dependent
	7.5	Joint Appearance					Wetting angle, reflectivity, ease of inspectability	Very subjective based on inspectors' eyes, example photos are important
	5	Flux Residue Appearance					Amber or clear, brittle or sticky, spread	Subjective but example photos are very important
	7.5	Compatiblity with current AOI					# of false calls	Too many false calls can require tweaking parameters for all production programs
		Weighted Category Results	*0*	*0*	*0*	*0*		
		TESTABILITY						
0		Residue probe-ability					Visual or tactile; flying probe if available	Residues should comply but not shatter
		Post-reflow pin probe time window					Number of days before false fails occur	Depends on paste, heat exposure, reflow environment, ambient environment
		Contact resistance					Resistance measurements	Initial, and track increase over days after reflow
		Test Fixture Maintenance					Test Engineering analysis or assessment	Can be subjective
		Weighted Category Results						
		RELIABILITY						
0		Surface Insulation Resistance					>10^8 Ohms per J-STD-004B	3rd party verification in SIR chamber
		Complete removal of residues					ROSE, <6 ug NaCl equiv/sq in, or Ion Chromatography	ROSE tests overall wash process; IC tests in specific areas
		Residue removal under low-standoff					Ion Chromatography	Upper limits vary by product and test method
		Post-assembly materials compatiblity					Specific to post-assembly process	Underfill, conformal coating, potting
		Weighted Category Results	*0*	*0*	*0*	*0*		
		SUPPLIER RATING AND VALUE PROPOSITION						
0		Distribution/ Supply Chain					Local distribution channels to maintain inventory	2 different lots always available
		Technical Support					Tech support: responsiveness, accessability and resource	Support during trials indicates capabilities
		Shelf Life/ Storage Conditions					Assmembler sets criteria	WS shorter shelf life than NC. Some need refrigeration and others don't.
		Reclaim Services					Reclaim availability	Very important if wave soldering
		Compaitibility w/ under stencil chemistry					Flux dissolves in current chemistry for under wipe	IPA is not compatible with all NC lead-free pastes
		Lead version available same flux vehicle					Lead and lead-free have same flux vehicle	If using both alloys, both pastes would have similar print properties
		Weighted Category Results	*0*	*0*	*0*	*0*		

Total points: 111

	Paste A	Paste B	Paste C	Paste D
OVERALL WEIGHTED TOTAL:	0	0	0	0
Normalized on 1-4 scale (4=best)	0.0	0.0	0.0	0.0

Figure 11. Solder paste evaluation scorecard

SUMMARY

The intent of the test kit concept is to make solder paste testing fast, easy, and as straightforward as possible. All the pieces of the kit were designed with ease of use in mind.

The common test vehicle will enable different users to compare experimental results, leading to faster process development and dissemination of knowledge.

FUTURE WORK

A website where experimental results can be uploaded and essential files for testing can be downloaded, is currently under construction.

The downloadable files will include:

- Kit configurator, or BOM cost-sample size spreadsheet
- Stencil Gerbers
- Pick and Place files
- ODB++ files
- Scorecard

When the website is complete, it can be linked to from the SMTA main website. Until then, files can be obtained by emailing the author (chrys@sheaengineering.com) directly.

The website is expected to host uploaded experimental results. Investigators will be able to share, review, or post suggestions in a discussion forum which will also be on the website.

Additionally, PCB support tooling has been designed for MPM, DEK and EKRA printers. It is available through a quick-turn printer tooling manufacturer[5].

AVAILABILITY

As of February 2019, the first production lot of PCBs are on order and will undergo a First Article Inspection prior to their commercial release. The kit's elements are complete, with the exception of the reference manual and the publication of the statistical methods.

Based on the best information at the time of publication, PCBs should be available by the beginning of April 2019, with the website up shortly thereafter. The reference manual and statistical methods are anticipated to be available online by late summer 2019.

REFERENCES

[1] R. Lawrence andC. Shea "Solder Paste Qualification Testing for EMS Production,"Proceedings of the SMTA International Conference, October, 2017

[2]Results of on-line poll of SMTA webinar attendees during presentation of the test kit, March, 2018.

[3] Practical Components, Los Alamitos, CA

[4] Dixon, D., et al, "Development of a Solder Paste Test Vehicle for Miniaturized Surface Mount Technology," Proceedings of IPC APEX/EXPO 2018

[5] Rapid Tooling, Plano, TX

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Appendix A
Nested Solder Paste Evaluation Steps

Solder Paste Qualification Tests Page 1

Start Time: _____

	Print Speed: _____	**Print Pressure:** _____	**Separation Speed:** _____	**Squuegee Length** _____	
	Populated (Top) Side				
Print and Reflow	**Print Number**	**Board/Barcode Number**	**SPI index Number**	**SPI Time Stamp**	**Populate (Y/N)**	**Reflow (Y/N)**	**Observations/Comments**
	KNEAD TO ACHEIVE WORKING STATE and CLEAN STENCIL					**Underwipe 2-3X. Start print with back->front**
	1	**001**			**Y**	**Y**	**POPULATE AND REFLOW**
	2	**002**			**Y**	**Y**	**POPULATE AND REFLOW**
	3	**003**			**Y***	**Y***	**HOLD AND POPULATE/REFLOW WITH SECOND SET**
	4	**004**			N	N	
	5	**005**			N	N	
	6	**006**			N	N	
	7	**007**			N	N	
	8	**008**			N	N	
	Clean stencil with Wet-Vac-Vac wipe					
	9	**009**			N	N	
	10	**010**			N	N	
	Stop Time: _____					

>>> Remove Stencil for Abandon Time Test <<<

Set stencil on another frame, paste side up, and cover it with cardboard from the stencil box. Set timer for 4 hours.

Solder Paste Qualification Tests Page 2

Start Time: _____

Unpopulated (Bottom) Side

Print, Slump and Stencil Life

Print Number	Board/Barcode Number	SPI index Number	SPI Time Stamp	Cold Slump	Hot Slump	Observations/Comments
KNEAD TO ACHEIVE WORKING STATE and CLEAN STENCIL						Underwipe 2-3X. Start print with back->front
11	101			Y	N	SPI, Set timer for 20 minutes - SPI
Clean stencil with 1 Wet-Vac-Vac wipe						
12	102			N	Y	SPI->Place in box oven at 182°C for 20 minutes and set timer - >SPI
Clean stencil with 1 Wet-Vac-Vac wipe						
13	103			N	N	Reflow
14	104			N	N	Reflow
15	105			N	N	Reflow
Stop Time: _____						
11	101a			Post-slump SPI of print 22		2nd SPI for slump readings
12	102a				Post-slump SPI of print 23	2nd SPI for slump readings

>>> Knead continuously for 2 hours <<<

Set printer for continuous knead or maximum number of knead strokes. Set timer.

Solder Paste Qualification Tests Page 3

>>> After continuous kneading, underwipe the stencil 2-3X to remove the excess solder paste <<<

Start Time: _____

Unpopulated (Bottom) Side

Print, Slump and Stencil Life

Print Number	Board/Barcode Number	SPI index Number	SPI Time Stamp	Cold Slump	Hot Slump	Observations/Comments
CLEAN STENCIL						Underwipe 2-3X. Start print with back->front
16	206			Y	N	SPI Set timer for 20 minutes - SPI
Clean stencil with 1 Wet-Vac-Vac wipe						
17	207			N	Y	SPI->Place in box oven at 182°C for 20 minutes and set timer - >SPI
Clean stencil with 1 Wet-Vac-Vac wipe						
18	208			N	N	Reflow
19	209			N	N	Reflow
20	210			N	N	Reflow
REMOVE AND CLEAN STENCIL						Clean in offline stencil cleaner and return to storage
Stop Time: _____						
16	206a			Post-slump SPI of print 127		2nd SPI for slump readings
17	207a				Post-slump SPI of print 128	2nd SPI for slump readings

>>> Reinstall Top Side Stencil <<<

Do NOT knead

Solder Paste Qualification Tests Page 4

Start Time: _____

Populated (Top) Side							
Print and Reflow	Print Number	Board/Barcode Number	SPI index Number	SPI Time Stamp	Populate (Y/N)	Reflow (Y/N)	Observations/Comments
	NO KNEADING!!! CLEAN STENCIL						Underwipe wet-vac-vac. S
	21	301			Y	Y	POPULATE AND REFLOW
	22	302			Y	Y	POPULATE AND REFLOW
	23	303			N	N	POPULATE AND REFLOW BOARD #3 FROM EARLIER
	24	304			N	N	
	25	305			N	N	
	26	306			N	N	
	27	307			N	N	
	28	308			N	N	
	Clean stencil with Wet-Vac-Vac wipe						
	29	309			N	N	
	30	310			N	N	
	REMOVE AND CLEAN STENCIL						Clean in offline stencil cleaner and return to storage

Stop Time: _____

Tests are complete