



Deep Dive into PCB Characteristics for Correlation/Simulation at 224G and Below

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Samtec, Inc.

- This presentation is based on the work from our 2024 DesignCon presentation:

Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz

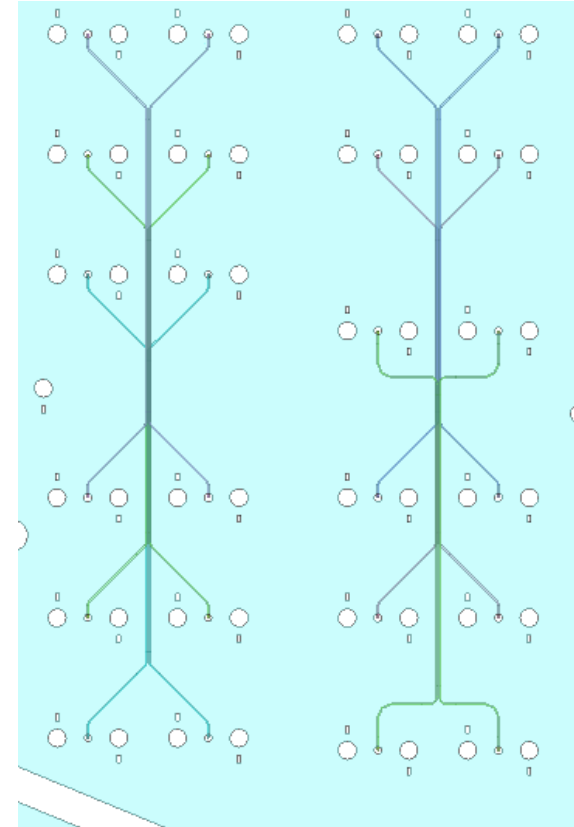
- For a more complete discussion of the topic, please see that presentation/paper
 - [Reach out to DesignCon for information on accessing the conference materials](#)

Introduction

- This presentation will discuss building nominal PCB simulation models
 - Nominal models are built prior to the board being fabricated
 - They are meant to predict final PCB performance
 - Used for optimization
- Getting the nominal model wrong means wasted resources
 - Engineering hours to redo and fix the problem
 - Money on fabricating multiple revisions of a PCB
- The goal is to get build an accurate model the FIRST time

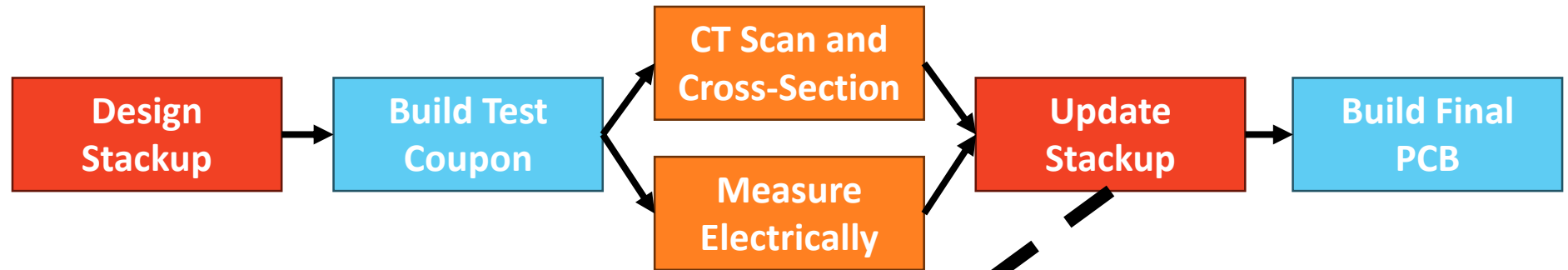
Introduction

- It takes a lot of work to build an accurate nominal model
 - Correctly modelling stackup
 - Getting all geometry accurate
 - Accurately modelling material properties
- There are many techniques that go into nominal models
 - Topic of numerous research since Signal Integrity became a field
 - Some of the information is conflicting
 - Some is also only accurate to certain structures

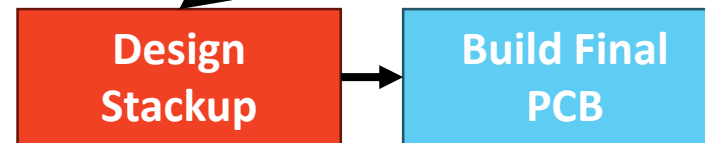


Workflows of PCB Design

With Test Coupon:



Without Test Coupon:

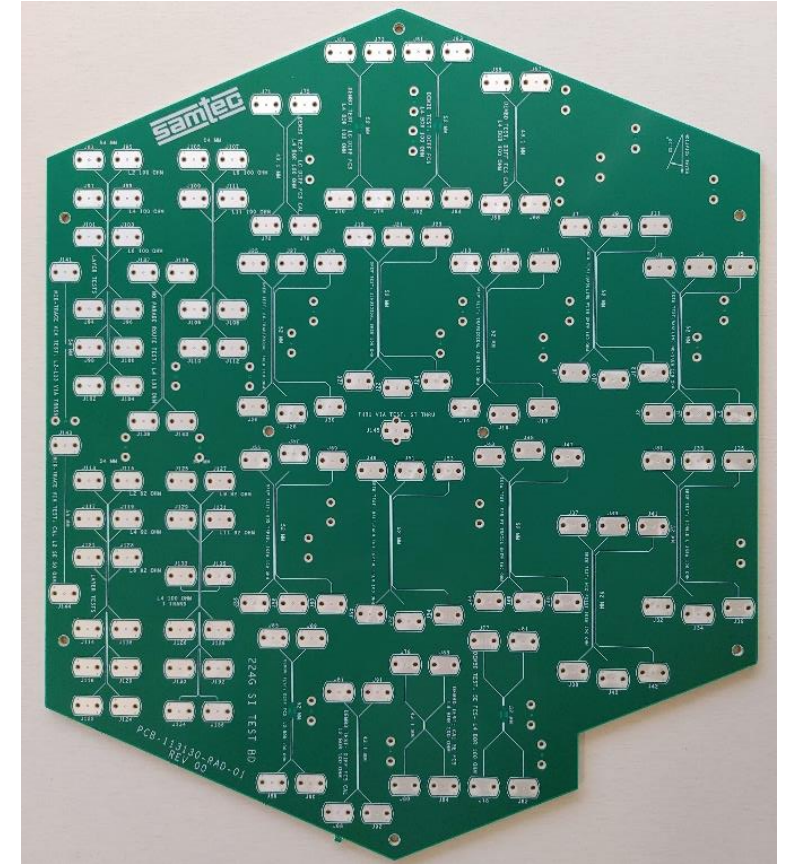




Case Study into PCB Design Without a Test Coupon

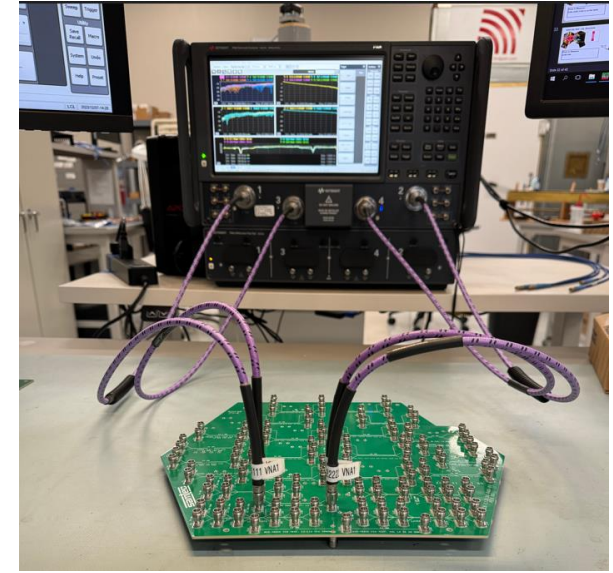
224G PCB Overview

- This PCB was designed and built by Samtec to test 224G PCB performance
 - Build on next-gen materials
 - Designed with a bandwidth of 70-80GHz
 - Designed using best-practices for PCBs
- This PCB will be used to show reasonable correlation
 - Close correlation can be achieved without prior stackup characterization

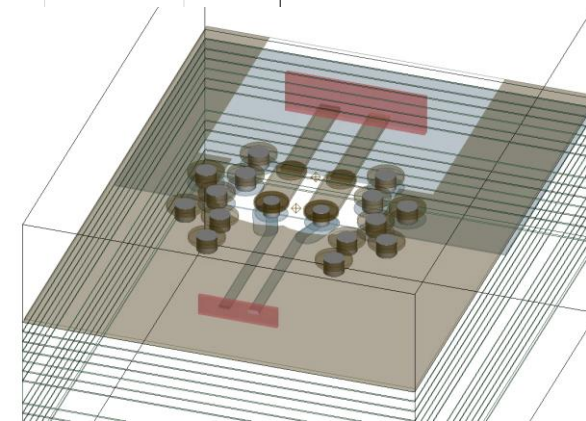
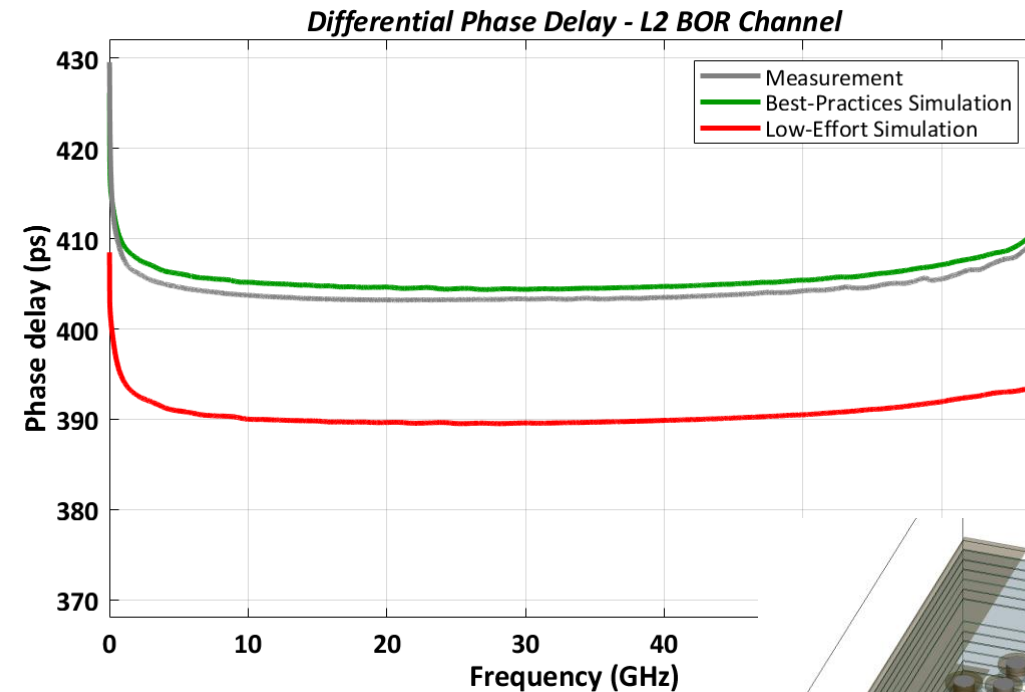
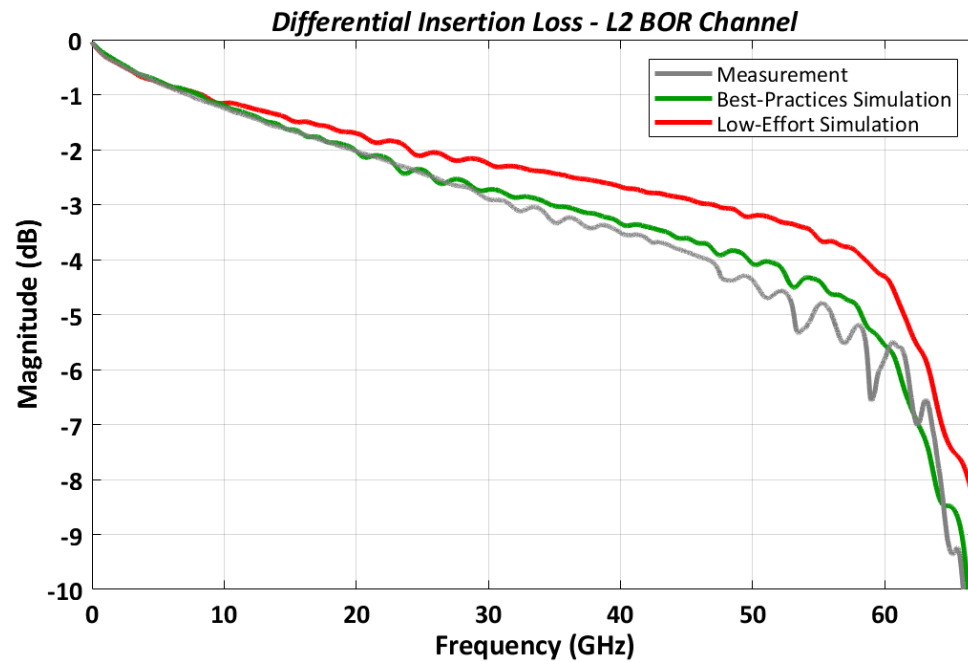


Overview of Data

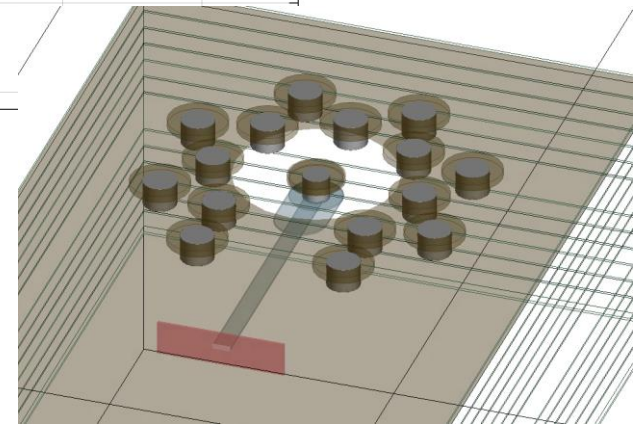
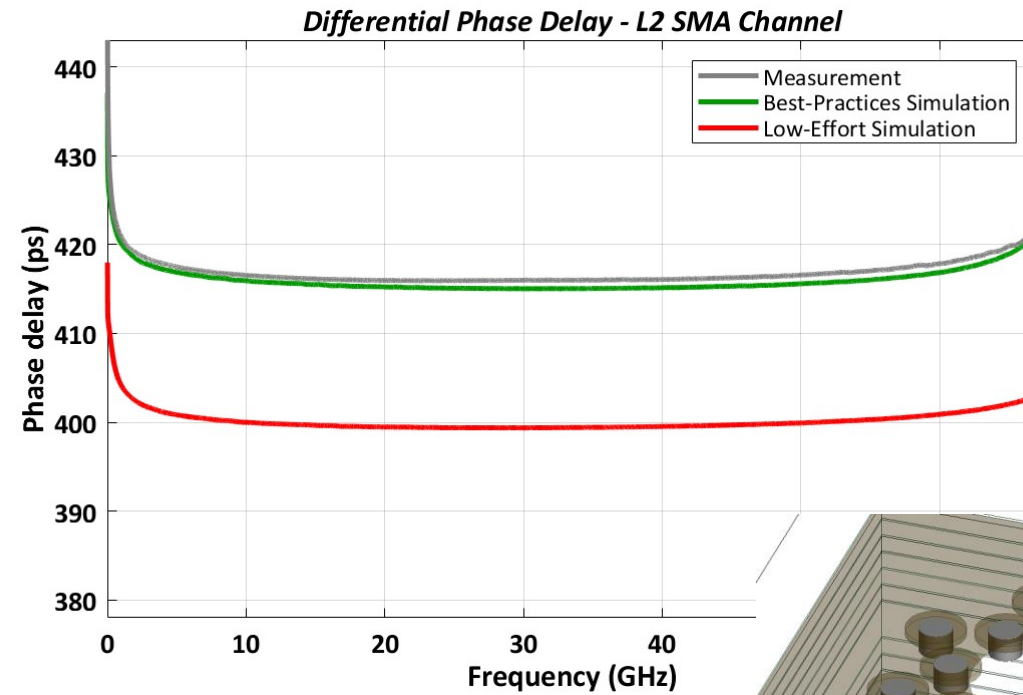
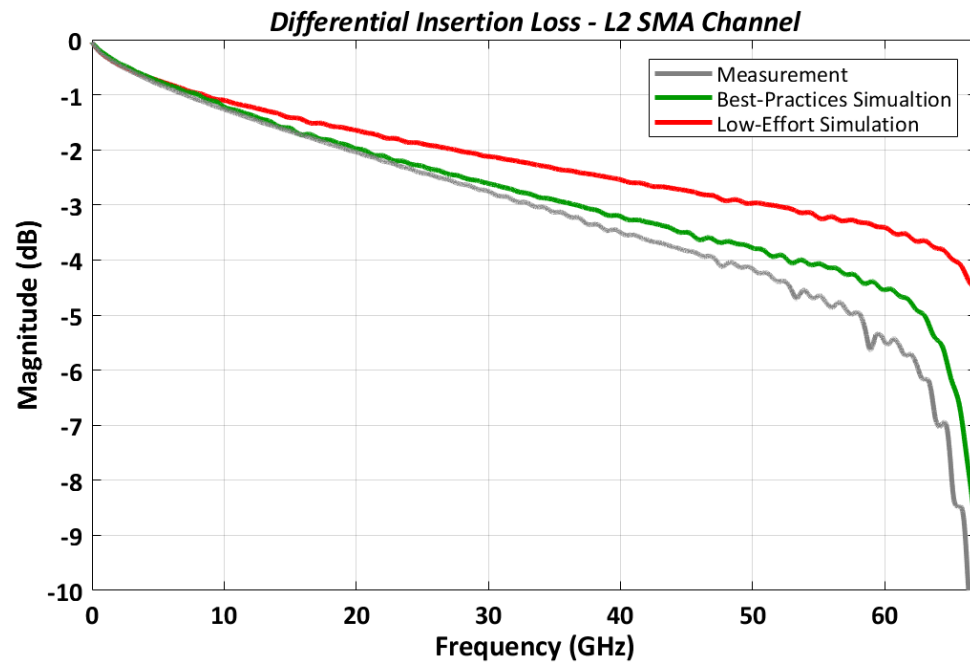
- The measurements will show:
 - Measurement Data
 - Best-Practices Simulation
 - Low-Effort Simulation
- Both simulations use the same:
 - Dimensions of structures
 - Values for relevant characteristics
- Simulations differ only in simulation methodology
 - Implementation of characteristics
- Manufacturing variation is not included



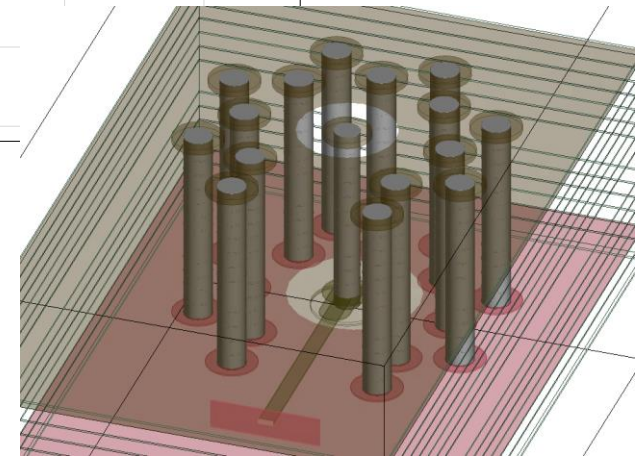
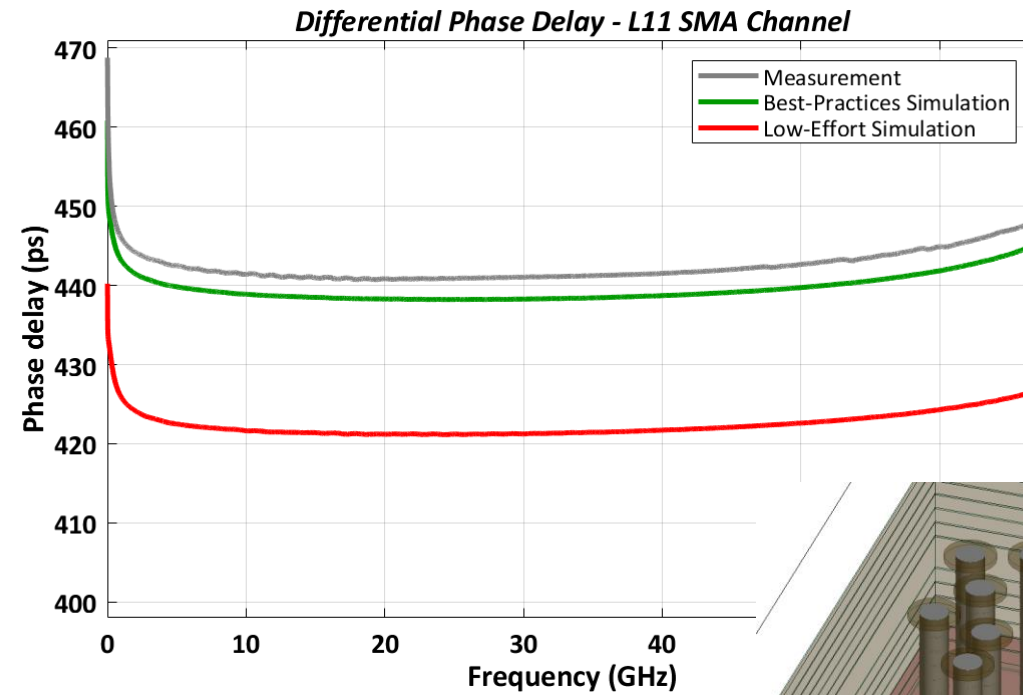
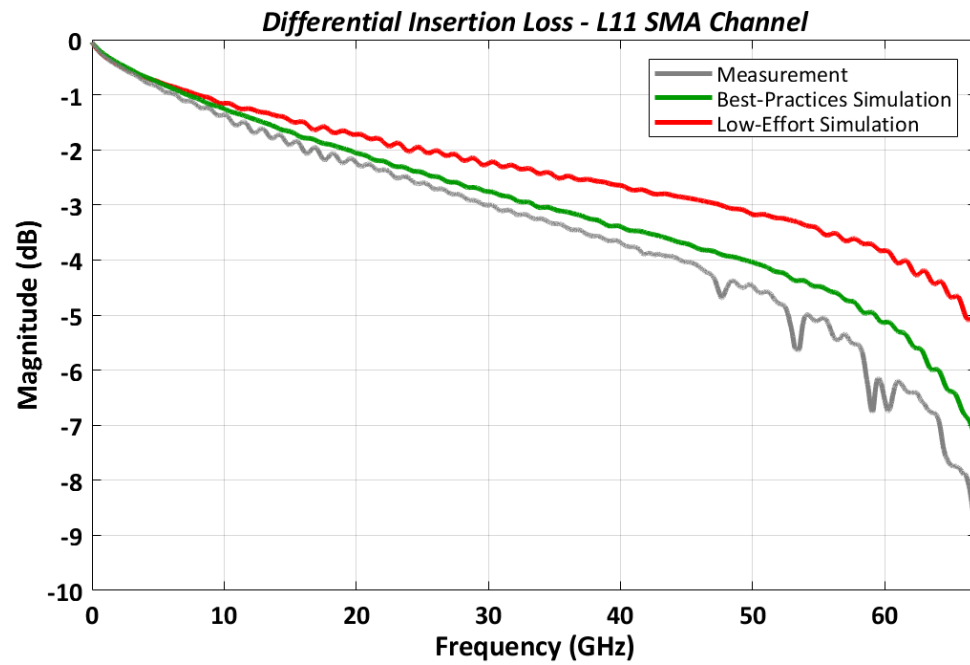
Measurements – L2 BOR-Like Structure



Measurements – L2 SMA Launch



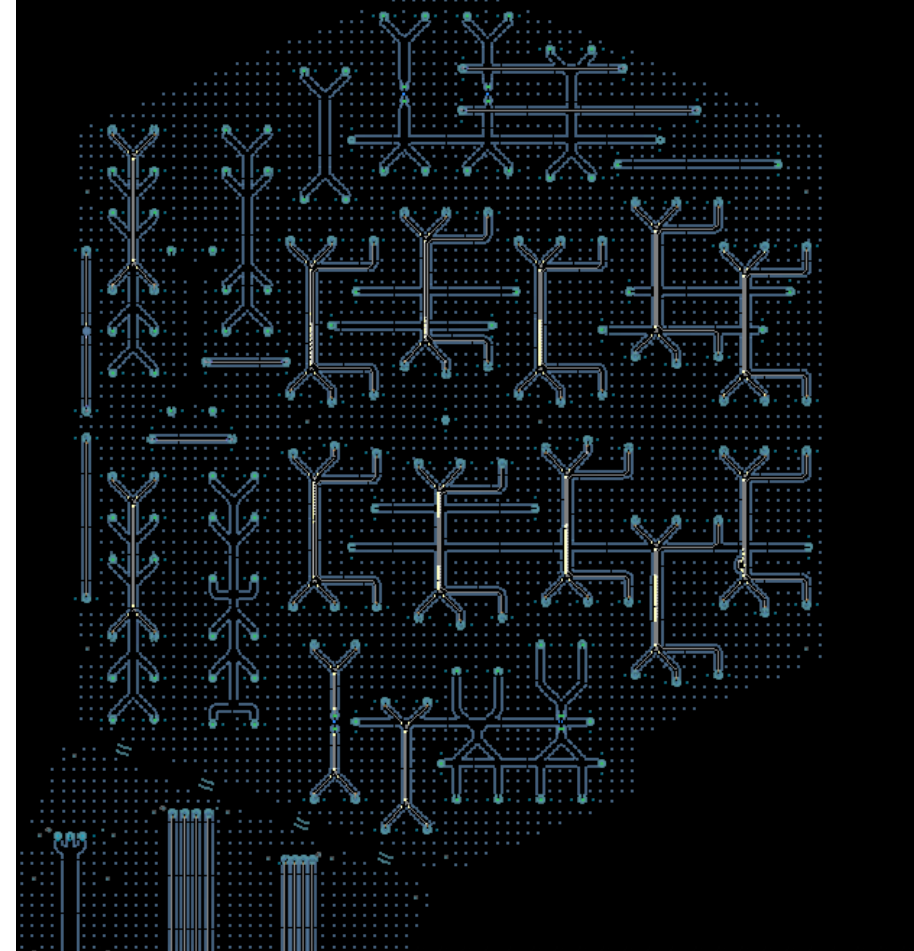
Measurements – L11 SMA Launch



Summation of Data



- This data shows that designing without prior characterization can achieve functional designs
 - Good implementation of characteristics is key
- Better correlation could be achieved
 - Building a test coupon
 - Or utilizing previous builds of stackup
 - Considering manufacturing variation



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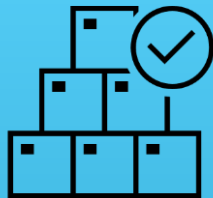
Simulation Methodology

3 Categories of Simulation Correlation

Manufacturing Information

Basic PCB Information

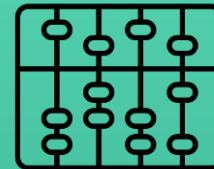
- Stackup
- Drill Size
- Trace Dimensions



Simulation Methodology

Modelling Techniques

- Surface Roughness
- Dielectric Modelling
- Etching



Manufacturing Variation

Fabrication Tolerances

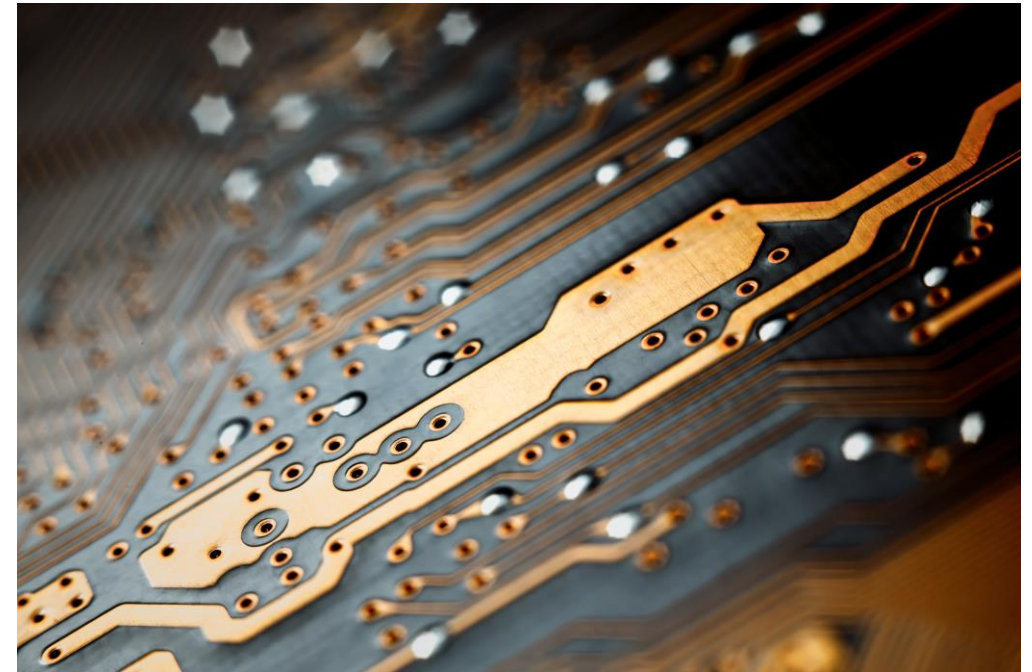
- Backdrill Depth
- Impedance Variation
- Misregistration



Simulation Methodology Characteristics



- There are many characteristics that must be considered in building PCB models
- This presentation will look at each characteristic
 - Define it
 - Recommend how to simulate it
 - Explore its characterization in the field
- This list will show all relevant characteristics
 - For high-speed PCB simulation
- Characteristics are separated by category
 - Material
 - Environmental



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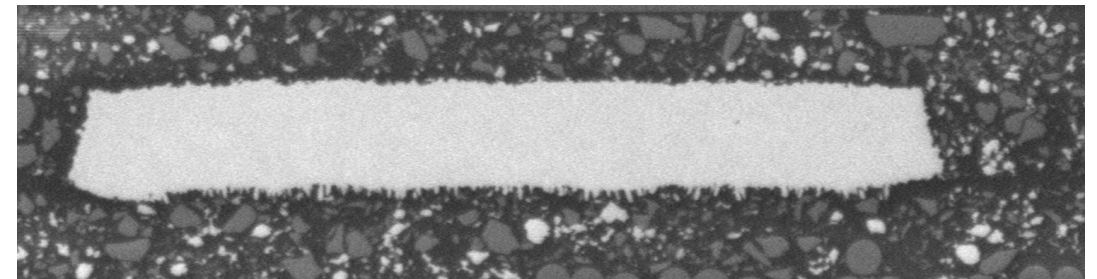
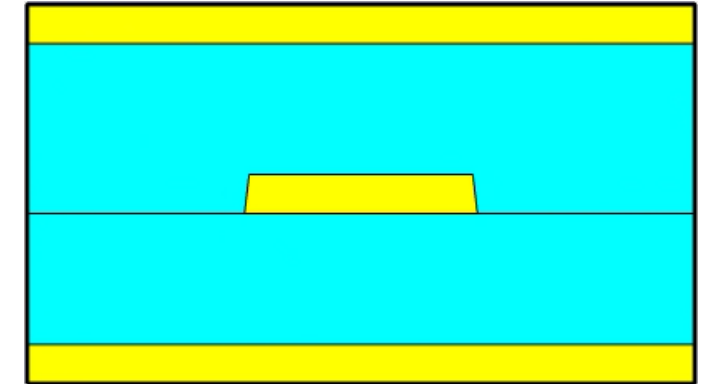
Material Characteristics

Surface Roughness



- Description:
 - Describes height imperfections on surface of copper foil
- Implementation:
 - Use a mathematical model to approximate complex geometry
 - Numerous models exist
 - Most popular is currently the Huray model
- Additional Notes:
 - Different surface roughness profiles for Drum/Matte
 - Matte is core-facing
 - Drum is prepreg-facing

**Confidence Level:
High**



Surface Roughness

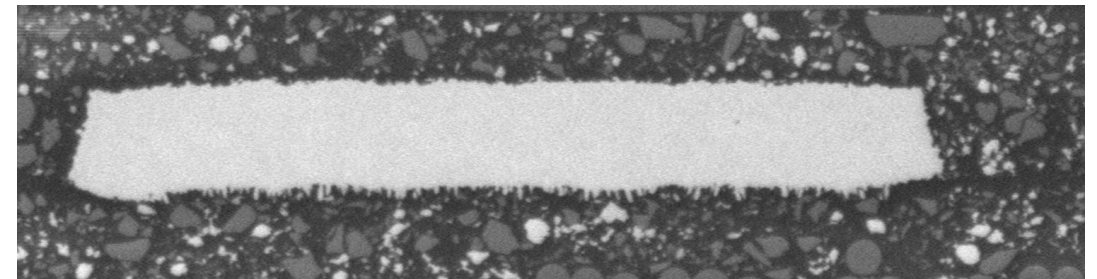
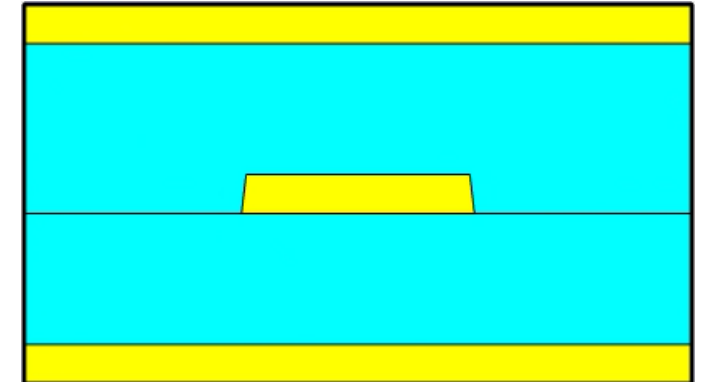
- Methods of Implementation:

- Use the Huray model

**Confidence Level:
High**

- Recommendation for Implementation:

- Roughness Factor of 8.33
 - Or use a Hall-Huray Surface Ratio of 4.8869
- Use the following equations for individual Matte/Drum Nodule Radius
 - $r_{matte} = 0.06 * R_{Z_matte}$
 - $r_{drum} = 0.06 * R_{Z_drum}$
- Use the following equation for combined Nodule Radius
 - $r_{avg} = \frac{0.06(R_{Z_matte} + R_{Z_drum})}{2}$

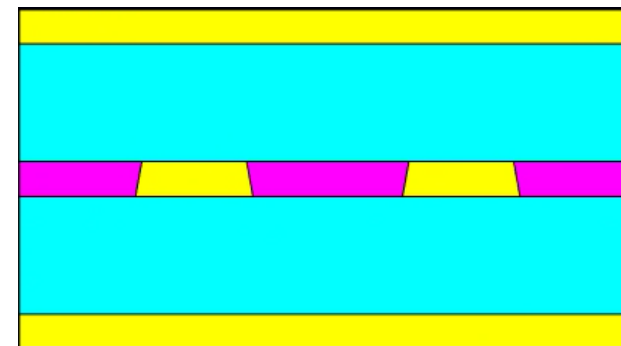


Dielectric Modelling



- Description:
 - Modelling of PCB dielectric materials
- Implementation:
 - Use dielectric properties from manufacturing information and implement a Djordevic-Sarkar model
 - Bulk materials can be implemented in many ways
- Additional Notes:

**Confidence Level:
Medium**



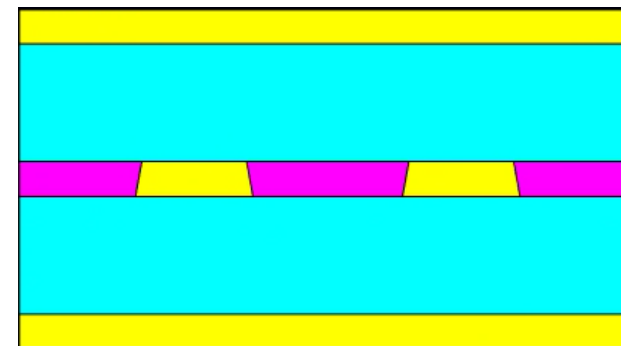
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			Pl	1.40	
			Sig	.60	
EM-892K	1/2 oz HTE	1	.48	Preg	4.72 2.86
	(2)1035*73%				
EM-892K	1/2 oz HVLP3	2	.20	Sig	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	3	.80	Pln	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
	1/2 oz HVLP3	4	.20	Sig	.60
EM-892K	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	5	.80	Pln	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	6	.20	Sig	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	7	.80	Pln	.60
EM-892K	(3)1078*73%		.24	Preg	11.76 2.89
EM-892K	1/2 oz HVLP3	8	.80	Pln	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	9	.20	Sig	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	10	.80	Pln	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	11	.20	Sig	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	12	.80	Pln	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	13	.20	Sig	.60
EM-892K	(2)1035*75%		.48	Preg	4.72 2.86
	1/2 oz HTE	14			
			Sig	.60	
			Pl	1.40	
			S/M	.5	3.20

Dielectric Modelling



- Methods of Implementation:
 - There are multiple ways to implement
 - Standard prepreg/core modelling
 - Anisotropic modelling
- Recommendation for Implementation:
 - Standard Modelling
 - Modify dielectric properties by some percentage
 - 5% increase in Dk
 - 15% increase in Df
 - Anisotropic Modelling
 - Increase XY-axis dielectric properties by some percentage
 - 4-12% increase in Dk and Df
 - Area of ongoing research by multiple groups

**Confidence Level:
Medium**

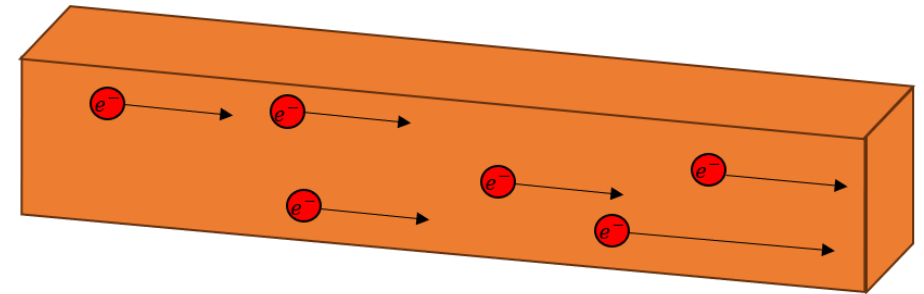


			S/M	.5	3.20
			PT	1.40	
			Sig	.60	
EM-892K	1/2 oz HTE	1			
	(2)1035*75%		.48	Preg	4.72 2.86
EM-892K	1/2 oz HVLP3	2	.20	Sig	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	3	.80	Pin	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	4	.20	Sig	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	5	.80	Pin	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	6	.20	Sig	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	7	.80	Pin	.60
EM-892K	(3)1078*73%		.24	Preg	11.76 2.89
EM-892K	1/2 oz HVLP3	8	.80	Pin	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	9	.20	Sig	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	10	.80	Pin	.60
	0.005 (2)1035 73%			Core	5.00 2.89
	1/2 oz HVLP3	11	.20	Sig	.60
EM-892K	(2)1035*75%		.60	Preg	4.60 2.86
EM-892K	1/2 oz HVLP3	12	.80	Pin	.60
	0.005 (2)1035 73%			Core	5.00 2.89
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	1/2 oz HTE	14			
			Sig	.60	
			PT	1.40	
			S/M	.5	3.20

Conductivity

- Description:
 - Fundamental Electrical property that describes current flow through metal
- Implementation:
 - Apply conductivity(S/m) to metal material
- Additional Notes:

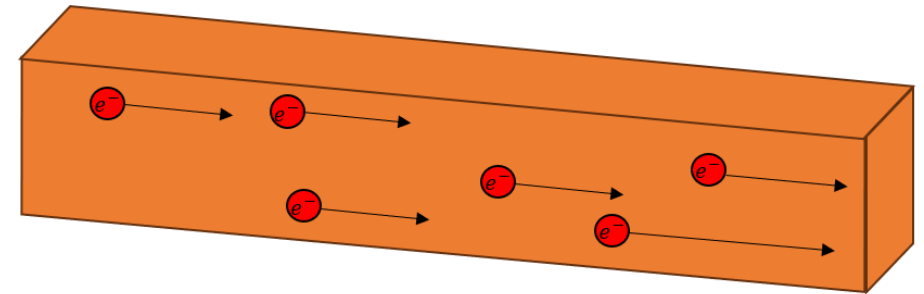
**Confidence Level:
High**



Conductivity

- Recommendation for Implementation:
 - Simulate copper foil with $5.8e7(S/m)$ Conductivity
 - At 20 degrees Celsius

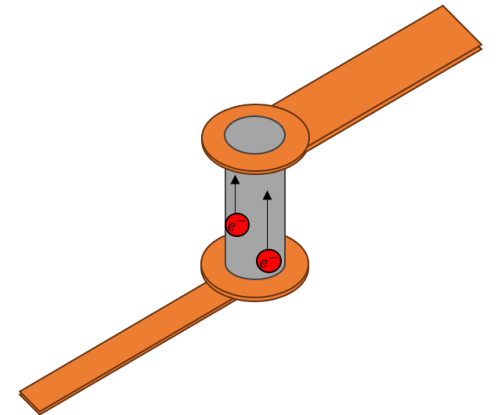
**Confidence Level:
High**



Via Conductivity

- Description:
 - Fundamental Electrical property that describes current flow through vias
- Implementation:
 - Apply conductivity(S/m) to metal material
- Additional Notes:
 - Neither characterized or manufactured in the same way as copper foil
 - Will be less conductive than foil

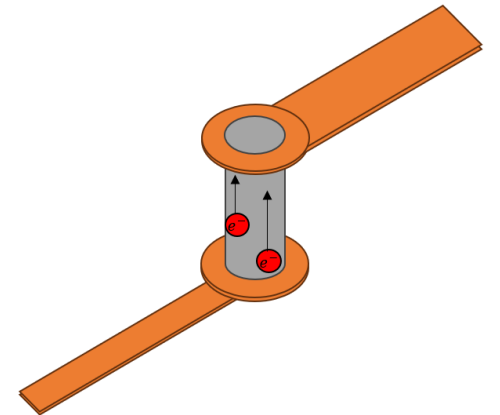
**Confidence Level:
Medium**



Via Conductivity

- Recommendation for Implementation:
 - Simulate via barrel with $0.5e6(S/m)$ Conductivity
 - At 20 degrees Celsius

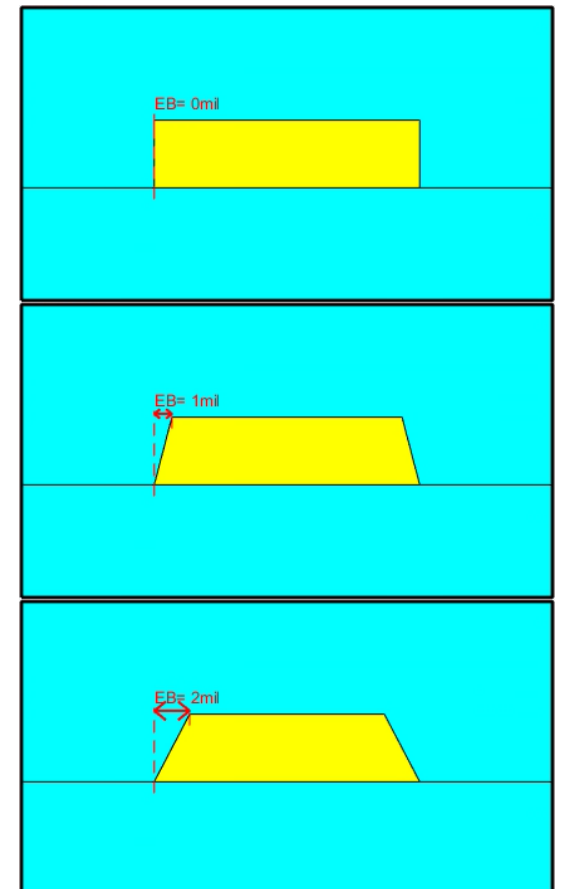
**Confidence Level:
Medium**



Etching

- Description:
 - Trapezoidal shape of final structures on copper foil resulting from etching process by PCB fabricator
- Implementation:
 - Impedance Controlled Structure:
 - Add a trapezoidal shape from etching
 - Adjust the width to hit nominal impedance
 - Non-Impedance Controlled Structure:
 - Add a trapezoidal shape from etching
- Additional Notes:

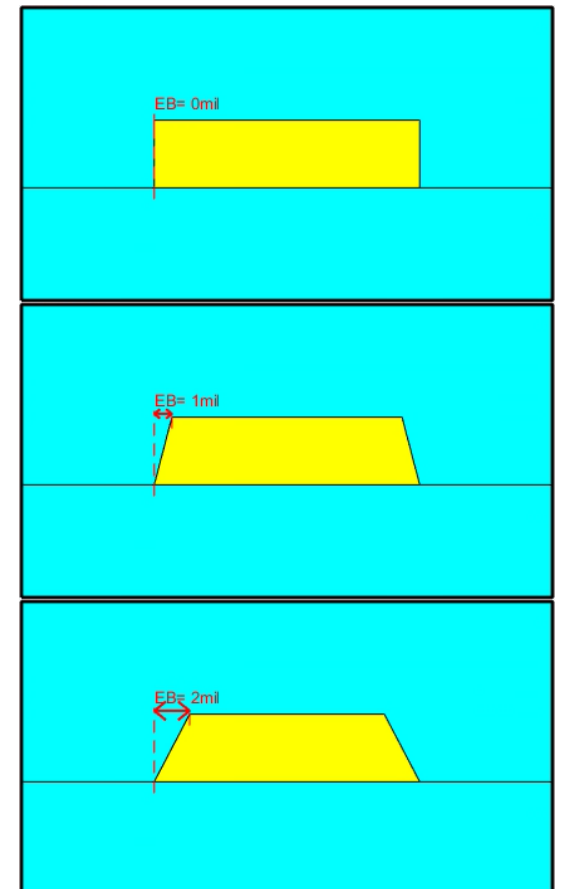
**Confidence Level:
High**



Etching

- Methods of Implementation:
 - Can either use Etch-Back or Etch Factor
 - Etch-back is shown in the images on the right
 - Etch-factor uses the following equation
 - $EF = \frac{2 * Thickness}{TW_{Bottom} - TW_{Top}}$
- Recommendation for Implementation:
 - Stripline
 - For ½ oz foil, use a 1mil Etch-Factor
 - For 1 oz foil, use a 1.5mil Etch-Factor
 - Microstrip
 - Use a 2mil Etch-Factor

Confidence Level:
High

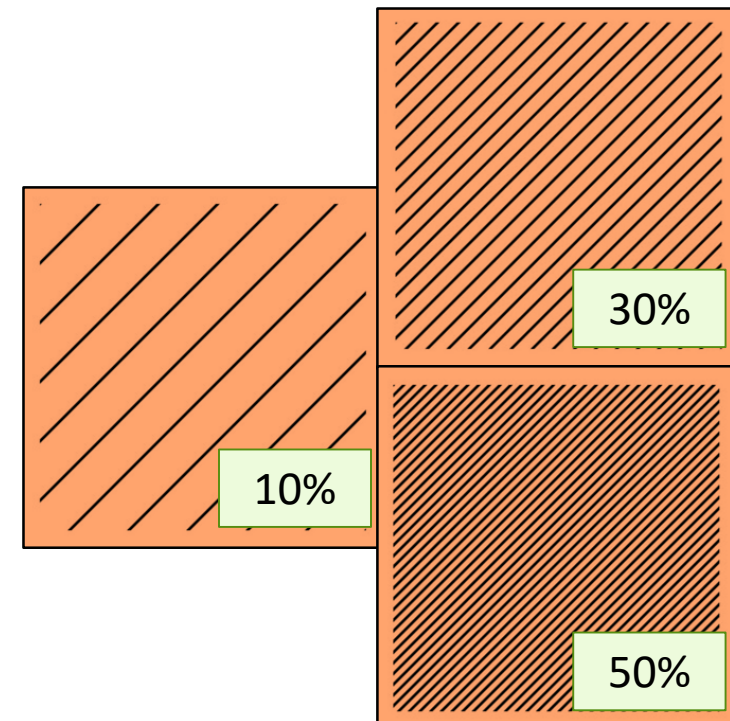


Copper Utilization



- Description:
 - Adjustments made to the prepreg dielectric height based on the percentage copper on the attached signal layer
- Implementation:
 - Calculate the utilization on the signal layer
 - Subtract that volume from the total volume of the prepreg to create a new thickness
- Additional Notes:

**Confidence Level:
High**



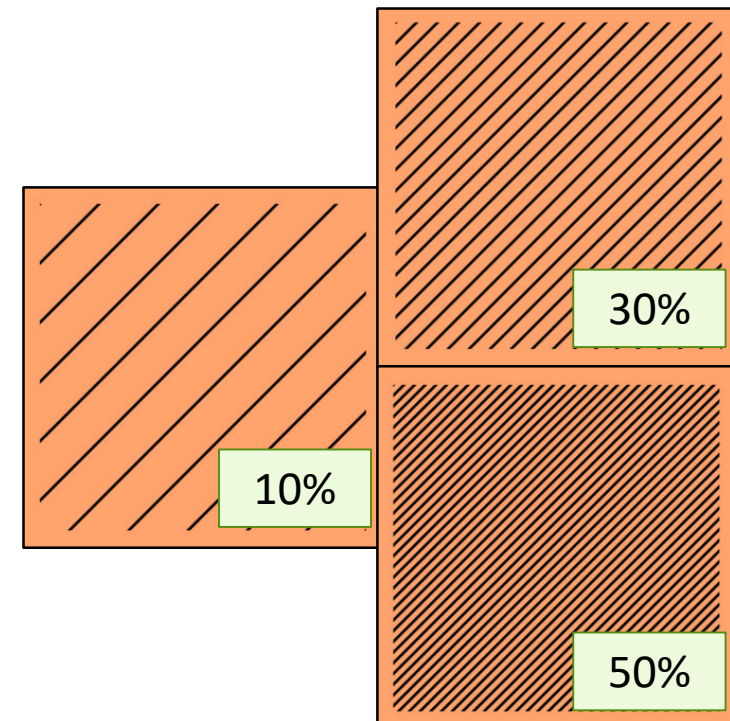
Copper Utilization

- Recommendation for Implementation:

- Use equation to modify the prepreg stack-height

- $Thickness = Nominal\ Thickness - Foil\ Thickness * \left(1 - \frac{Copper\ Utilization\ \%}{100}\right)$

**Confidence Level:
High**



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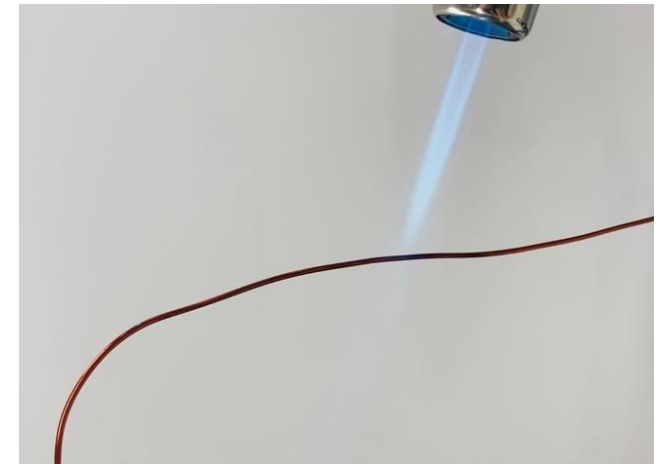
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Environmental Characteristics

Copper Temperature

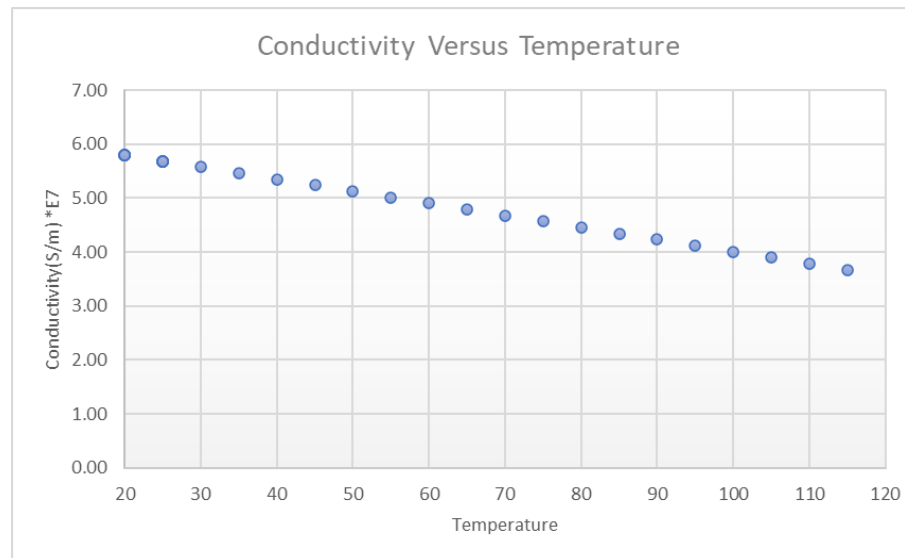
- Description:
 - Change in Copper conductivity due to changes in temperature
- Implementation:
 - Include temperature dependence equation in conductivity of copper materials
- Additional Notes:

**Confidence Level:
High**

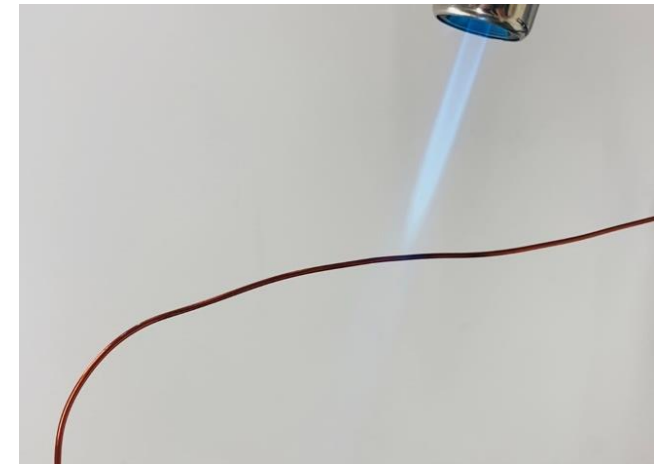


Copper Temperature

- Recommendation for Implementation:
 - Build equation directly into material properties
 - $Conductivity = 5.8 \times 10^7 * (1 - (.00386 * (T - 20)))$
 - Temperature is in Celsius
 - If solver doesn't include temperature sensitivity it will have to be manually built in



**Confidence Level:
High**



Dielectric Temperature



- Description:
 - Change in effective dielectric properties due to change in temperature
- Implementation:
 - Include temperature dependence equation in dielectric properties
 - Change properties when changing a temperature variable
- Additional Notes:

**Confidence Level:
Medium**



Dielectric Temperature



- Recommendation for Implementation:
 - Modify dielectric properties by some percentage
 - .033% increase in Dk per degree Celsius
 - .19% increase in Df per degree Celsius
- At a 50 degrees Celsius increase that would be:
 - 1.67% increase in Dk
 - 9.5% increase in Df

**Confidence Level:
Medium**



Humidity



- Description:
 - Change in effective dielectric properties due to humidity levels
- Implementation:
 - Modify dielectric properties to reflect change in humidity
- Additional Notes:
 - It is difficult to characterize the effect of humidity on PCB performance
 - PCBs take a long time to absorb water vapor
 - Water absorption will vary across dielectric
 - Getting good measurements is difficult

**Confidence Level:
Low**



Humidity



- Recommendation for Implementation:
 - Modify dielectric properties by an additive amount
 - 0.001 increase in Df
 - Note that due to the nature of the available data, this is considered on/off
 - Low humidity is nominal
 - High humidity is with the increase in Df
 - Likely more accurate with low-loss materials

**Confidence Level:
Low**



Lifespan



- Description:
 - Describes degradation of the material properties in the PCB over time
 - Results from melting/settling and formation of air pockets
- Implementation:
 - Change the Dk and Df of the dielectric materials
- Additional Notes:
 - This method only covers dielectric decay, and not destructive failures due to lifespan
 - These failures can instead cause opens, thus breaking the channel

**Confidence Level:
Medium**



Lifespan



- Recommendation for Implementation:
 - Modify dielectric properties by some percentage
 - 5% increase in D_k
 - 30% increase in D_f
 - Note this is meant to simulate 5 years of dielectric decay

**Confidence Level:
Medium**



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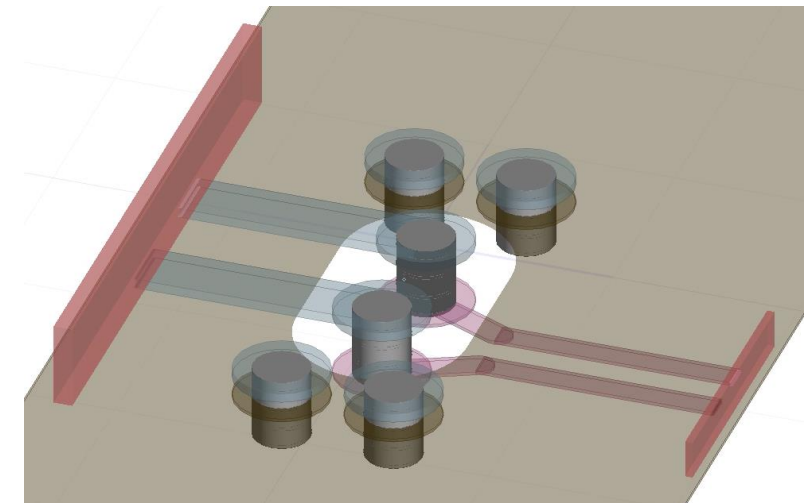
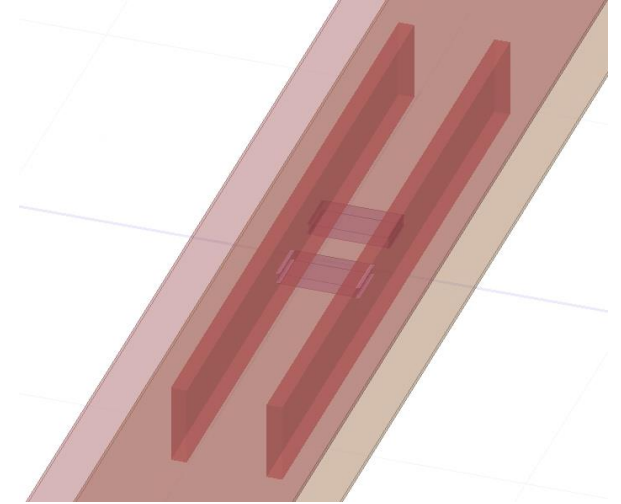
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Sensitivity Analysis

Sensitivity Analysis Overview



- This analysis will look at all the discussed characteristics
 - Demonstrate relative impact
 - Help determine where time/effort is best spent
 - Identify likely culprits from miscorrelation
- The analysis is done using a simulated DOE
 - Done in a 3D EM Field Solver
 - Designed to be stackup agnostic
- Evaluated structures:
 - Differential Stripline
 - Differential Layer-to-Layer Via



DOE

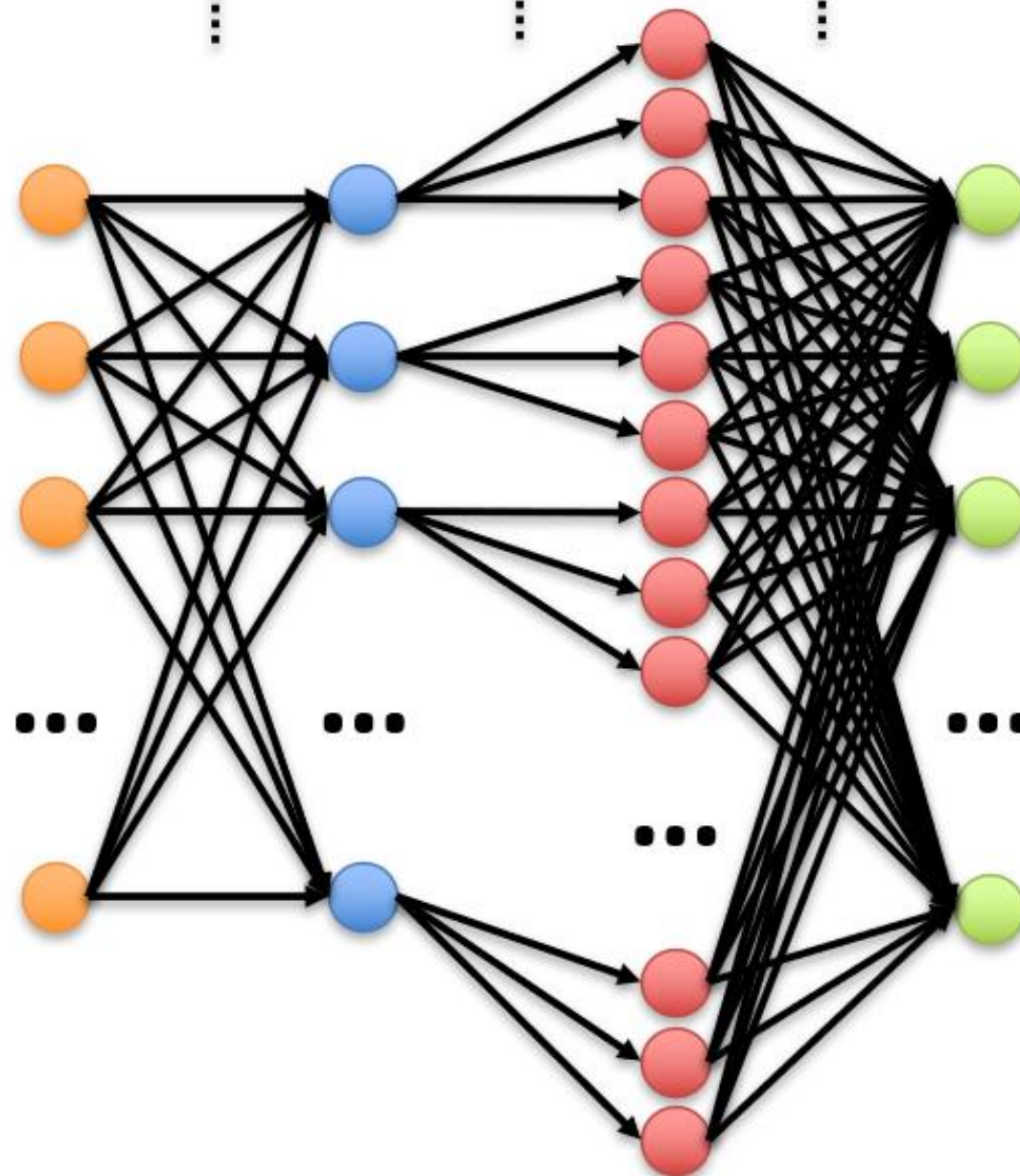
- Stackup Design
 - 100 unique models
 - Each w/ parametric sweep
 - 36 variations
 - Run to 100GHz
- Combined chart of data on next slides
 - Narrow Range
 - Broad Range

Manufacturing
Information

Design of
Experiments

Parametric
Sweeps

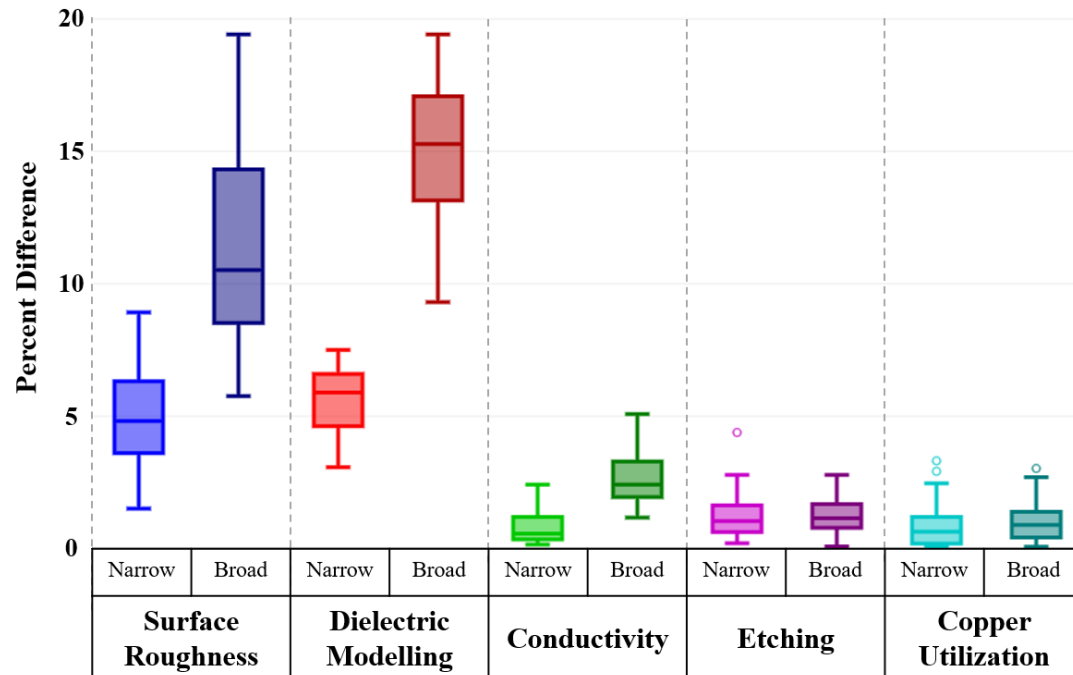
Characteristic
Data



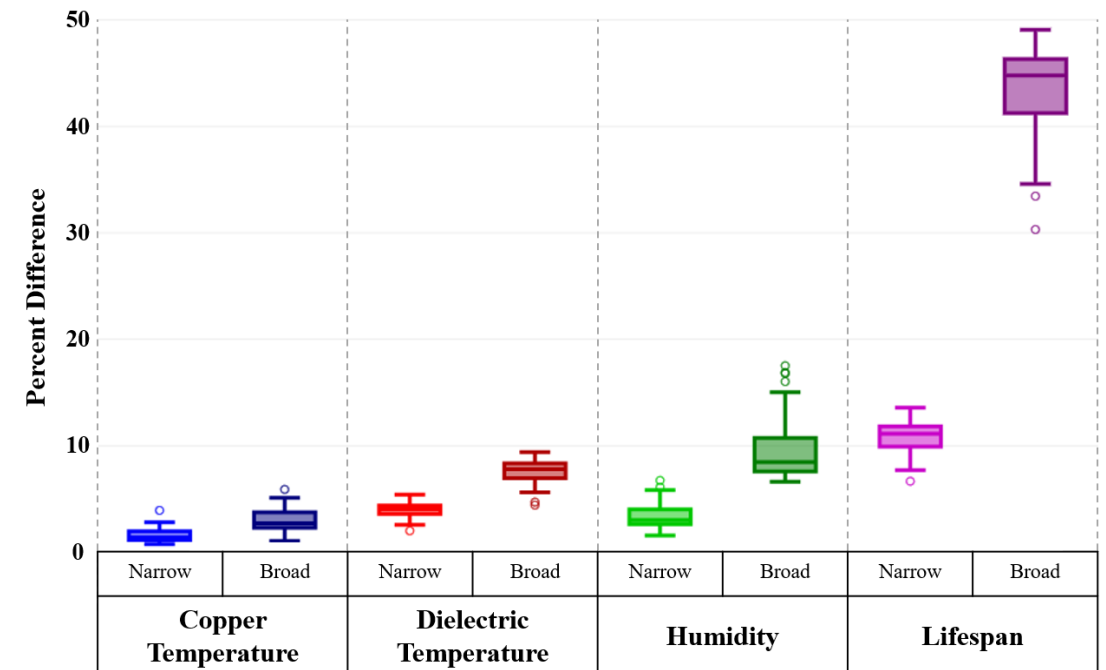
Differential Stripline DOE Results



Box and Whisker of Stripline Material Data



Box and Whisker of Stripline Environmental Data



Stripline Material Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Surface Roughness	5.11%	11.41%	High
Dielectric Modelling	5.68%	15.19%	Medium
Conductivity	0.88%	2.68%	High
Etching	1.18%	1.22%	High
Copper Utilization	0.85%	1.01%	High

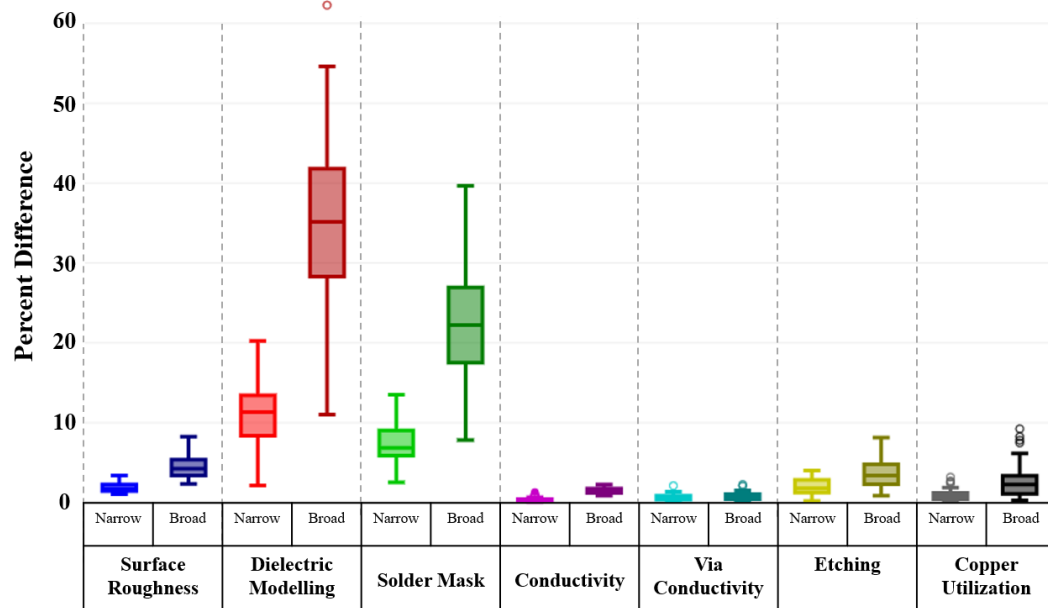
Stripline Enviromental Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Copper Temperature	1.60%	3.03%	High
Dielectric Temperature	3.94%	7.59%	Medium
Humidity	3.39%	9.78%	Low
Lifespan	10.72%	43.32%	Medium

Differential Layer-to-Layer Via DOE Results



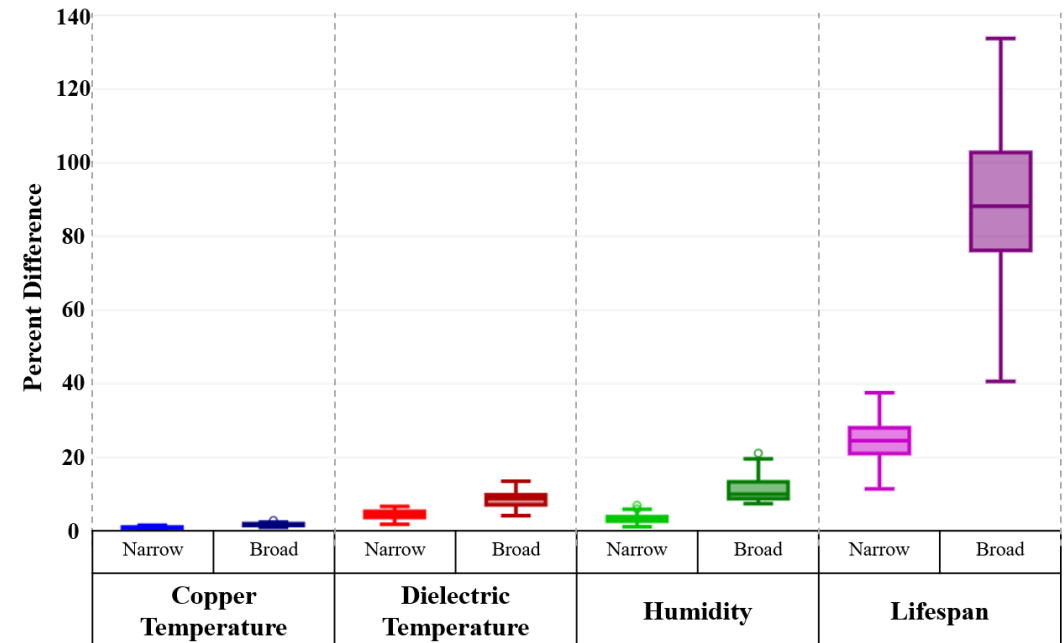
Box and Whisker of Via Material Data



Via Material Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Surface Roughness	1.82%	4.41%	High
Dielectric Modelling	11.38%	35.60%	Medium
Soldermask	7.45%	22.80%	Low
Conductivity	0.37%	1.49%	High
Via Conductivity	0.65%	0.79%	Medium
Etching	2.01%	3.66%	High
Copper Utilization	0.98%	2.81%	High

Box and Whisker of Via Environmental Data



Via Enviromental Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Copper Temperature	0.93%	1.79%	High
Dielectric Temperature	4.50%	8.53%	Medium
Humidity	3.47%	11.24%	Low
Lifespan	24.42%	89.07%	Medium

The background of the slide is a dark field filled with numerous glowing, curved lines in shades of orange, red, and blue, creating a sense of motion and energy.

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Conclusion

Conclusion

- This presentation is meant to recommend simulation methodologies for PCB development
 - The methods are not accurate in 100% of cases
 - Best judgement should be used in implementation
- As more complete data becomes available it should be substituted
 - Material characterization, surface roughness profile, ect...
- This should give designers a good starting point
 - Increasingly important for 224G development and beyond

- This presentation is based on the work from our 2024 DesignCon presentation:

Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz

- For a more complete discussion of the topic, please see that presentation/paper
 - [Reach out to DesignCon for information on accessing the conference materials](#)



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Backup



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DOE Further Details

Additional Details on DOE



- The DOE was designed to cover a wide variety of stackups and board types
 - This was intended so that the results of the sensitivity analysis best represented a variety of applications
 - The standard deviation of the data is higher as a result
 - However, the averages should be more accurate to all common 56-224G applications
- Two different DOEs were performed
 - One for differential stripline trace
 - One for a differential layer-to-layer via transition
- The DOE varied based on manufacturer information
 - One of the three categories from the introduction
 - Represents basic PCB background information

Differential Stripline Trace DOE Ranges

- Prepreg Dk
 - 2.8 – 4
- Prepreg Df
 - 0.001 – 0.02
- Prepreg Dielectric Thickness
 - 3mil – 6mil
- Core Dk
 - 2.8 – 4
- Core Df
 - 0.001 – 0.02
- Core Dielectric Thickness
 - 3mil – 6mil
- Copper Thickness
 - 0.25oz – 1oz
- Trace Pitch
 - 8mil – 15mil

Differential Stripline Trace DOE Ranges

- Prepreg Dk
 - 2.8 – 4
- Prepreg Df
 - 0.001 – 0.02
- Prepreg Dielectric Thickness
 - 3mil – 6mil
- Core Dk
 - 2.8 – 4
- Core Df
 - 0.001 – 0.02
- Core Dielectric Thickness
 - 3mil – 6mil
- Copper Thickness
 - 0.25oz – 1oz
- Trace Pitch
 - 8mil – 15mil
- Via Pitch
 - 28mil – 35mil
- Drill Size
 - 8mil – 12mil
- Plating Thickness
 - 1oz – 3oz
- Soldermask Dk
 - 3 – 4.5
- Soldermask Df
 - 0.01 – 0.025
- Soldermask Thickness
 - 0.5mil – 2mil

Parametric Sweep



- Parametric sweeps were run using a 3D EM Field Solver
 - Each individual stackup was implemented from the DOE and run
- The results were then all combined together and averaged to get the numbers shown in the DOE results table
 - Percent difference from nominal was used for this calculation
 - This gives the fairest comparison between characteristics where nominal is 0 (such as humidity) and characteristics where nominal is in the middle of the range (like temperature)
- Formula used for percent difference:

$$\text{Percent Difference} = \frac{\left(\frac{|Nominal - RangeHigh| * 100}{\frac{|Nominal + RangeHigh|}{2}} + \frac{|Nominal - RangeLow| * 100}{\frac{|Nominal + RangeLow|}{2}} \right)}{2}$$



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DOE Ranges

What Information this Section Covers:



- This section will provide more information on the ranges that were used for characteristics in the DOE
- For more detailed discussion, see the DesignCon Paper on this topic
- For each characteristic, the information covered is:
 - Units
 - What units were used for that characteristic
 - Narrow Range
 - What were the exact numbers of the narrow range
 - Broad Range
 - What were the exact numbers of the broad range
 - Basis for Ranges
 - How were the ranges calculated
 - What data/resources were used to determine the ranges

Surface Roughness Ranges



- Unit
 - Rz (microns)
- Narrow Range
 - 0.8-3.0 μm
- Broad Range
 - 0.8-10.0 μm
- Basis for Ranges
 - Used surface roughness numbers for common foil types in the 56-224G range
 - Identified as HVLP-HVLP5

Dielectric Modelling Ranges



- Unit
 - Dielectric Constant
- Narrow Range
 - 0 – 15% increase in D_f
 - 0 – 5% increase in D_k
- Broad Range
 - 0 – 45% increase in D_f
 - 0 – 15% increase in D_k
- Basis for Ranges
 - Used research papers which observed variation on dielectric properties from manufacturer datasheets

Soldermask Ranges



- Unit
 - Dielectric Constant
- Narrow Range
 - 0 – 15% increase in D_f
 - 0 – 5% increase in D_k
- Broad Range
 - 0 – 45% increase in D_f
 - 0 – 15% increase in D_k
- Basis for Ranges
 - The same values were used as for Dielectric Modelling due to a lack of prior research

Conductivity Ranges



- Unit
 - Siemens per meter (S/m)
- Narrow Range
 - $5.6 - 5.8 \times 10^7 \left(\frac{S}{m}\right)$
- Broad Range
 - $4 - 5.94 \times 10^7 \left(\frac{S}{m}\right)$
- Basis for Ranges
 - Based on experience of industry experts and outside research showing reduction in realized copper foil conductivity

Via Conductivity Ranges



- Unit
 - Siemens per meter (S/m)
- Narrow Range
 - $0.5 - 2.5 \times 10^7 \left(\frac{S}{m}\right)$
- Broad Range
 - $0.5 - 5.94 \times 10^7 \left(\frac{S}{m}\right)$
- Basis for Ranges
 - Based on experience of industry experts and copper conductivity ranges

Etching Ranges



- Unit
 - Total Width Variation on Top of Trace
- Narrow Range
 - +/- 10%
- Broad Range
 - +/- 20%
- Basis for Ranges
 - Speaking with PCB fabricators to determine variation that can be expected in PCBs

Copper Utilization Ranges



- Unit
 - Percentage Utilization on Copper Layer
- Narrow Range
 - 10 – 40%
- Broad Range
 - 0 – 100%
- Basis for Ranges
 - Speaking with industry experts to determine copper utilization for most ranges in 56-224G PCB designs

Copper Temperature Ranges



- Unit
 - Degrees Celsius (°C)
- Narrow Range
 - 15 – 70 °C
- Broad Range
 - 0 – 105 °C
- Basis for Ranges
 - Narrow range is based on ASHRAE Class A2 temperature standard
 - Broad range is based on speaking with industry experts on what gradient temperatures can be expected relative to ASIC position

Dielectric Temperature Ranges



- Unit
 - Degrees Celsius (°C)
- Narrow Range
 - 15 – 70 °C
- Broad Range
 - 0 – 105 °C
- Basis for Ranges
 - Narrow range is based on ASHRAE Class A2 temperature standard
 - Broad range is based on speaking with industry experts on what gradient temperatures can be expected relative to ASIC position

Humidity Ranges



- Unit
 - Humidity Percentage
- Narrow Range
 - 0 - 0.00091 increase in Df
- Broad Range
 - 0 - 0.00294 increase in Df
- Basis for Ranges
 - Used research papers which observed variation on dielectric properties from humidity

Lifespan Ranges



- Unit
 - Dielectric Constant
- Narrow Range
 - 0 – 30% increase in Df
 - 0 – 5% increase in Dk
- Broad Range
 - 0 – 200% increase in Df
 - 0 – 10% increase in Dk
- Basis for Ranges
 - Used research papers which observed variation on dielectric properties from lifespan



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Additional Sources

What Information this Section Covers:



- This section covers some of the most useful sources the authors found on the subject of each of the characteristics
- These resources provide a good overview of each characteristic:
 - [Talk through how the characteristic works](#)
 - [Give an overview of using the characteristic in models](#)
- For a complete list of sources, see the DesignCon paper on this topic

Surface Roughness Additional Sources

- J. A. Marshall, “A. F. Horn III, C. J. Caisse, et al., “Measuring Copper Surface Roughness for High Speed Applications”, IPC Proceedings.

- This paper discusses the basics of surface roughness
- Goes over notations seen on most datasheets

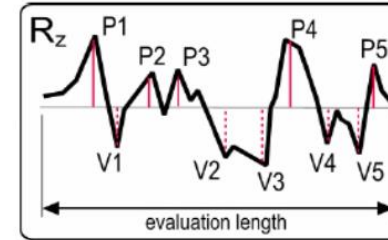


Figure 2 – Rz

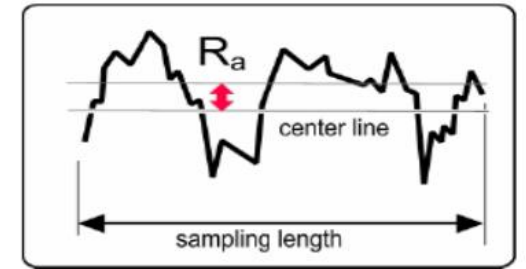


Figure 3 - Ra

- Y. Shlepnev, “Conductor surface roughness modeling: From ‘snowballs’ to ‘cannonballs’”. 2019 Simberian.

- This paper discusses building a Huray Model
- Goes over how the math behind getting accurate surface roughness models

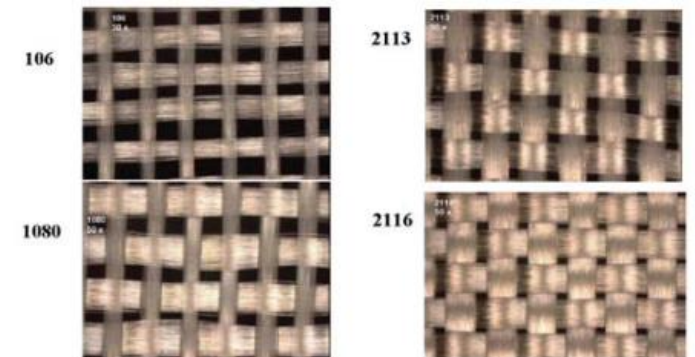
$$RF_i = 1 + \frac{3}{2} \cdot sr_i; \quad sr_i = \frac{2}{3} \cdot (RF_i - 1) \quad (6)$$

Dielectric Modelling Additional Sources

- A. Djordevic, R. Biljic, V. Likar-Smiljanic and T. Sarkar, "Wideband Frequency-Domain Characterization of FR-4 and Time-Domain Causality," IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, vol. 43, no. 4, pp. 662-667, 2001.
 - This paper provides details on implementing the Djordevic-Sarkar Dielectric Model

$$\epsilon_r = \epsilon' - j\epsilon'' = \epsilon'(1 - j \tan \delta).$$

- Altera, "PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing".
 - Provide a reference for selecting and implementing a dielectric material
 - Discusses basics of fiber weave effect on high-speed signals



Soldermask Additional Sources



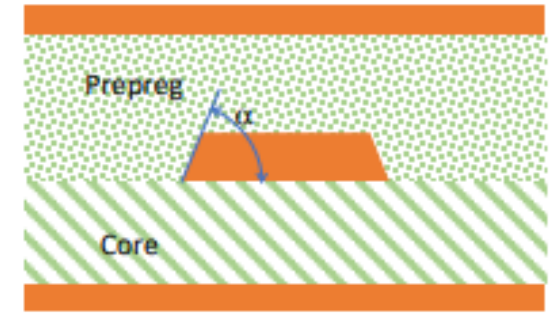
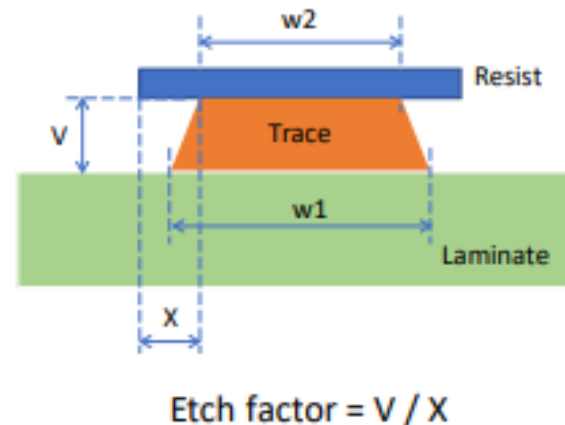
- Y. Chen, F. Ye, Q. Hu, L. Kang, S. Zhang and J. Chen, "Research on the Influence of Solder Mask on Signal Integrity in High Speed PCB," 2021 IEEE 15th International Conference on Electronic Measurement & Instruments (ICEMI), Nanjing, China, 2021, pp. 259-263, doi: 10.1109/ICEMI52946.2021.9679657.
 - This paper discuss the importance of soldermask in high speed signaling
 - Goes over different soldermask uses and their effects on signal integrity

TABLE I. THE MATERIAL CHARACTERISTICS OF THREE KINDS OF SOLDER MASK

	FR-4	Common	Low Loss
Dk	4.4	3.8	3.2
Df	0.02	0.028	0.014

Etching Additional Sources

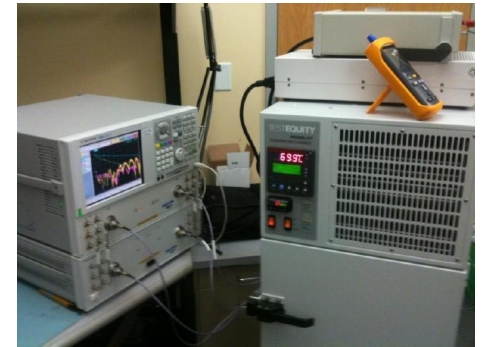
- G. Blando, R. Bakleh, et al., “Etch Factor Impact on SI & PI”, DesignCon 2019.
 - Looks at the impact of etching on crosstalk and impedance
 - Goes over the basics on how etching can be determined



Copper Temperature Additional Sources



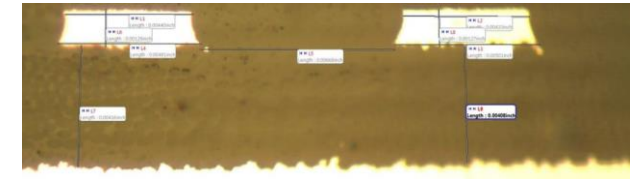
- J. Miller, Y. Li, K. Hinckley, G. Blando, B. Guenin, I. Novak, A. Dengi, A. Rebelo and S. McMorro, "Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance," in DesignCon, Santa Clara, 2012.
 - Goes over transmission line losses with respect to temperature
- J. Loyer, R. Kunze and G. Brist, "Humidity and Temperature Effects on PCB Insertion Loss," in DesignCon, Santa Clara, 2013.
 - Similar to previous paper, also looks at transmission line losses with respect to temperature



Dielectric Temperature Additional Sources



- J. Loyer, A. Burkhardt, R. Kunze and R. Attril, "Accurate Insertion Loss and Impedance Modelling of PCB Traces," in Design Con, Santa Clara, 2013.
 - Looks at copper and dielectric side-by-side and tries to separate out the impacts



- J. Miller, Y. Li, K. Hinckley, G. Blando, B. Guenin, I. Novak, A. Dengi, A. Rebelo and S. McMorrow, "Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance," in DesignCon, Santa Clara, 2012.
 - Goes over the impact of dielectric in regards to temperature



Humidity Additional Sources

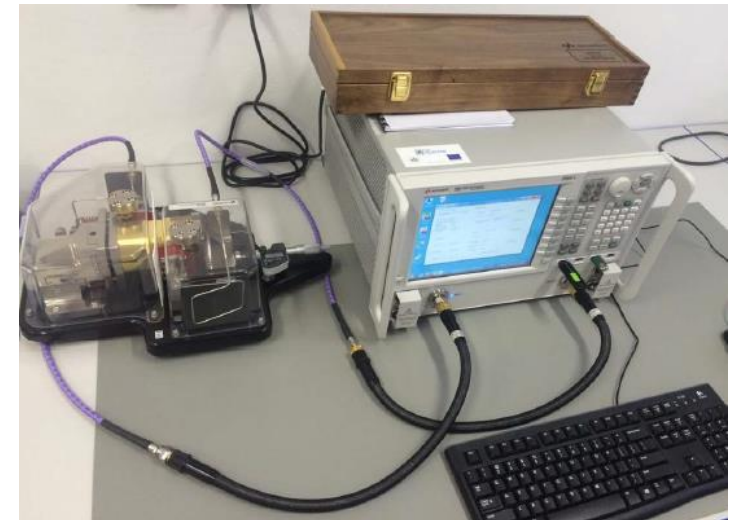
- J. Miller, Y. Li, K. Hinckley, G. Blando, B. Guenin, I. Novak, A. Dengi, A. Rebelo and S. McMorrow, "Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance," in DesignCon, Santa Clara, 2012.
 - Explains how humidity measurements are performed
 - Looks at the interrelationship between temperature and humidity



Lifespan Additional Sources



- T. Rovensky, A. Pietrikova, O. Kovac and I. Vehec, "Influence of accelerating ageing on LTCC and PCB substrates' dielectric properties in GHz area," 2016 39th International Spring Seminar on Electronics Technology (ISSE), Pilsen, Czech Republic, 2016, pp. 189-192, doi: 10.1109/ISSE.2016.7563186.
 - Goes into the background on lifespan
 - Explains how tests are conducted and looks at the resulting data





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