Life in the Fast Lane –

Signal Integrity for Embedded Computing Applications

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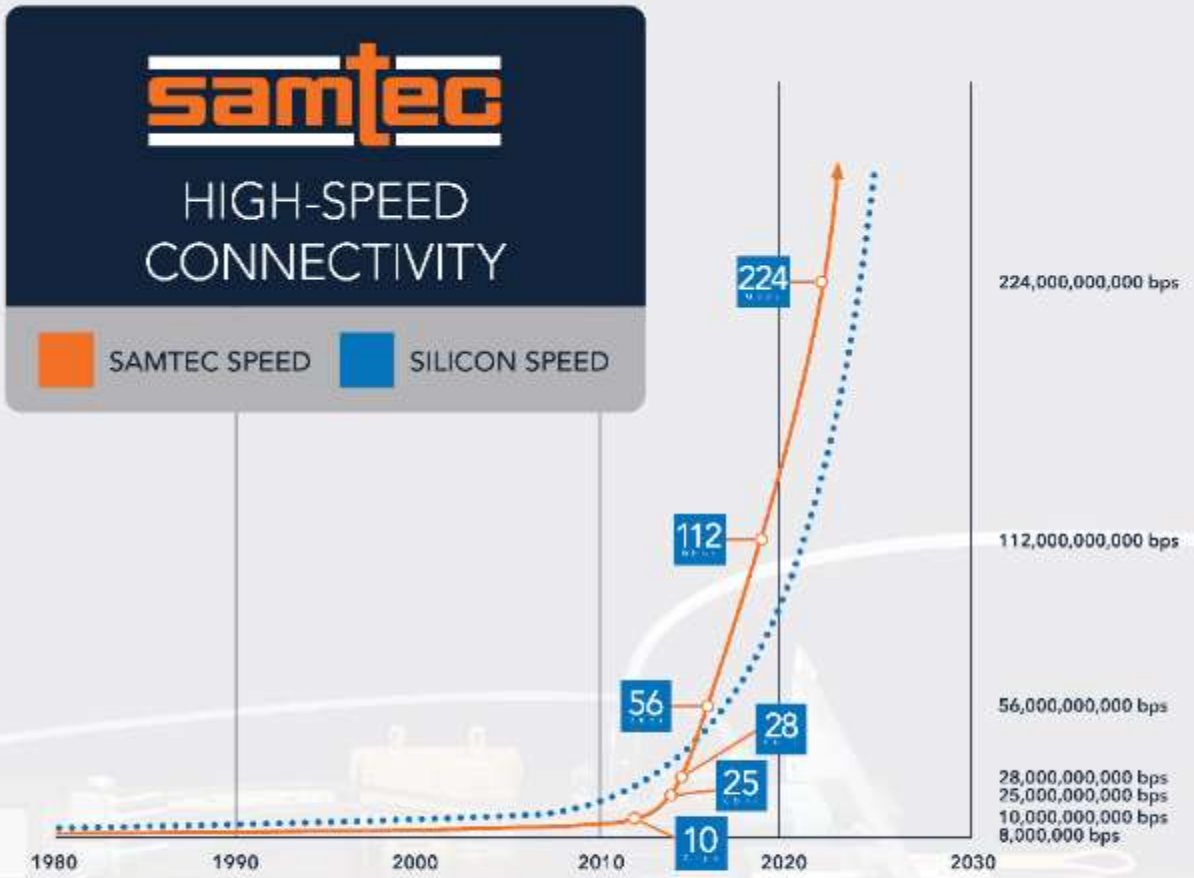
INNOVATIVE TECHNOLOGIES • SUDDEN SERVICE • GLOBAL REACH

THE TECHNICAL RENAISSANCE IS...

...driven by ***progress***, challenged with unprecedented performance ***demands***, a catalyst for next level technologies and ***innovation***...

samtec

HIGH-SPEED CONNECTIVITY



...and enabled by Samtec's

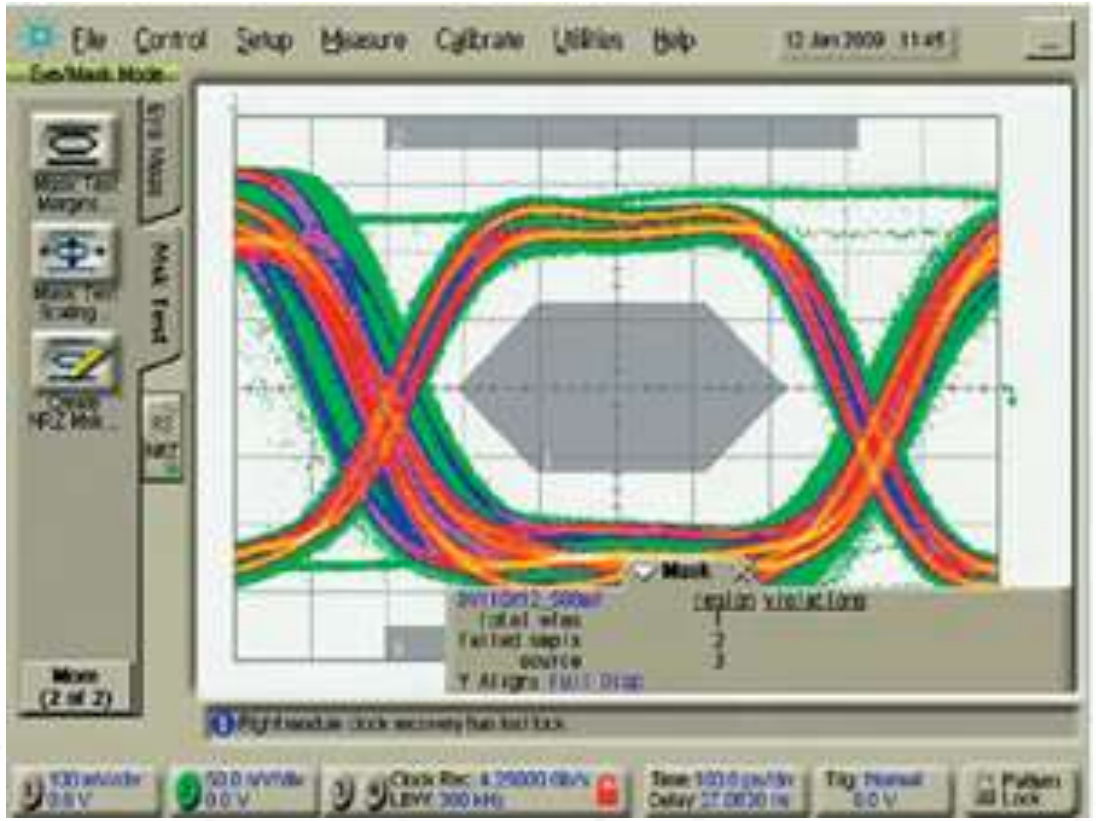
SILICON-TO-SILICON™ SOLUTIONS

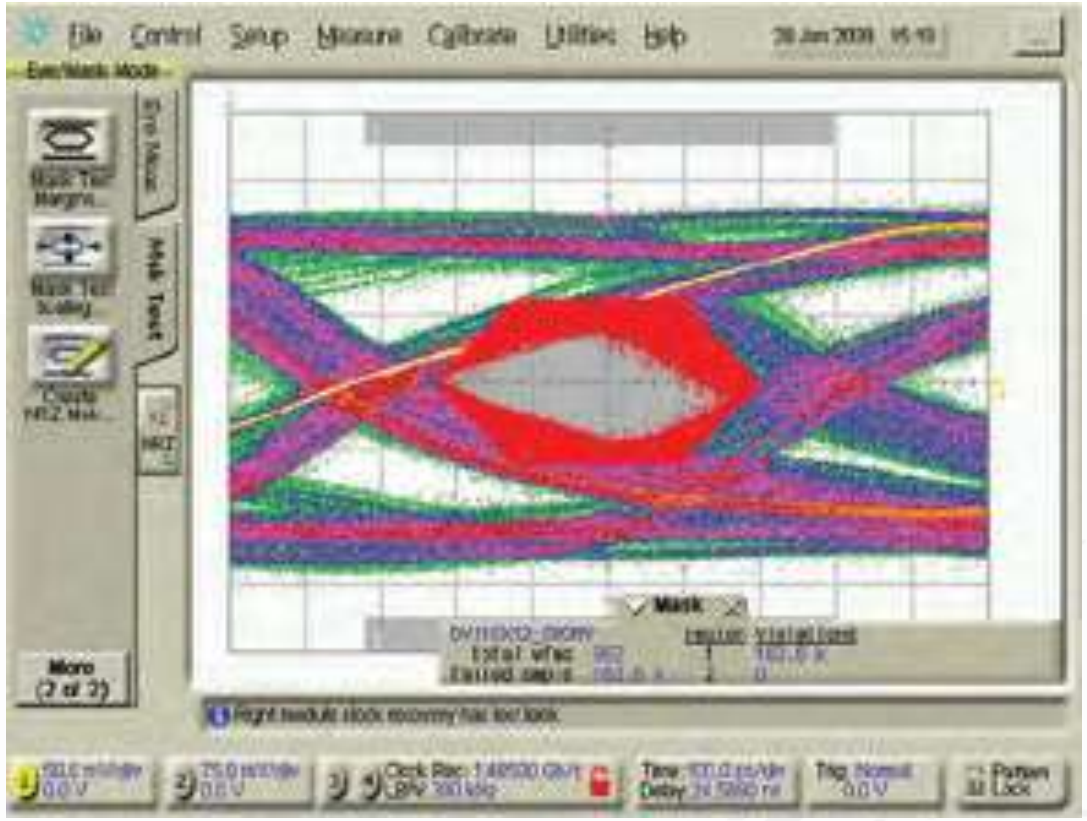
SILICON-TO-SILICON™ CONNECTIVITY SOLUTIONS

samtec

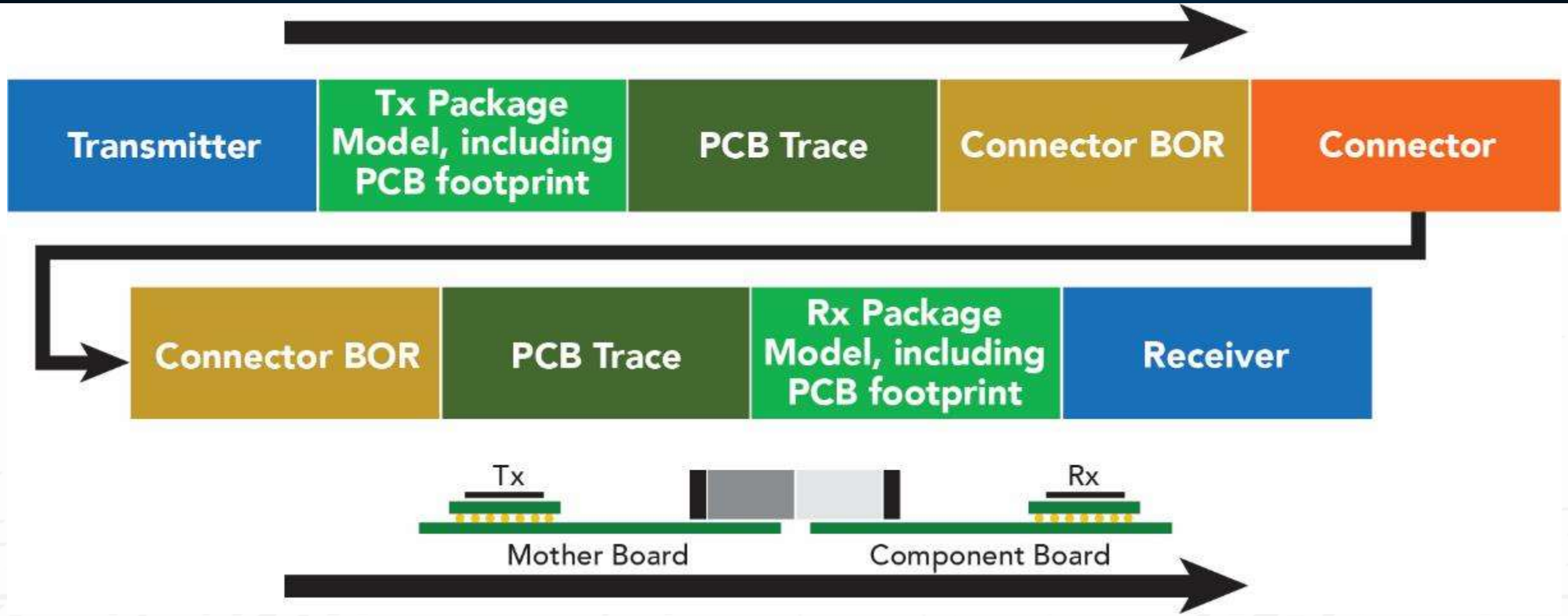
...INNOVATIVE **PRODUCTS** & **NEXT GEN SYSTEM EXPERTISE** ENABLING FULL CHANNEL OPTIMIZATION

More Than Meets the Eye



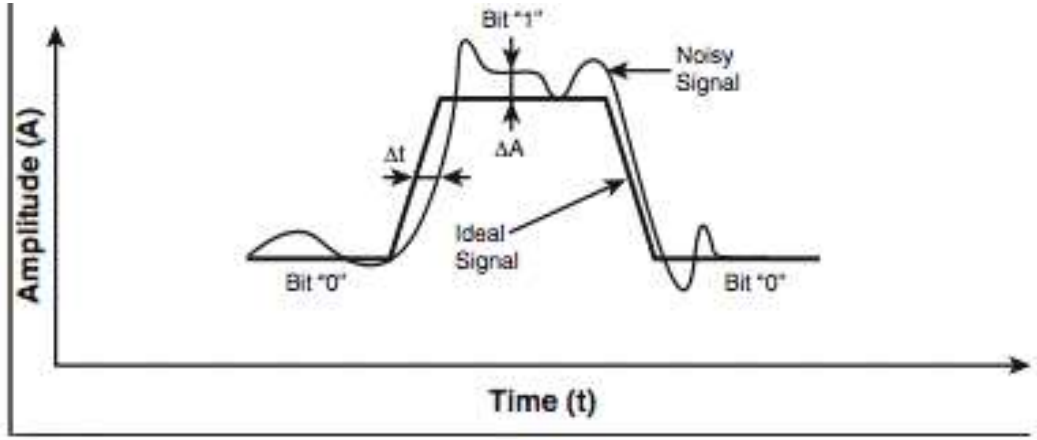


Typical High-Speed Signal Channel

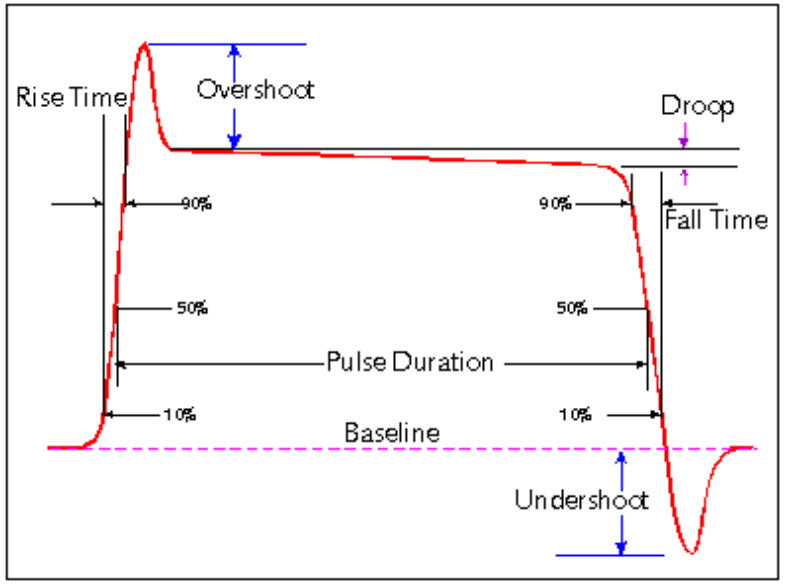


Frequency Components in Digital Signals

- **Nyquist Rate**
- Defined as f > 2B, or typically f = 2B in high-speed designs
- Majority of the signal energy is at Nyquist, although many other frequency components exist to create a digital signal



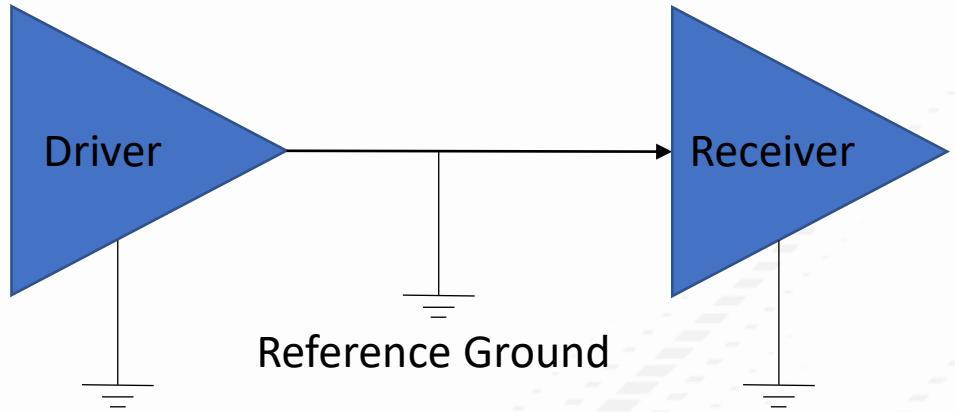
- **Rise Time/Fall Time**
- Much higher frequency component



- **Noise**
- Any amplitude or frequency component you don't want
- Determine loss budgets for the high-speed interfaces

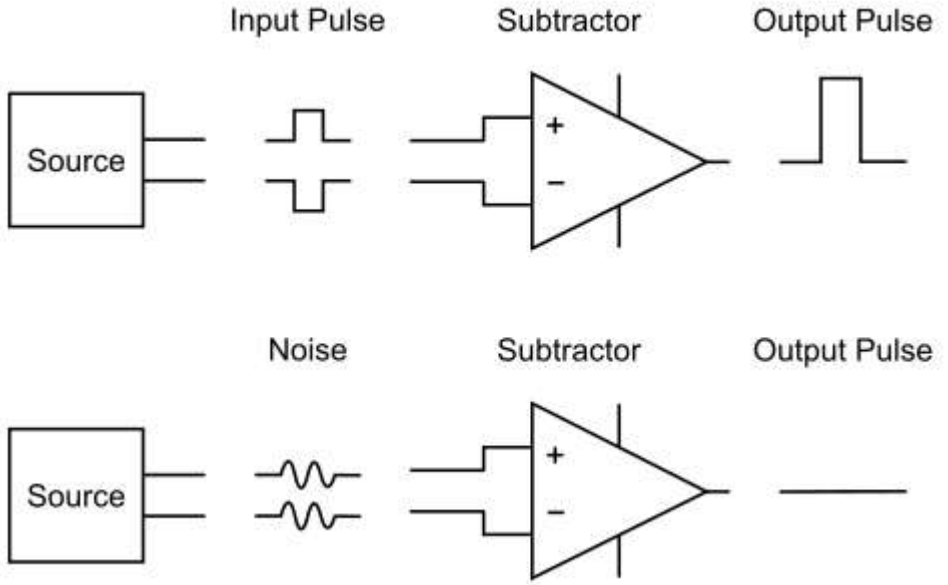
Single Ended (SE) Signals

- A single point to point connection
- Requires a ground reference to return current to the source
- Prone to noise
- Typical SE signals include:
- SDI
- CoaXpress
- RS-232
- I2C
- SPI
- RF
- Control signals



Differential Pair (DP) Signals

- DPs were introduced to create coupling immunity to transmission lines
- Requires 2x the amount of conductors as SE signals
- Requires a positive (p) and negative (n) signal

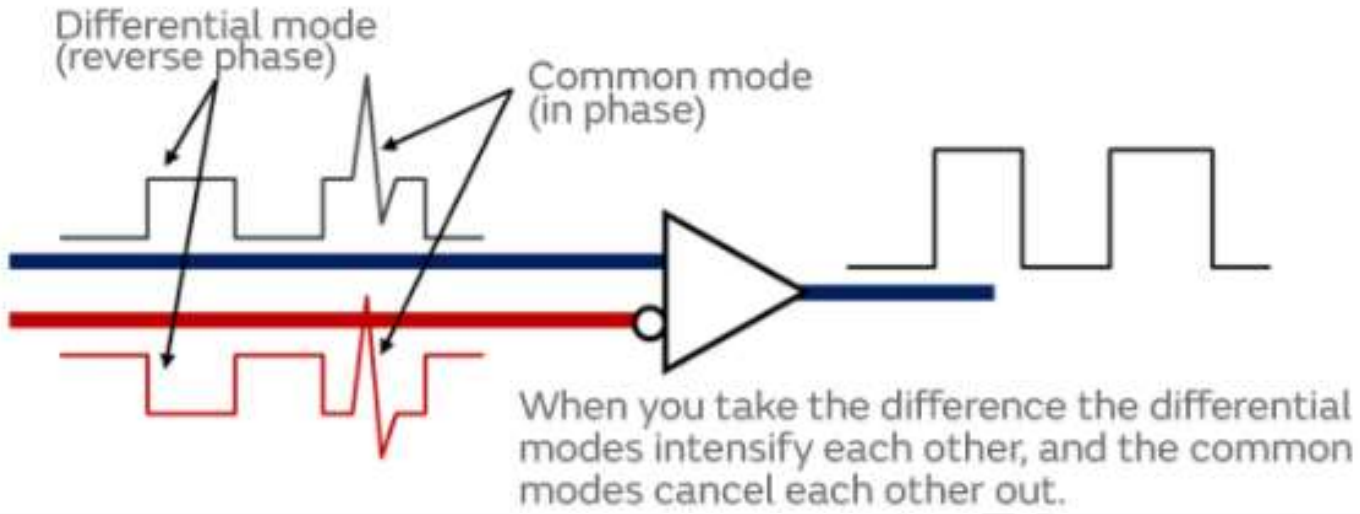


Differential Pair (DP) Signals

- Because a positive and negative signal are transmitted, the net current is ZERO
- No return line is required

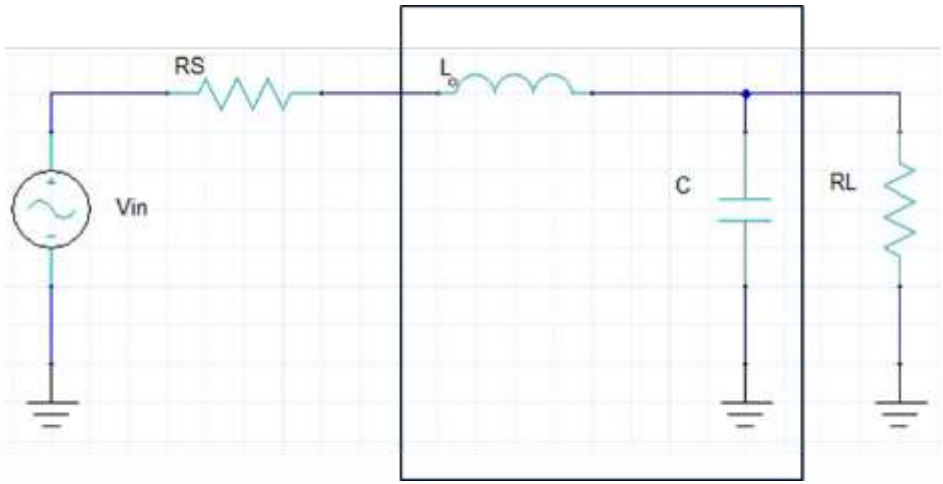
- DPs are used to cancel COMMON MODE NOISE
- Noise that is coupled in the same polarity to both conductors

- Important to keep DP close together s that they couple the same noise



Matching – Why Do We Care?

- Matching the source to the load gives the maximum possible power output (i.e. high efficiency)
- Example RLC circuit
- Matching for signal integrity involves balancing impedance
- Lost power due to mismatch in high-speed circuits can cause significant issues (or not!)



Impedance Mismatches

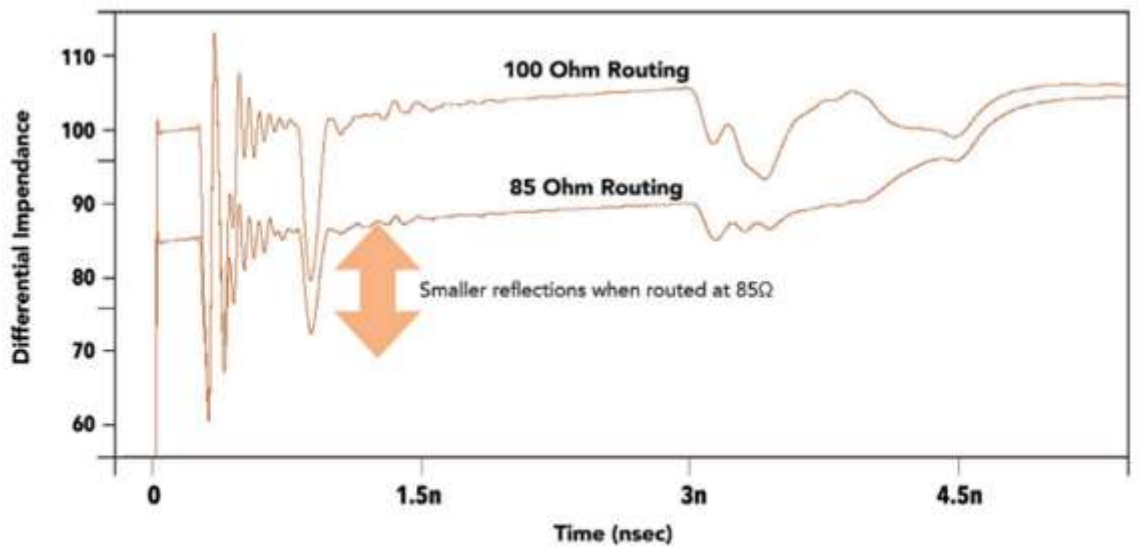


Figure 10: This figure shows an example of two TDR responses from a PCIe® system: one model with the PCB trace at 85 Ω and the other at 100 Ω. Note the physical locations on the bottom of the graph and their subsequent effect on the system's characteristic impedance. This graph shows larger discontinuities at 100 Ω.

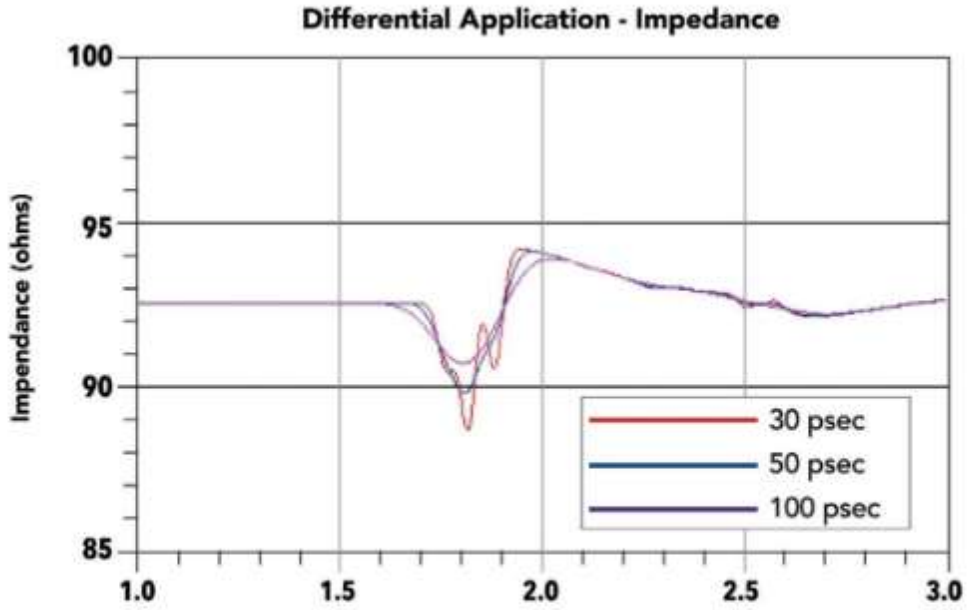
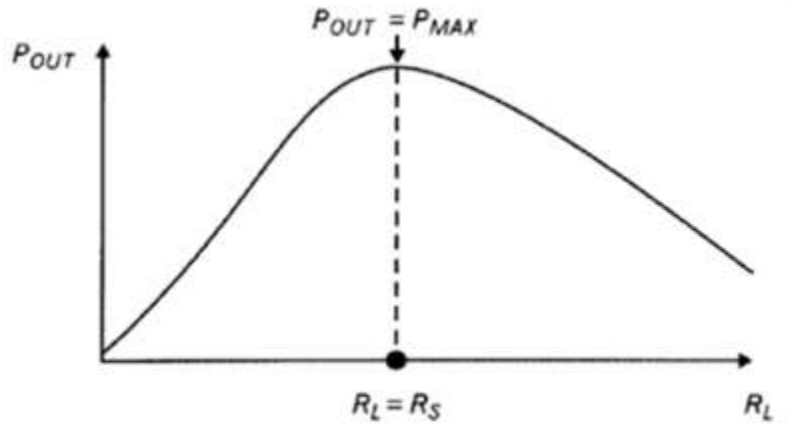


Figure 11: Measured TDR Differential Impedance for a Samtec NovaRay® 7 mm stack height from high-speed characterization reports with three apparent impedances at 30, 50 and 100 ps rise times.

Insertion Loss (IL)

- Insertion Loss is the total amount of power loss through a component, expressed in dB
- Note that Insertion Loss is a negative value as it is loss, but is typically expressed as a positive value
- S21 is the typical desired s-parameter for insertion loss, and is normally equivalent to S12
- Too much insertion loss leads to bit errors due to low voltage
- Several components affect the insertion loss (i.e. power loss):
  - Reflection Loss – due to impedance mismatches
  - Coupling or radiated Loss – lost in crosstalk, EMI
  - Dielectric Loss – energy lost in the material dielectric
  - Conductor Loss – energy loss in the conductor itself



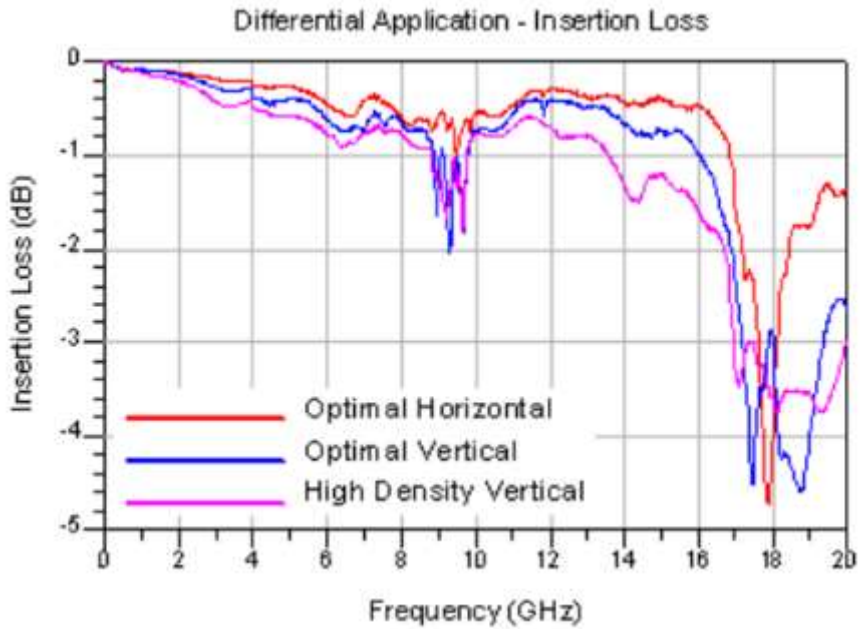
Insertion Loss (IL)

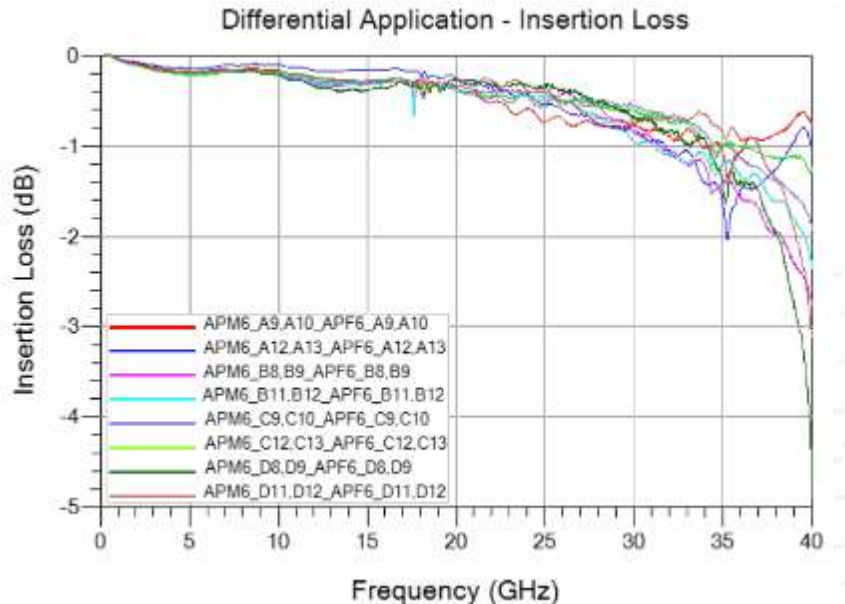
- Typical spec for channel insertion loss is ~5dB
- This is a general guideline – it totally depends on the channel design
- High power switches and FPGA's can handle as low as -30dB of insertion loss

- Insertion loss is non-linear over frequency

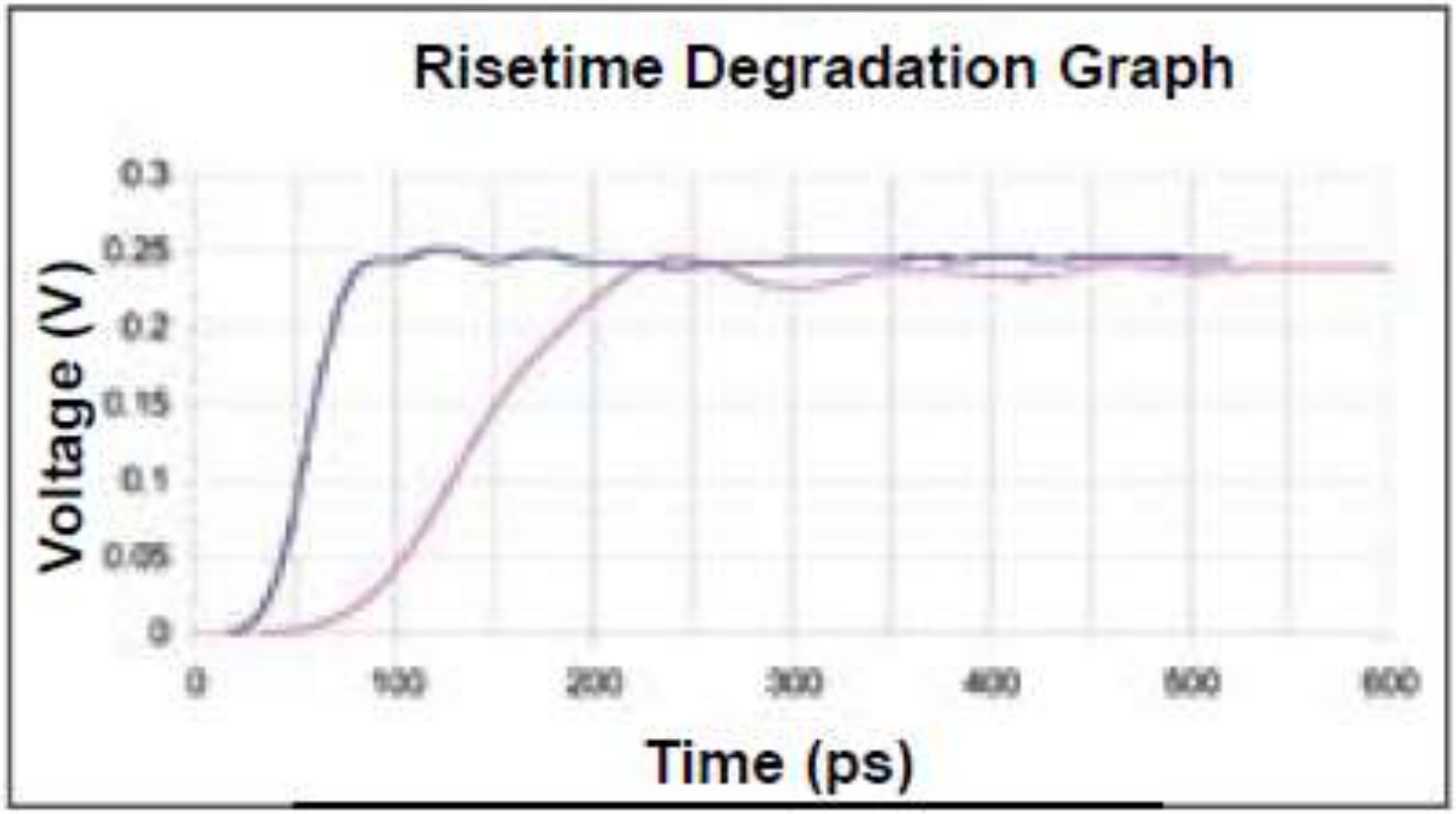
- For short traces, insertion loss is due to a poor match

- For longer channels, insertion loss is typically due to attenuation





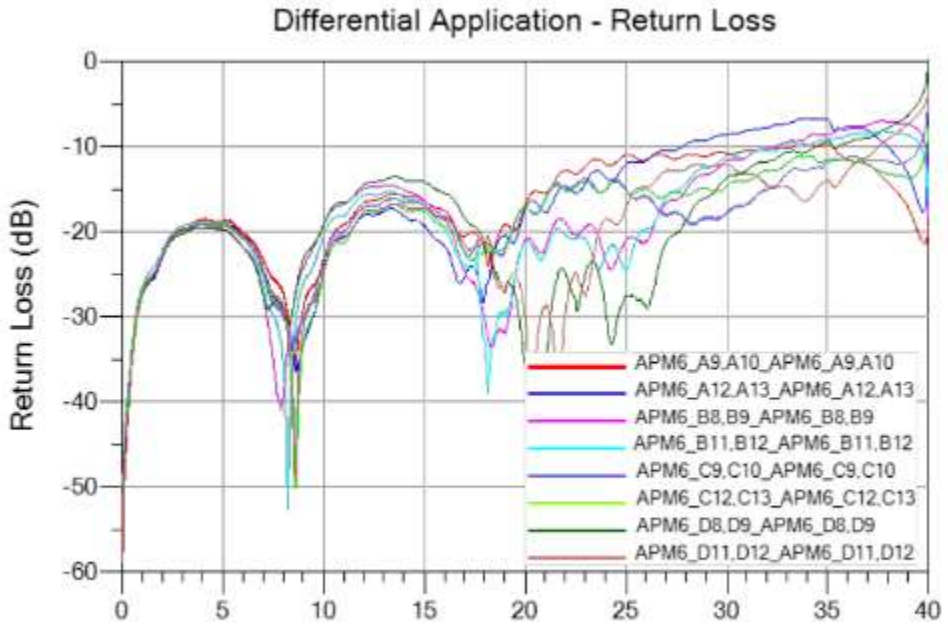
Risetime Degradation

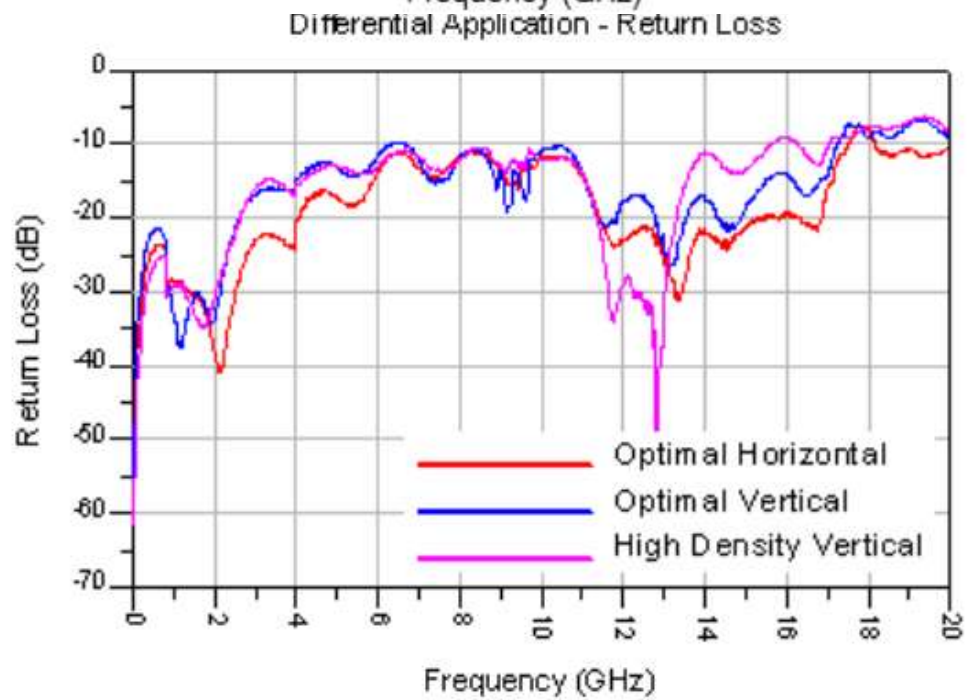


Input of 37ps and Output of 116ps = 309%
Rise Time Degradation

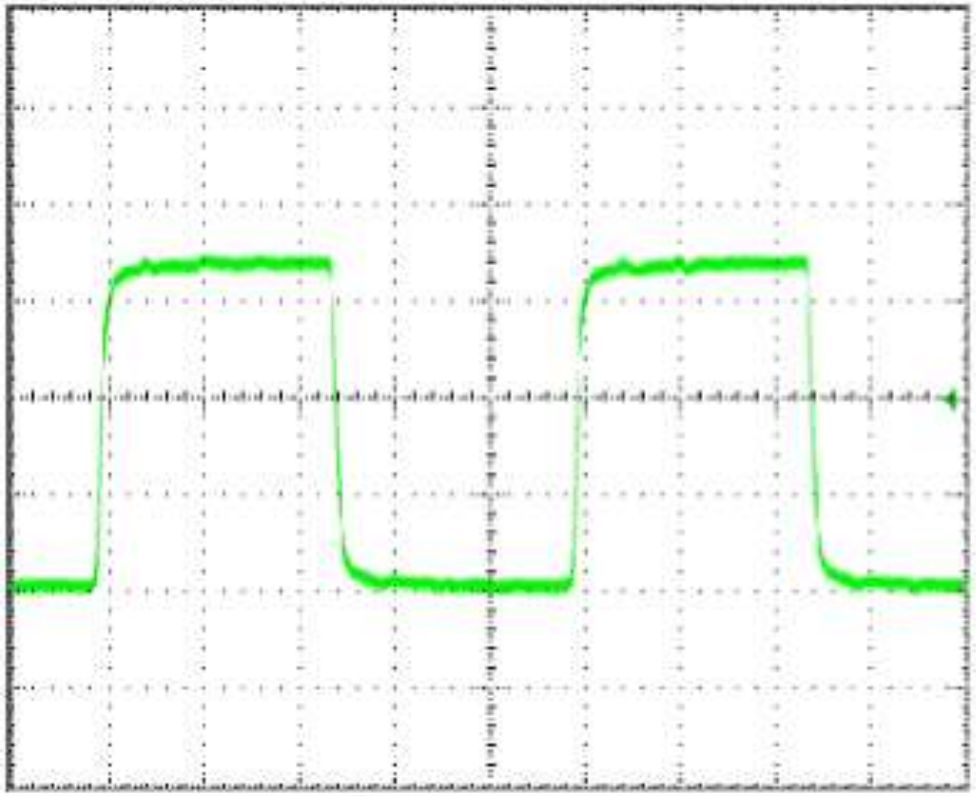
Return Loss (RL)

- The amount of energy reflected in a channel, expressed in dB
- Caused by impedance mismatch, which are in turn caused by discontinuities
- S11 and S22 would be the equivalent s-parameters in a 2-port network
- Return Loss = 10 log ($P_{in}/P_{reflected}$)

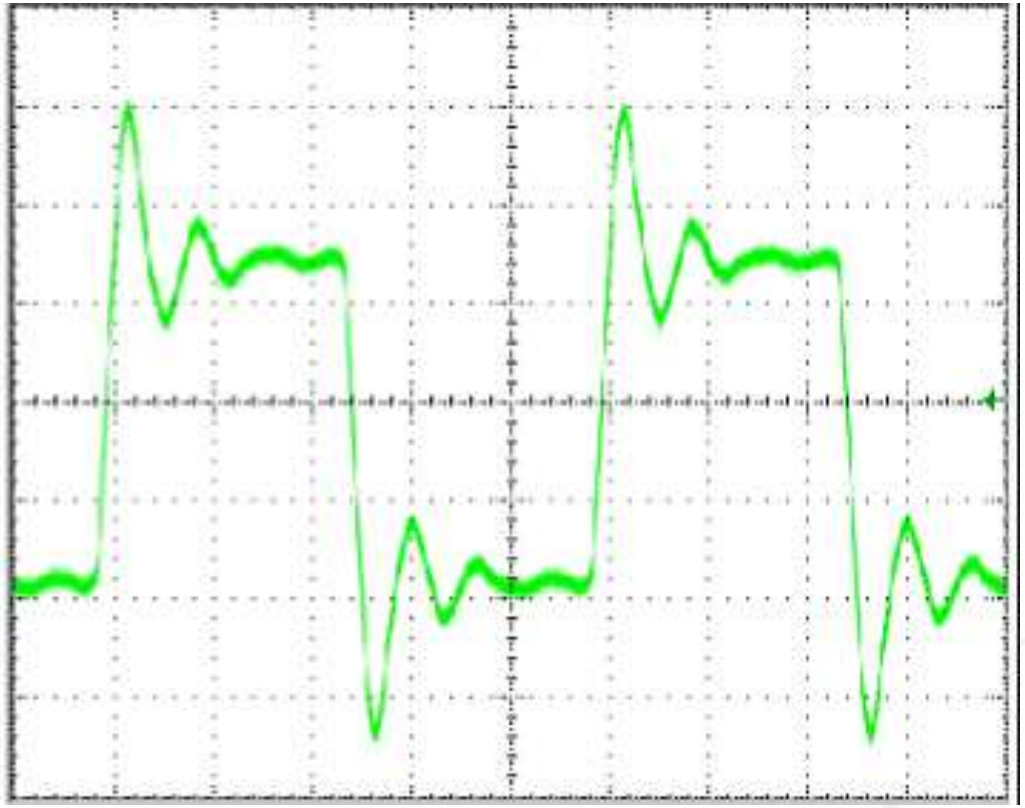




Reflection: Ringing/Ringback



Well-matched signal



Mismatched circuit

Return Loss (RL) Design Tips

- Typical acceptable return loss in digital electronics is -10dB
- This represents a 10% power reflection
- Allows for a fair amount of mismatch margin
- Depends on system requirements as some receivers are more/less sensitive than others

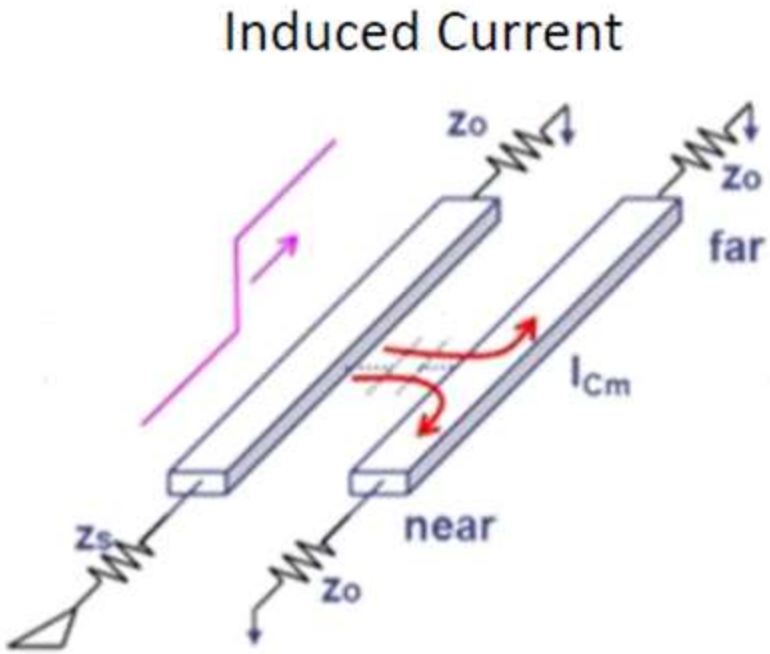
- RF systems can have requirements of < -15dB
- This represents a tight impedance match

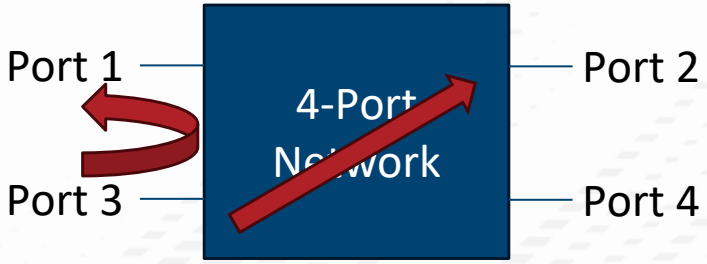
- Reflections can be dampened by IL
- Adding channel length after an area of mismatch can help a lot!

- Vice-versa if there's not much margin in IL budget
- Good RL = less energy lost (due to reflection) = better IL

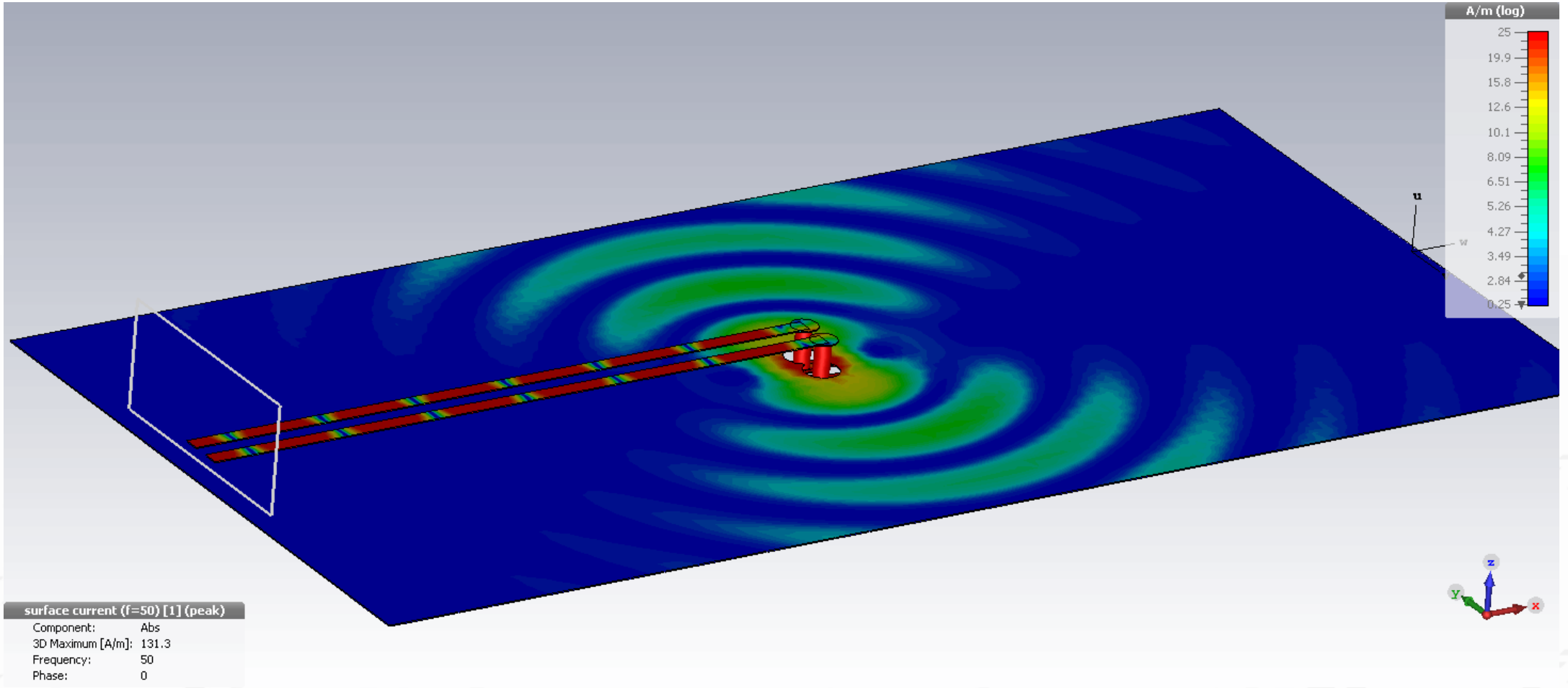
Crosstalk (XTLK)

- Unwanted noise coupled from an adjacent port or ports
- NEXT = NEAR END Crosstalk
  - Crosstalk coupled to the Tx end
- FEXT = FAR END Crosstalk
  - Crosstalk coupled to the Rx end
- Example above would be S13 and S23
- The same concept as EMI
- -30dB to -40dB is typically for NEXT/FEXT
  - Depends on system design!
- Some sensitive analog signals require > -70db

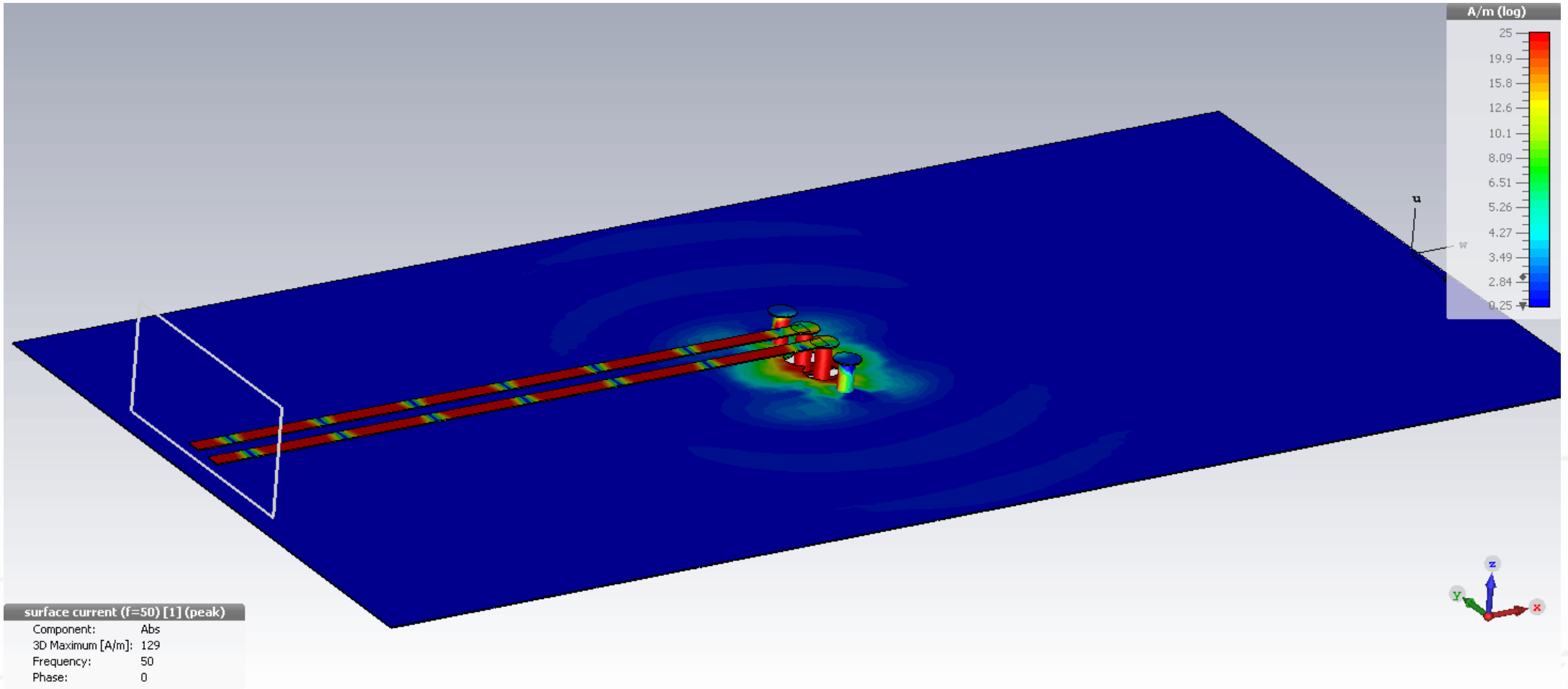




Via Transition



Effects of Ground Stitching



“Rules of Thumb”

- Impedance mismatch is fine if it’s within reason
- There’s no such thing as a perfect match

- Rules of thumb:
- Typical receivers can handle 5-7dB IL
  - A high-end FPGA can handle ~30dB IL
- 10dB or better RL for digital systems
- ~40dB XTLK

- Depends on the application and receiver specs
- Know the IC requirements
- Simulation is best to help prevent issues!

Design Tips to Improve SI

- Insertion Loss?
- Use better PCB materials
- Use Eye Speed Twinax Samtec Flyover® cables instead of routing through PCB
- Improve the design's impedance match –> less reflection = better insertion loss

- Return Loss?
- Match is the key!
- Add insertion loss to dampen reflections
  - Create more distance between adjacent signals (reduce the capacitance)
- Pulling pins between adjacent pairs
- Single ended vs. differential pair

Design Tips to Improve SI

- Crosstalk/EMI?
- Keep aggressive signals away!
- Use a stripline instead of microstrip (inner layer vs. outer layer)
- Use ground stitching and other layout methods to shield your signals
- Instead of pulling pins, tie them to ground to absorb the coupled energy
- Single ended vs. differential pair

- At the end of the day, it's all about choosing the right component and a good layout…
- Stackup
- Via and antipad design
- Via technology
- Proper routing of your diff pairs
- Appropriate guard traces and ground stitching

Computer-On-Module for High Performance Computing

- Why a new standard?
- The COM Express connector is limited
- Max. 32 lanes PCIe Gen 3.0 (8 Gb/s)
- Max. 10 Gb Ethernet per signal pair

- COM-HPC target
- Support for PCIe Gen 5.0 (32 Gb/s)
- 64 PCIe Lanes
- Min. 25 Gb Ethernet per signal pair to support 100 Gb Ethernet
- Update of other interfaces

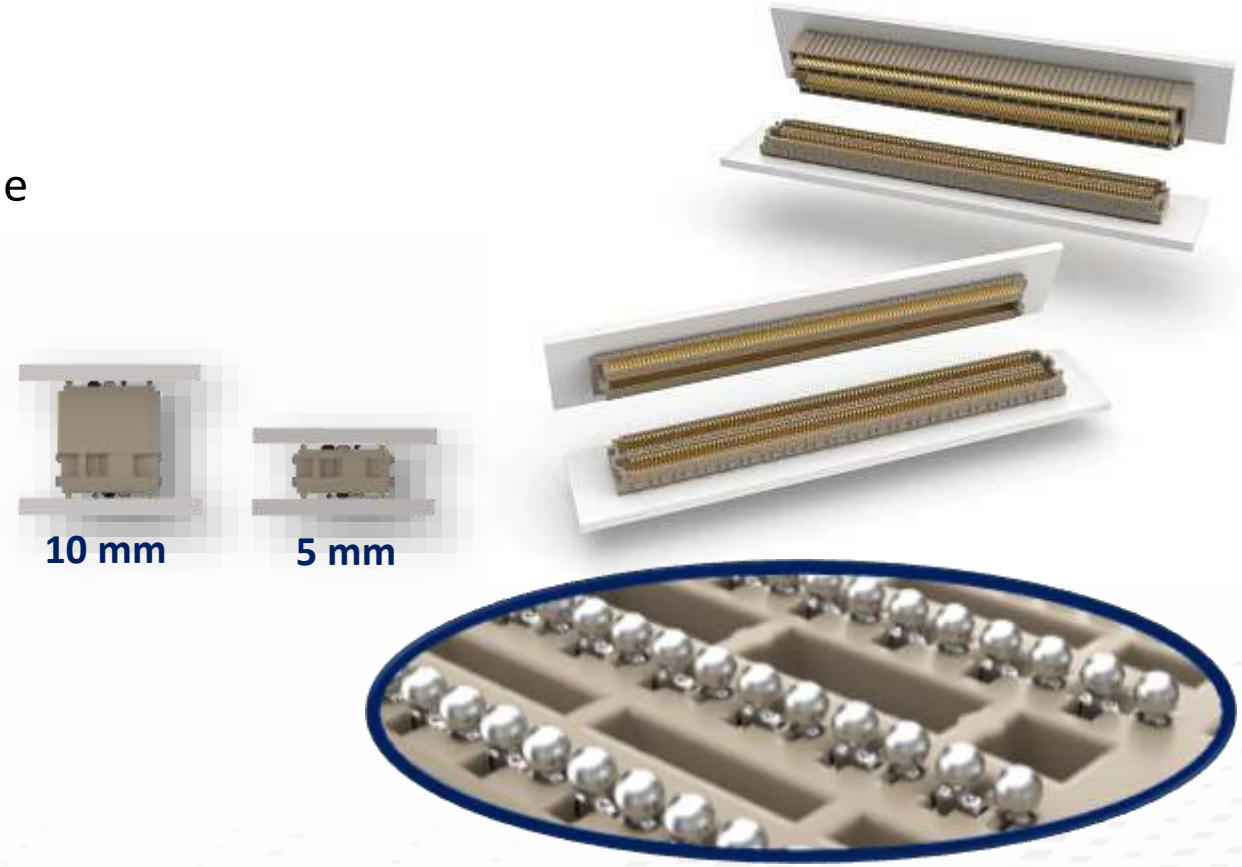
Feature	COM-HPC	COM Express
Connector Bandwidth	32 Gbps	10 Gbps
Connector Pins	800	440 max
Full size DIMMS	up to 8	up to 2
SO-DIMM Support	up to 4	up to 2
CPU power support	150W	80W
PCIe	up to 5.0	up to 3.0
PCIe lanes	65	32
10G BASE-T	2	1
Ethernet KR interfaces	8 at up to 25 Gbps	up to 4 at 10 Gbps
USB Support	Up to USB4	Up to USB 3.0
Non x86 CPU Support	Yes	No

- COM-HPC® will not replace COM Express®

- It extends the Server-On-Module ideas

Samtec COM-HPC Interconnect Solutions

- High-performance, flexible open-pin-field array
- High-speed PCIe® 6.0 and 100 Gb Ethernet capable
- 400 pin BGA mount (4 rows x 100 columns)
- 0.635 mm pitch
- 2.2 / 2.4 / 2.2 mm row pitch
- Dimensions: 68.62 mm x 9 mm x (5mm or 10mm)
- Up to 360 W at 11.4 – 12.6 Volts

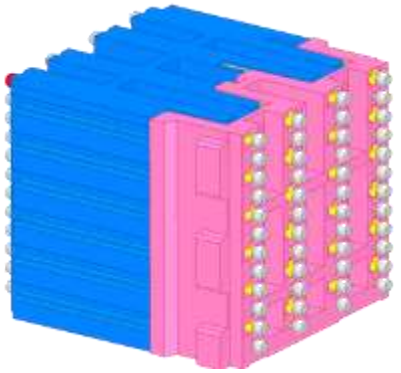


BGA mount increases density and performance

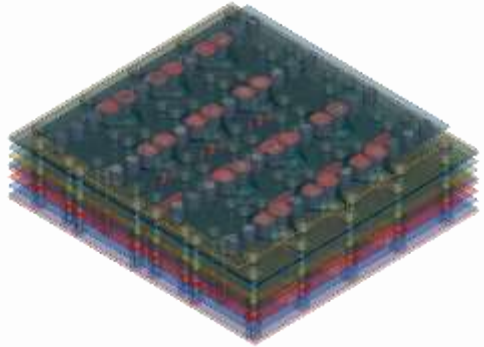
SI Simulation Results

- Determine loss budgets for the high-speed interfaces
- Built and solve 3D models to create S-parameters of key system components
  - Module and Carrier PCB models
  - Connector models
  - Stripline models
- Built and simulated channel topologies
- Results were documented in the specification

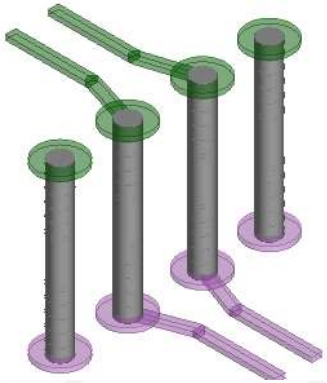
COM-HPC 5mm Connector Model



COM-HPC 10mm Connector Model



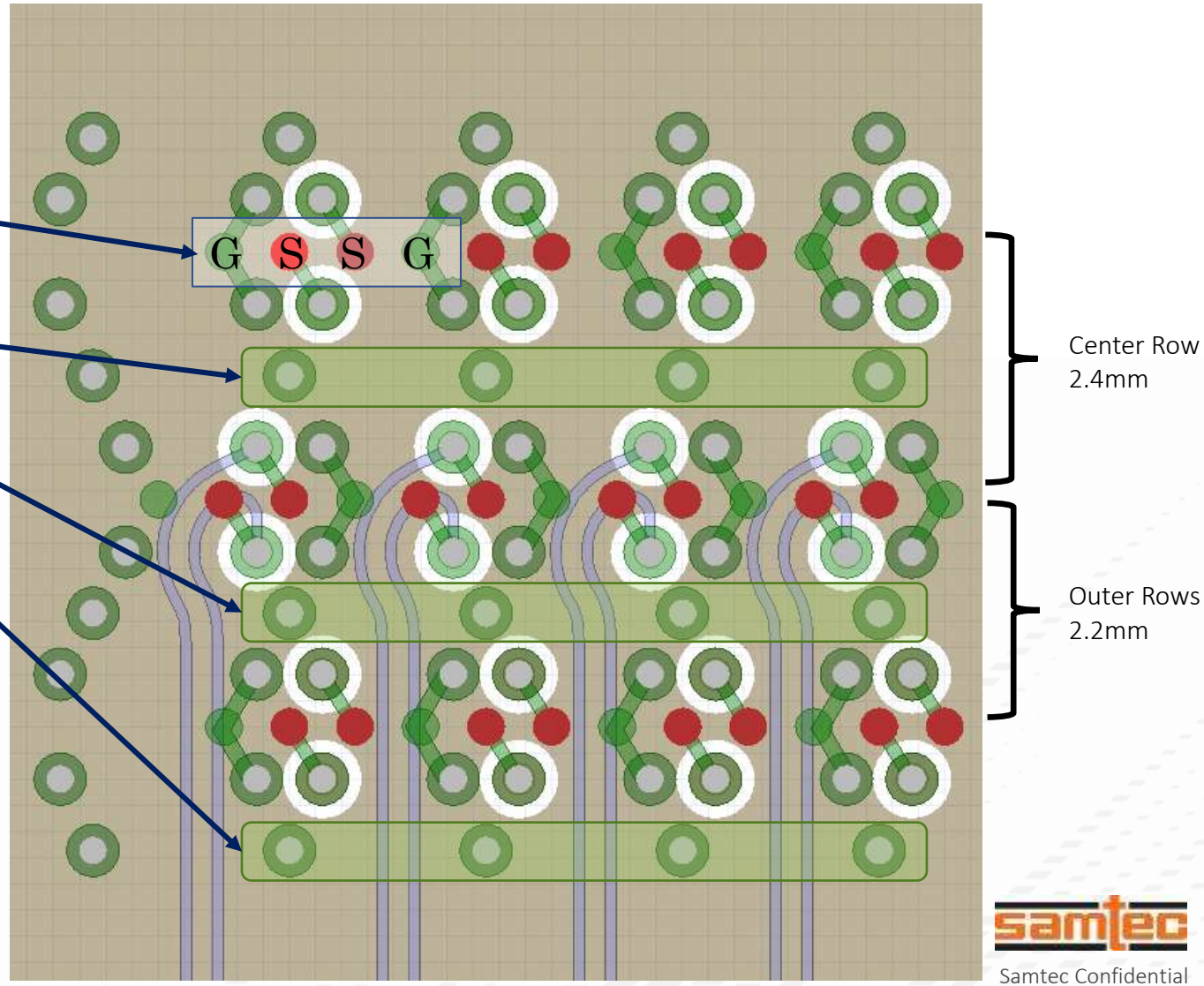
Module and Carrier PCB Models



Differential Via and Stripline Models

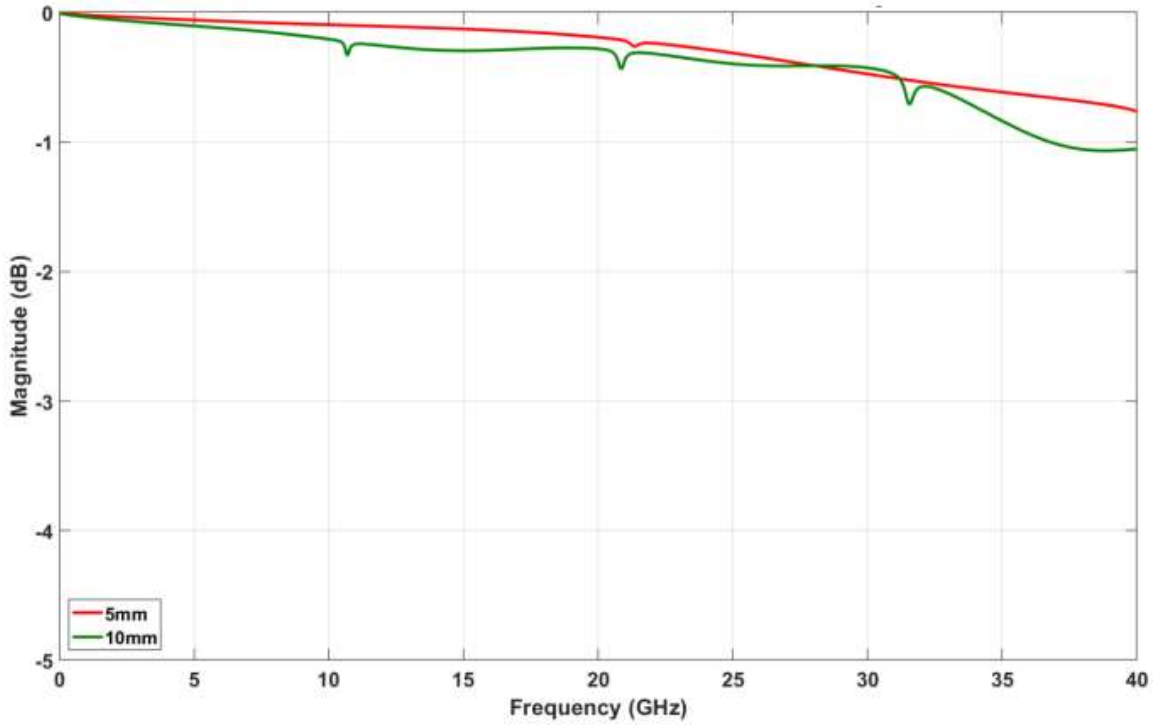
Recommended Differential Pair Breakout

- Increased row-to-row spacing:
- Maintains density (GSSG)
- Allows more GND VIAs
- Reduces Crosstalk
- Eases differential routing

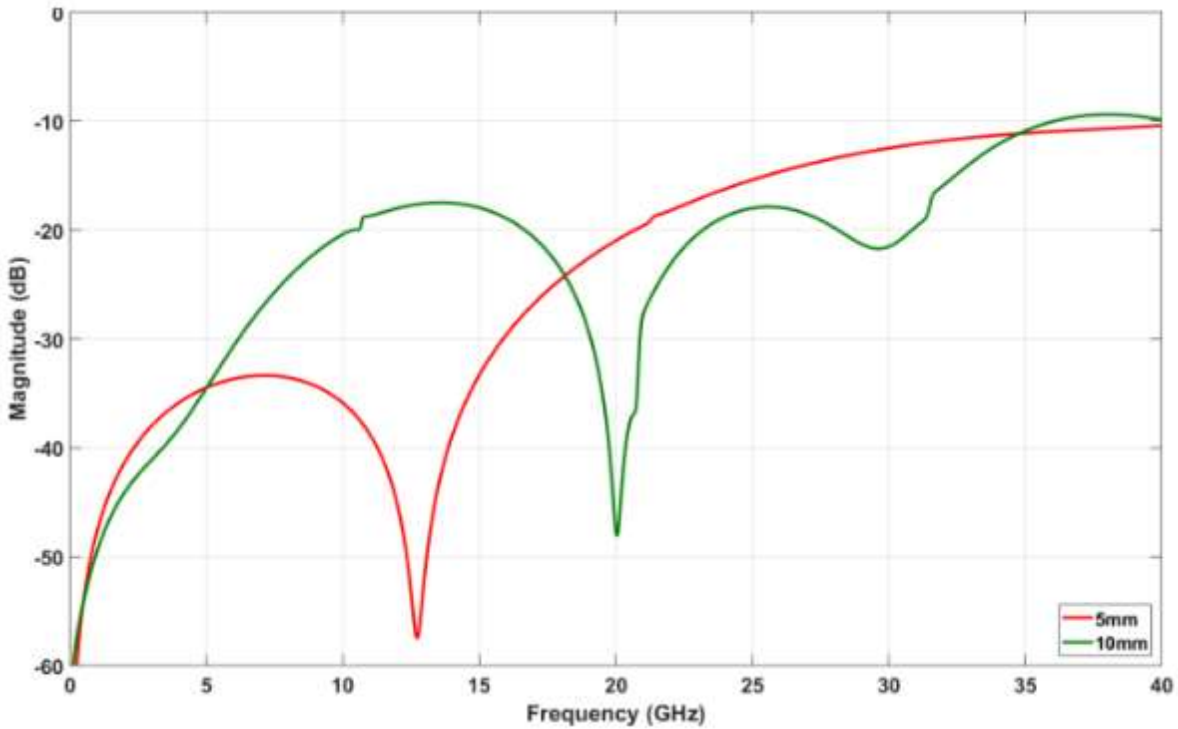


COM-HPC Interconnect Solutions SI Performance

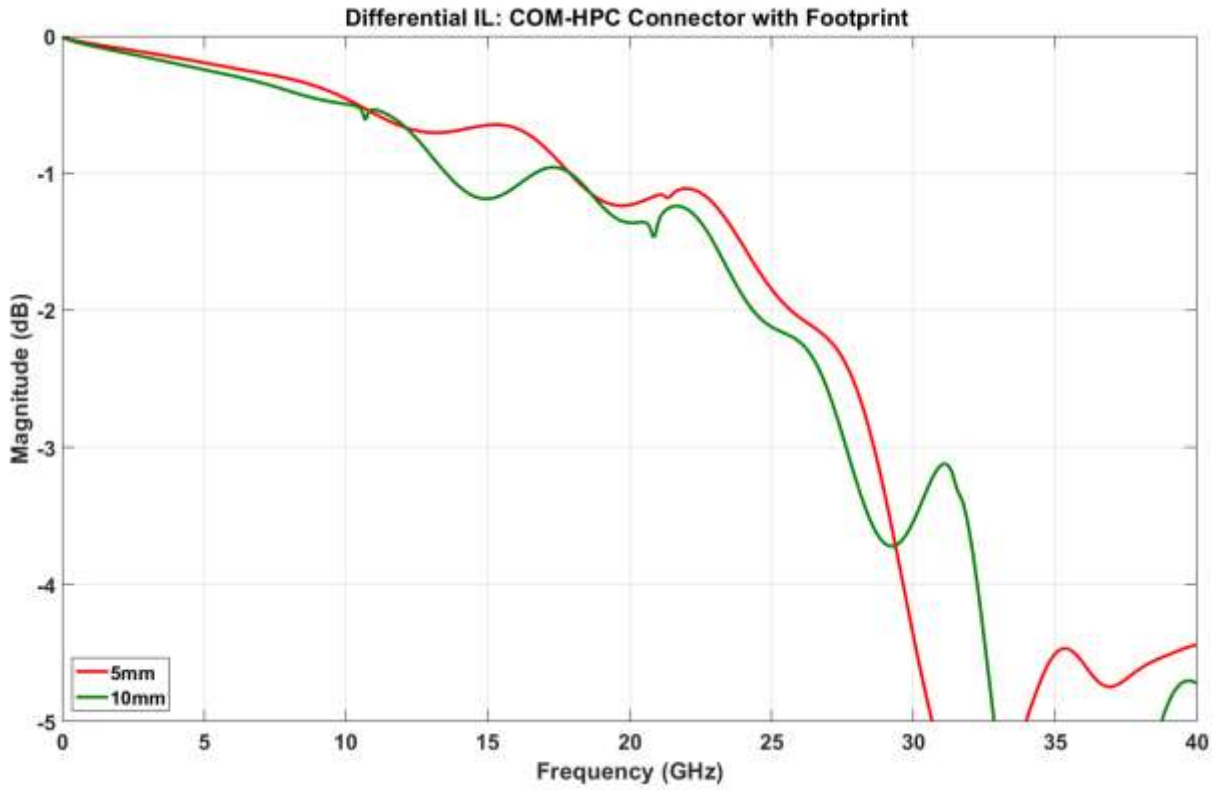
Differential IL: COM-HPC Connector

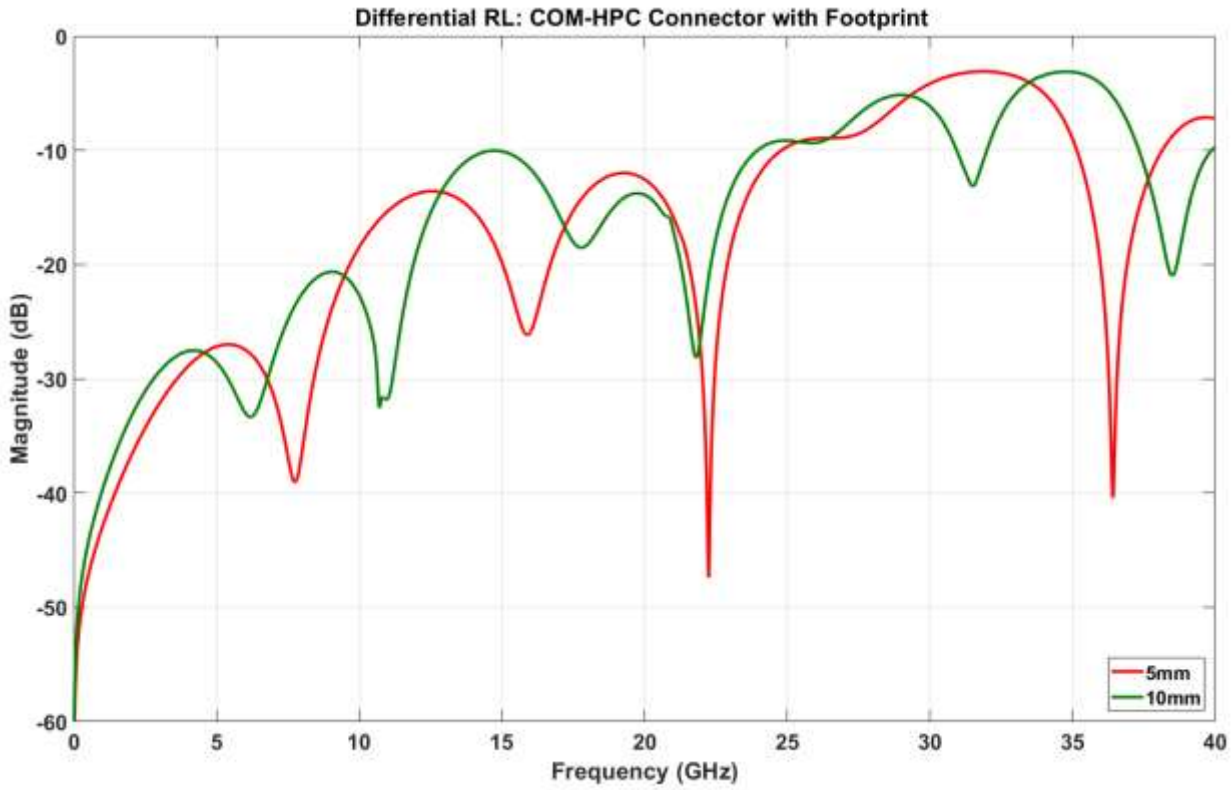


Differential RL: COM-HPC Connector



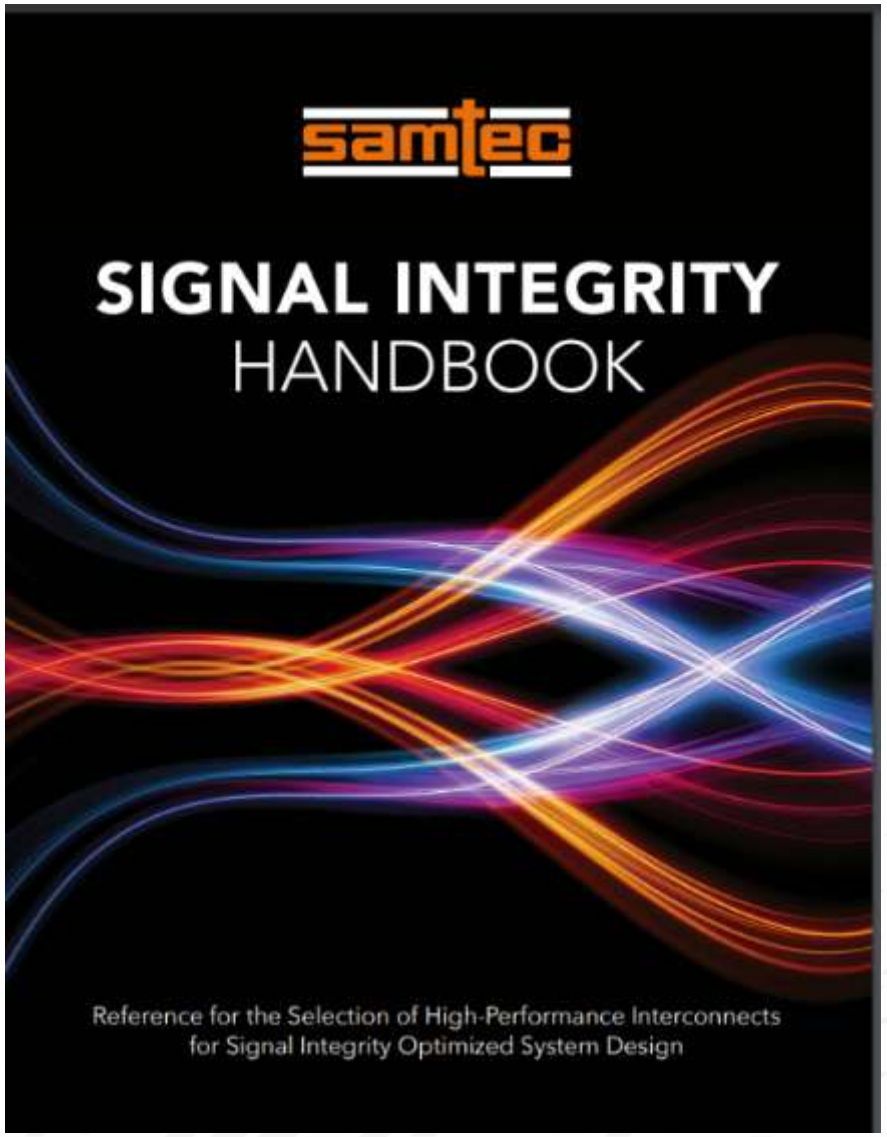
COM-HPC Interconnect Solutions SI Performance





Key Takeaways

- Samtec's global team of SI technical experts, online design tools and world-class customer service are available to support any high-speed embedded application
- Samtec offers a comprehensive portfolio of high-performance interconnect solutions ideally suited for embedded applications
- Samtec's new Signal Integrity Handbook offers an introductory resource to basic SI fundamentals
- For more information:
- www.samtec.com/SIG
- SIG@samtec.com



SUDDEN SERVICE®