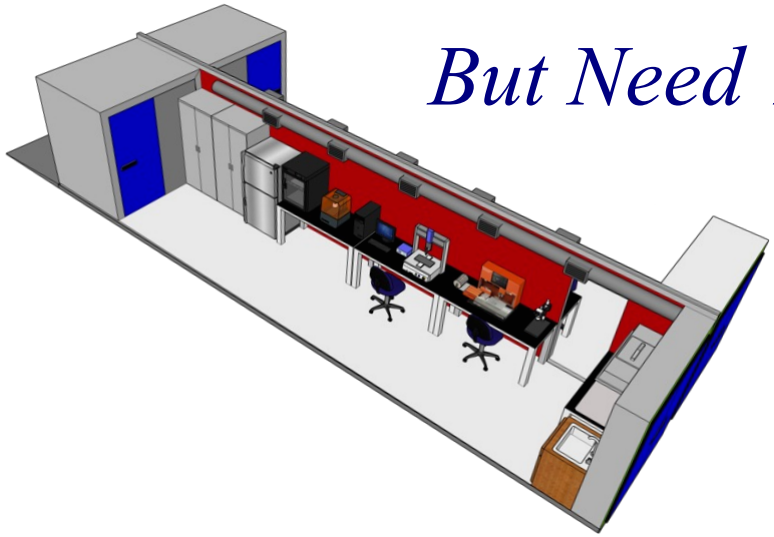
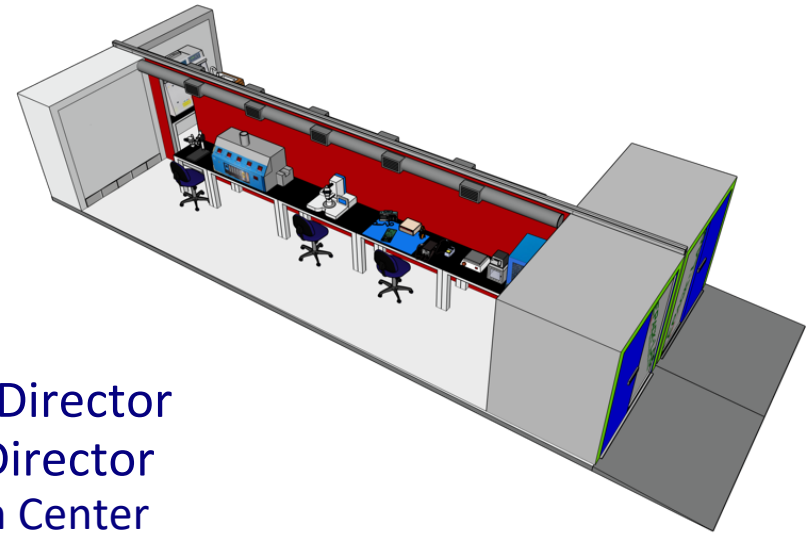
An Electronic Packaging Lab In A Box (for YOUR Community College)

But Need You For Deployment





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U.S. Department of Commerce, NIST, National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packaging Research and Development (R&D)

NOFO: 2025-NIST-CHIPS-NAPMP-01

Credit: Adobe Stock

- The NAPMP seeks to drive U.S. leadership in advanced packaging and provide the technology and skilled workforce needed for packaging manufacturing in the United States.
- Within a decade, NAPMP-funded activities, coupled with CHIPS manufacturing incentives, will establish a vibrant, self- sustaining, profitable, domestic advanced packaging industry where advanced-node chips manufactured in the United States and abroad can be packaged in appropriate volumes within the United States and innovative designs and architectures are enabled through leading-edge packaging capabilities.
- In combination with other CHIPS for America education and workforce efforts, NAPMP-funded activities will produce the diverse and capable workforce needed for the success of the domestic packaging sector.
- The objective of this NOFO is to enable, through R&D, innovative new advanced packaging flows suitable for adoption by U.S. industry.

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CHIPS R&D anticipates making available up to approximately $1,550,000,000 for funding

Anticipated amounts ranging from ~$10M to ~$150M over a five (5) year period of performance.

This NOFO envisions projects in five (5) R&D Areas:

R&D Area	Total Funding	Anticipated Max Award
(1) Equip., Tools, Processes, and Process Integration	$450M	$150M
(2) Power Delivery and Thermal Management	$250M	$50M
(3) Connector Technology, Incl. Photonics and RF	$250M	$100M
(4) Chiplets Ecosystem	$300M	$75M
(5) Co-Design / EDA	$250M	$100M

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Where do you fit in?

What can you do?
What can your company do?
What can this do for your Company?

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1.7 Project Level Non-Technical Plans

1.7.1 Education and Workforce Development (EWD) Plans

- NAPMP investments are intended to create innovation-driven domestic manufacturing capability, which requires fostering a diverse and capable domestic workforce with access to good jobs, such as those consistent with the Good Jobs Principles.
- The combination of expertise, facilities, and equipment required to meet the technical targets described in Section 1.4 provide *exceptional opportunities for tailored EWD programs*.
- In developing an EWD plan, CHIPS R&D *encourages applicants to consult the*
  - CHIPS R&D Education and Workforce Development (EWD) Plan Guidebook and
  - Department of Commerce Workforce Development Strategy Principles.

… describe any efforts to **attract and retain a diverse student and trainee population** and to demonstrate that the EWD efforts are worker-centered, industry-aligned, and promote high-quality jobs.

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Electronic Packaging *Lab in* A Box *(EPACK-LAB) Program*

Formal Edu driven by professional educators:

- Engineering science learning modules
- Training modules for the physical lab

Personnel additions & support:

- Electronics Manufacturing Technology Educator
- 2nd/3rd Career technical support Instructors
- Curriculum integration and collaboration

Infrastructure coordination for student:

- Full tuition waiver
- Childcare
- Incentive stipends

Industry-Wide sustainability support

- Empower small business two-way partnership
- Expand the 'BOX' to be a prototyping business

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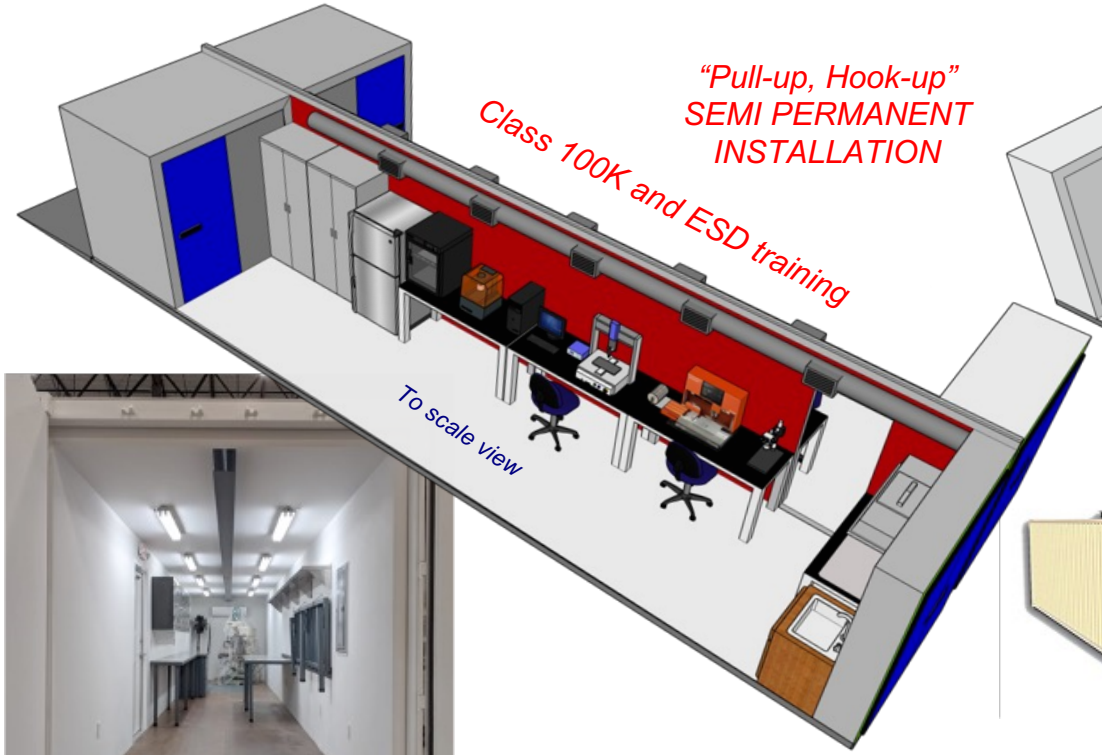
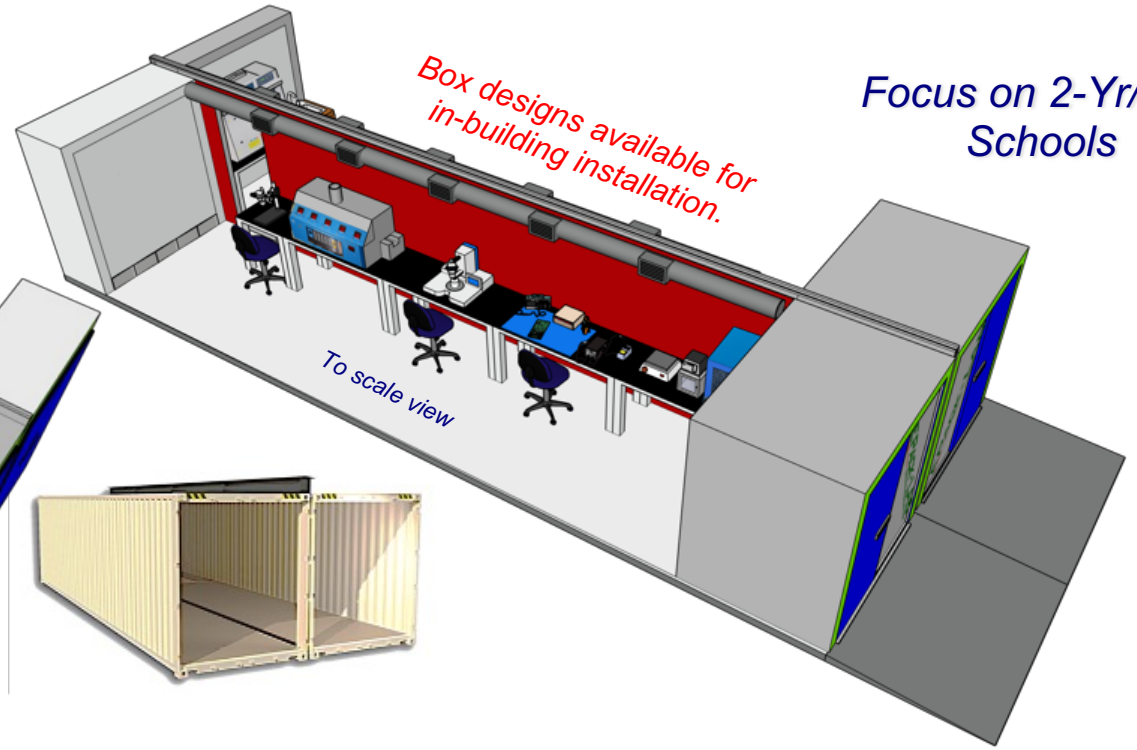
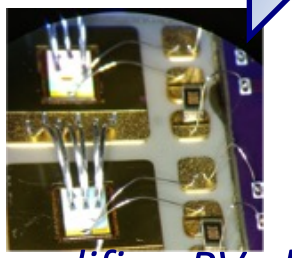




Focus on 2-Yr/4-Yr Schools

The EPack-LAB trains the manufacturing workforce in processes to:

Integrate chips into packages



Integrate packages into boards

Integrate boards into systems

Example Project Outcomes: *Audio amplifier, PV phone charger, Drone propulsion, LED light show, etc.*

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Example: Process Flow for Students

Pre-Project Work [Use Mfgr Mgmt. Syst.]
1. Create CAD & ckt layout drawings:
   - Housing, Assembly fixture(s), PCBs
2. 3D print housing and fixtures
3. Order parts and materials
   - Chips, solder, PCB, etc.

Needed Parts & Materials:
1. Semiconductor chips and electronic components
2. die attach (solder, from fridge)
3. substrates/PCBs
4. assembly fixtures
5. module housing and terminals

START:
1. Enter cleanroom, follow lab protocols
2. Vacuum shoes, use tacky mat
3. Wear lab coat. eye protection, gloves
4. Use ESD bands where needed

PROCESS PREPARATION

Retrieve materials
Verify documentation

Start belt oven
Verify profile/settings

Clean chips
and substrates

Load solder dispenser &
program. Verify cycle

Load pick-n-place parts
& map. Verify cycle

PROCESS FLOW

DISPENSING OPERATION
Mount substrates/PCBs
Dispense solder
Verify results

COMPONENT PLACEMENT
Verify component placement map
Load substrate/PCB
Place components. Verify results

SOLDER REFLOW
Run substrates/PCBs thru oven
Verify results with shear testing

WIRE BONDING
Verify bond pattern
Bond chips

FINAL PACKAGING
Mount substrates/PCBs and terminals in housing. Dispense encapsulate. Vacuum cure encapsulant.

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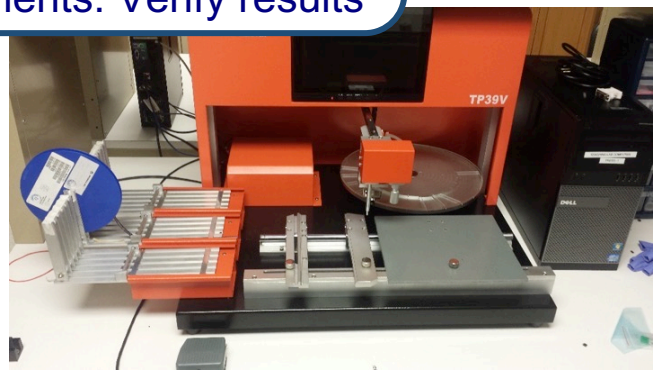
PREES: PROCESS FLOW

DISPENSING OPERATION
Mount substrates/PCBs
Dispense solder
Verify results

COMPONENT PLACEMENT
Verify component placement map
Load substrate/PCB
Place components. Verify results



SOLDER REFLOW
Run substrates/PCBs thru oven
Verify results with shear testing

WIRE BONDING
Verify bond pattern
Bond chips

INFORMATION TECHNOLOGY FOR MANUFACTURING:
- Computer Aided Design
- Statistical Process Control (SPC)
- Manufacturing Execution Systems (MES)
  - Process Management [e.g. Simul8]
  - Supply Chain Management [e.g. Simul8]

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WE NEED TO CREATE A SEED "PROPOSAL" FOR FUNDING

WHAT OUR PROPOSAL WILL DO:

Identify and Organize Infrastructure Teams To:

- Contact 2Yr/4Yr college administrators to define the rural needs
- Contact small rural businesses to define their workforce needs
- Advertise and solicit potential "2nd/3rd – Career" technical training staff
- Contact large equipment manufacturers to define human/machine interface needs (AR/VR)
- Contact national technology development HUBs to synergize with their WFD/EWD programs

Create metrics and a preliminary business plan to identify potential business(es) to design, build, transport, install & warrant an EPack-LAB fabrication facility

Develop a National Proposal Team bringing together the above Teams, MEC Hubs, and identify the key metrics and budget for national deployment of the EPack-LAB program

SIGN UP TO MAKE A DIFFERENCE

https://go.ncsu.edu/epack-lab-partners

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3D Heterogeneous Power Integration Incorporating ANN ML and Genetic Algorithms for TSV/TGV Optimization

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