Switch-Mode Power Supply Layout

BEST PRACTICES FOR PCBA DESIGN

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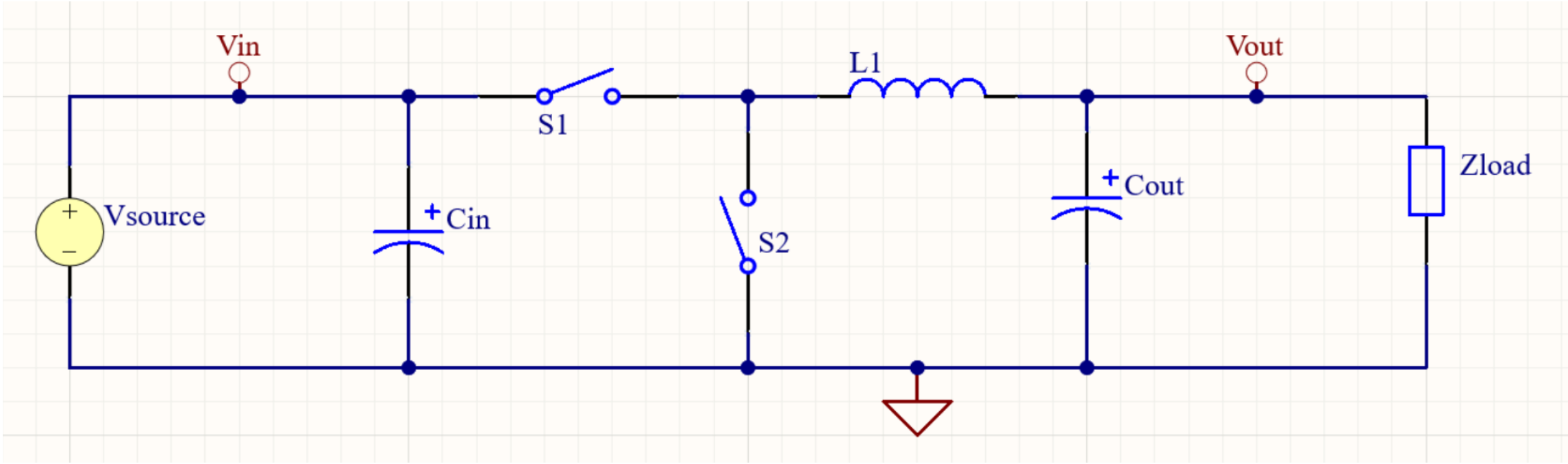
Agenda

- Review of Switch-Mode Power Supply (SMPS)
- Why EMI and SI matter
  - Electro-Magnetic Interference
  - Signal Integrity
- Circuit Theory and Wave Theory
- When is a signal “High Frequency”
- SMPS and High Frequency
- Recommendations
  - Good Practices
  - PCB Stackups
- Questions and discussion

Types of SMPS Circuits

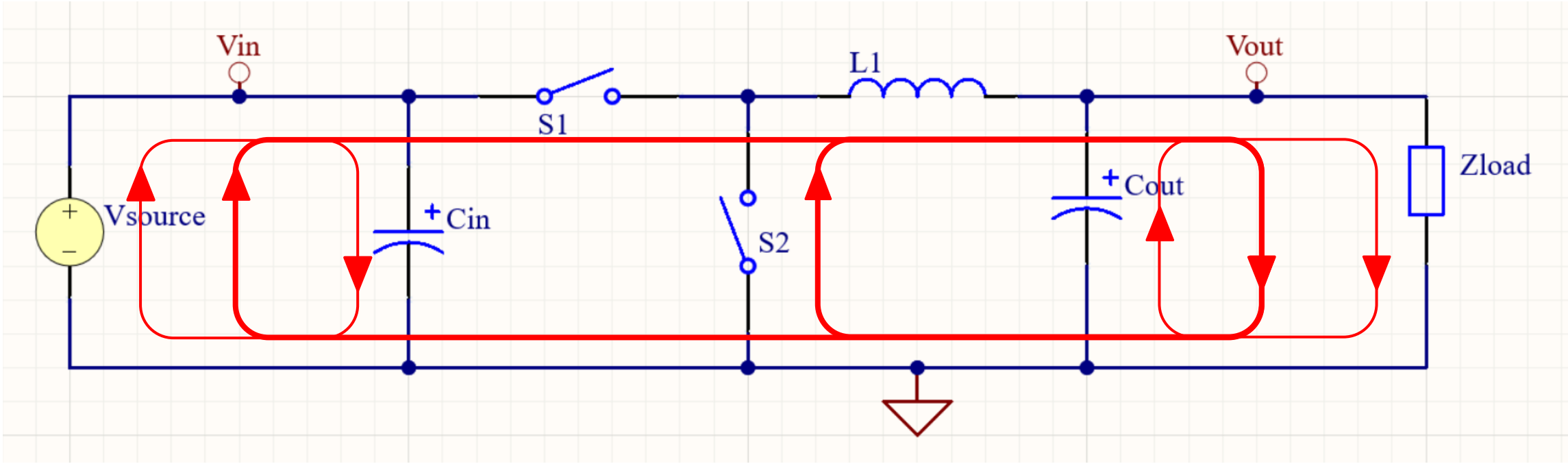
Buck-Mode SMPS

Simplified circuit (power only)



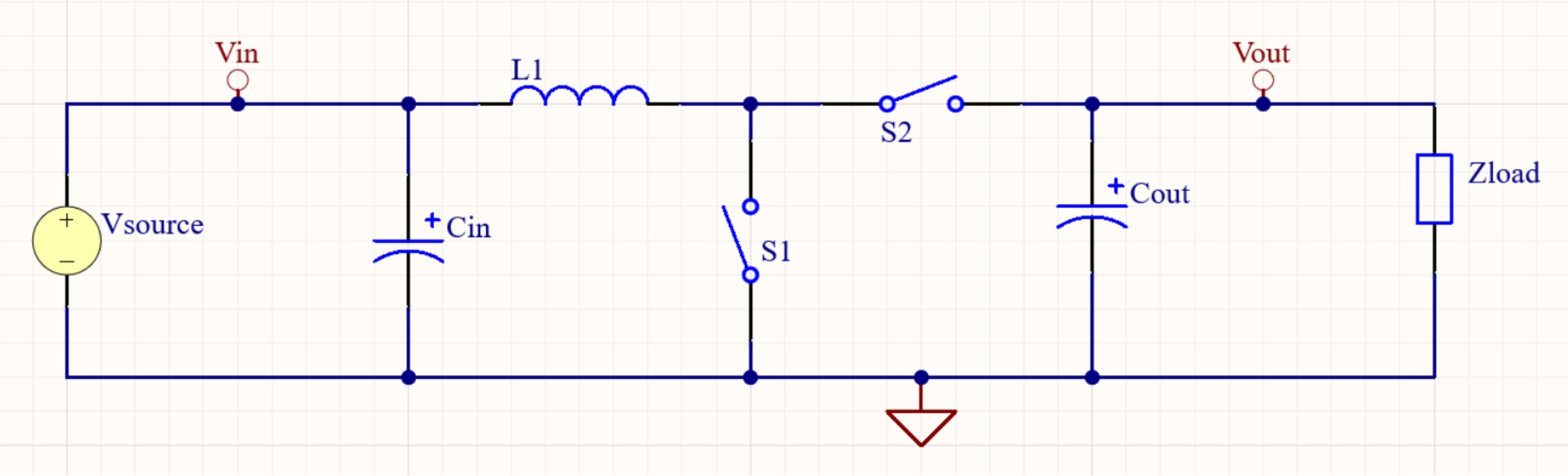
Buck-Mode SMPS

Current Flow



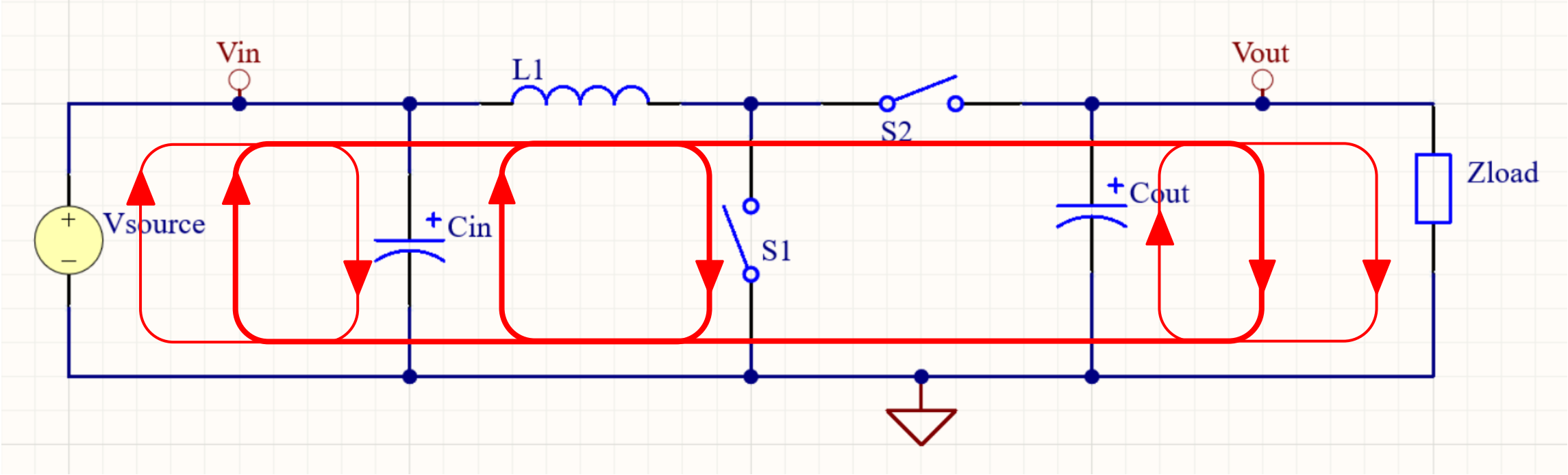
Boost-Mode SMPS

Simplified circuit (power only)



Boost-Mode SMPS

Current Flow



EMI and SI

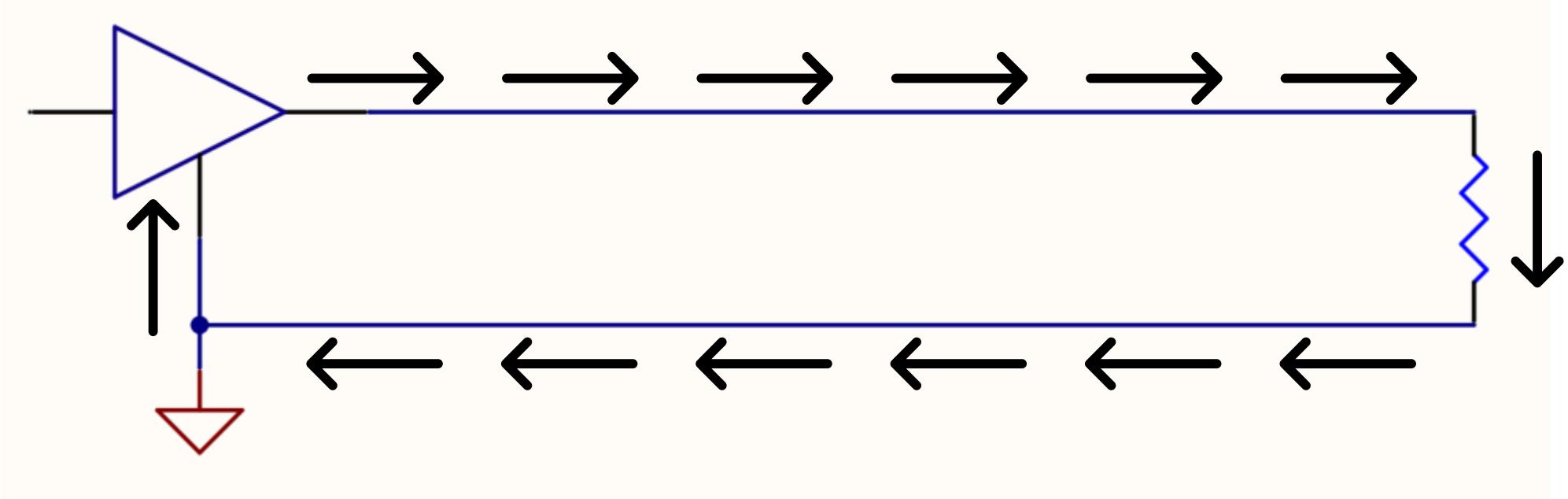
EMI and SI

- Everything we sell must obey FCC rules.
- An SMPS inherently has high frequency.
- Any part of a circuit with high frequency could interfere with other circuit parts.
- The principles for avoiding EMI problems are very similar to maintaining good SI.

Good layout habits will pay off later

Circuit Theory and Wave Theory

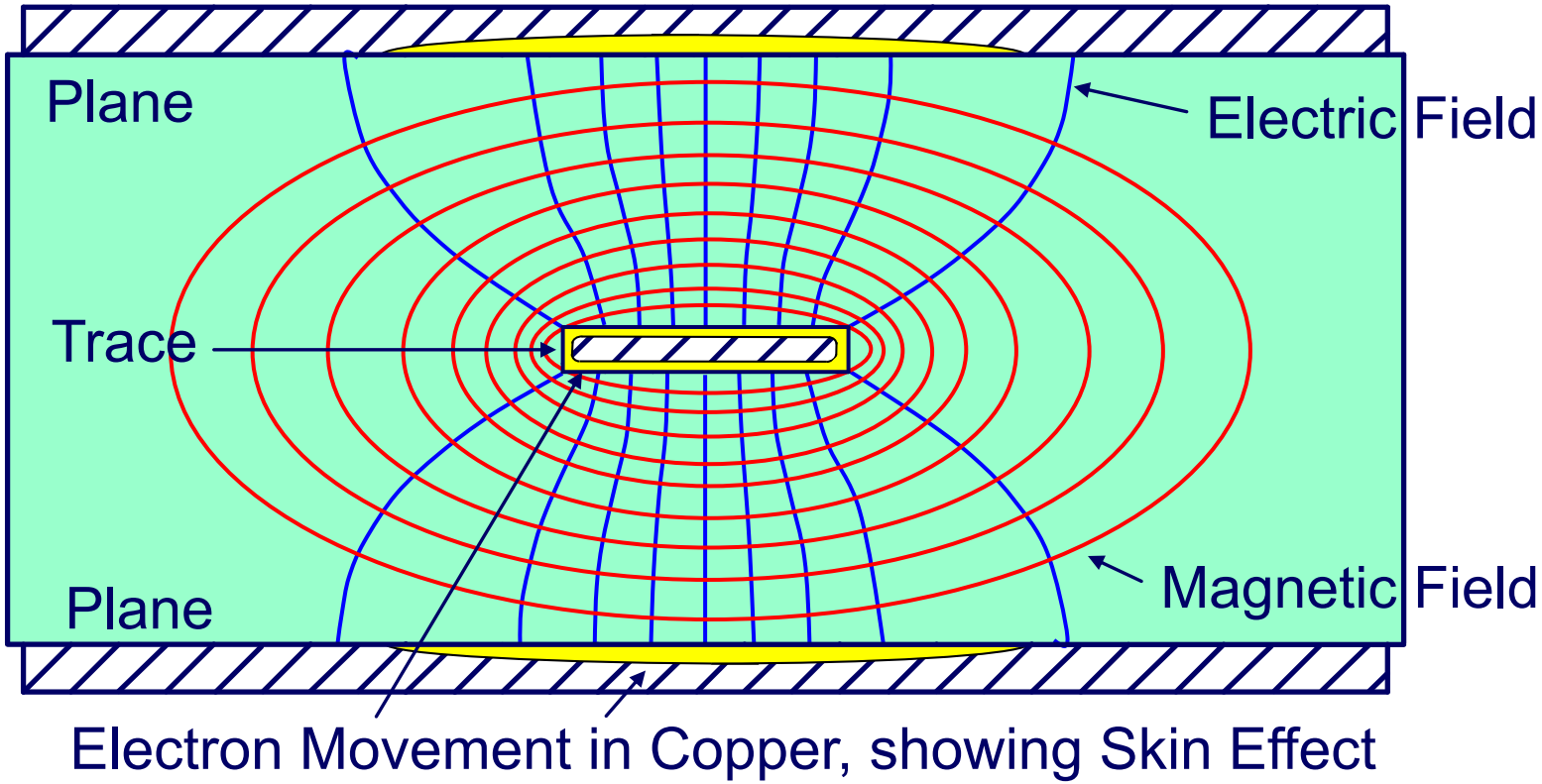
Circuit Theory…



… is WRONG

Voltage and Magnetic Fields

Stripline (Inner layer trace and return planes)



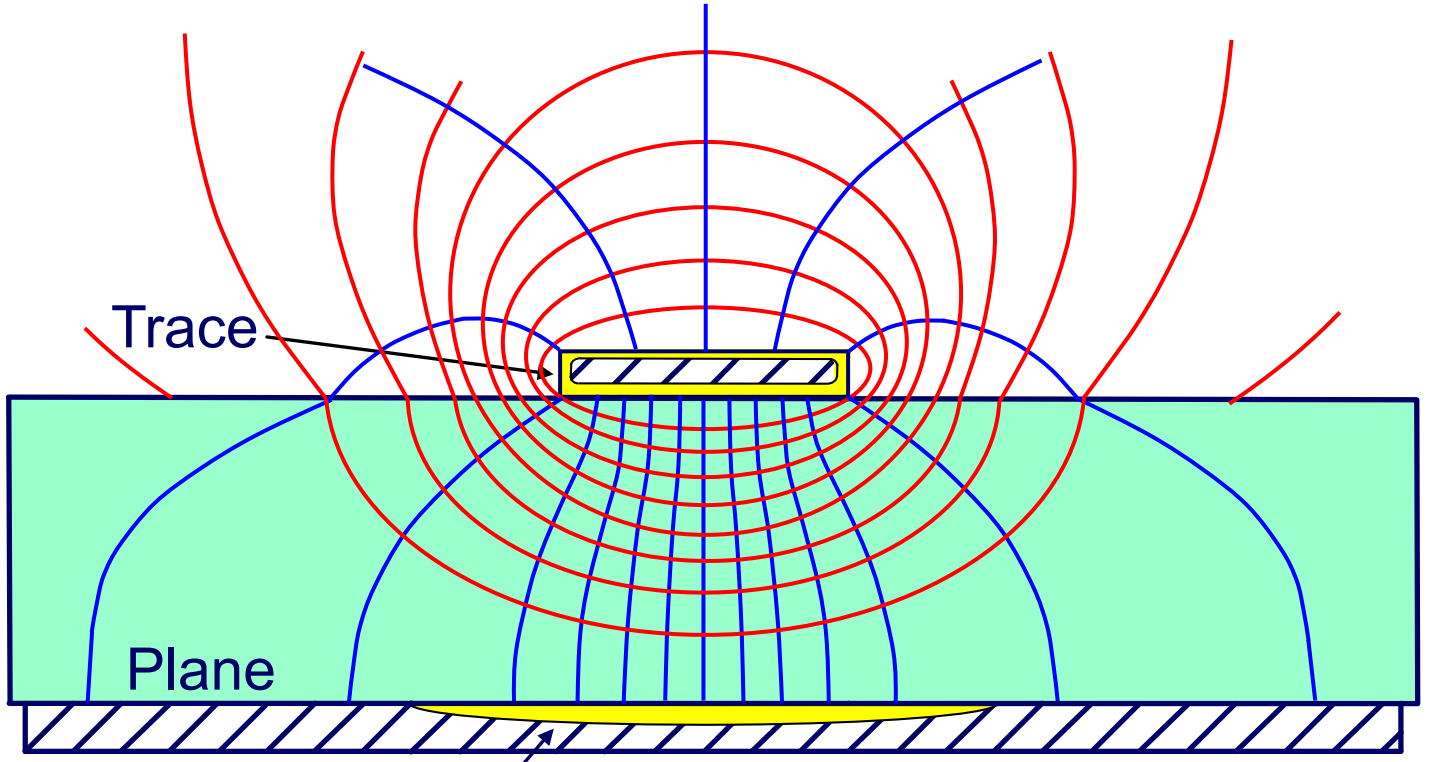
Original source:

RHARTLEY ENTERPRISES
CONTROL OF NOISE, EMI & SI

Low Volume Fields (EM Wave), Completely Contained.

Voltage and Magnetic Fields

Microstrip (Outer layer trace and return plane)



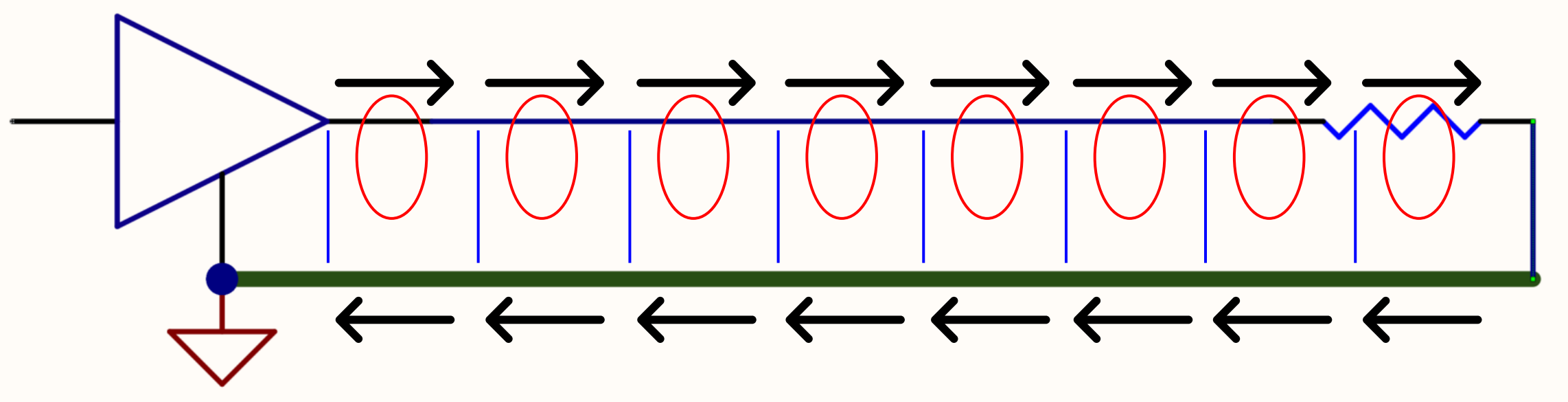
Original source:

RHARTLEY ENTERPRISES
CONTROL OF NOISE, EMI & SI

Moderate Volume Fields (EM Wave), Mostly Contained.

Voltage, Current, and Waves

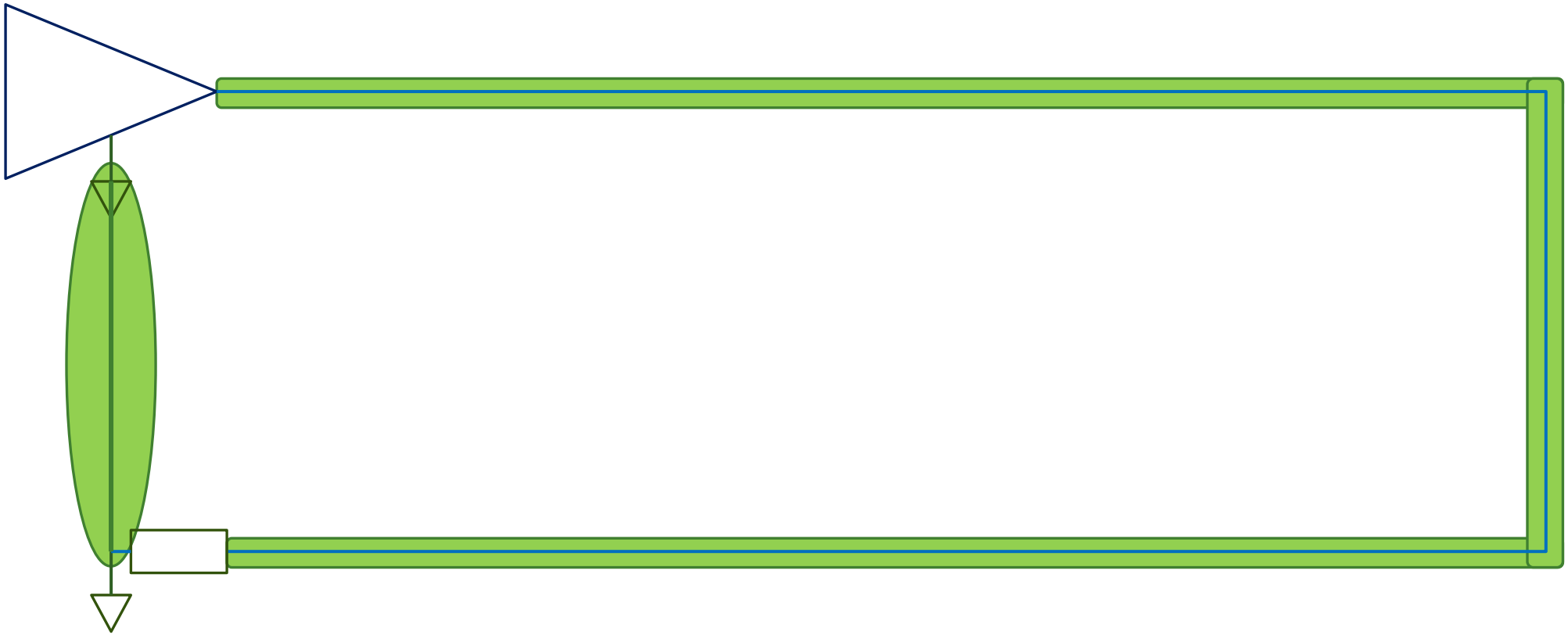
- How does the signal go from the source to the load?



Energy is in the Waves (traveling *between* the layers)

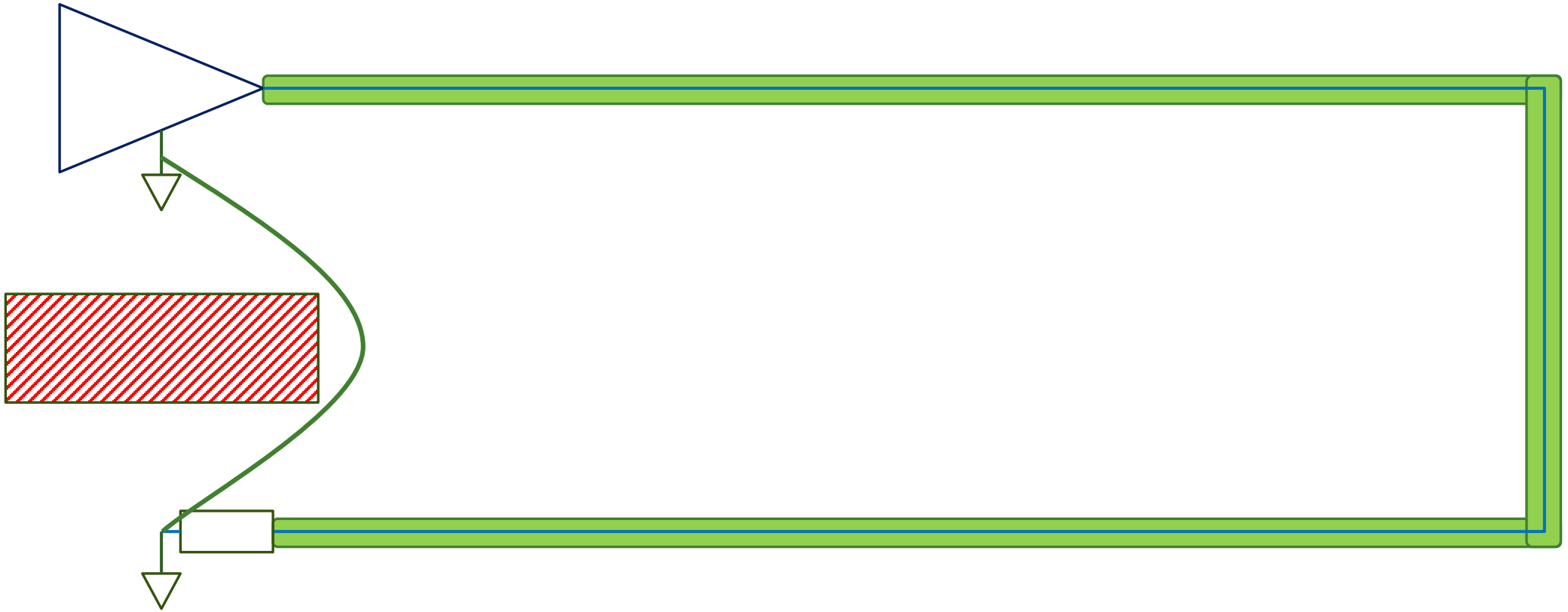
Path of Return Current

- 2-Layer board, components and signals on top, “ground” plane on bottom



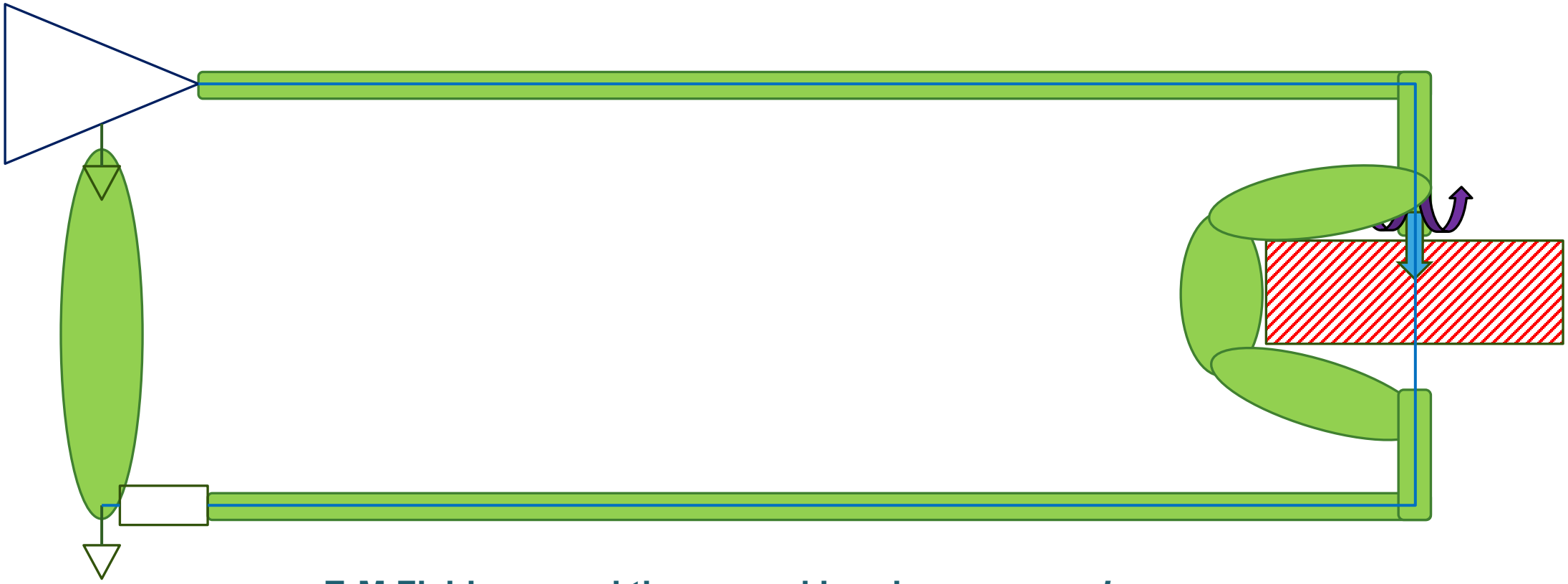
Path of Return Current

- Same layout, except there's a cutout in the ground plane (between source and load)



Path of Return Current

- Same layout, except there's a cutout in the ground plane (under the trace)



E-M Fields around the ground break are a *mess!*

High Frequency

What makes “High Frequency”?

- Frequency ranges where it becomes a problem
- Edge rate v. Repetition rate

What makes “High Frequency”? (part 2)

- The **Rise Time** of a signal has an equivalent frequency:

$$f \approx 0.35 / t_r$$

- Frequency (repetition rate) tells you how often the problem happens

- Rise Time tells you how bad the problem is

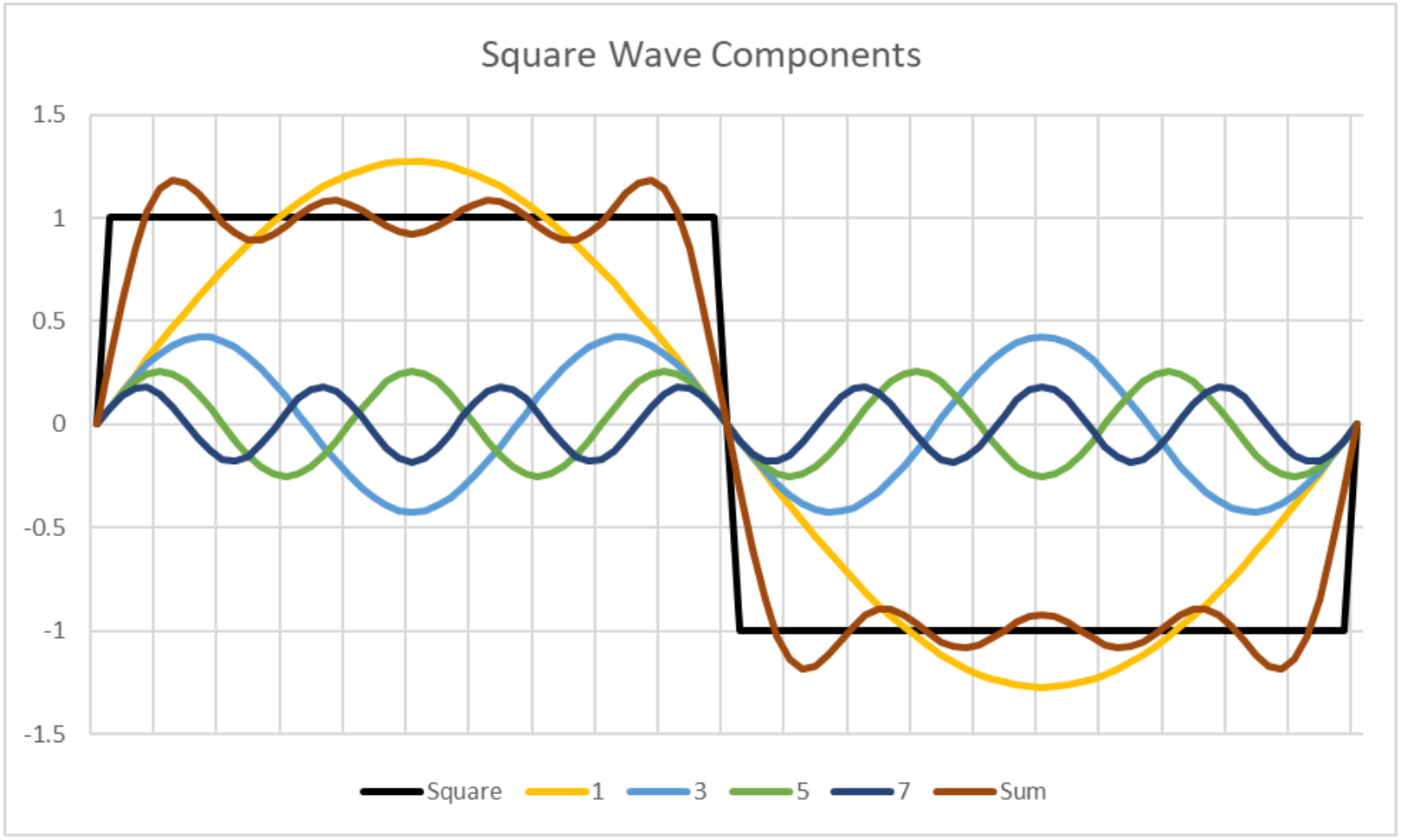
Edge Rate is the important factor

Why focus on “Rise Time”?

- The concern is about EM energy radiating out of the circuit
- Large dV/dt can radiate an Electric Field
- Large di/dt can radiate a Magnetic Field
- In the far field, they are one signal that can interact with other circuits

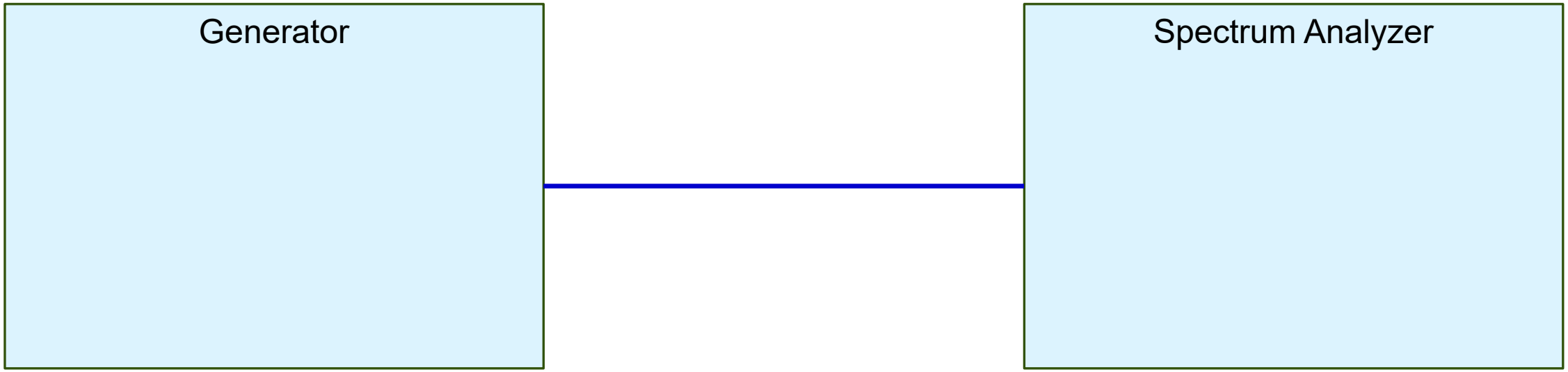
EMI problems are usually found with high di/dt

Is a Square Wave “High Frequency”?



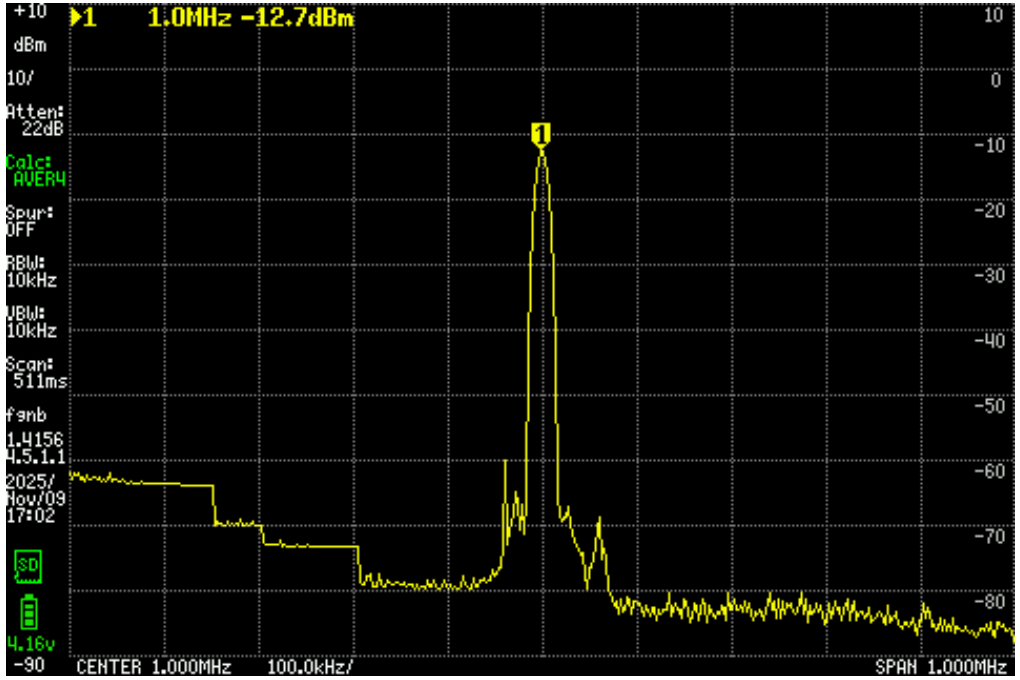
A Square Wave contains Sine Waves

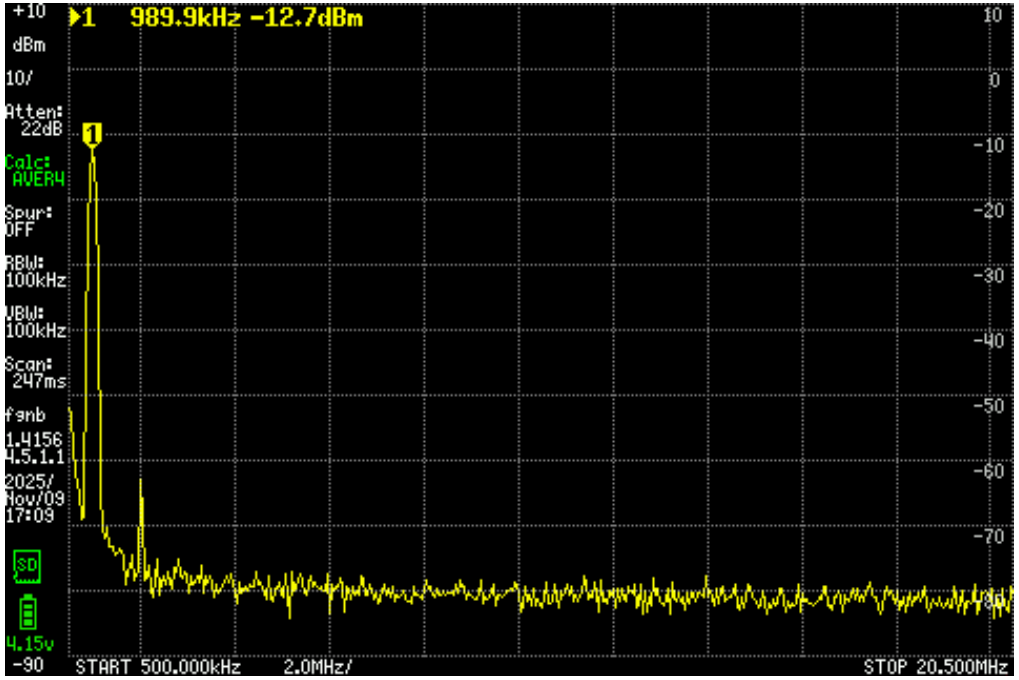
Demonstration: Square Wave and Sine Wave



Sine wave on Spectrum Analyzer

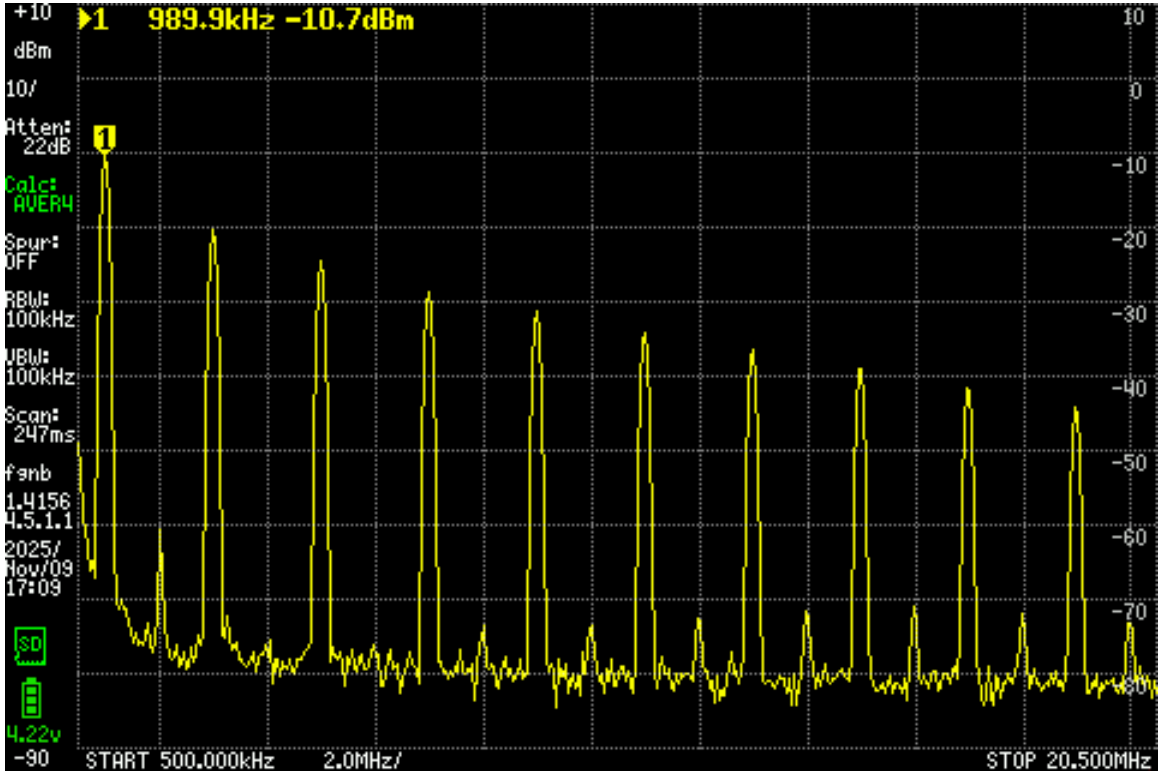
1 MHz output (different frequency range on SpecAn)





Square wave on Spectrum Analyzer

1 MHz output (same extended frequency range on SpecAn as last Sine wave picture)



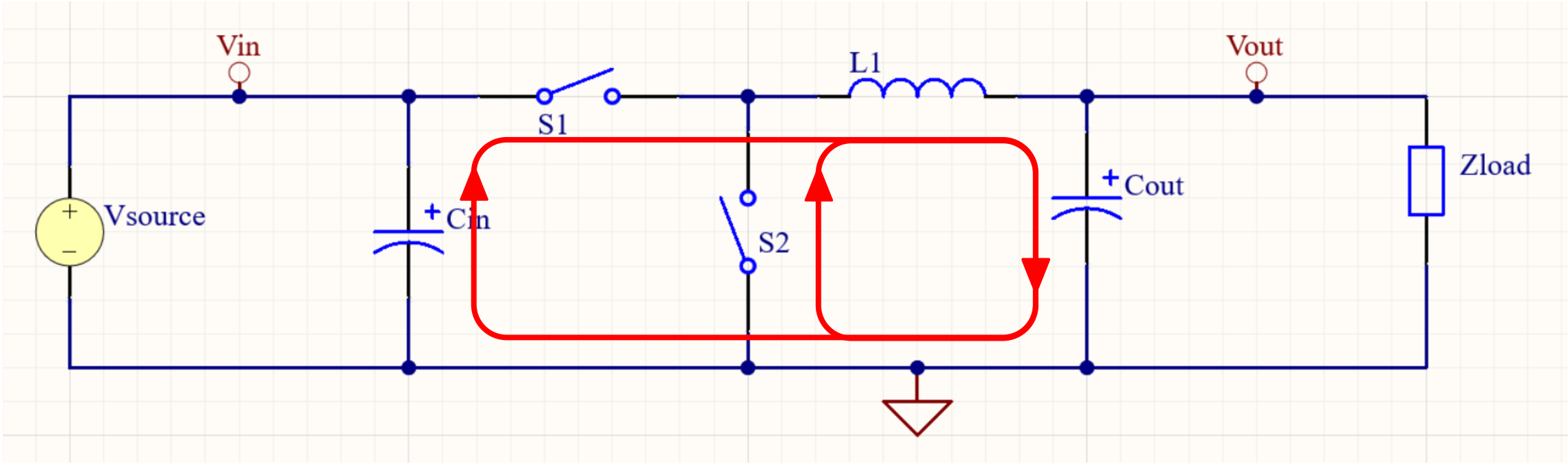
SMPS and High Frequency

Energy Paths in SMPS Circuits

- DC energy and AC energy are following different (but overlapping) paths
- The paths depend on the type of SMPS
- The Signal and Return Paths have a big impact
  - EMI
  - Efficiency
  - Stability

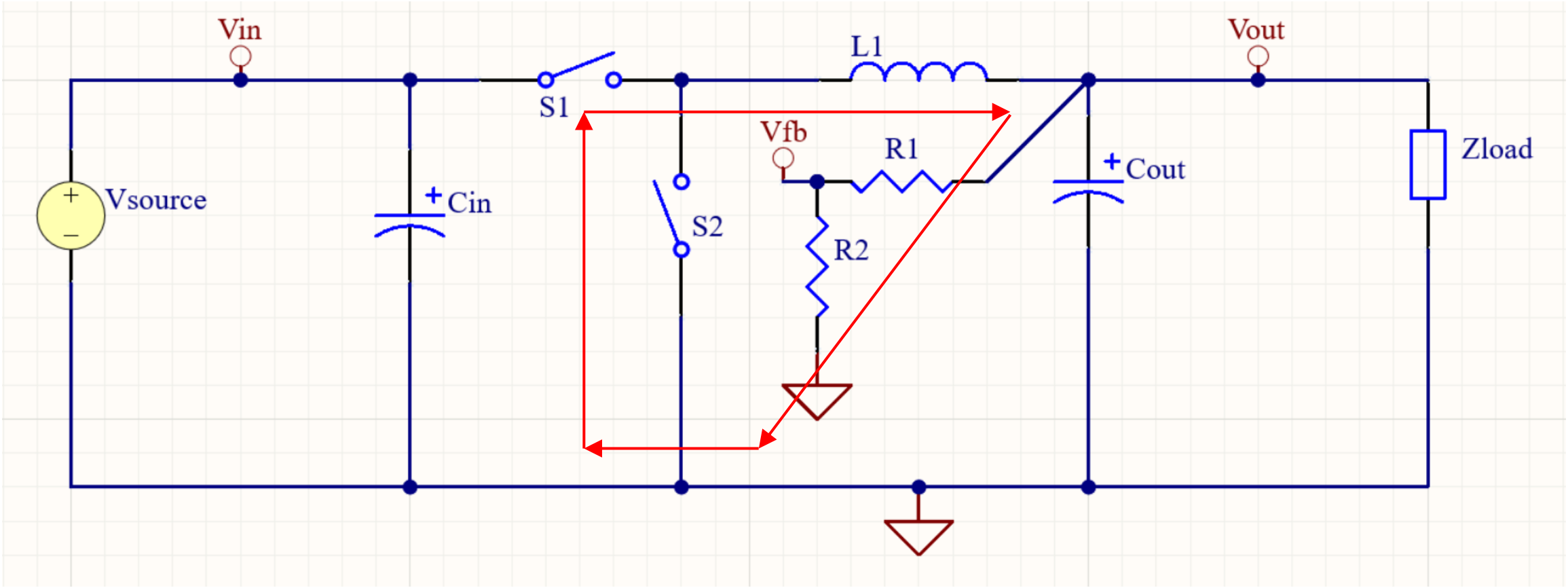
Buck-Mode SMPS

AC Current Loops (internal)

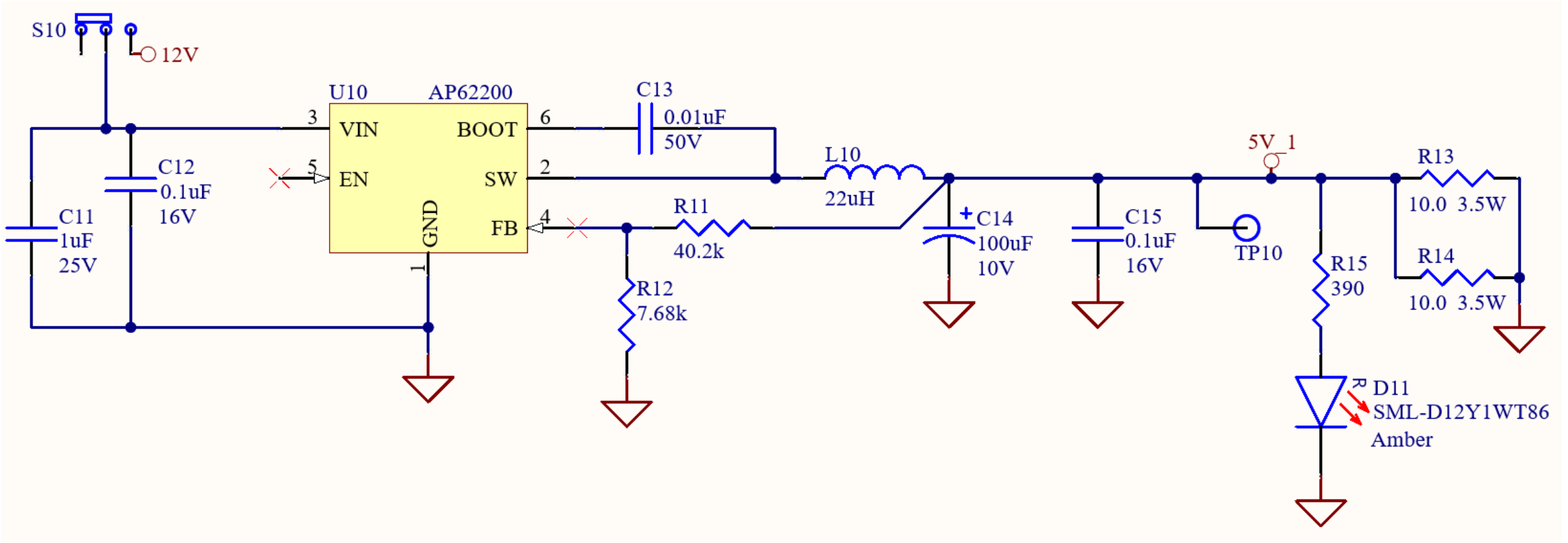


Buck-Mode SMPS

Showing Feedback



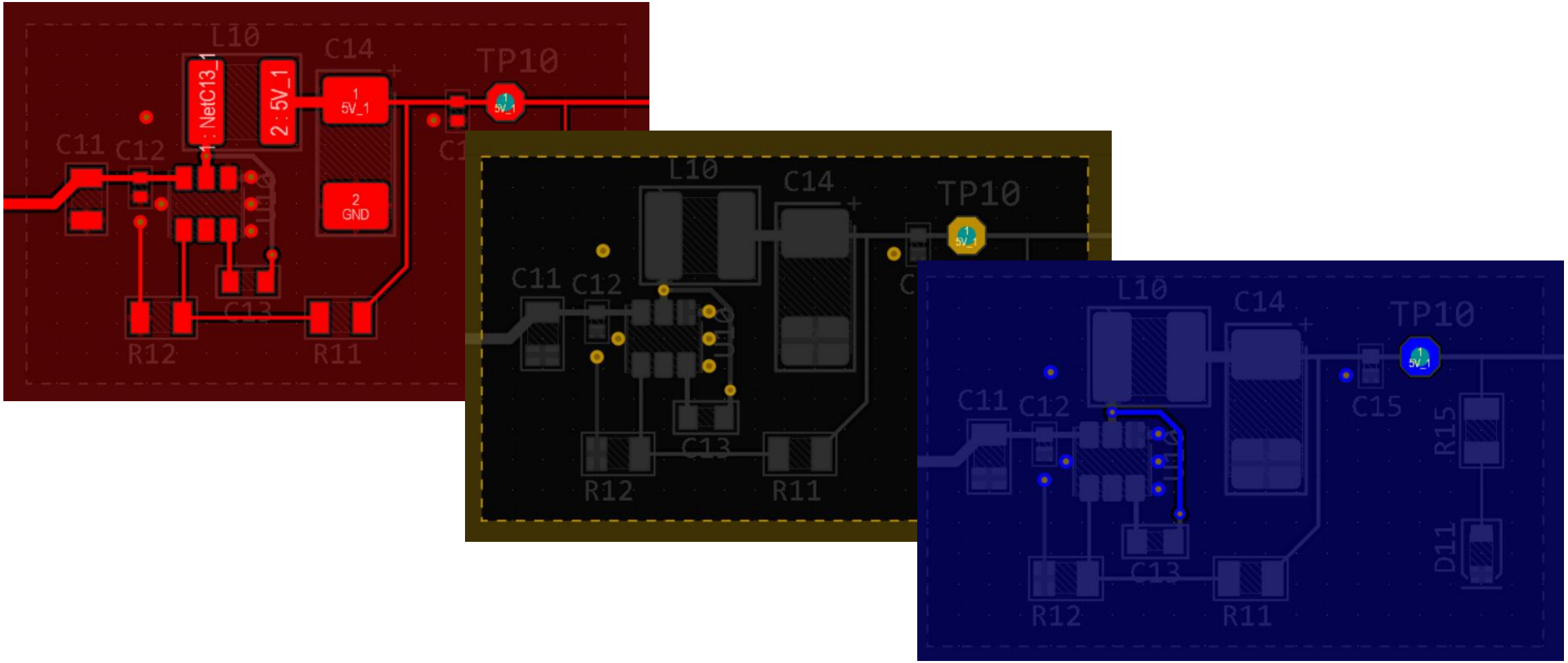
Demonstration: Best Layouts and Not-so-good Layouts



Identical circuit, different layouts

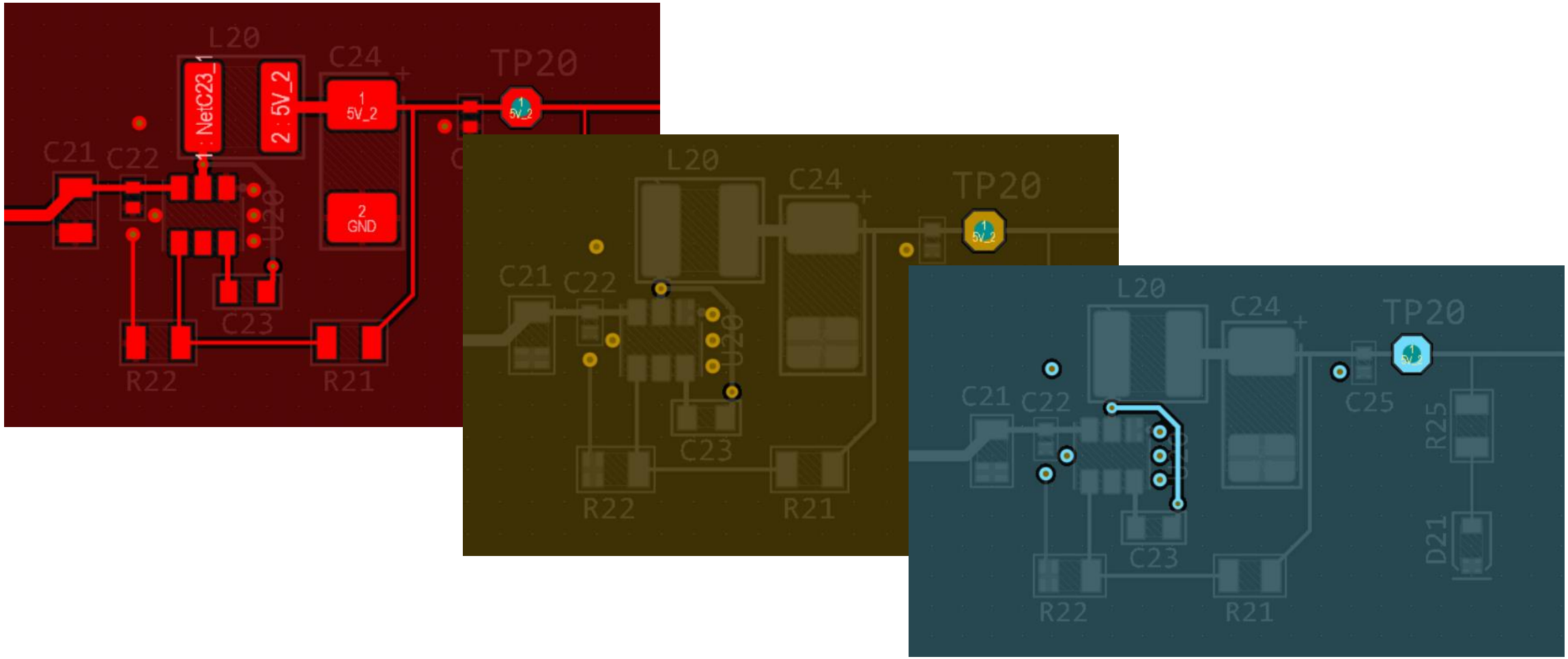
Circuit 1

Ground on Layer 4



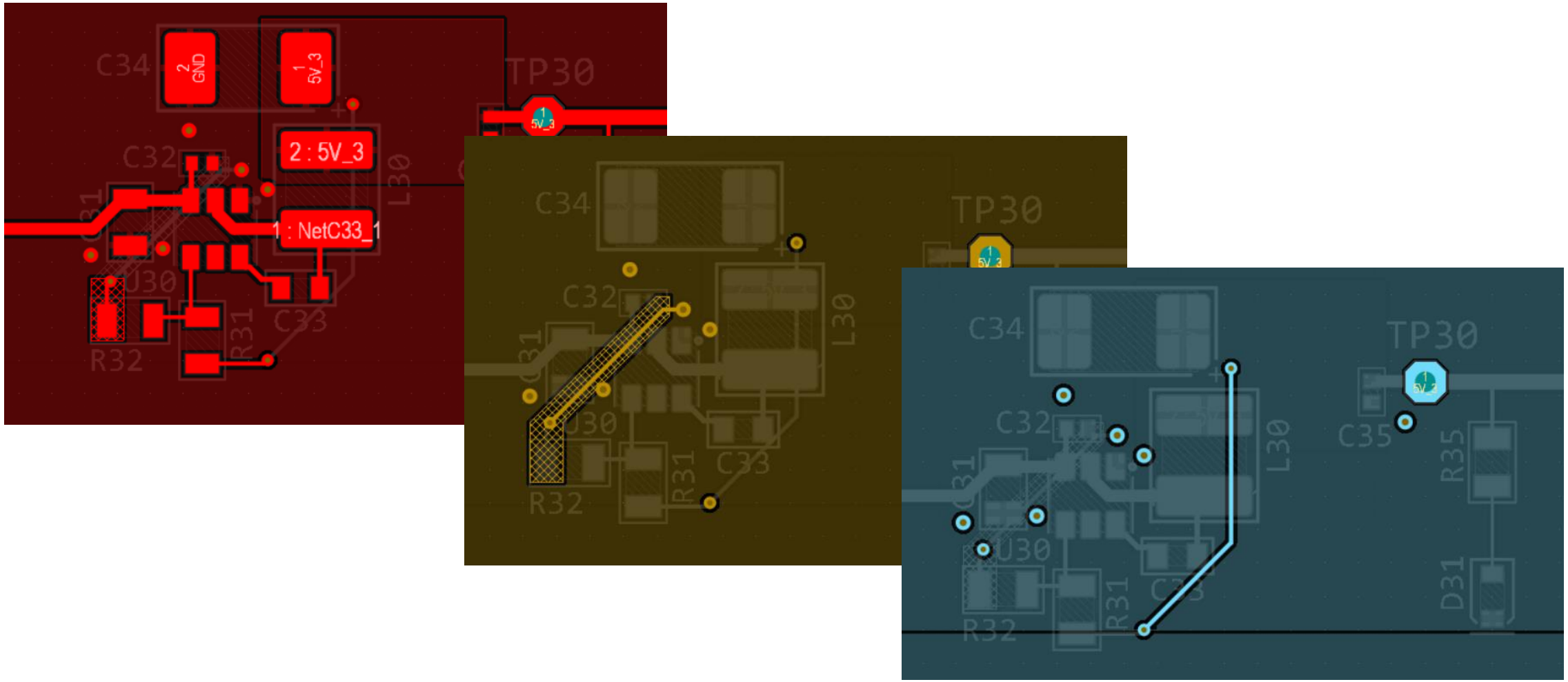
Circuit 2

Same as 1, except Ground on Layer 2



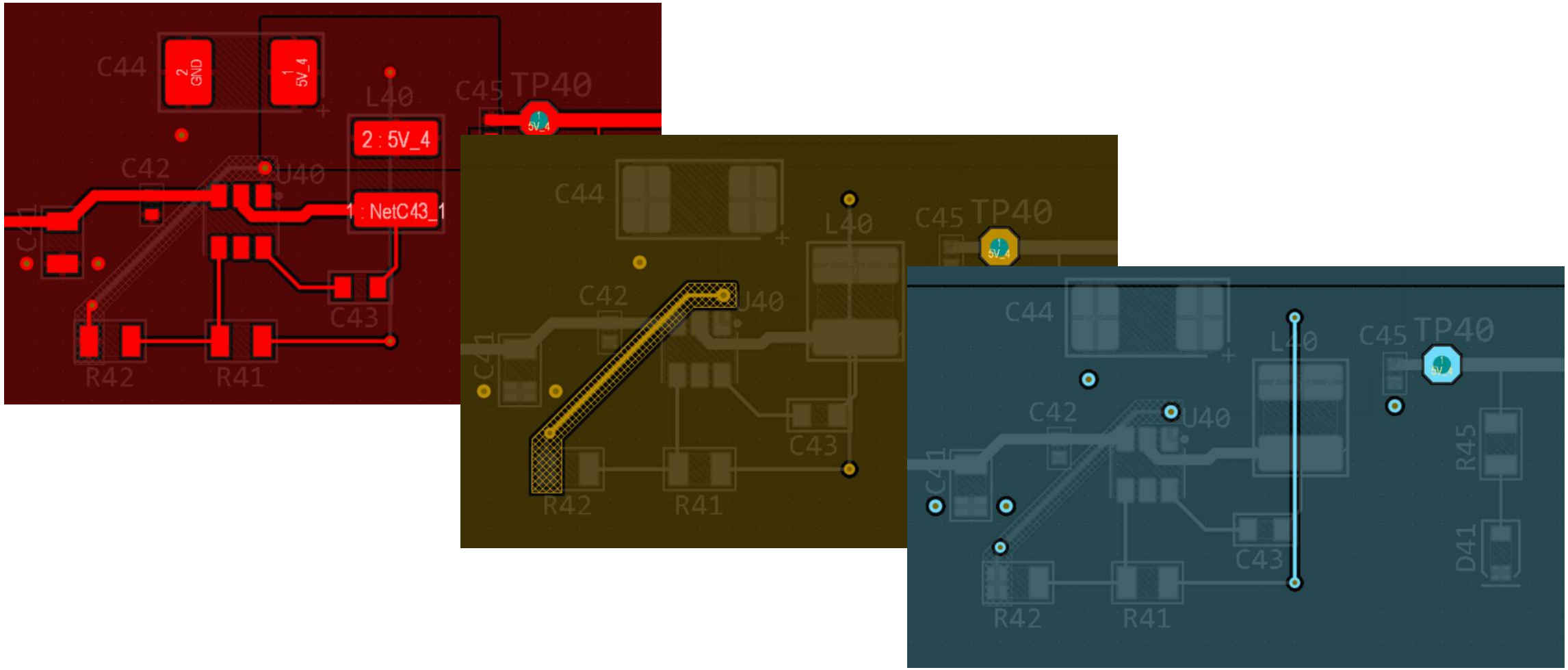
Circuit 3

Flipped L & C; small polygon for Vout; special return path for Vfb



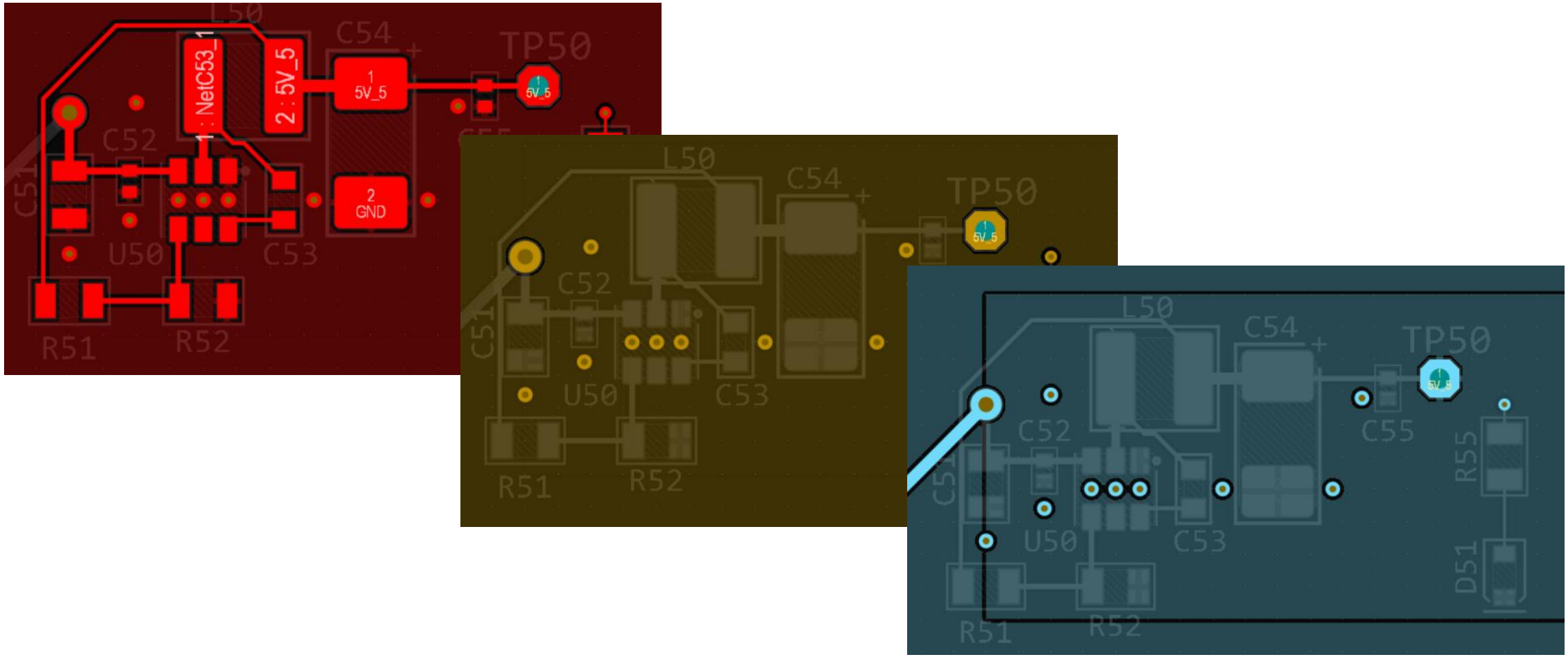
Circuit 4

Same as 3, except components spread out



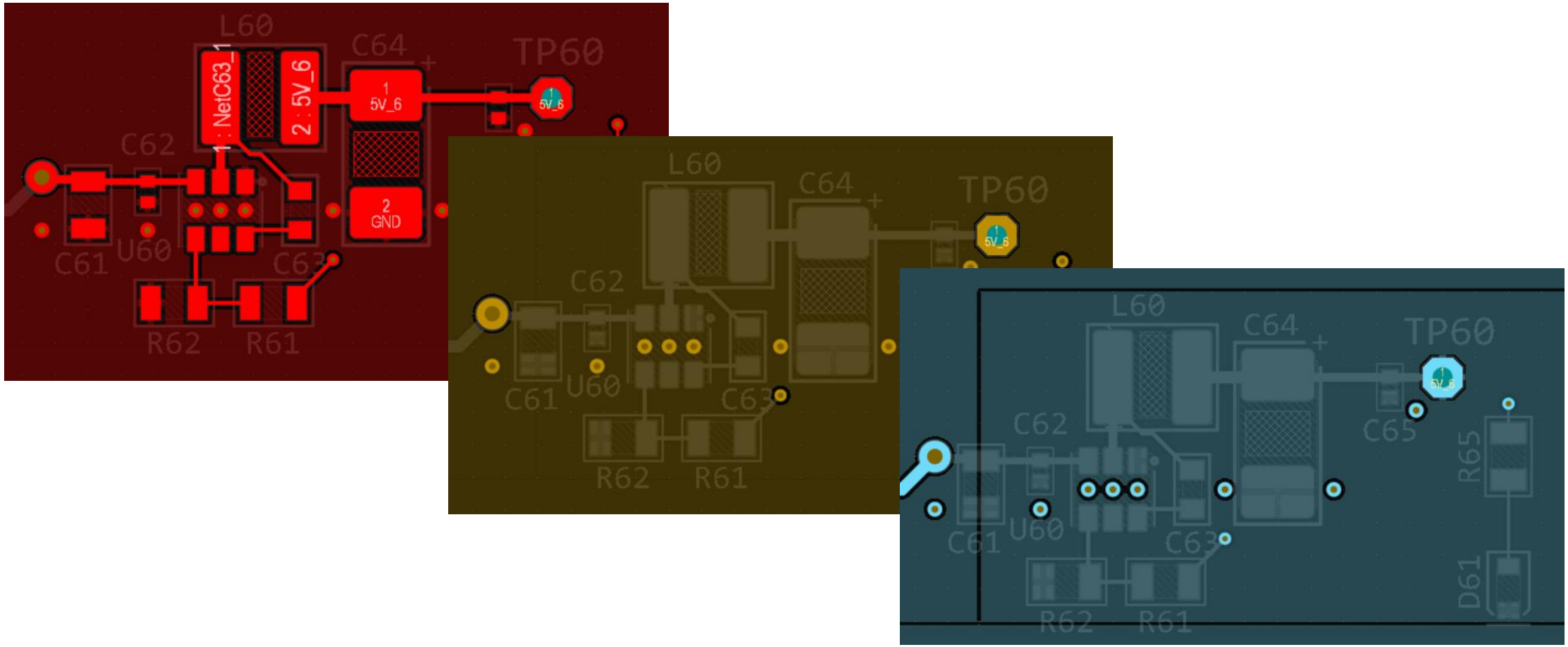
Circuit 5

“Recommended” : Tight spacing, Full Polygon on Power Plane for Vout



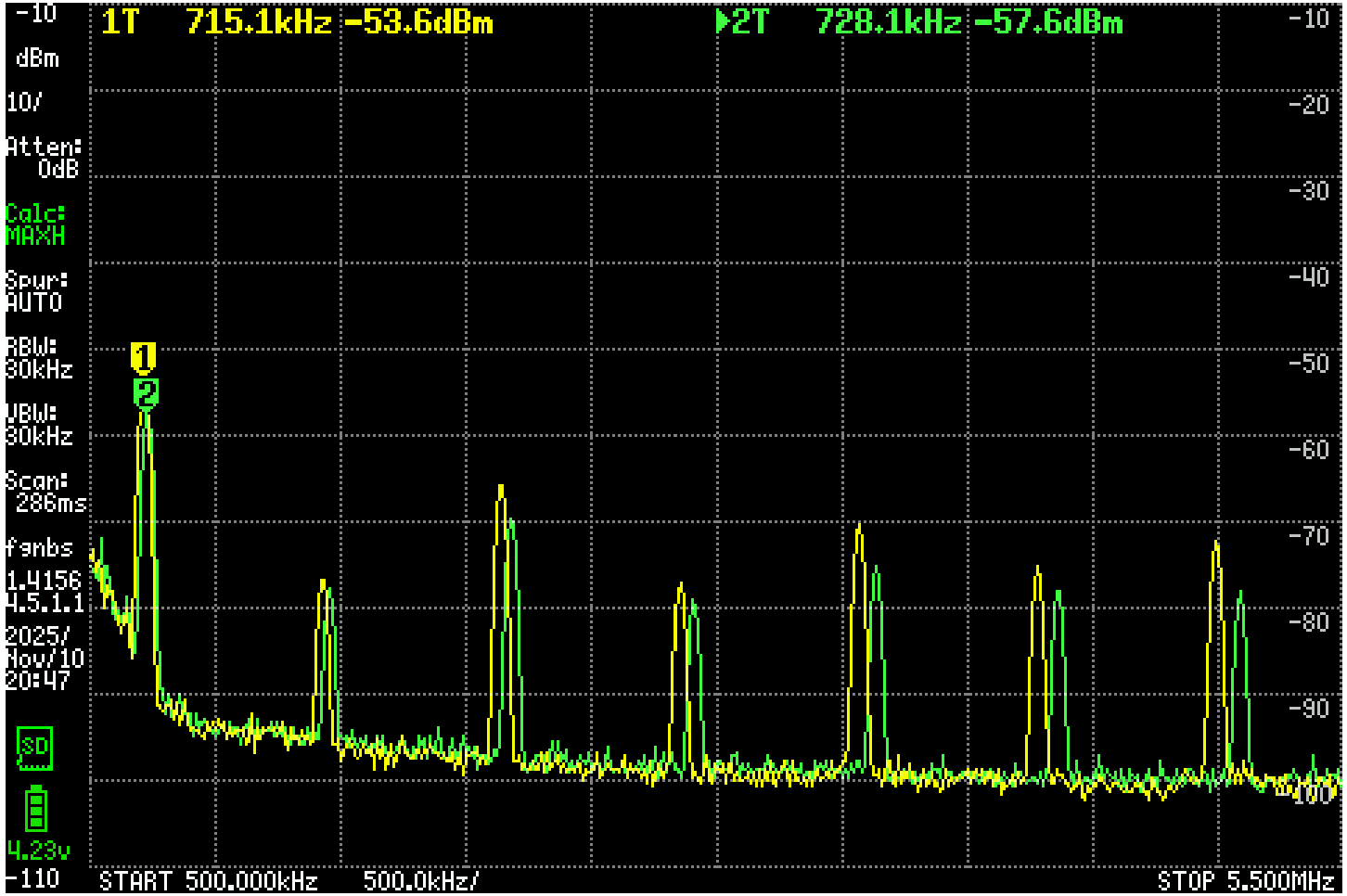
Circuit 6

“New Recommended” – Removed copper under L & C; Better path for Feedback resistors



Circuit 1 v 2

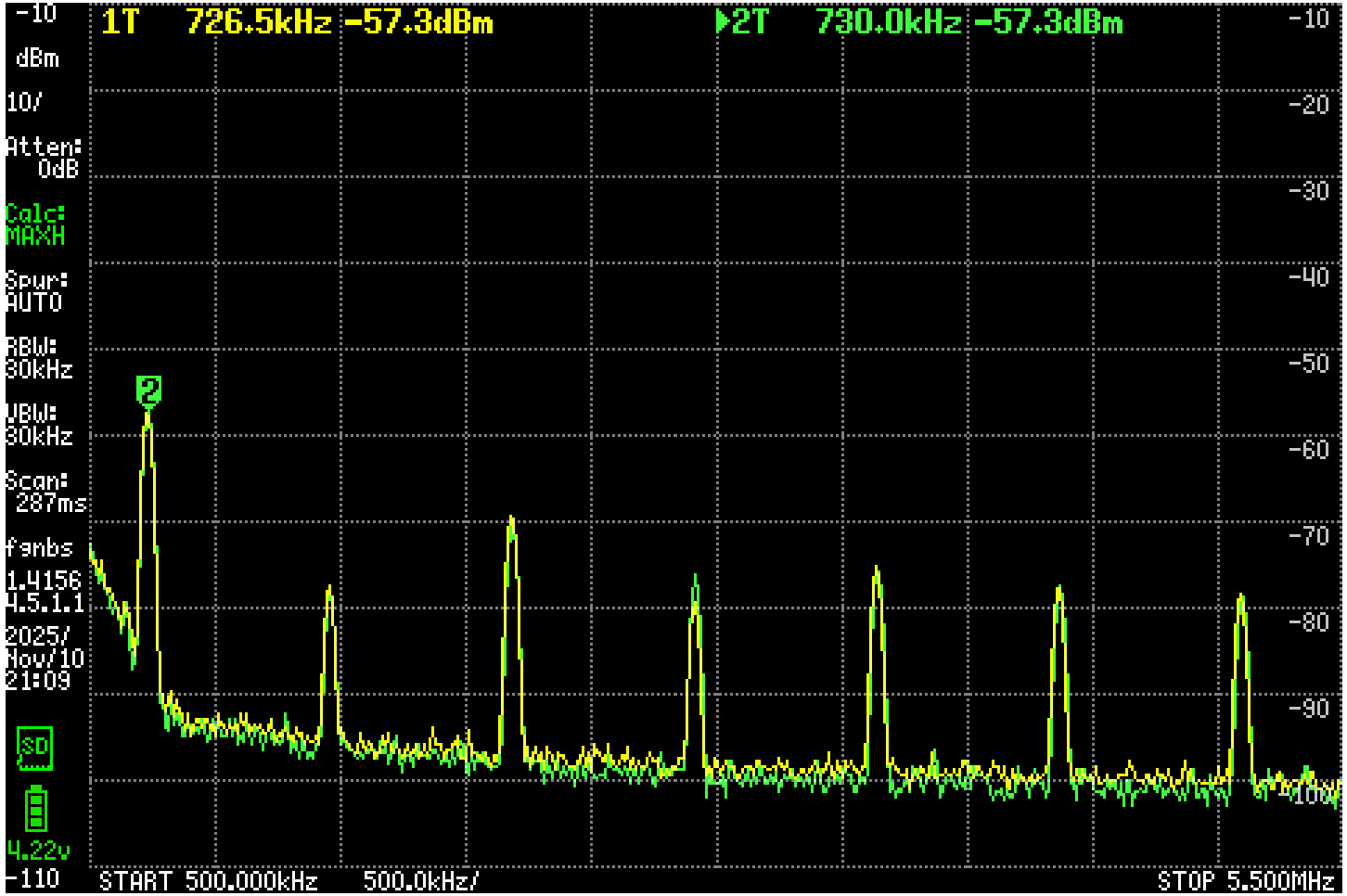
Does Ground on Layer 2 or 4 make a difference?



Closer Ground improves EMI by about 4 dB!

Circuit 2 v 3

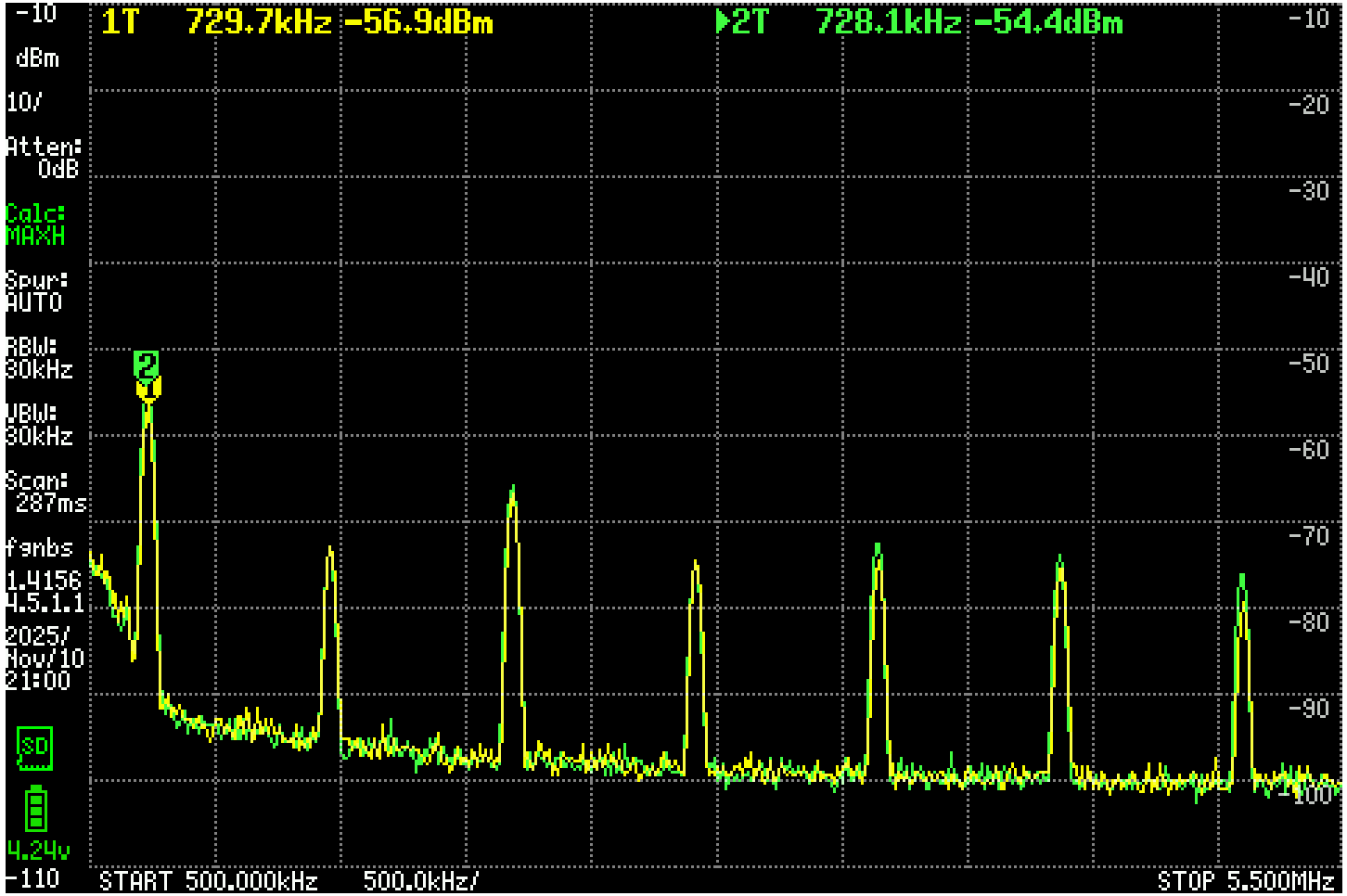
Does Flipped L & C, Vout polygon, or special feedback return path make a difference?



No significant differences

Circuit 3 v 4

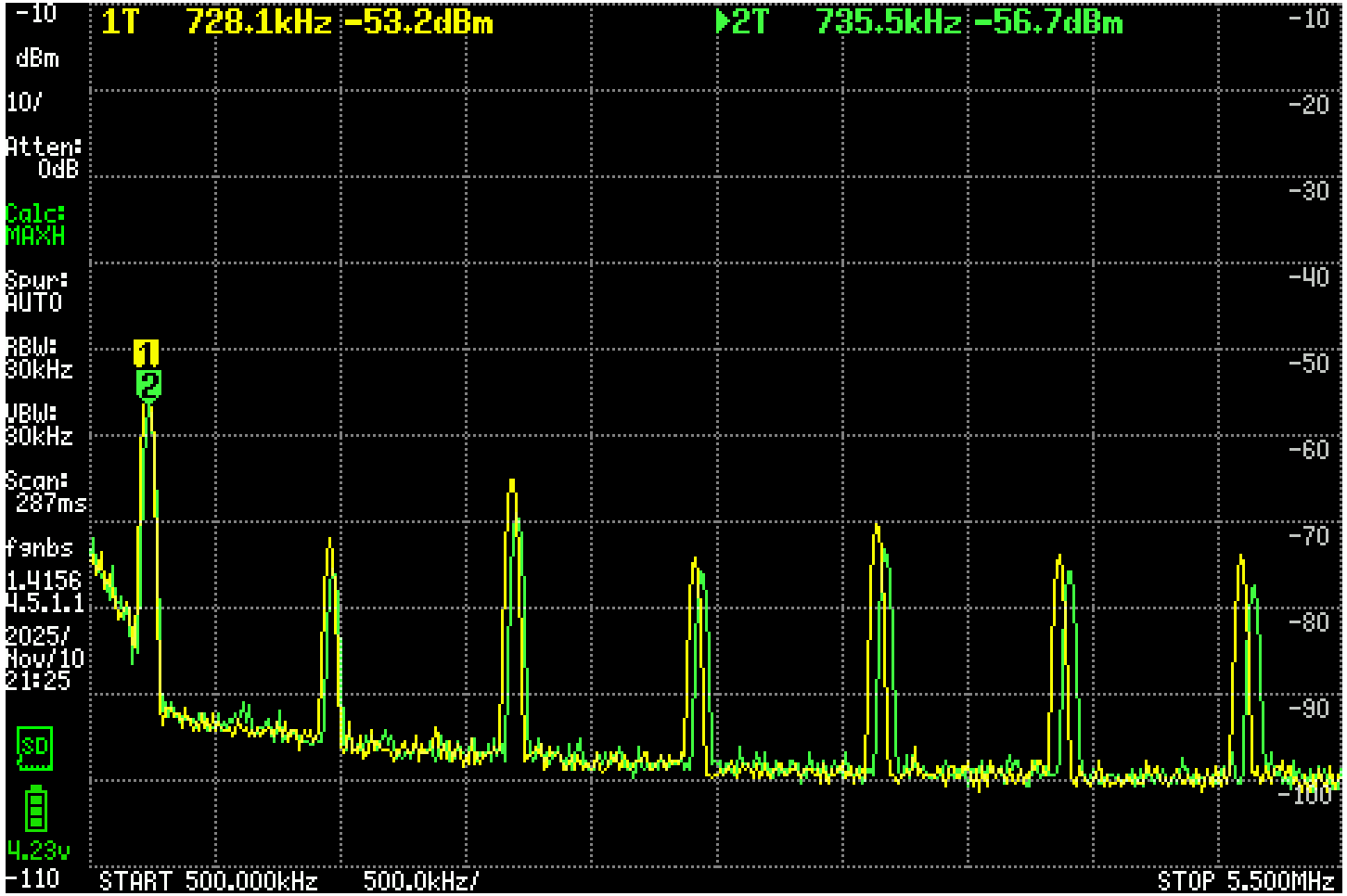
Does component spacing make a difference?



Tighter spacing improves EMI by about 2.5 dB

Circuit 4 v 5

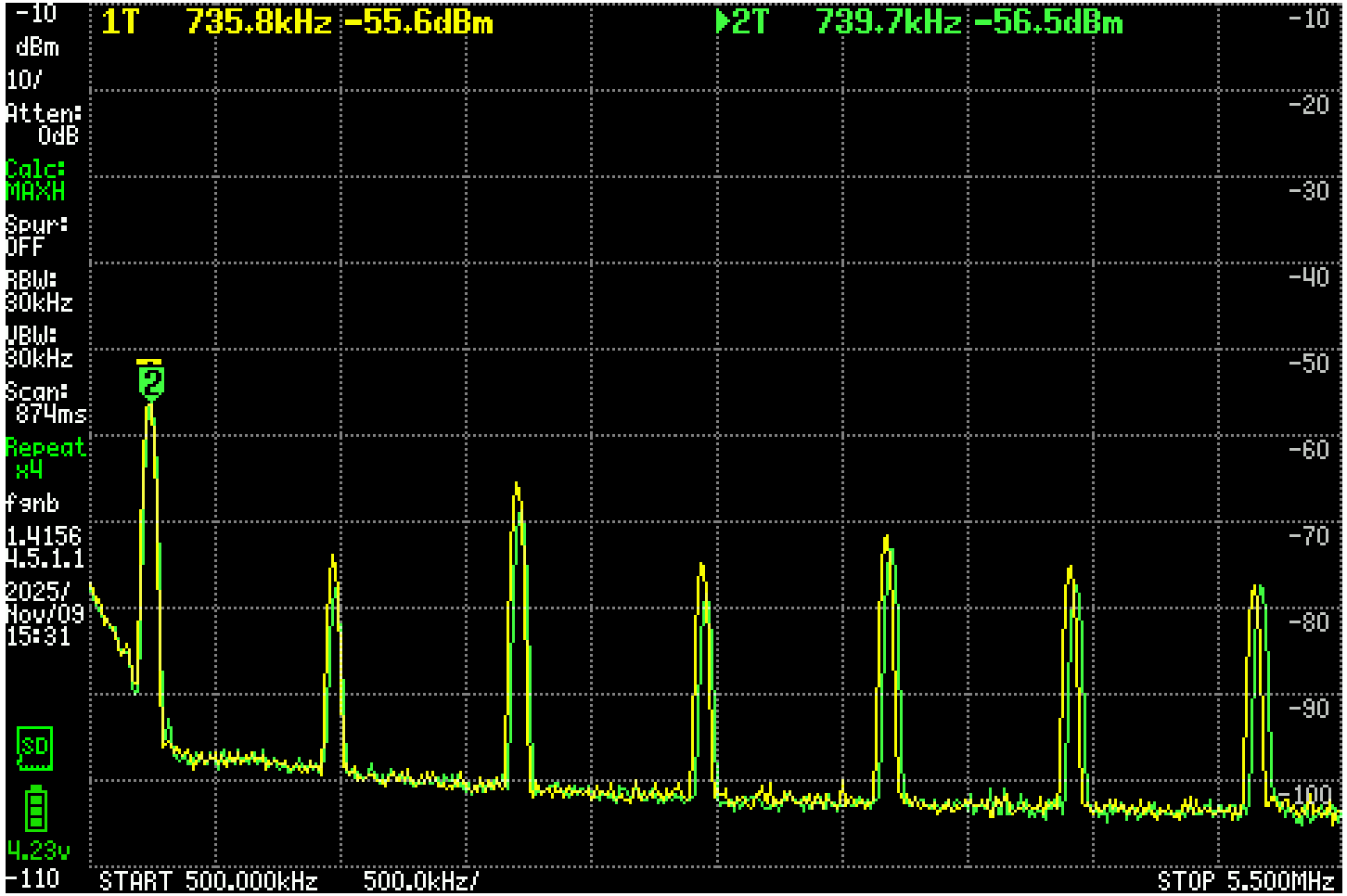
Does Tight Spacing, and Large Vout Polygon on Power Plane, make a difference?



Tight Spacing and Power Polygon improves EMI by about 3 dB

Circuit 5 v 6

Does removing copper under L & C, and new feedback path make a difference?



Removed Copper and New Feedback Path *slightly* improves EMI by about 1 dB

Recommendations

Good Practices – SMPS Specific

- Switchers definitely contain high frequencies
- Design for Return Path
  - Ground plane under the circuit is best
  - Layout critical signal paths first – power loops need to be tight
  - The Feedback circuit needs an unbroken return path (for SI)
- Filters (input and output) are important
  - Close to the noise sources
  - Keep frequency response in mind
- High (DC) current traces need to be wider, especially when they are long

Good Practices – from the SMPS measurements

- Ground Plane *directly* under circuit (adjacent layer) is most important
- Tight Component Spacing (reduced current loop area)
- Vout Polygon (on power plane) – probably helps
- Removing copper under L & C (component layer only) – may help
- Feedback path from power plane – may help
- Isolated return path – don’t bother
- Small polygons for L & C node – don’t bother

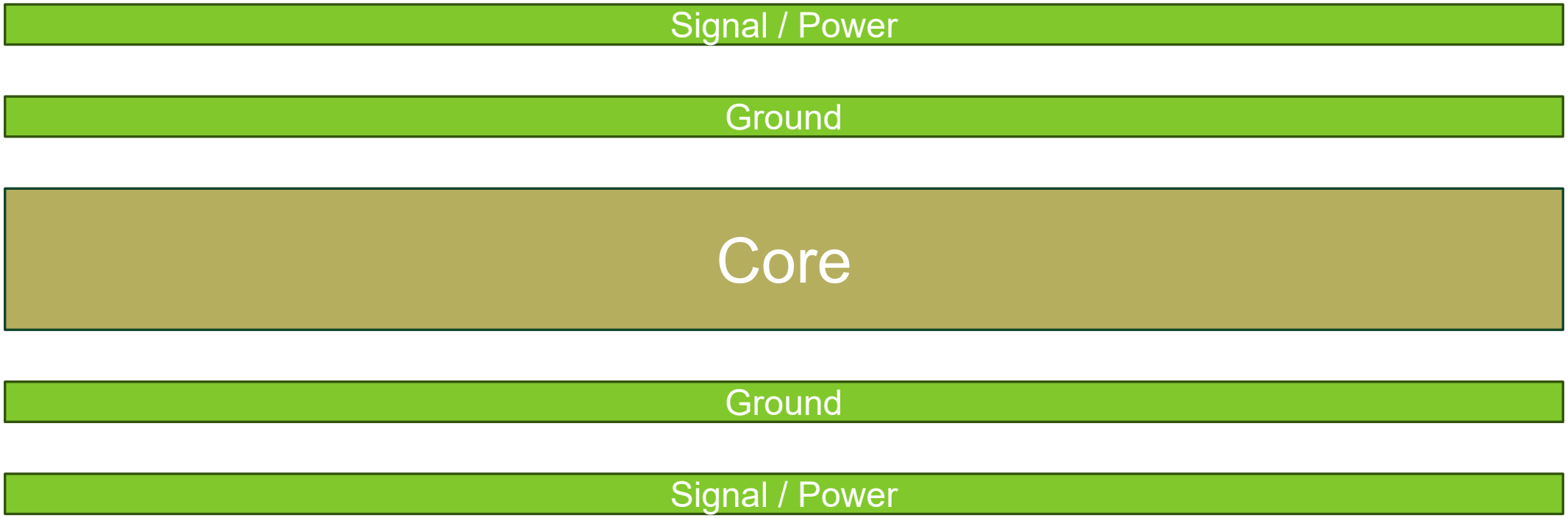
Good Practices

- Recognize what parts of your circuit contain high frequencies
- Design for the possibility of higher frequencies than originally planned
- Design for Return Path
  - Layout critical signals first
  - The slower signals can go around, and tolerate compromises
- Don’t use high-speed parts unless needed
- Don’t depend on “the way we’ve always done it” to still work in the future

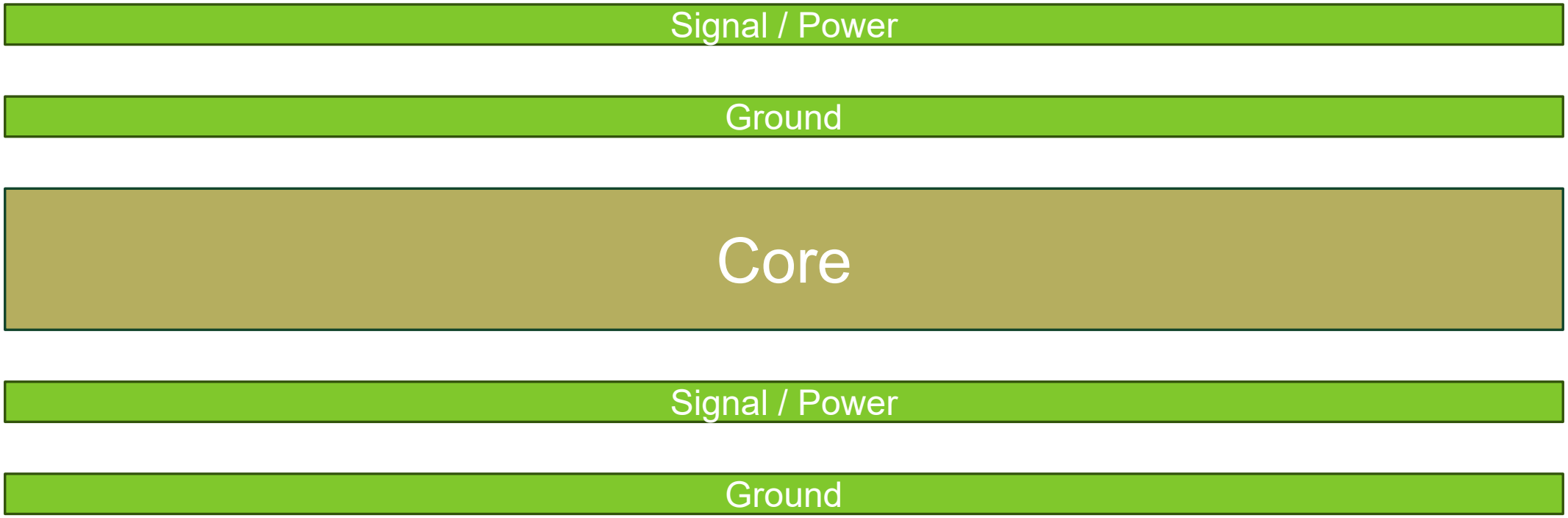
Recommended PCB Stackup – 4 Layers

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5
1	Top		Signal	1oz	1.7mil	
	Dielectric 1	FR-4	Core		14mil	4.8
2	Ground		Signal	1oz	1.4mil	
	Dielectric 3		Prepreg		28mil	4.2
3	Power		Signal	1oz	1.4mil	
	Dielectric 2		Core		14mil	4.2
4	Bottom		Signal	1oz	1.4mil	
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5
	Bottom Overlay		Overlay			

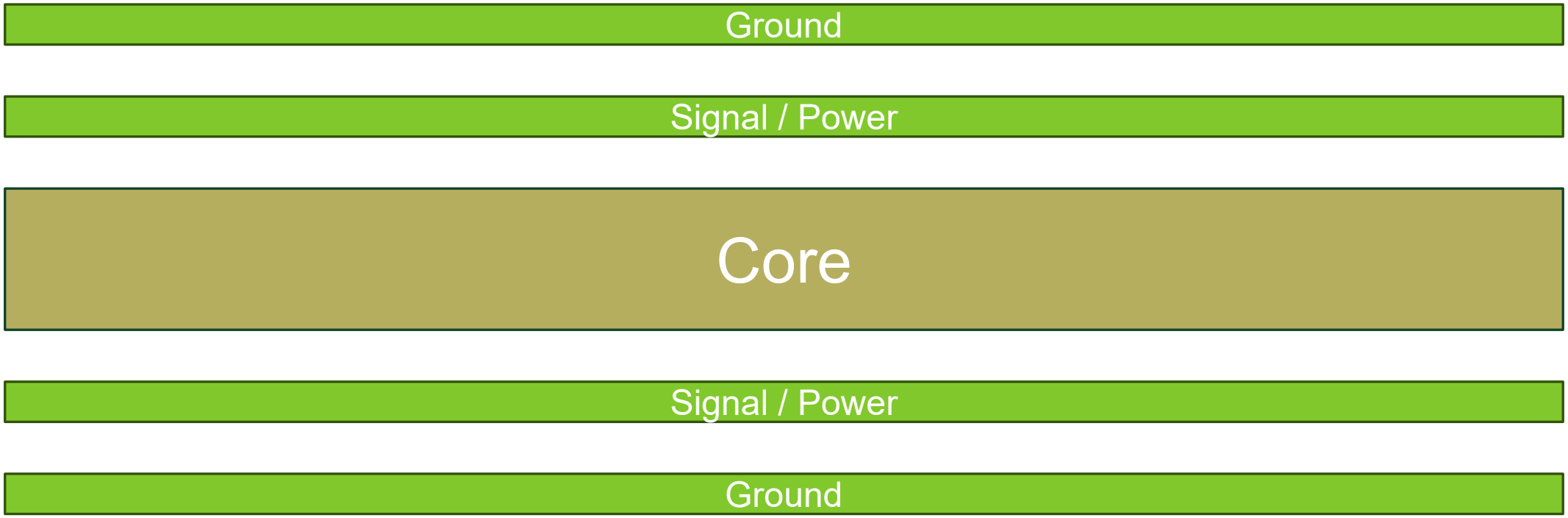
Recommended PCB Stackup – 4 Layers



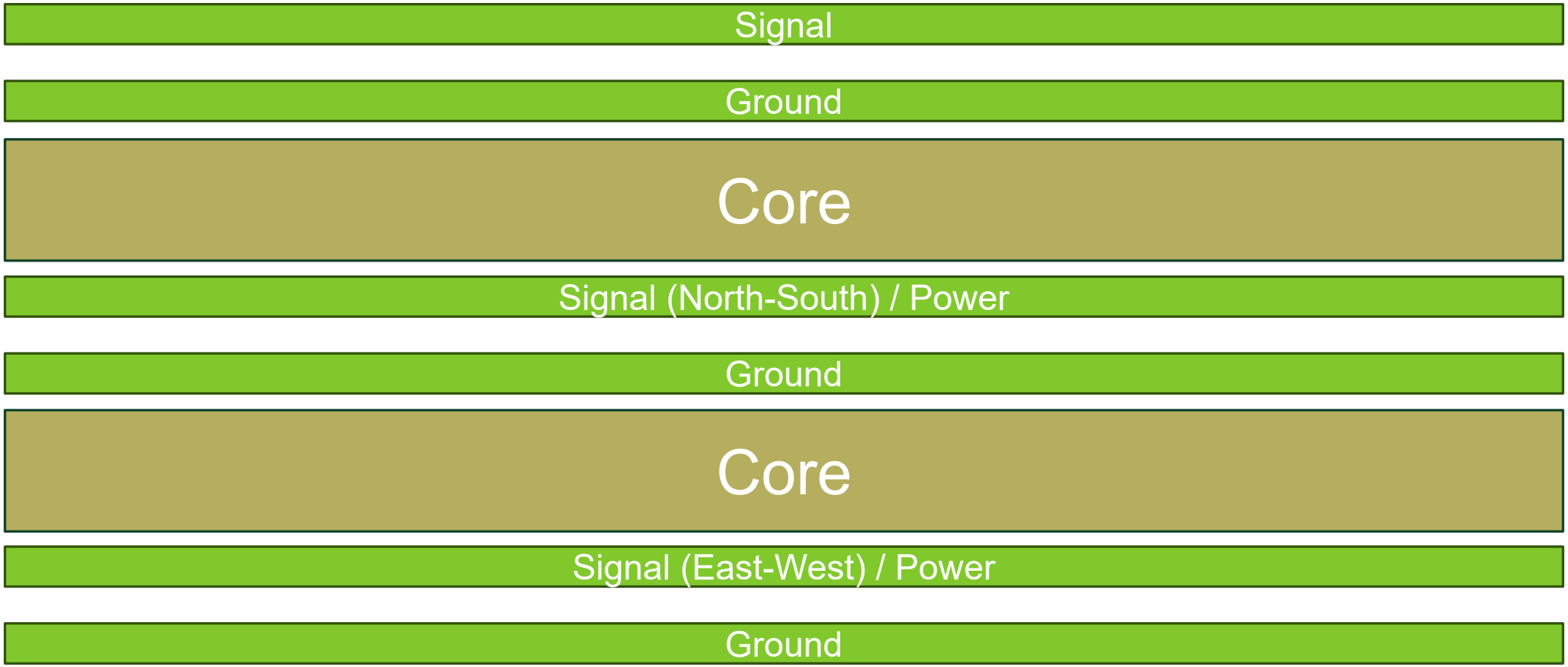
Recommended PCB Stackup – 4 Layers



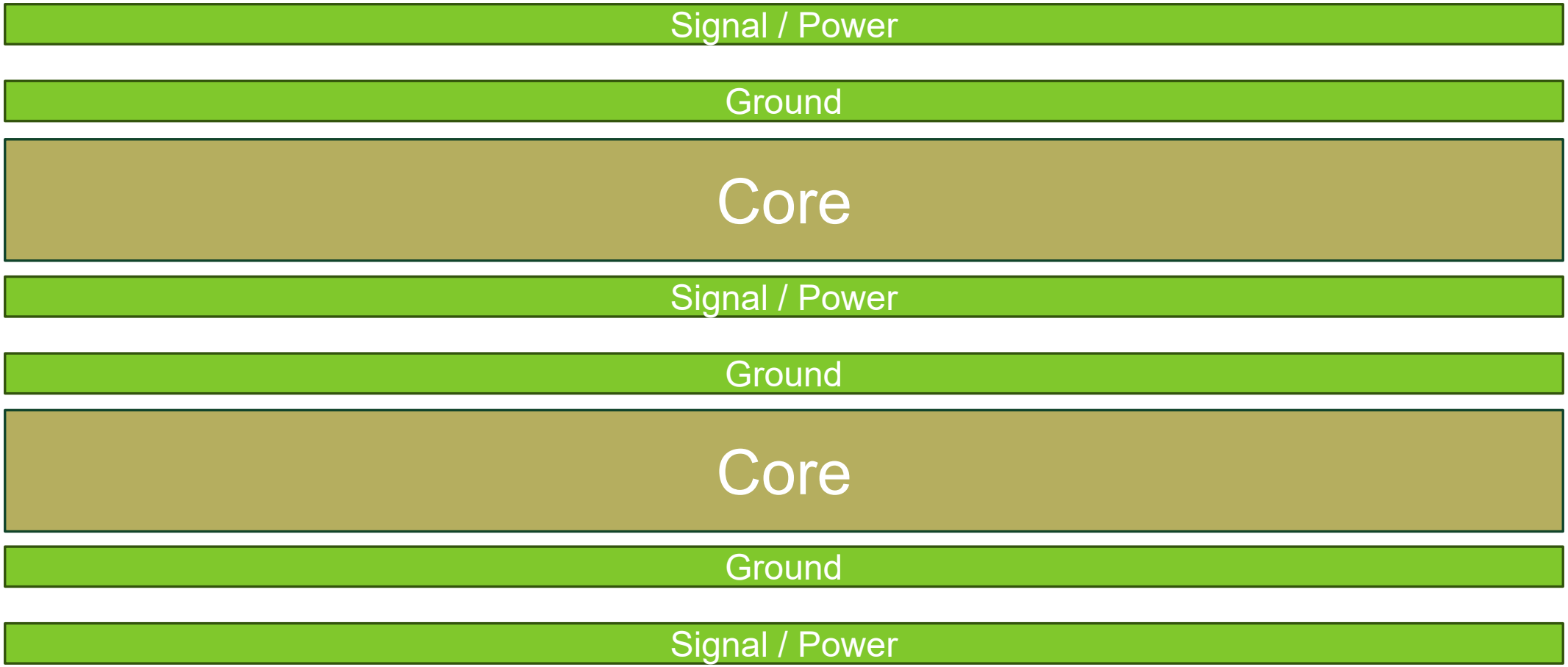
Recommended PCB Stackup – 4 Layers



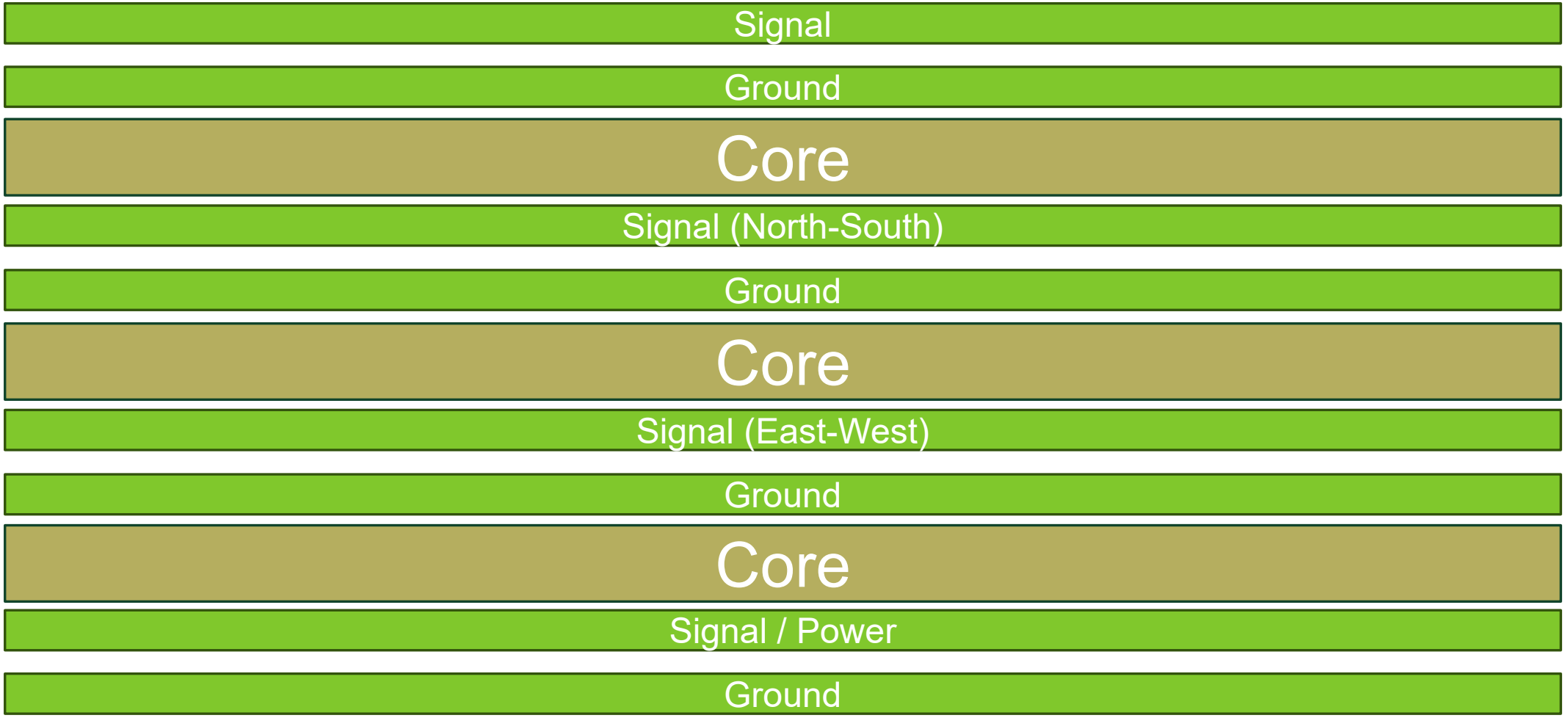
Recommended PCB Stackup – 6 Layers



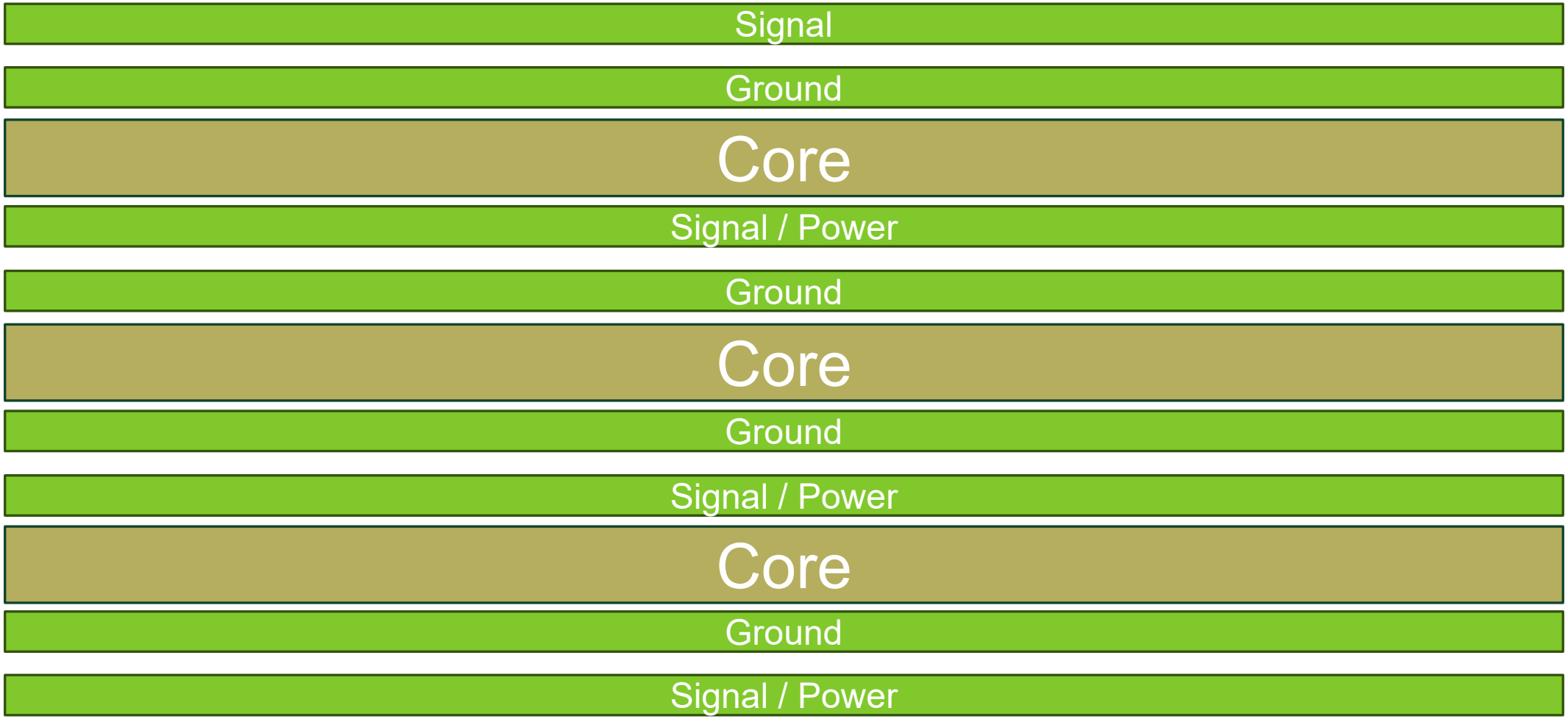
Recommended PCB Stackup – 6 Layers



Recommended PCB Stackup – 8 Layers



Recommended PCB Stackup – 8 Layers



Questions and Discussion

Questions?