

The background of the slide is a dark teal gradient. On the left side, there is a vertical strip of abstract blue and black patterns, resembling a digital or data visualization. A solid red rectangle is positioned in the top right corner.

Overview of Allegro IDA and Optimality Explorer

EXPLORING ADVANCED TOOLS FOR
DATA ANALYSIS AND OPTIMIZATION

Outline



Why IDA....shift left



What is IDA (In Design Analysis)



How can IDA improve you designs and speed up time to market



Optimality how can this optimize your design with AI

Why IDA

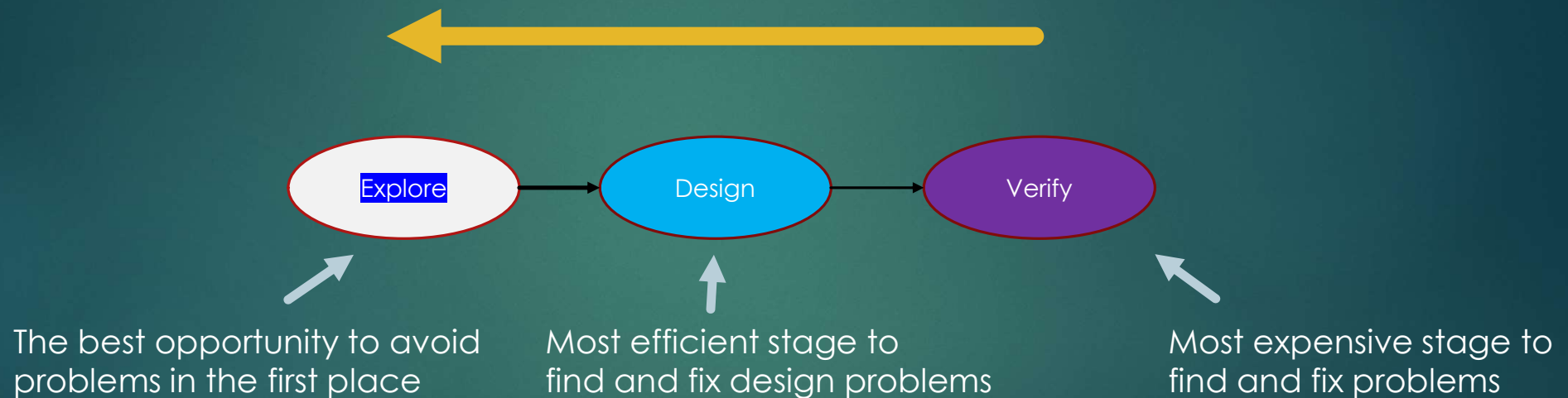
To Constrain or Not To Constrain

- ▶ Constraint driven design is the backbone of any solid design methodology
 - ▶ Focus is on finding and resolving violations
 - ▶ Traditionally involves Constraint Manager and DRC Markers
 - ▶ Existing options for Impedance, Coupling and Return Path
 - ▶ Rules are required
 - ▶ But may be a hinderance to starting any kind of analysis
- ▶ Screening Analysis also has a place
 - ▶ Rules are not required
 - ▶ Easier to get a snapshot of the entire design or any portion
 - ▶ Focus is on result viewing
 - ▶ New Analysis Workflows offer new methodologies to enhance existing design flows



Problem Statement

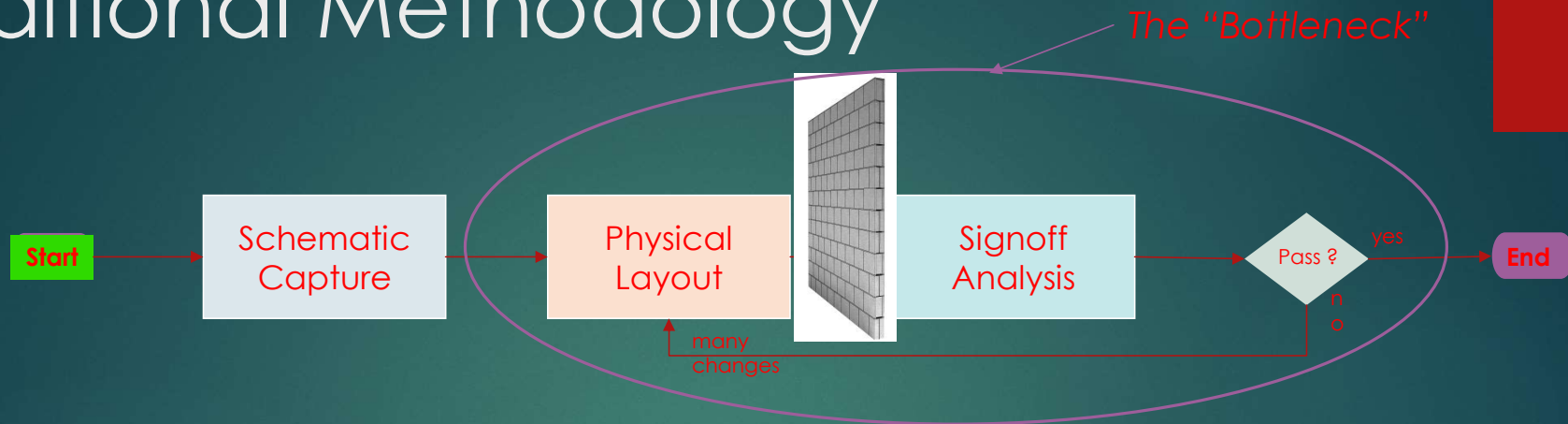
- ▶ With time-to-market, cost, and performance pressures, system designers are seeking a “shift left” to streamline their methodologies



Must move beyond just post-layout verification

Accomplishing this involves tools, methodology, and some re-thinking of organizational roles

Traditional Methodology



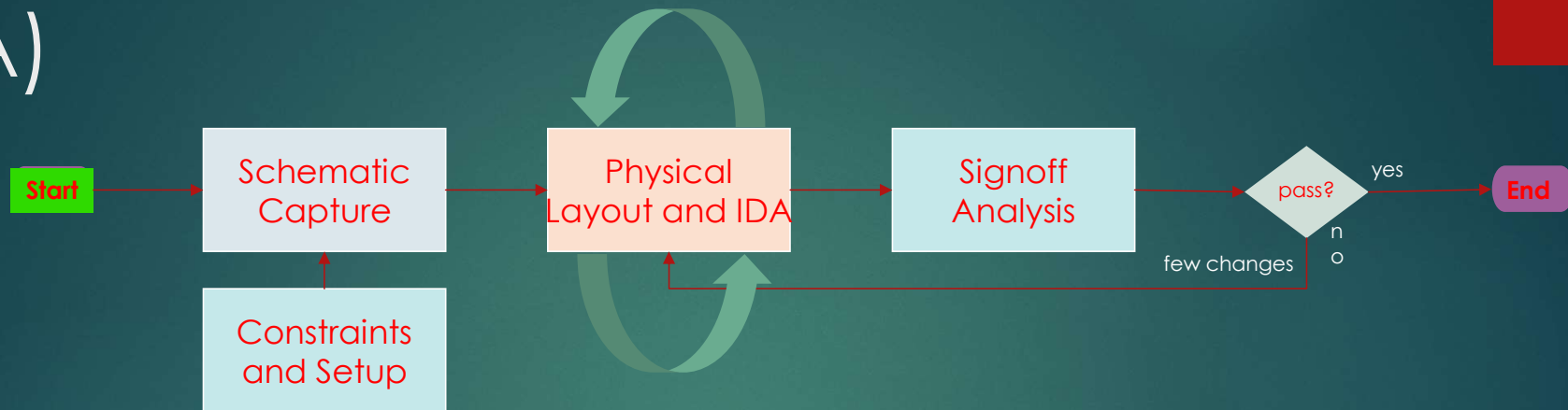
- ▶ Physical layout goes “over the wall” to analysis expert
- ▶ Eventually some requested changes go back to layout designer
- ▶ Changes get manually implemented; issues resolved?
- ▶ Back over the wall the layout goes
- ▶ Inefficient:
 - ▶ Multiple iterative loops, disrupting schedule
 - ▶ Manual changes
 - ▶ Across organizations
 - ▶ Bottlenecked by Analysis Expert resources

Design Engineer

Layout Designer

Analysis Expert

Methodology with In-Design Analysis (IDA)



- ▶ The design engineer and analysis expert provide constraints and analysis setup before the physical layout
- ▶ Layout designer empowered with actionable, real-time analysis feedback in their native environment, where they can quickly make edits and re-analyze independently
- ▶ Fewer issues at the signoff stage
- ▶ Efficiency goes up and schedule compresses

Design Engineer

Layout Designer

Analysis Expert

Collaborative Design Environment

Multi-Stakeholder Participation

Allegro IDA enables multiple stakeholders to actively participate in the collaborative design process.

Real-Time Feedback

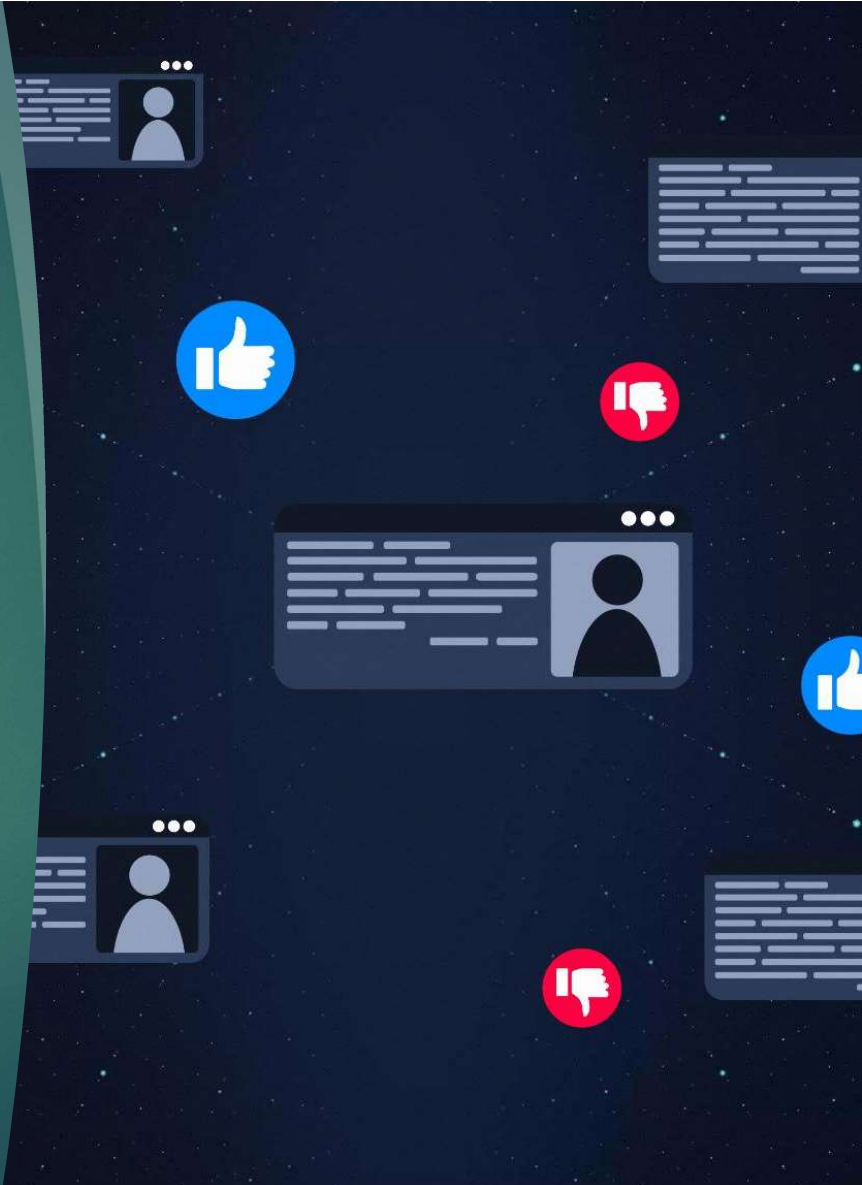
Real-time feedback and shared analysis results enhance communication and decision-making among team members.

Integrated Communication Tools

Integrated communication tools streamline teamwork and ensure alignment for higher quality designs.

Seamless Workflow Integration

The workflow supports seamless integration with other platforms, boosting overall project efficiency.



Workflow Integration and Benefits

Seamless Workflow Integration

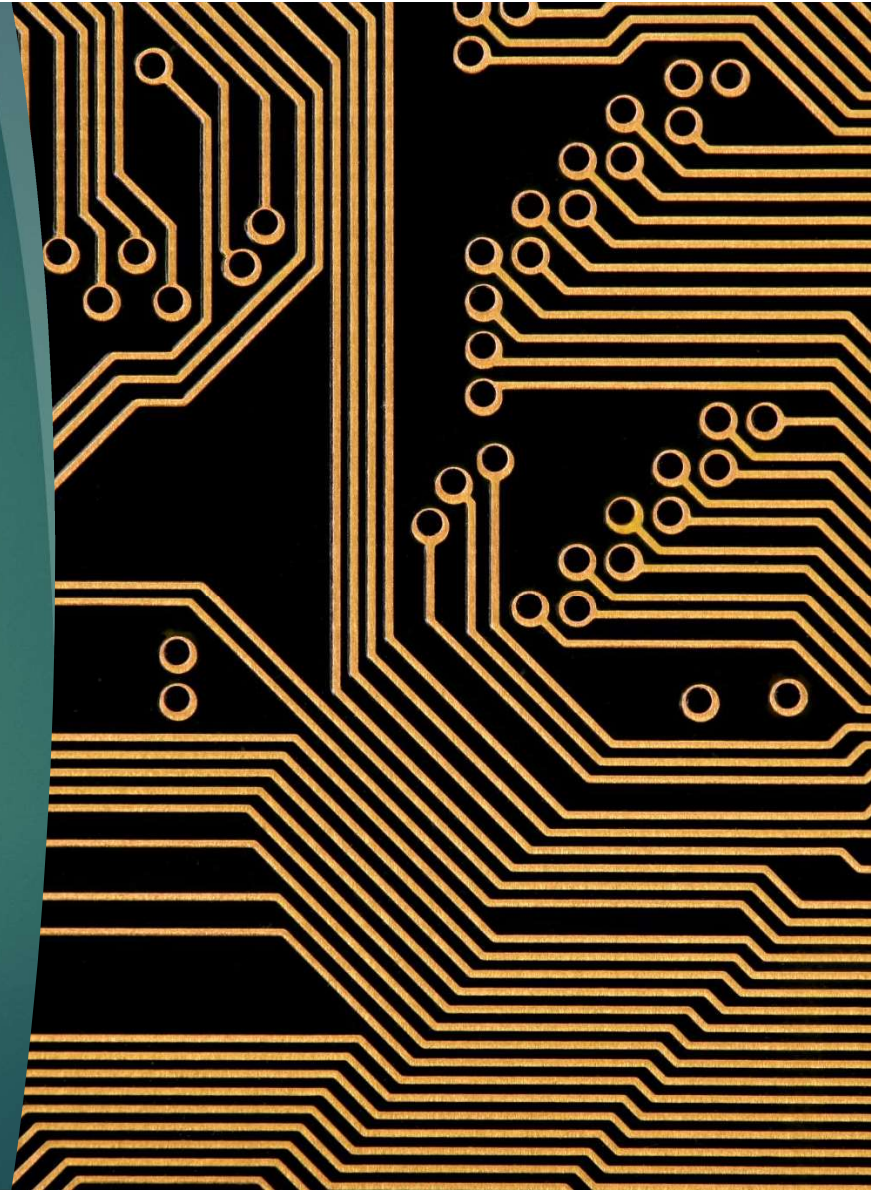
Integration facilitates smooth transitions between design, analysis, and optimization phases, streamlining the overall process.

Error Reduction and Efficiency

Reducing manual effort and errors accelerates the design cycle and improves overall productivity and accuracy.

Comprehensive EDA Solution

Supports schematic capture, layout design, and system-level optimization for a complete electronic design automation workflow.



Why Use IDA

Real-Time Analysis

IDA provides real-time analysis, allowing designers to detect and solve issues during the design process promptly.

Integrated Checking

The tool offers integrated checking capabilities that improve design quality by identifying problems early.

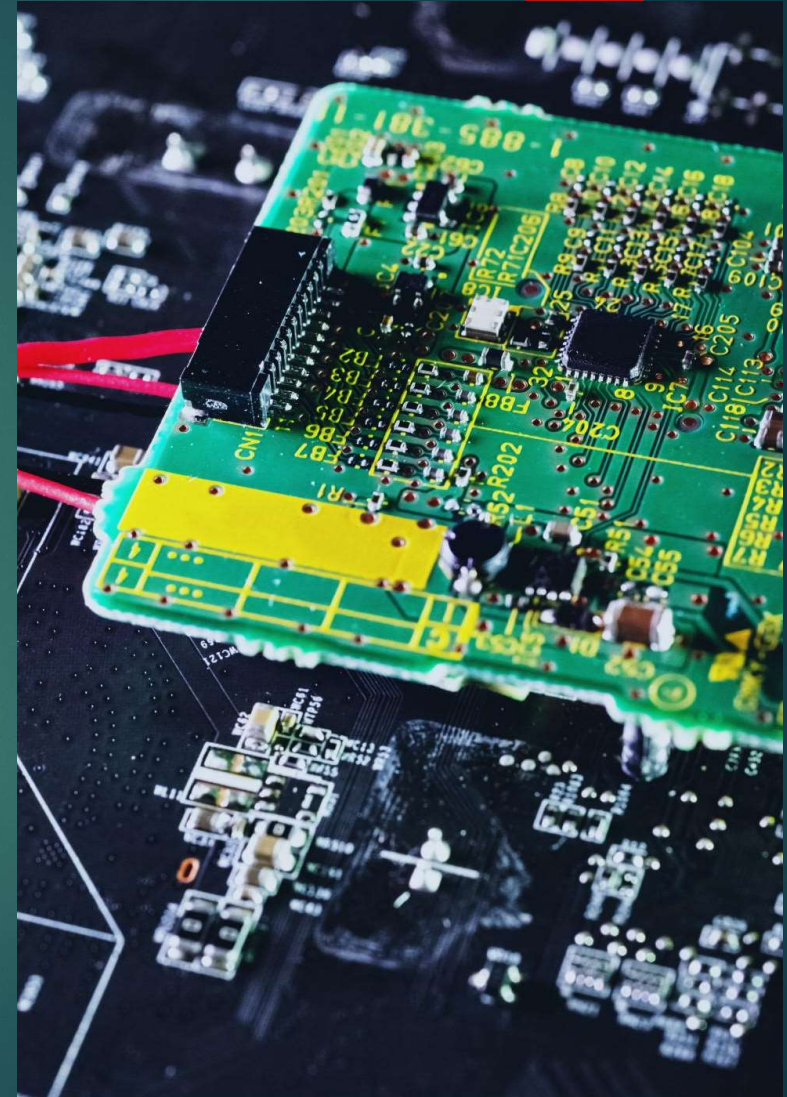
Enhanced Collaboration

IDA enhances team collaboration by seamlessly integrating with other design tools and supporting communication.

Supports Various Analyses

It supports multiple analysis types like signal and power integrity, ensuring comprehensive design validation.

IDA Features and Flows



Aurora IDA workflows

Impedance Analysis Screening

- Global view of results more accessible
 - Graphics
 - Tables and plots
- Look for outliers
 - Single-ended impedance

Crosstalk Analysis

Both tables support cross-probing and ability to show details

Each neighbor table includes coupling data

Power Inductance Workflow

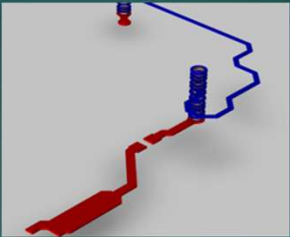
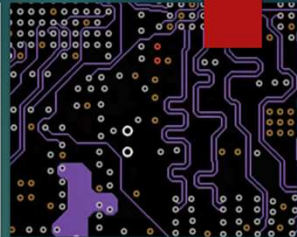
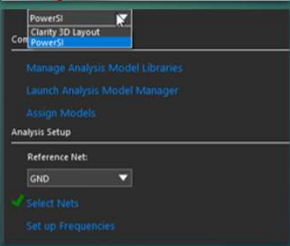
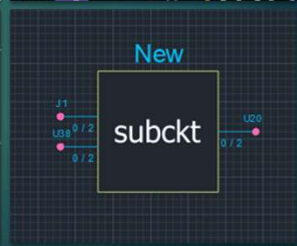
- Checks decap-to-IC loop

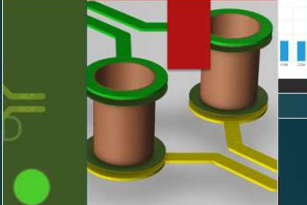
DC Resistance

- Measured dc resistance on any pad
- Exportable csv
- Helps with defining the appropriate across multiple PDN's

Interconnect Model Extraction

- Clarity™ 3D Solver and Sigrity™ PowerSI® engines are directly integrated into the Allegro® environment
- User selects nets of interest in the Allegro environment
- Extraction engine is transparently invoked, and the resulting S-parameter model is pushed into Topology Explorer




Simulation Support for Unrouted Nets

- Partially routed and unrouted signal nets are automatically modeled with transmission line models based on ratnest, user-defined parameters, and Manhattan distances

Topology Workbench

- Integrated workflow in Sigrity™ Aurora
- Extract single-ended and differential signals into Topology Explorer
- Explore what-if scenarios and develop constraints
- Stand alone tool or embedded into AllegroX environment.



- Can create a quick partial layout from existing Allegro® footprints
- Floorplan placement of critical components
- Prototype routing for critical classes of nets



Interconnect Model Extraction

- ▶ Integrated Simulation Architecture
 - ▶ Clarity™ 3D Solver and Sigrity™ PowerSI® engines embedded in Allegro® PCB design environment
 - ▶ Direct net selection within Allegro triggers automated extraction
- ▶ Automated S-Parameter Model Generation
 - ▶ Transparent invocation of extraction engine
 - ▶ S-parameter models pushed into Topology Explorer for simulation
- ▶ Technical Advantages
 - ▶ Seamless data flow between design and analysis tools
 - ▶ High-fidelity interconnect modeling
 - ▶ Accelerated design validation

Interconnect Model Extraction

Integrated Simulation Architecture

- Clarity™ 3D Solver and Sigrity™ PowerSI® engines are natively embedded in the Allegro® PCB design environment
- Designers can select nets of interest directly within Allegro, triggering automated extraction

Automated S-Parameter Model Generation

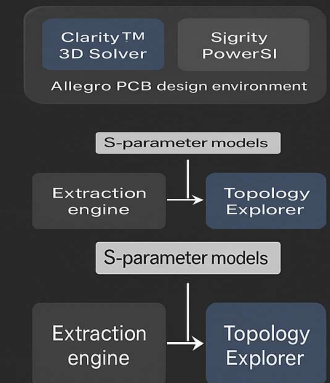
- The extraction engine is invoked transparently
- Resulting S-parameter models are automatically pushed into Topology Explorer for further simulation and analysis

Automated S-Parameter Model Generation

- The extraction engine is invoked transparently
- Resulting S-parameter models are automatically pushed into Topology Explorer for further simulation and analysis

Technical Advantages

- No manual export/import between tools – seamless data flow
- High-fidelity interconnect modeling for signal integrity and power integrity simulations

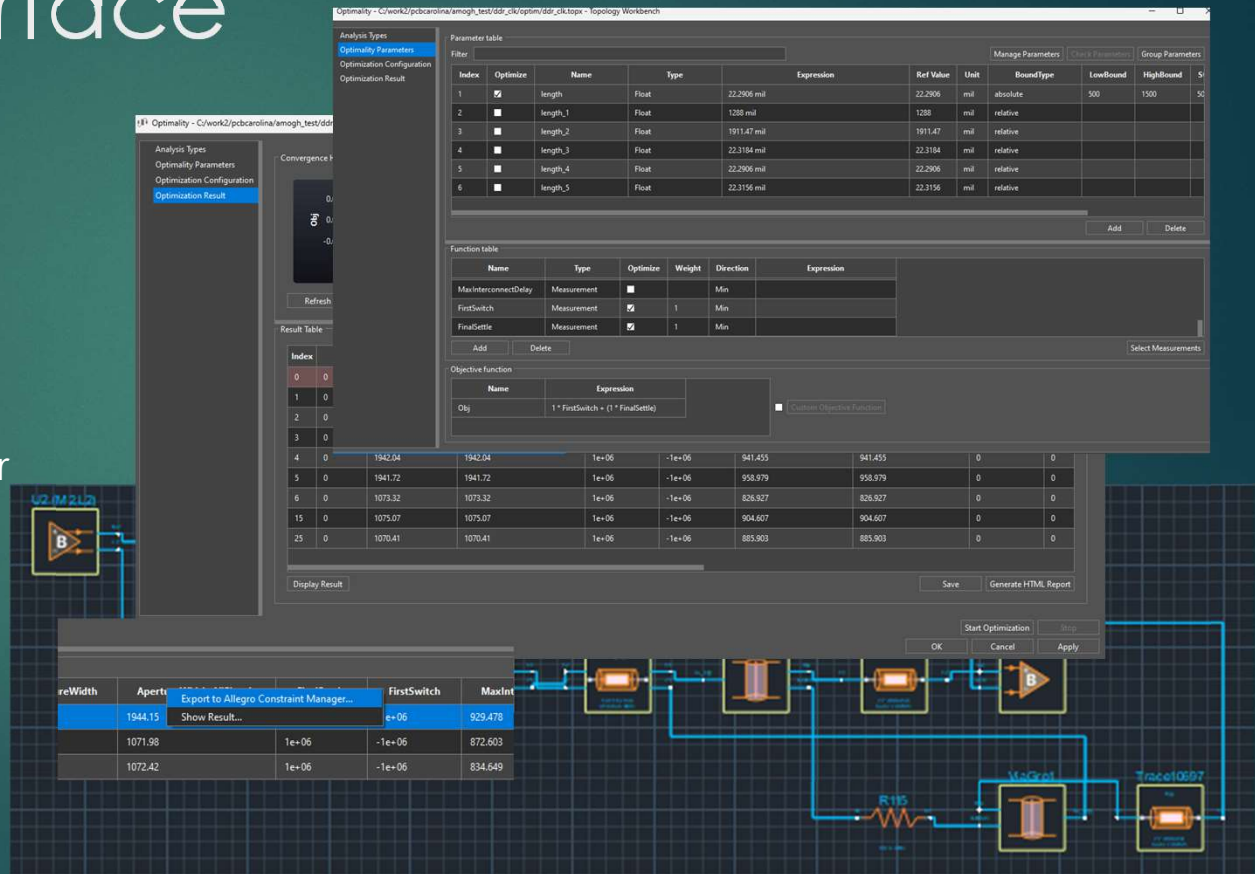


Topology Workbench and Optimality interface

Optimized simulation based upon defined criteria. Using an AI agent to help pick most optimum simulation and results

This could help predict and produce constraints based up your extracted nets in simulation.

Cut detailed simulation sweeps down by 100x



Optimization Workflows

Comprehensive System Design

Optimization workflows address thermal management, signal integrity, and mechanical constraints in system design.

Guided Problem Solving

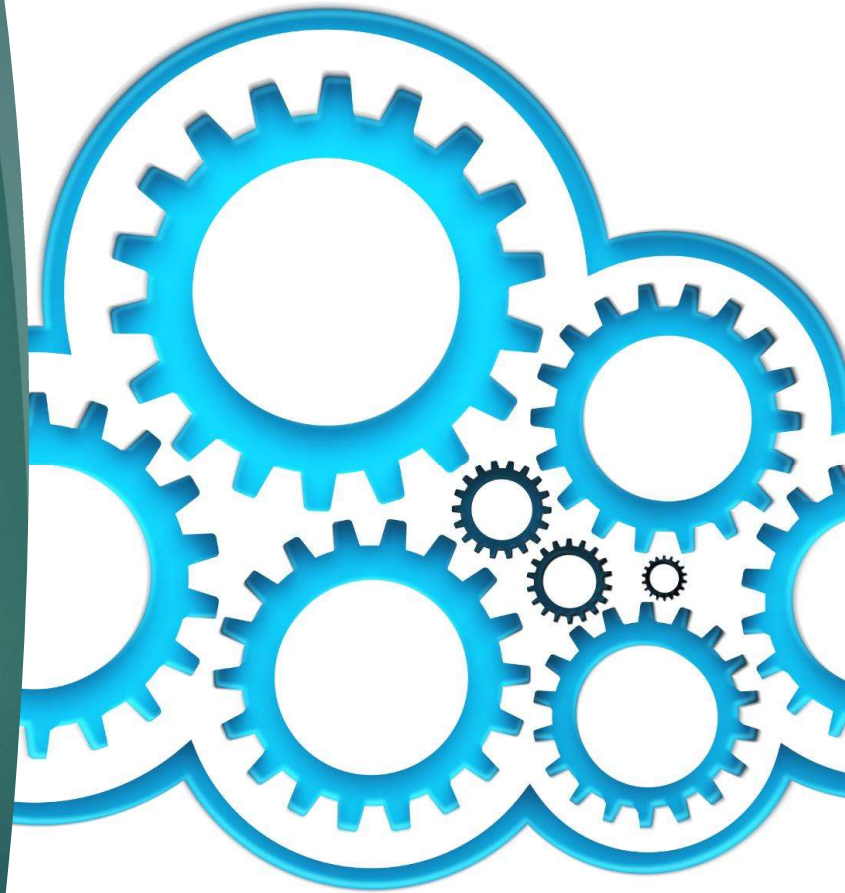
Workflows assist users in identifying issues, evaluating alternatives, and implementing effective solutions.

Iterative Optimization

The tool supports continuous improvement through iterative optimization and refinement processes.

Enhanced Performance and Reliability

Following optimization workflows leads to optimal product performance and enhanced reliability.



System Design Strategy

Strategic Planning in Design

System design strategy involves careful planning and execution to meet defined project goals effectively.

Optimality Explorer Benefits

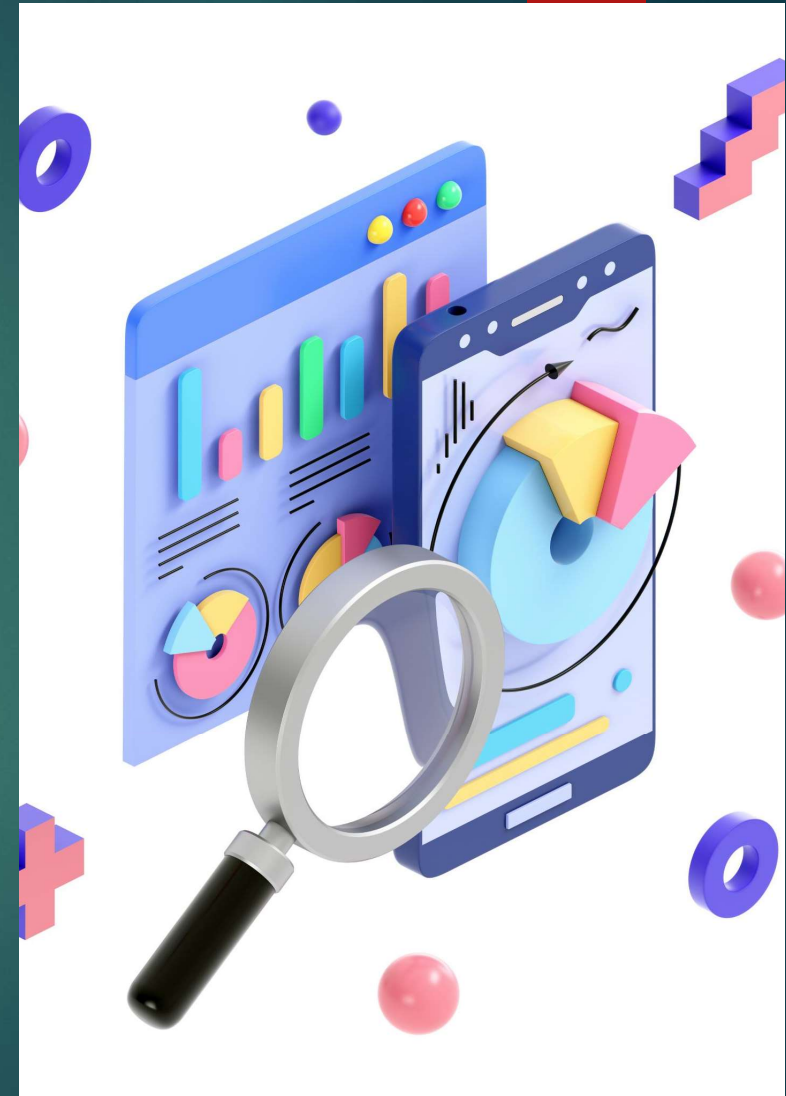
Optimality Explorer aids in strategic decisions by revealing design trade-offs and key performance metrics.

Alignment with Objectives

The tool helps align design choices with project goals to ensure all requirements are fulfilled.

Improved Outcomes

A well-defined strategy increases efficiency, reduces risks, and improves overall design results.



Overview of Optimality Explorer

Advanced Algorithm Optimization

Optimality Explorer uses cutting-edge algorithms to enhance system design strategies efficiently.

Multi-Discipline Support

Supports optimization workflows across thermal, mechanical, and electrical system analyses.

Actionable Insights and Recommendations

Provides clear insights and design recommendations to guide informed decision-making.

User-Friendly Interface

Features an intuitive interface that enhances user experience and accessibility in design workflows.

Optimality Explorer and Future Directions



Future Directions and Innovations

AI Integration Enhancement

Enhanced AI integration aims to improve analysis and design optimization in Allegro IDA and Optimality Explorer.

Expanded Analysis Capabilities

Expanding analysis capabilities enables deeper insights into design performance and problem-solving.

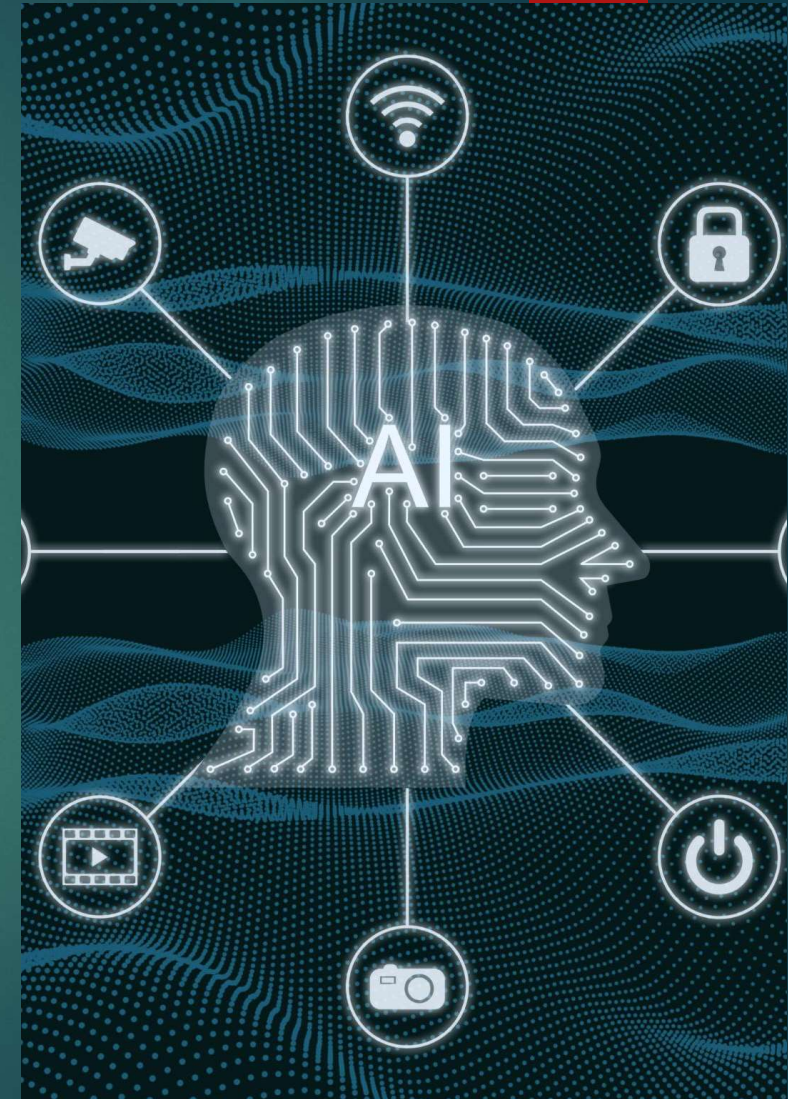
Improved User Interfaces

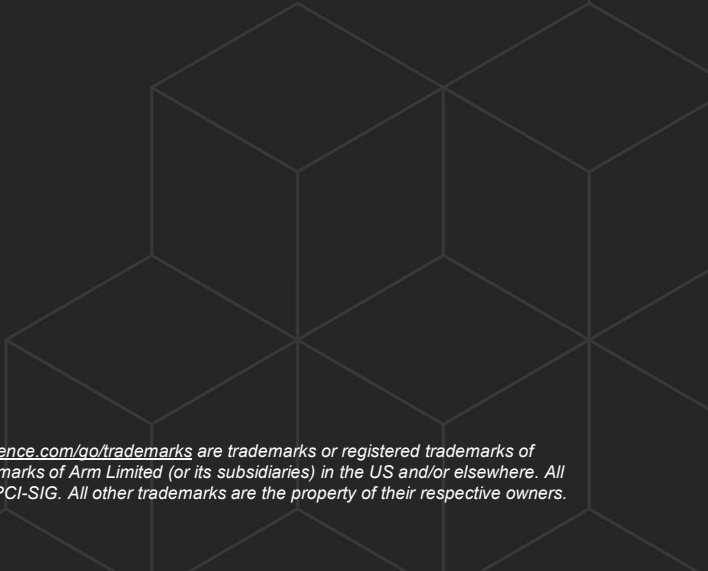
Improved user interfaces streamline workflows and enhance user experience for designers.

Automation and Workflow Streamlining

Innovations focus on increasing automation to speed up processes and improve product delivery time.

Optimality Explorer and Future Directions





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Overview of Allegro IDA & Optimality Explorer

Integrated Analysis

Real-time SI/PI checks within PCB design

Correct-by-Design

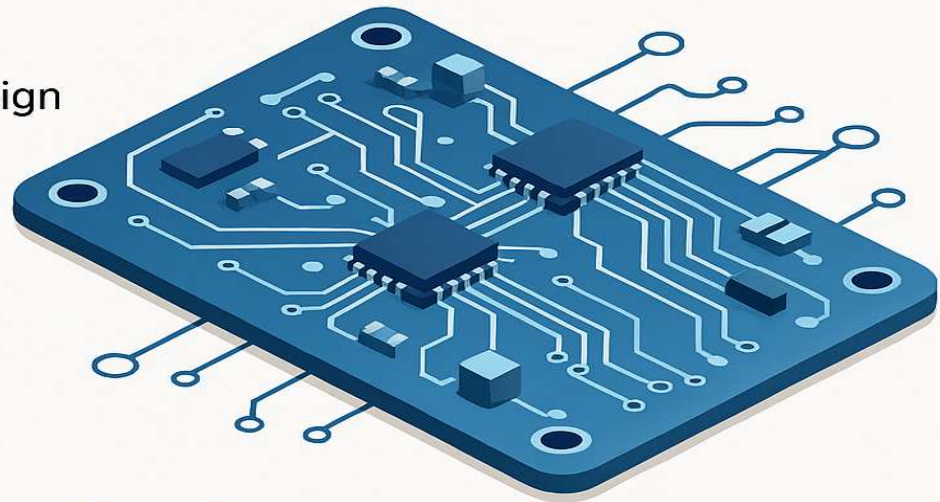
Embedded verification reduces errors early

Collaboration

Multi-stakeholder workflows with real-time feedback

Optimization

Intelligent algorithms for thermal, mechanical, electrical design



Benefits

Faster cycles, fewer errors

Improved design quality

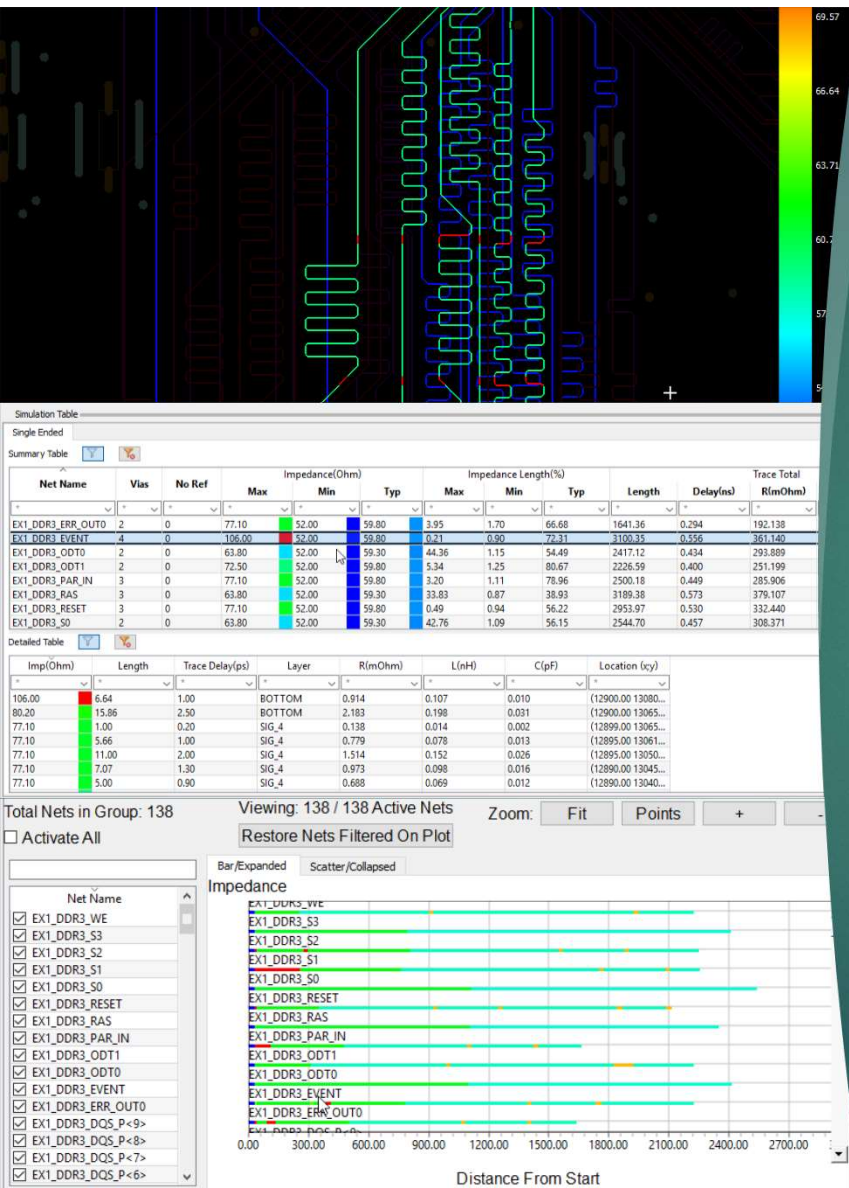
Future

AI integration

Expanded analysis

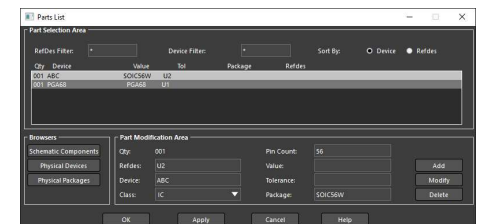
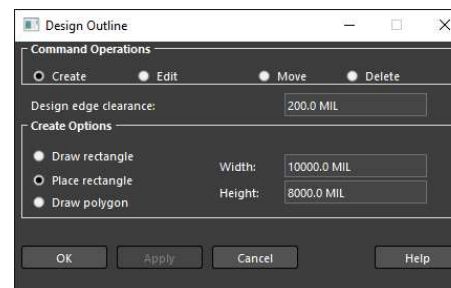
Impedance Analysis Screening

- ▶ Global view of results more accessible
 - Graphics
 - Tables and plots
- ▶ Look for outliers
 - Single-ended and differential impedance



Easily Create a Physical Mock-Up

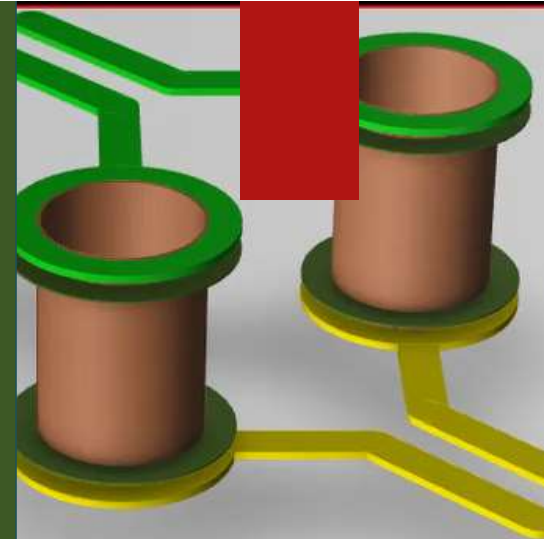
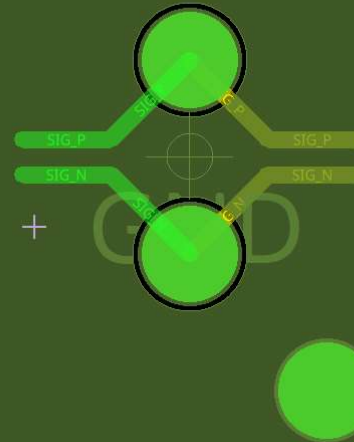
- ▶ Can create a quick partial layout from existing Allegro® footprints
- ▶ Floorplan placement of critical components
- ▶ Prototype routing for critical classes of nets



Via Wizard

- ▶ Topology Explorer via block
- ▶ Allegro® Via Generation
- ▶ Clarity™ Solver

3D



Length (L1): 50 MIL
Angle: 45
Width (W): 10 MIL
Spacing (S): 10 MIL
☐ Mirror Geometry



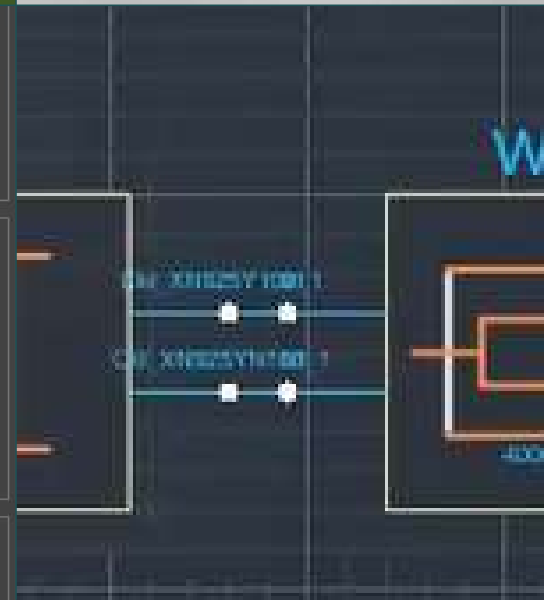
Differential Pair Pad Exit Traces

Pattern: Tight Gather
Layer: BOTTOM
Length (L1): 50 MIL
Angle: 45
Width (W): 10 MIL
Spacing (S): 10 MIL
☐ Mirror Geometry



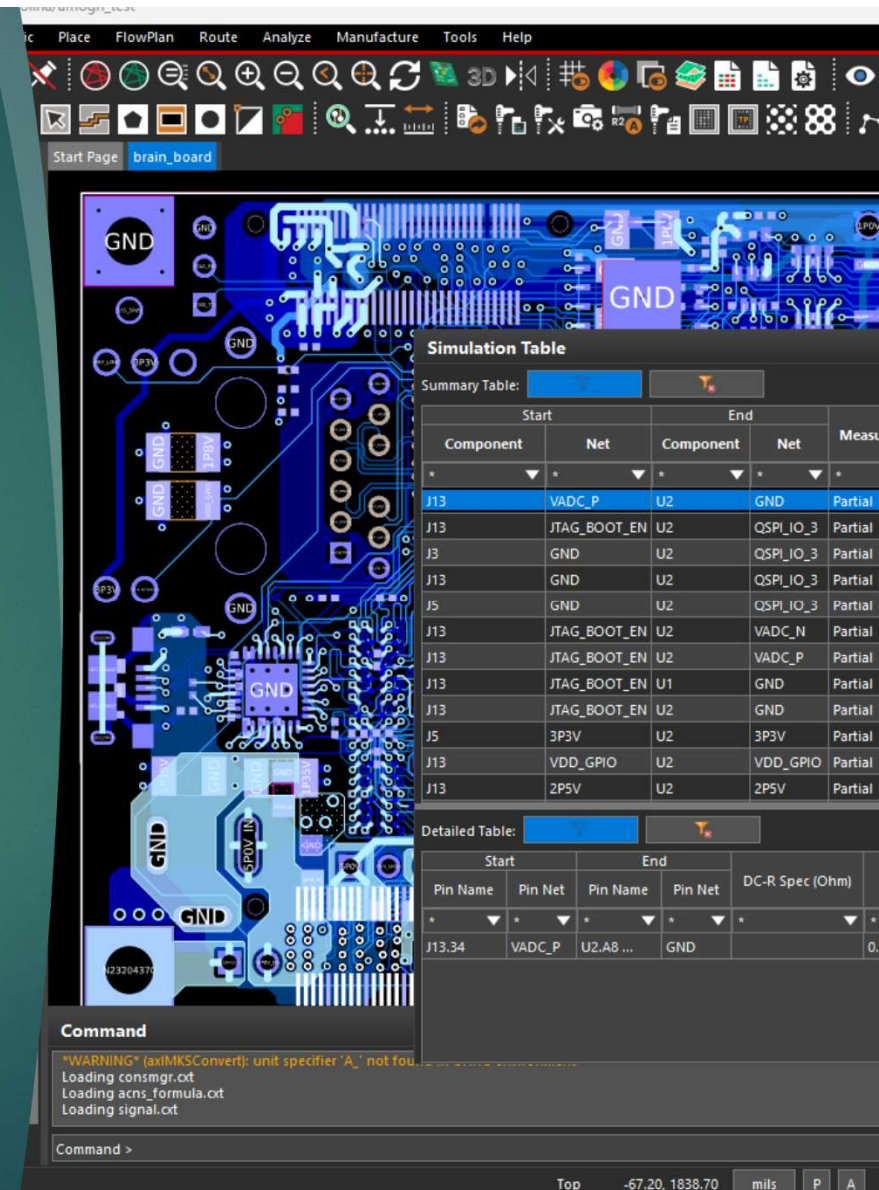
Return Path Via

Pattern: Single
Via Padstack: 55R36



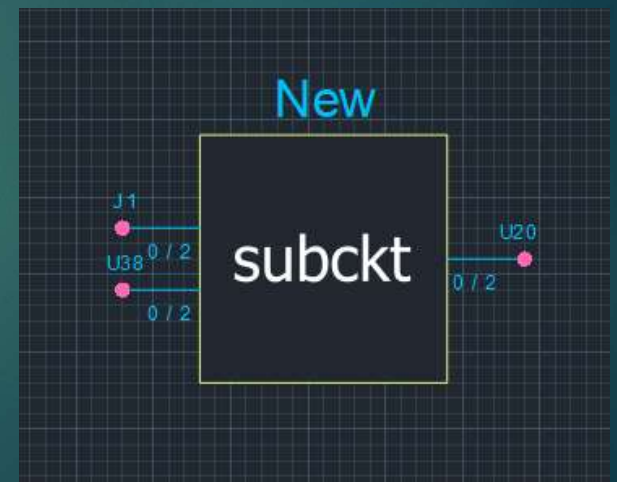
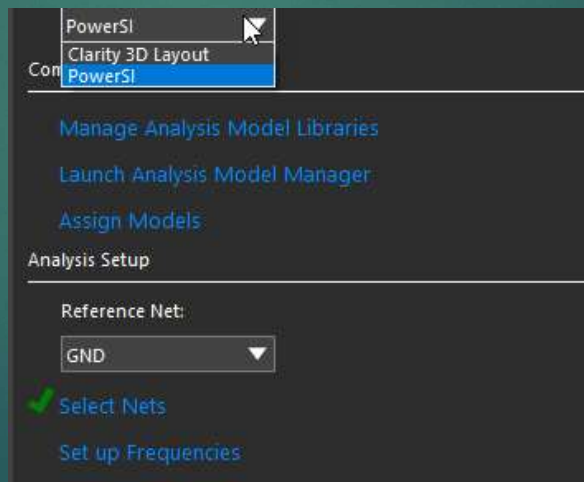
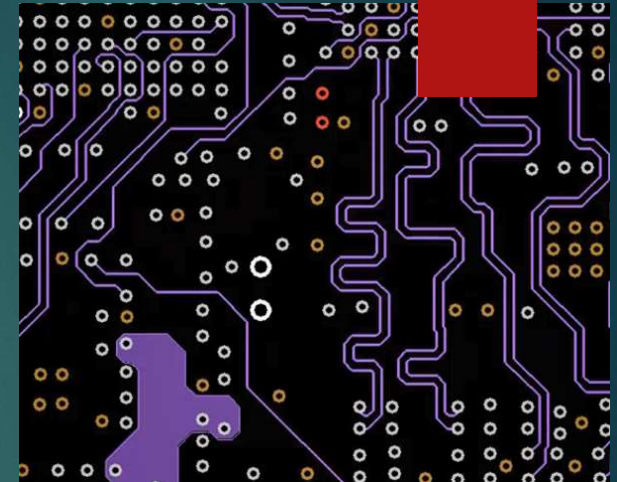
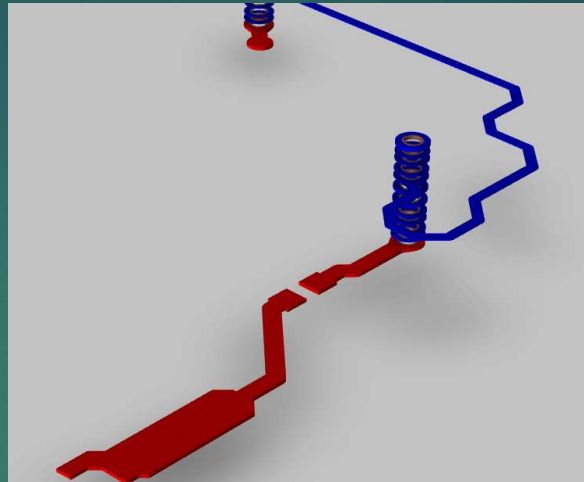
DC Resistance

- ▶ Measured dc resistance on any power net/plane
- ▶ Exportable csv
- ▶ Helps with defining the appropriate power delivery across multiple PDN's



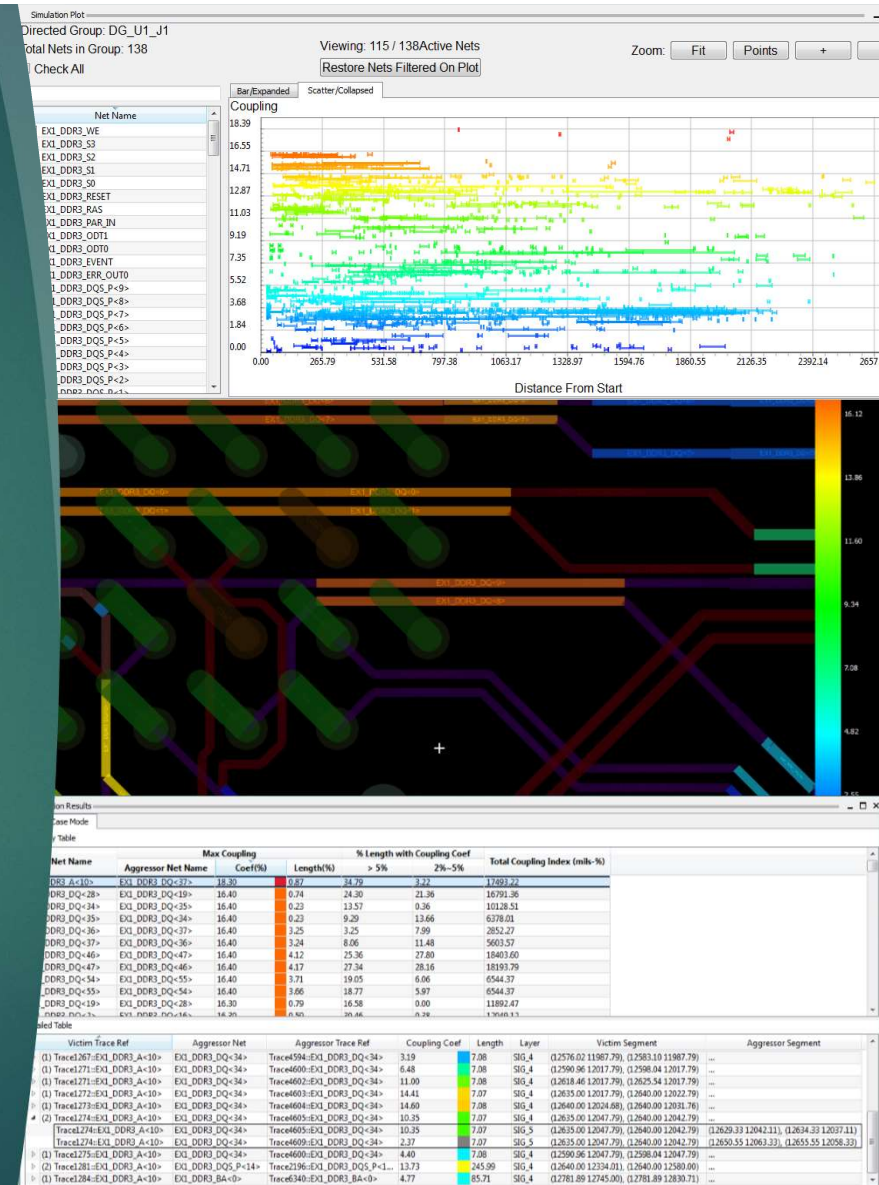
Interconnect Model Extraction

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Coupling Analysis Screening

- ▶ No SI models required
- ▶ Electrical coupling is more accurate than geometrical methods
- ▶ Global view of results
 - Graphics
 - Tables and plots

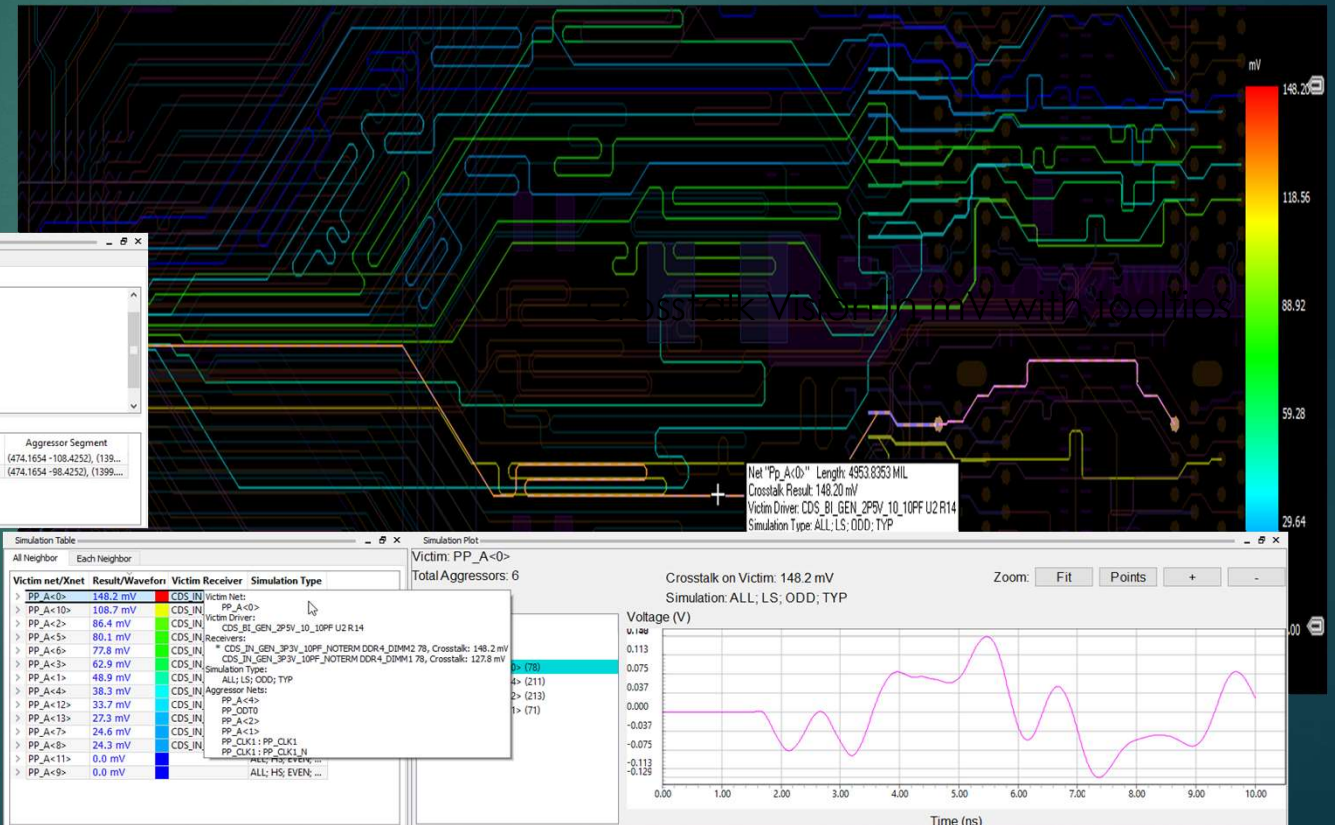


Crosstalk Analysis

Both tables support cross-probing
and ability to Show Details

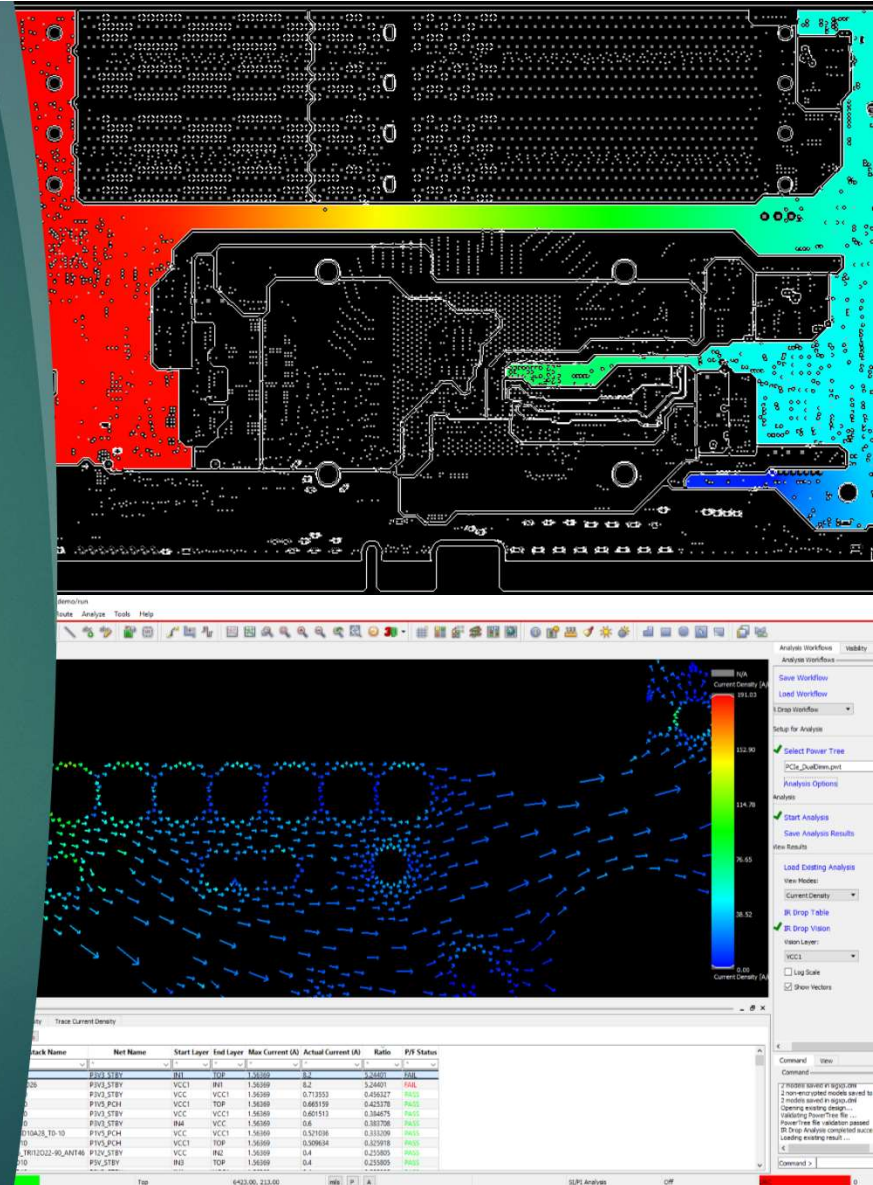
Each neighbor table
includes coupling data

Simulation Table									
All Neighbor									
Summary Table									
Victim net/Xnet	Aggressor net/X	Result/Waveform	Victim Receiver	Simulation Type					
	PP_CLK1	0.1 mV	CDS_IN_GEN_3...	EACH LS; ODD...					
	PP_A<1>	42.5 mV	CDS_IN_GEN_3...	EACH LS; ODD...					
	PP_A<2>	92.5 mV	CDS_IN_GEN_3...	EACH LS; ODD...					
	PP_ODT0	1.7 mV	CDS_IN_GEN_3...	EACH LS; ODD...					
	PP_A<4>	19.2 mV	CDS_IN_GEN_3...	EACH LS; ODD...					
▼ PP_A<10>	PP_CLK3	108.7 mV	CDS_IN_GEN_3...	EACH HS; ODD...					
	PP_CLK3	108.7 mV	CDS_IN_GEN_3...	EACH HS; ODD...					
▼ PP_A<2>	PP_A<0>	89.4 mV	CDS_IN_GEN_3...	EACH LS; ODD...					
Detail Table									
Victim Trace Ref	Aggressor Net	Aggressor Trace Ref	Coupling Coef	Length	Layer	Coupling Index	Victim Segment	Aggressor Segment	
Trace3832-PP_A<10>	PP_CLK3	Trace640-PP_CLK3	4.79	925.1929	LAY9-SIG3	4434.18	(474.1654 -100.1496), (...	(474.1654 -108.4252), (139...	
Trace3832-PP_A<10>	PP_CLK3_N	Trace607-PP_CLK3_N	14.28	925.1929	LAY9-SIG3	13215.60	(474.1654 -100.1496), (...	(474.1654 -98.4252), (1399...	



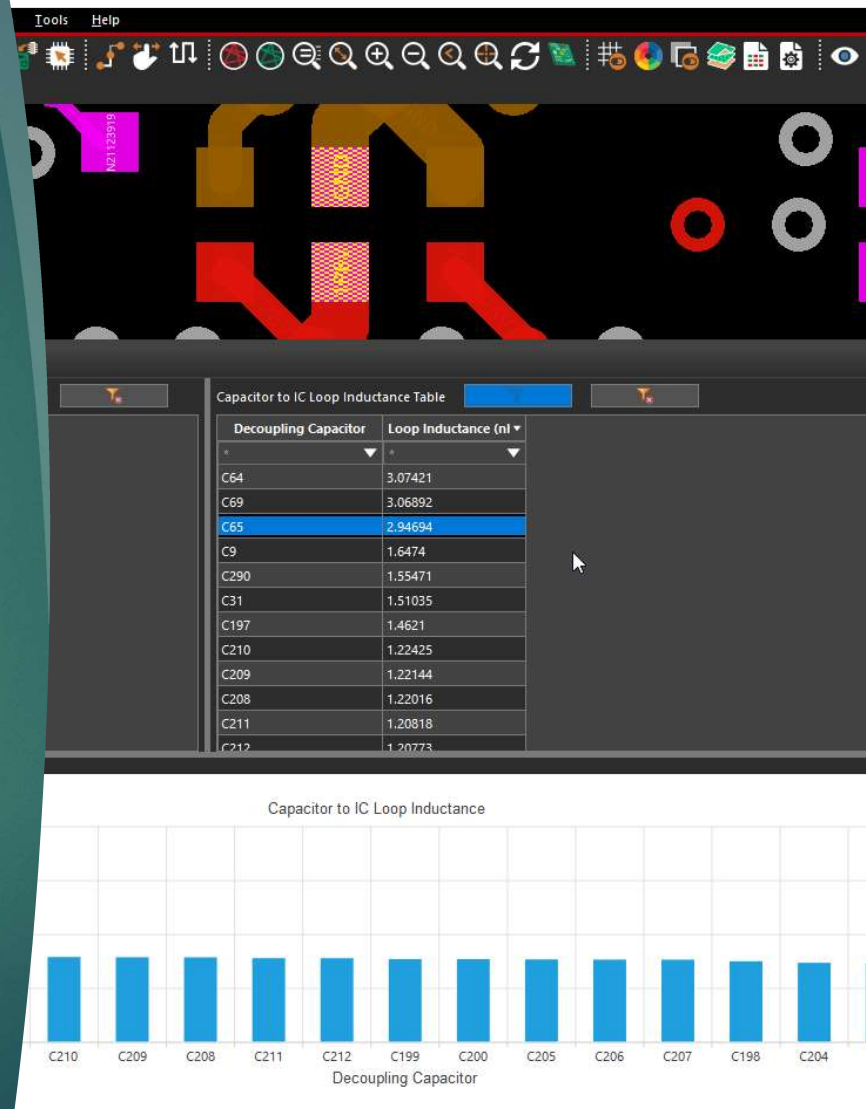
IR Drop Analysis

- ▶ IR drop vision can be displayed as voltage or IR drop
- ▶ Voltage drop
- ▶ Static voltage measurements
- ▶ Current flow and measured drops
- ▶ Graphical representation of individual or all power rails
- ▶ PowerDC engine



Power Inductance Workflow

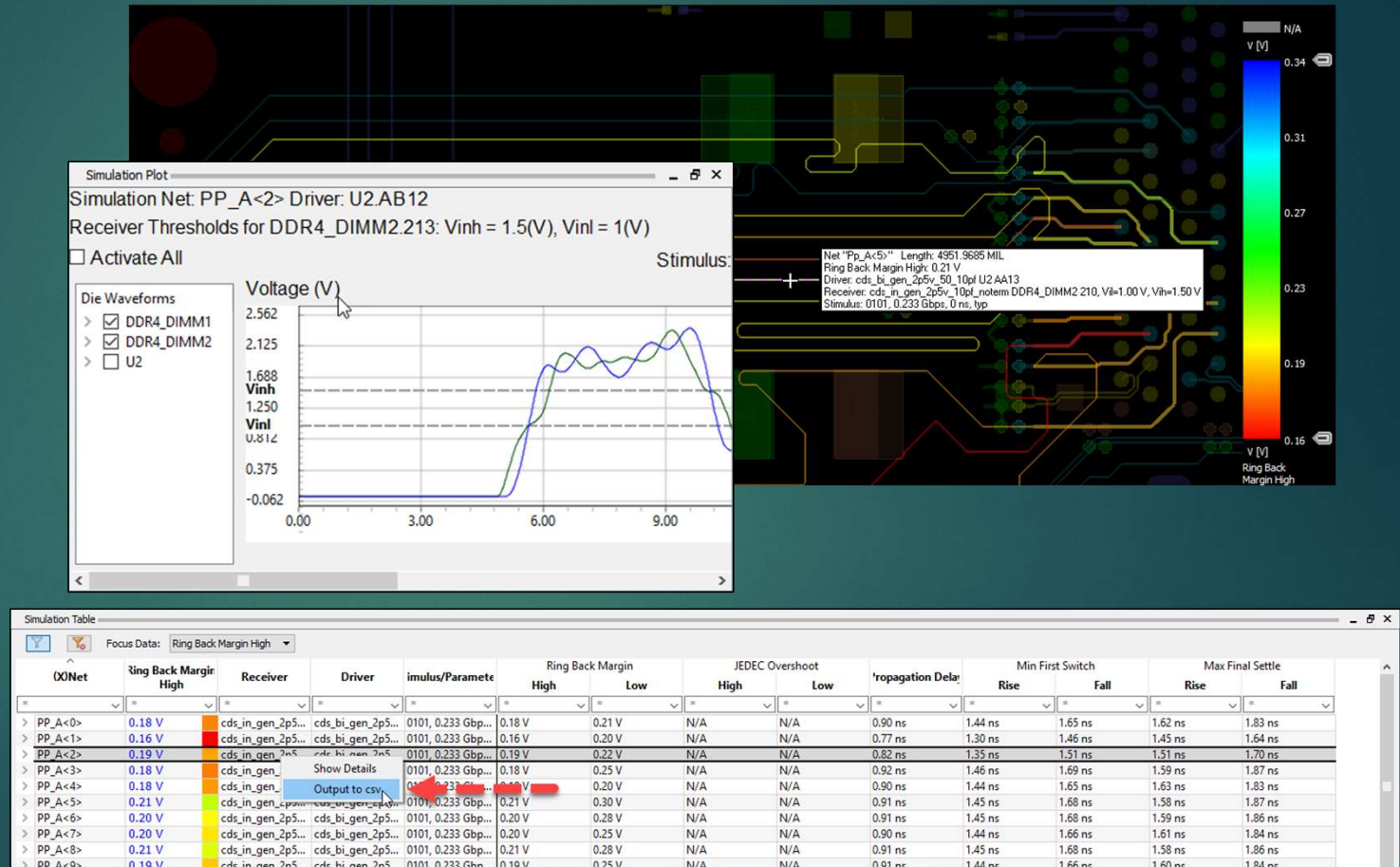
- Checks decap-to-IC loop inductance



Reflection Analysis

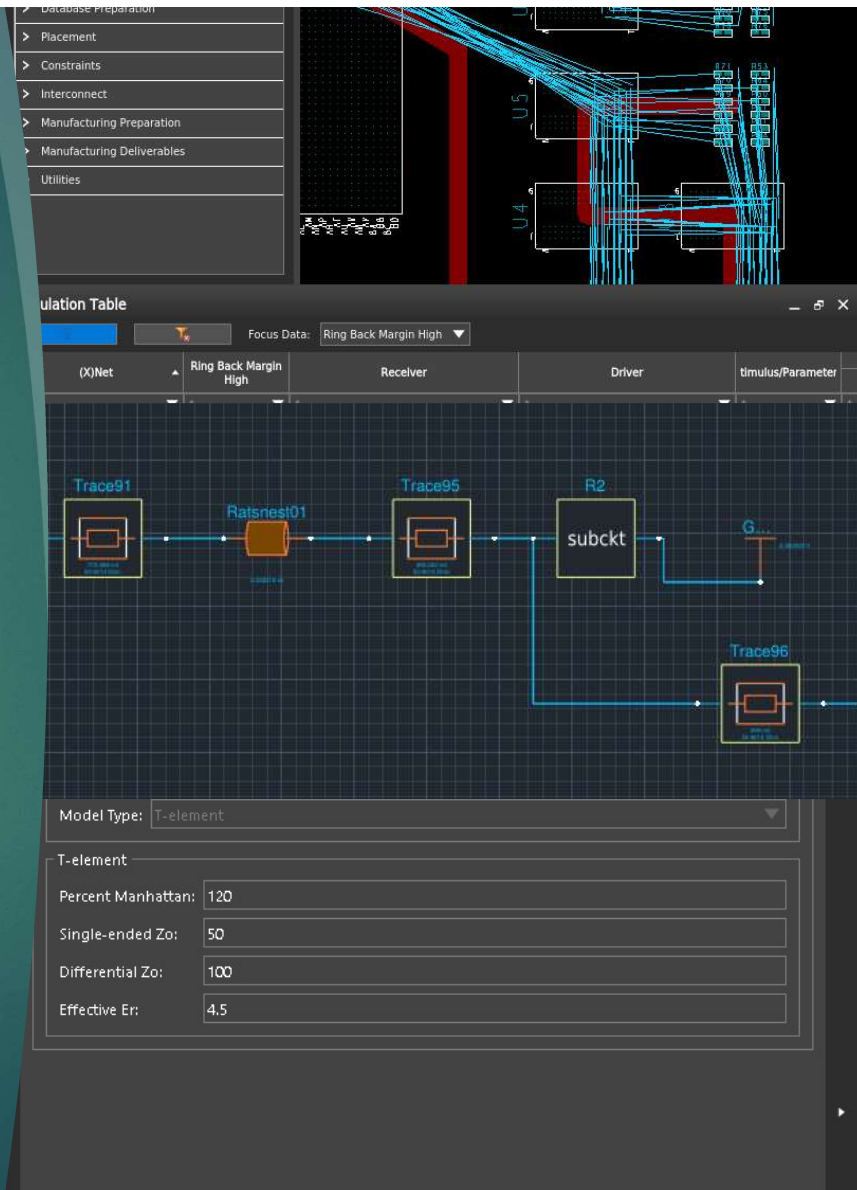
Vision is selected Focus
Data Measurement in
Table

Table supports cross-
probing, ability to
Show Details, and
CSV output



Simulation Support for Unrouted Nets

- ▶ Partially routed and unrouted signal nets are automatically modeled with transmission line models based on ratsnest, user-defined parameters, and Manhattan distances



Topology Extraction

(Topology Workbench)

- ▶ Integrated workflow in Sigrity™ Aurora
- ▶ Extract single-ended and differential signals into Topology Explorer
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