What’s New in Allegro X

Release 25.1 – September 2025

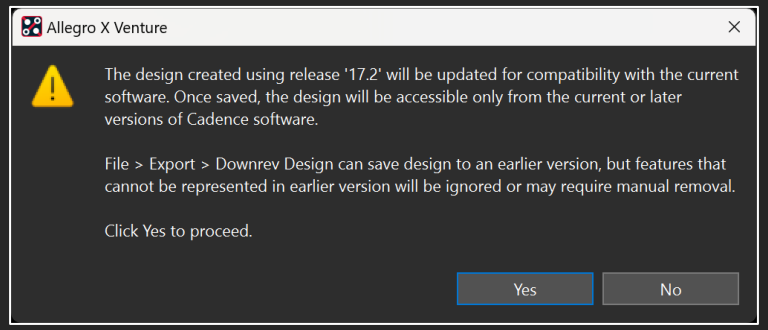
Allegro Product Engineering

Version 1.0

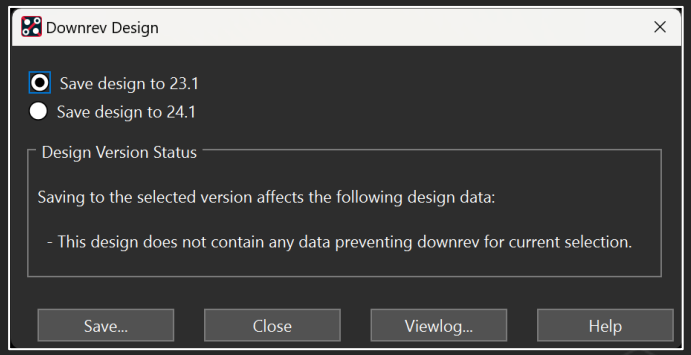
cadence®

Migration to 25.1
Layout Databases

- Database format
  - Designs from previous releases (**17.2, 17.4, 22.1, 23.1 and 24.1**) will go through an Uprev process when opened in **25.1** Layout Editor. Once saved, it will be in **25.1 format**



  - **25.1 designs** cannot be directly opened in previous releases. Downrev is available to save database to lower release, if necessary



  - Downrev will allow the database to be saved to either release 23.1 or 24.1 database format but saving to a release older than 23.1 will require opening the design using 23.1 software.

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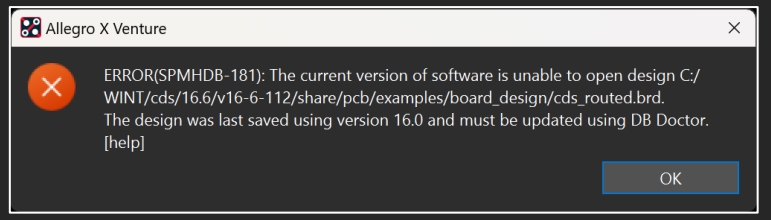
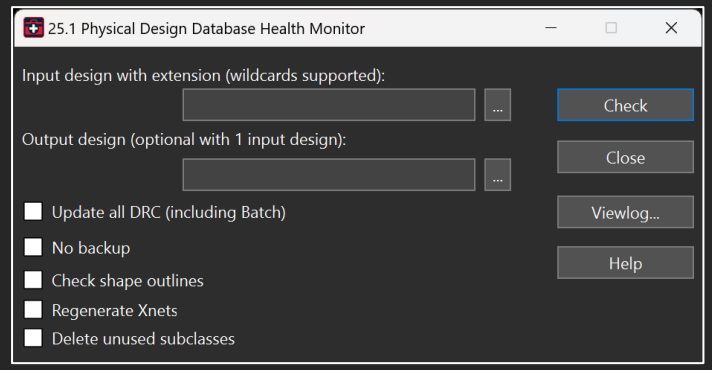
Migration to 25.1
Older Layouts and Libraries

- **16.6** designs and libraries cannot be used or opened directly in **25.1** and will require a manual update outside of Layout Editor using PCB DB Doctor (**dbdoctor_ui.exe**)
  - Libraries created in **17.2** or later could be directly used in **25.1**



- Library files saved in 25.1 or updated using PCB DB Doctor will be in 23.1 format, saves to lowest possible release, this can be seen using batch command **DBSTAT**
  - *C:\My_EDA_Libraries\>* **dbstat soic48w.dra**

    soic48w.dra: 23.1 NT



- Adding specific features to a library file will automatically save to version that feature was added
  - Add OpenType Fonts to symbols will save in 25.1 format so it can only be used in release **25.1 or higher**

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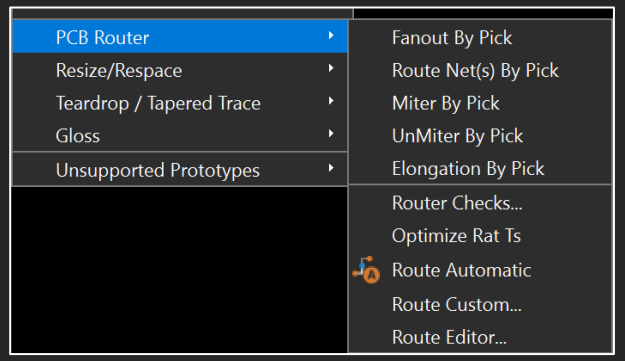
Migration to 25.1

Allegro PCB Router and License Requirements

- Allegro PCB Router (RHEL 8 Linux)
  - PCB Router is 32-bit application dependent on a set of 32-bit libraries not available in standard RHEL 8 Linux install
  - Required 32-bit libraries could be installed
    - **motif, libXp, libXext, libXt, libX11, elfutils-libelf, libxcrypt, glibc**
  - Without required 32-bit libraries installed on system PCB Router and related commands (***Route > PCB Router > ...***) will not run



Note: This limitation is specific to RHEL 8 Linux installations, Windows will continue to work and no longer requires 2012 Redistributable Package installed on the system.

- License requirements
  - License file must be updated to include 25.1 license keys, new licenses will be backward compatible to run previous software releases (17.2, 17.4, 22.1, 23.1, 24.1)

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Migration to 25.1
Allegro Classic Viewer

- Software advanced in release 23.1 caused Allegro Classic Free Viewer to be retired in favor of new Allegro Free Viewer, some benefits of the new viewer are
  - User-friendly interface, easy for average users, no advanced knowledge of Allegro X Layout tools
  - Improved layer display controls and access to information using built-in Search and Properties panels

- Existing customers using Allegro X PCB Editor sometimes need to open a second session for viewing purposes of PCB design (.brd) and with different interfaces it can be a challenge
  - Allegro Physical Viewer is available for the same look and feel but it requires a license

- In 25.1, we have restored Allegro Classic Free Viewer for customers to access directly from the standard Cadence install
  - There are no plans to provide a standalone Allegro Classic Free Viewer installation, only the Allegro Free Viewer installation will be available on the viewers download page

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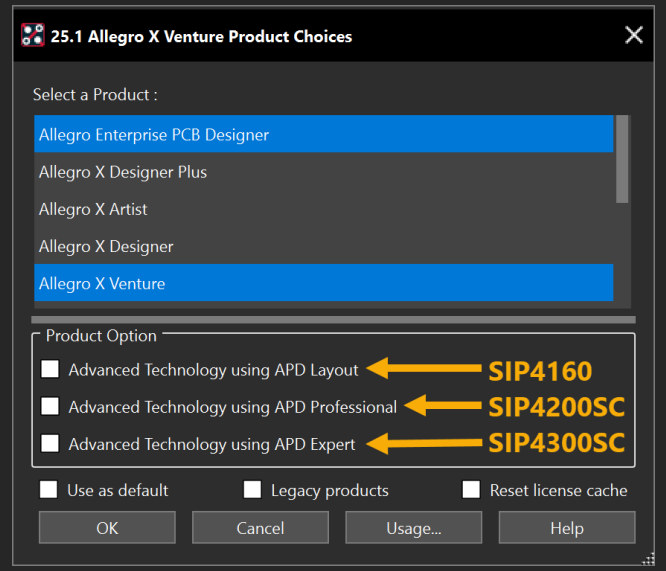
24.1 ISR6 (August 2025)

Extend Packaging functionality to Allegro X PCB Editor

- Provide access to select functionality available in Allegro X Advanced Package Designer inside of Allegro X PCB Editor
  - Select existing Packaging licenses as a Product Option



- Advanced Chip-on-Board Wirebonding
  - Increase wire bond limit from 100 pins to unlimited

- Metal Density Scan Report
  - Reports localized metal density across each layer of design
  - ***Manufacture > Metal Density Scan***

- Symbol Spreadsheet Import Command
  - Spreadsheet import to assign Net Name to pins of an existing Symbol
  - ***File > Import > Symbol Spreadsheet***

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Performance Improvements

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Performance Improvement Overall Strategy

Continuous Improvement

Improvements to existing algorithms in every release (ISR, QIRs, Base)

Driven from customer and proactive

i.e. Push Connectivity

Infrastructure Improvements

Targeting annual major releases

Medium term projects with known solution strategies like ongoing DRC improvements, voiding improvements, etc – targets 1 or 2 major releases

Scan Window based, multi threaded Boolean engine operations to help a range of applications DRC/DFM checks

Multi threading infrastructure for general algorithm pipelines

i.e. Acute Angle Checks

Long Term Improvements

In Prototyping/Discovery – plan will be published in the future (TBD)

Long term projects that are still under discovery and prototyping to address structural issues like scalability

i.e. Hierarchical Objects (i.e. Modules)

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Performance Improvement – In Every Release!

Action	24.1		25.1	
	Run Time	vs 2023	Run Time	vs 2024
Small Place Rep Module Import	0:01:09	16.6	0:00:36	1.9
Large Place Rep Module Import	1:10:21	3.6	0:20:14	3.5
Create Module	0:44:35	10.8	0:23:18	1.9
Place Module Destroyer	0:11:46	18.0	0:09:13	1.3
Large Module Refresh	6:56:09	1.8	0:23:51	17.4
DBDoctor	0:12:40	4.4	0:06:14	2.0
Cancel Moving Die - Cancel	0:00:08	2906.0	0:00:07	1.1
Cancel Moving Die - Select	0:00:55	1.1	0:00:52	1.1
Delete Via Structures	15:29:20	1.1	0:37:17	24.9
Update Via Structures / Redefine Structures	0:33:05	11.9	0:28:29	1.2
Edit Padstack	3:19:16	0.8	1:30:18	2.2
Insert Via/ Via Stitching/ Place Structures	0:01:43	9.0	0:00:49	2.1
ECO (Die Text In)	0:04:22	16.2	0:02:08	2.0
ECO (Library DRA) - GUI	0:17:23	4.3	0:13:20	1.3
Dynamic Shape Update	2:46:36	1.4	2:00:10	1.4
Move Die (Interactive)	1:01:27	1.0	0:30:26	2.0
Push Connectivity	0:00:45	3840.0	0:00:45	1.0
Design Summary Report	0:01:38	12.6	0:00:40	2.5
DRC Destroyer Cell 16 threads	0:29:51	1.0	0:01:34	19.1
DRC Destroyer Assembled Design 16 threads	0:26:38	1.4	0:14:32	1.8
DRC Destroyer Cell 32 threads	0:29:51	1.0	0:00:54	33.2
DRC Destroyer Assembled Design 32 threads	0:16:37	2.2	0:08:57	1.9

X times FASTER compared to benchmark times!

Report Any Slowness

- Please file performance related CCRs!
  - For any commands that you find that are slower than you think they should be
- Please include test cases so Cadence can analyze, prioritize, and address

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Areas with Recent Performance Improvements

6/16/2025 release and newer

- DRCs
- Import and Export Design Data (i.e., Die Text In, Module Import, etc.)
- Placement/Interactive Placement (i.e., Modules, Structures, Move Die, etc.)
- Routing/Interactive Routing
- SKILL & Ravel code runtime
- Dynamic Shapes and Voiding
- Designs with huge number of padstacks
- Refresh symbol, DBDoctor, Report
- Via Array (i.e., Delete), Degassing
- Show Element, Display
- 3DX View/3D Canvas DRC
- In-Design Analysis (IDA)

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Core Functionality Updates

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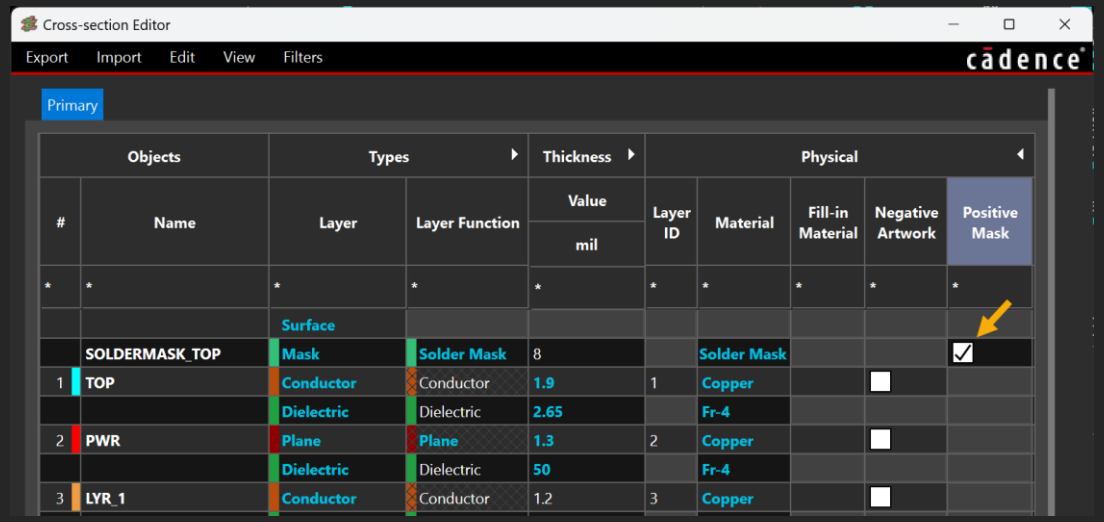
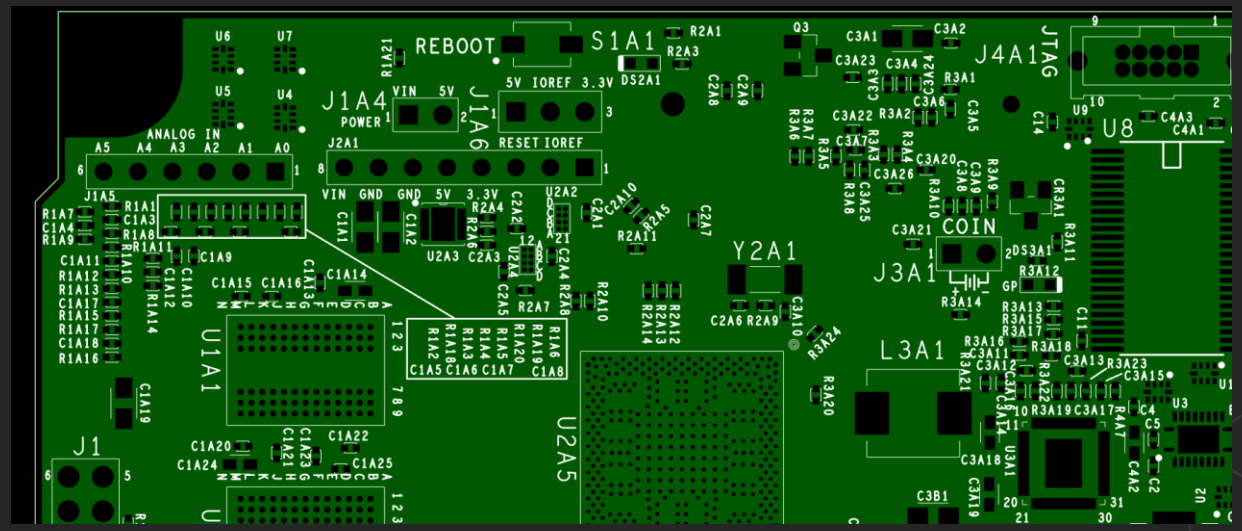
Positive Masks

- More realistic view in 2D helps clearly communicate design intent
  - 3DX Canvas, Allegro® X PCB DesignTrue™ DFM technology and manufacturing output
  - Positive mask dynamic shape uses Mask pads and other static objects to create mask openings

- Simple option in Cross-Section indicates Positive Mask new dynamic layer
  - No library/design changes required; all traditional negative mask objects generate openings in mask





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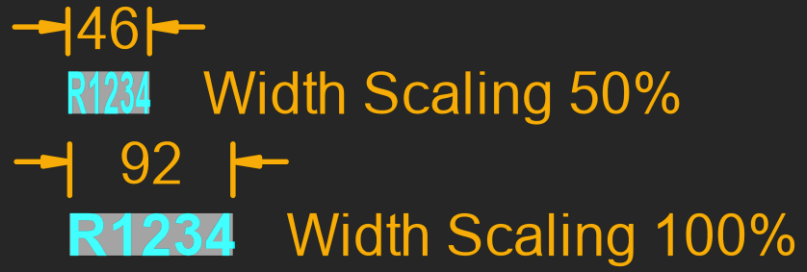
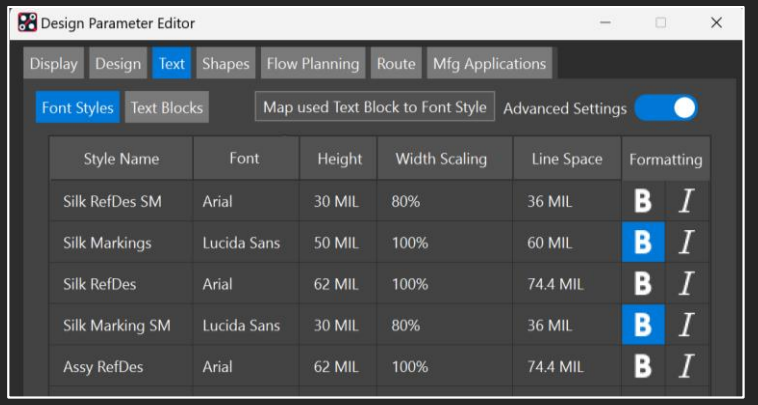
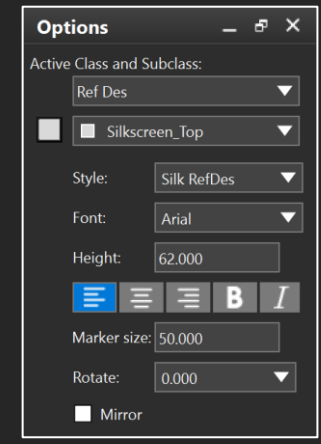
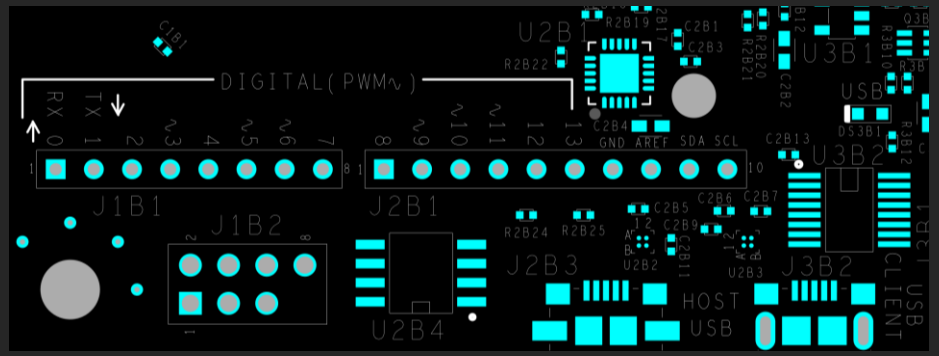
OpenType Fonts

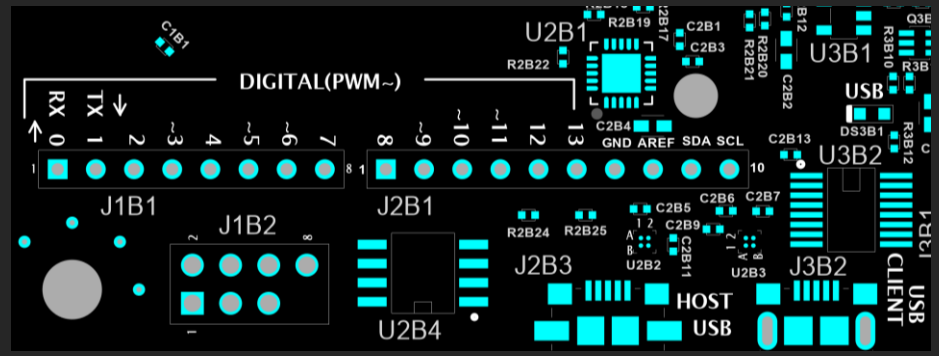




- Allegro® X PCB Design Platform has one standard block font for canvas rendering and manufacturing outputs
- OpenType Font support:
  - Input/edit text in specific font with consistent exports in manufacturing output and 3DX Canvas
  - Develop Styles to store font, % width, height and formatting (bold and italics)
  - Allegro X PCB DesignTrue™ DFM technology performs detailed checking of new fonts
  - 3DX Canvas support and visualization of OpenType fonts
- Allegro X text blocks still supported with mapping to a new font style
  - No library updates required; font replacement can be driven in layout







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Usability Improvements

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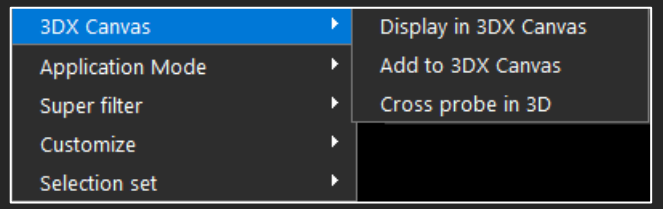
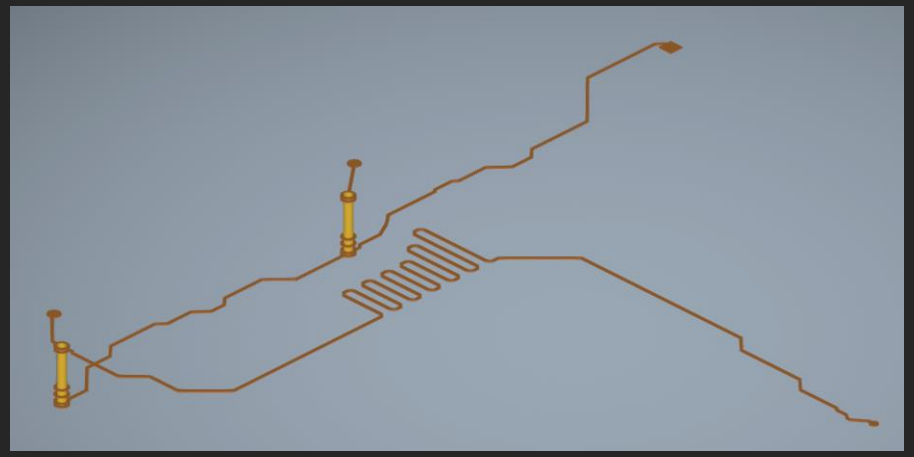
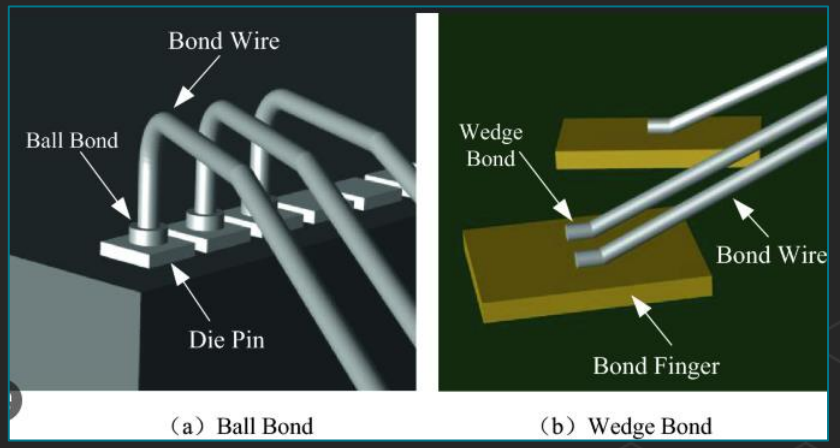
3DX Canvas

- Visualize Object selection(s) in 2D Canvas using via application mode ***RMB > 3DX Canvas***
  - Display in 3DX Canvas – pre-selected objects
  - Add to 3DX Canvas – Append newly selected objects
  - Cross Probe from 2D to 3D





- Added support for Ribbon Bonding and Attach Points for Packaging Designs



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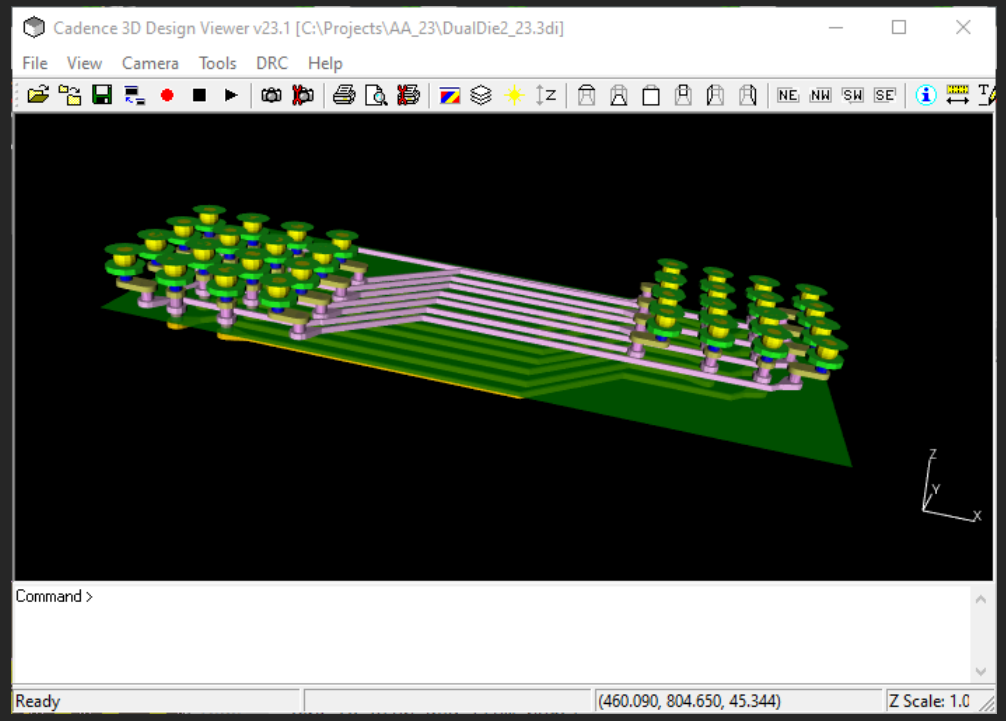
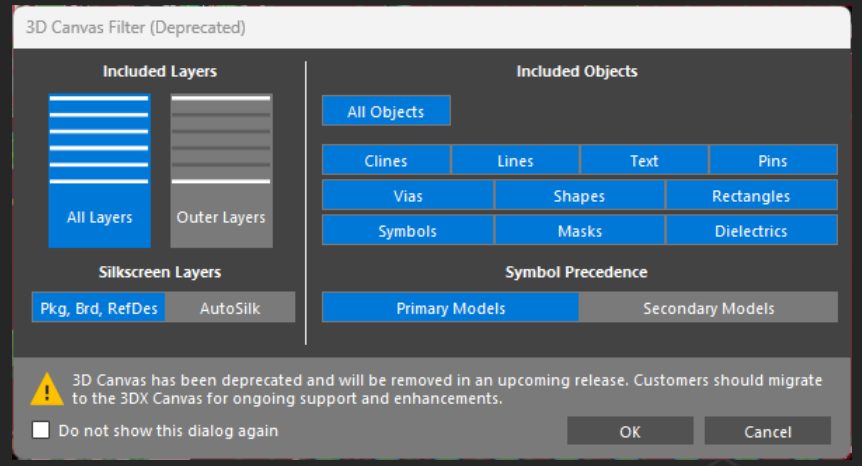
3DX Canvas

- Several updates to support In-Design Analysis Workflows in 3DX Canvas, including removal of Legacy Artwork 3D Viewer dependencies for Packaging.



Legacy 3D Design Viewer (Packaging)

- 3D Canvas has been deprecated in this release and will be removed in an upcoming release
  - Customers should migrate to 3DX Canvas for ongoing support and enhancements



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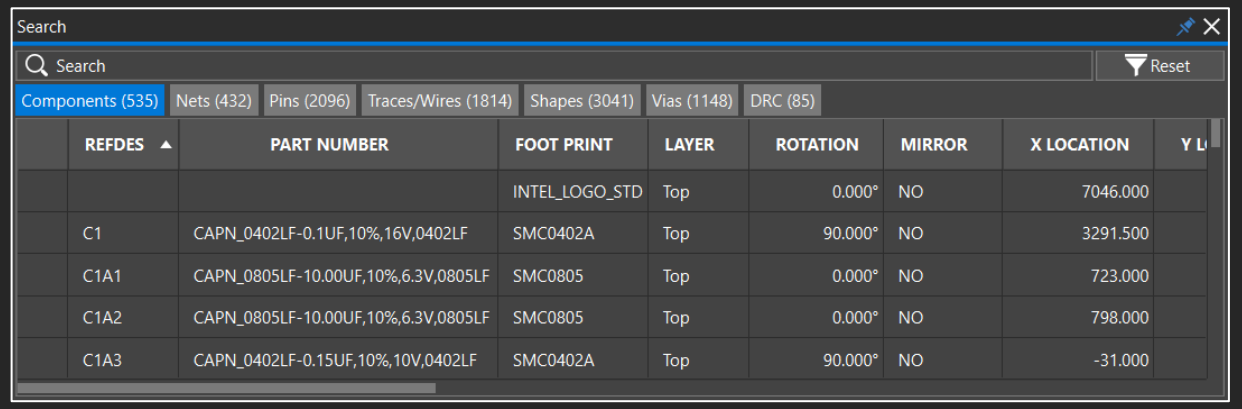
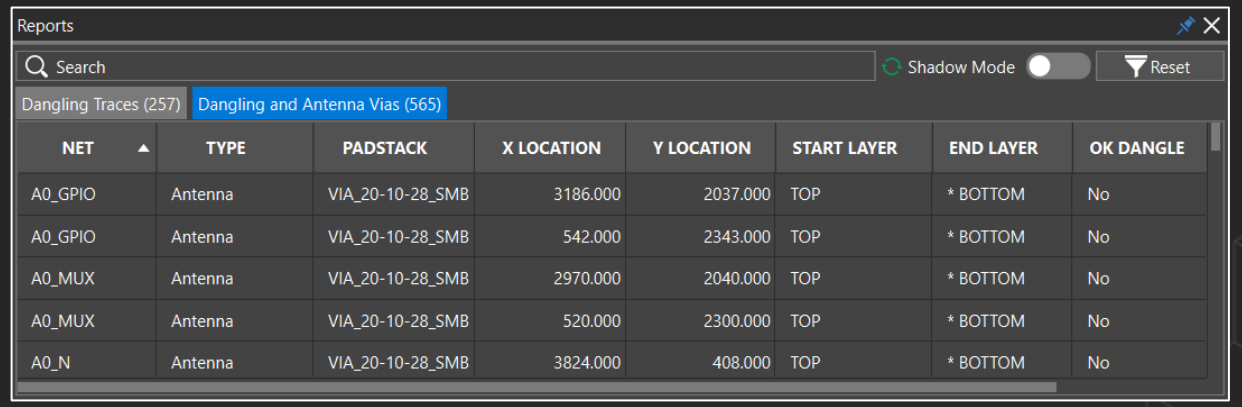
Docked Search and Reports Panels

- Docked Search Panel
  - Direct access to information organized in separate Objects tabs
  - Cross Probing ability between Search Panel and canvas
  - Alternative to Find By Query and Show Element
  - Integrated DRC Browser content
- Docked Reports Panel
  - Migration of select Quick Reports into a new Reports Panel
  - Allows quick canvas navigation during Report Reviews
  - Alternative to floating HTML Viewer window
  - Will continue to migrate other key reports into this new Report Panel



REFDES	PART NUMBER	FOOT PRINT	LAYER	ROTATION	MIRROR	X LOCATION	Y L
		INTEL_LOGO_STD	Top	0.000°	NO	7046.000	
C1	CAPN_0402LF-0.1UF,10%,16V,0402LF	SMC0402A	Top	90.000°	NO	3291.500	
C1A1	CAPN_0805LF-10.00UF,10%,6.3V,0805LF	SMC0805	Top	0.000°	NO	723.000	
C1A2	CAPN_0805LF-10.00UF,10%,6.3V,0805LF	SMC0805	Top	0.000°	NO	798.000	
C1A3	CAPN_0402LF-0.15UF,10%,10V,0402LF	SMC0402A	Top	90.000°	NO	-31.000	



NET	TYPE	PADSTACK	X LOCATION	Y LOCATION	START LAYER	END LAYER	OK DANGLE
A0_GPIO	Antenna	VIA_20-10-28_SMB	3186.000	2037.000	TOP	* BOTTOM	No
A0_GPIO	Antenna	VIA_20-10-28_SMB	542.000	2343.000	TOP	* BOTTOM	No
A0_MUX	Antenna	VIA_20-10-28_SMB	2970.000	2040.000	TOP	* BOTTOM	No
A0_MUX	Antenna	VIA_20-10-28_SMB	520.000	2300.000	TOP	* BOTTOM	No
A0_N	Antenna	VIA_20-10-28_SMB	3824.000	408.000	TOP	* BOTTOM	No

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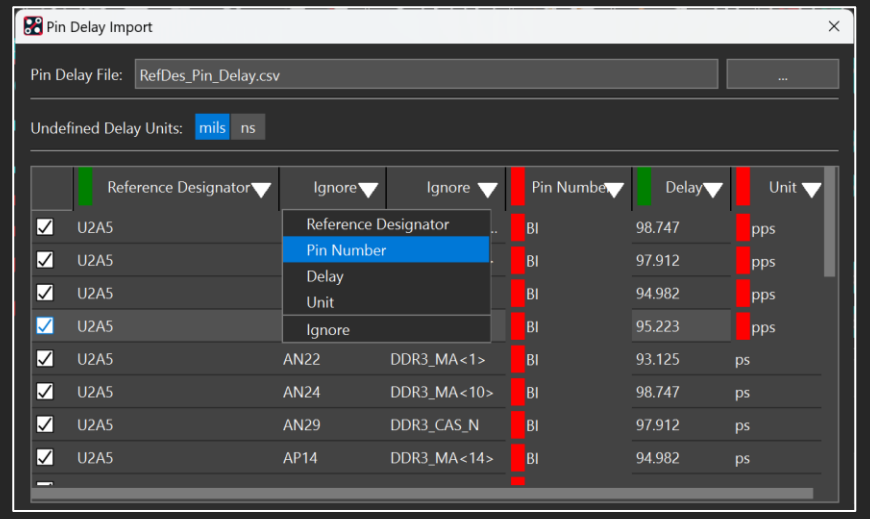
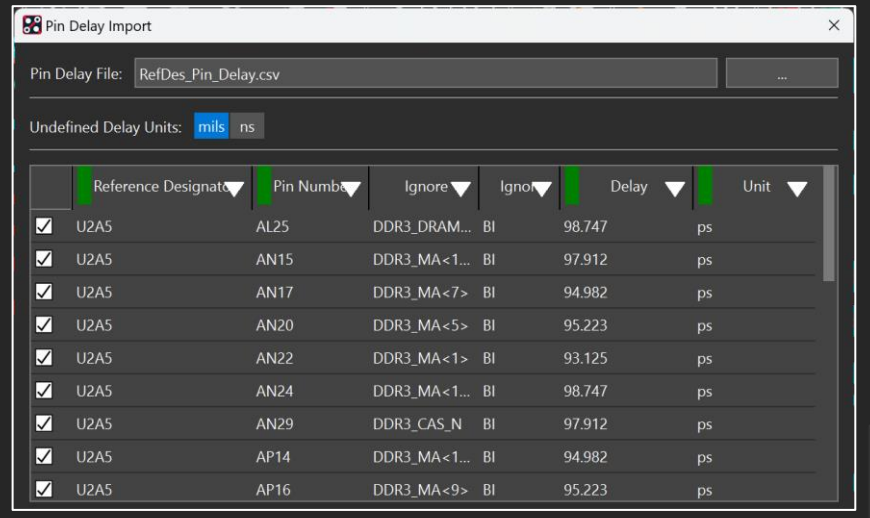
Pin Delay Import

- More capable than legacy feature providing ability to import several formats
  - Any Microsoft Excel file (.csv)
  - Allegro ® X Constraint Compiler – ObjectRule Table (.csv)
  - Existing Pin Delay format



- Loading CSV file in dialog will auto-detect columns and validate data prior to import
  - Ability to adjust columns categories and cell values
  - Queries database to ensure Reference Designator and Pin number combination exists, red color swatch cell indicates mismatch
  - Uncheck rows that should not be imported



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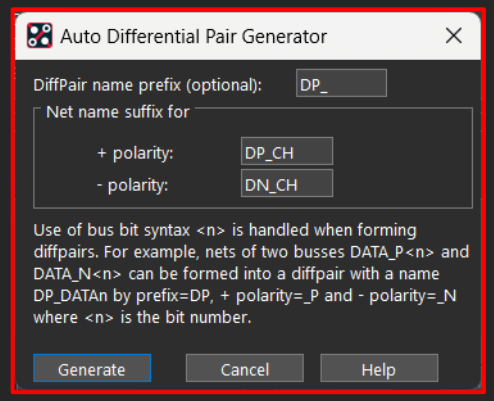
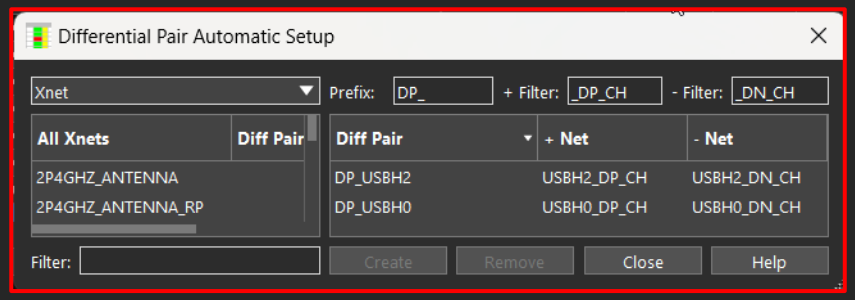
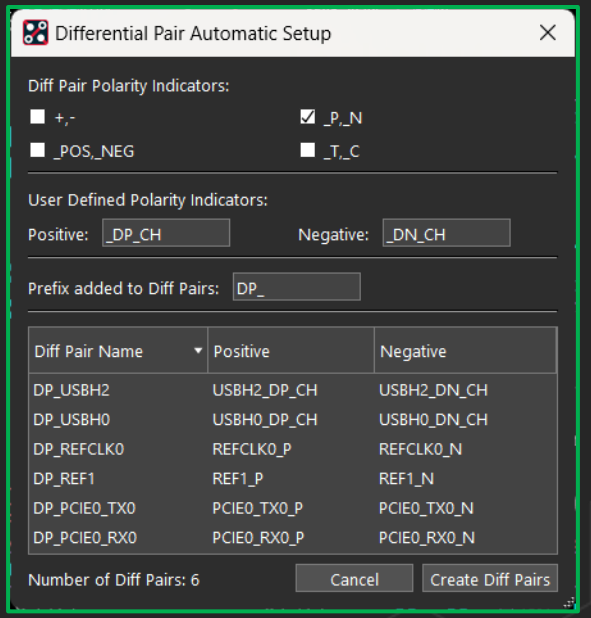
Differential Pair Automatic Setup

- Several ways to create Differential Pairs, manual and automatic, each having benefits but no centralized way to complete the task





- Integrated all best aspect of previous solutions into a single dialog to generate Differential Pairs quick inside and outside of Constraint Manager
  - ***Logic > Assign Differential Pair*** in Layout
  - ***RMB > Create > Differential Pair > Auto Setup*** in Constraint Manager



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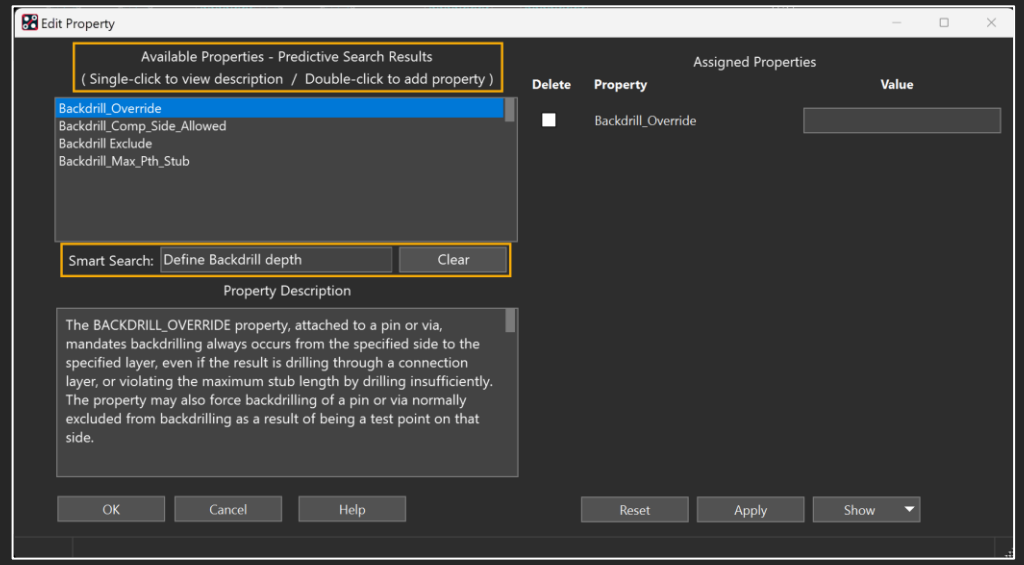
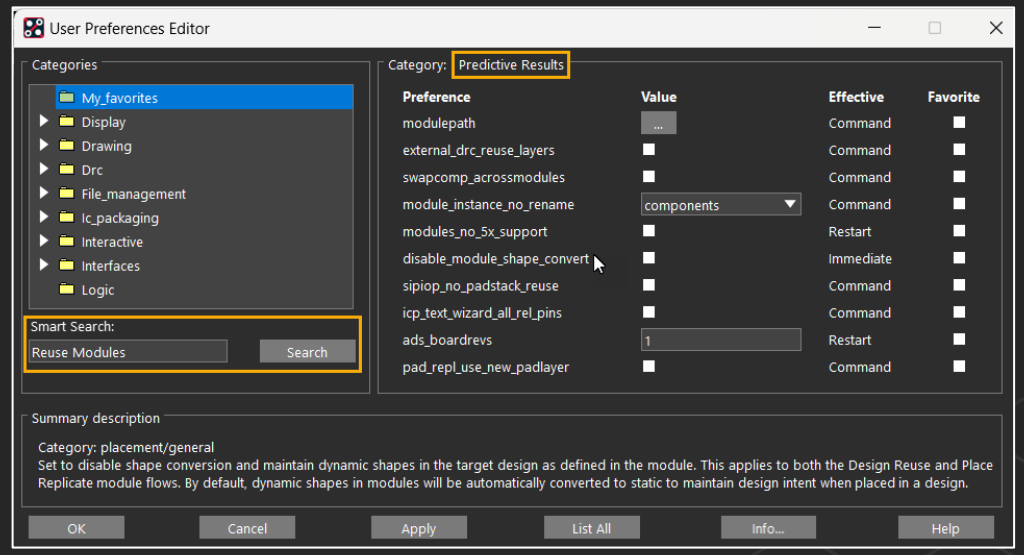
Smart Search

- Navigational guidance within the tool to support everyday design activities
  - Locate/apply object properties without advanced knowledge of property name along with providing detailed description of its use (no more scrolling thru a list of properties list)
  - User Preferences Editor finds your preferences quickly and easily (beyond searching thru descriptions)





- Plans to continue expansion in different areas on future releases (SKILL® API, Padstack Edit, Constraint Modes, Constraint Management)

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Constraint Management

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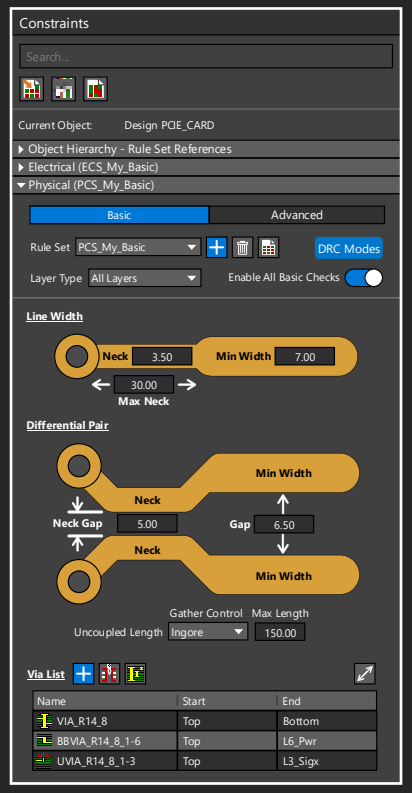
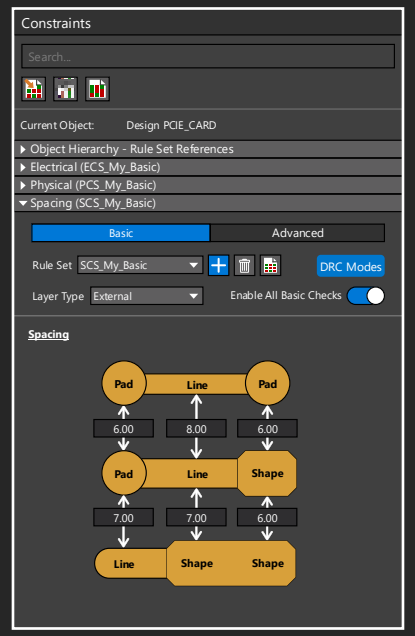
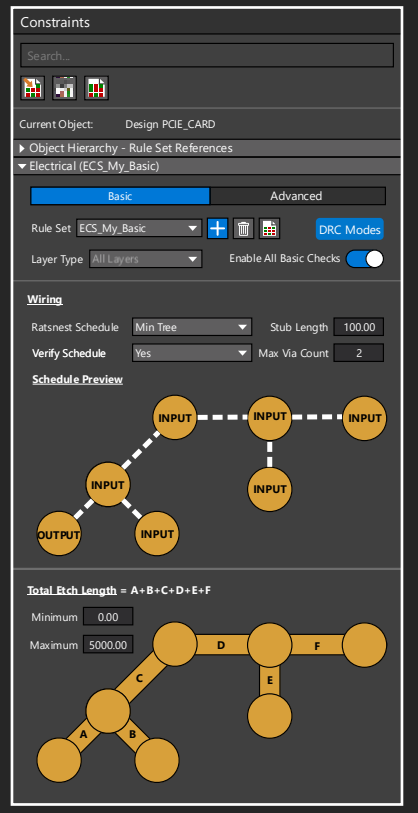
Constraint Panel – Gateway into Constraint Manager

- New Constraint Panel offers a streamlined and intuitive way to manage design constraints directly within layout canvas (Physical, Spacing, Electrical)
  - Access to all existing Constraints Sets with the ability to create new Constraint Set as required







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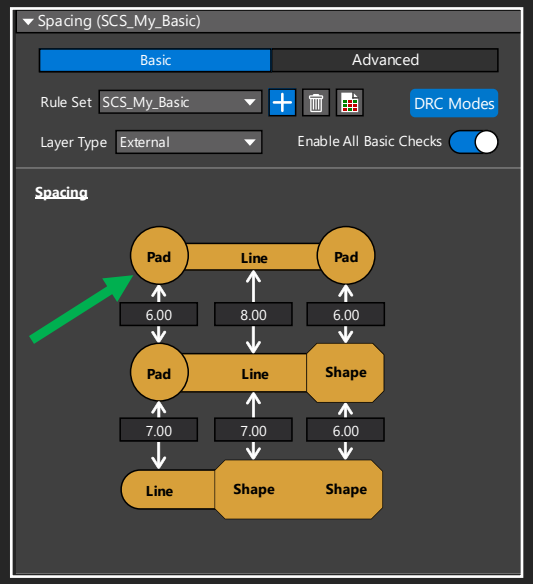
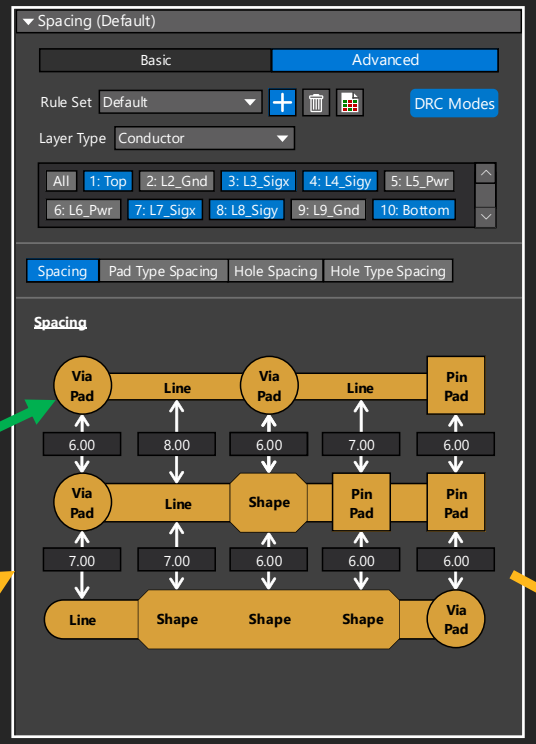
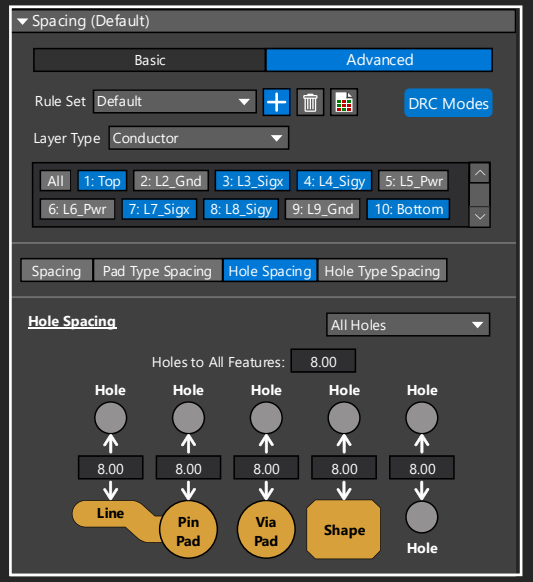
Constraint Panel – Gateway into Constraint Manager

- Enter values on hierarchal object to seed value at lower levels
  - Basic and Advanced slider expands to show more detailed Spacing rules
  - Navigate to lower levels only when exceptions are required

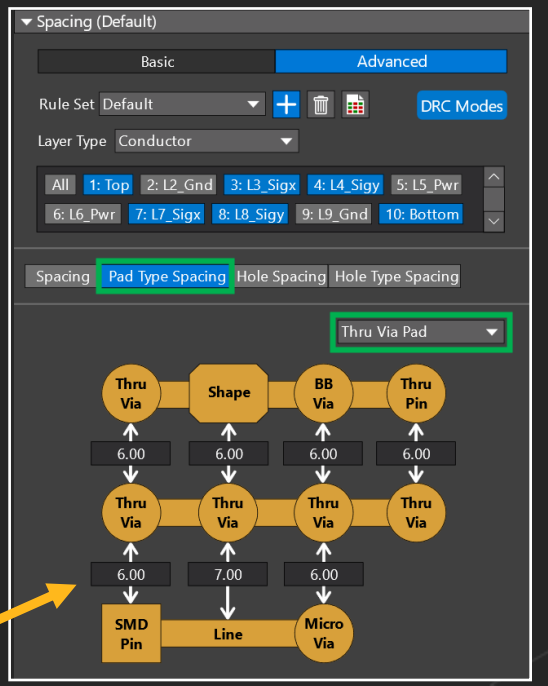


Basic Pad values seeds Advanced Spacing Via Pad and Pin Pad values





Advanced Spacing Via Pad value seeds Thru Via, BB Via and uVia under Pad Type Spacing to expand value entry



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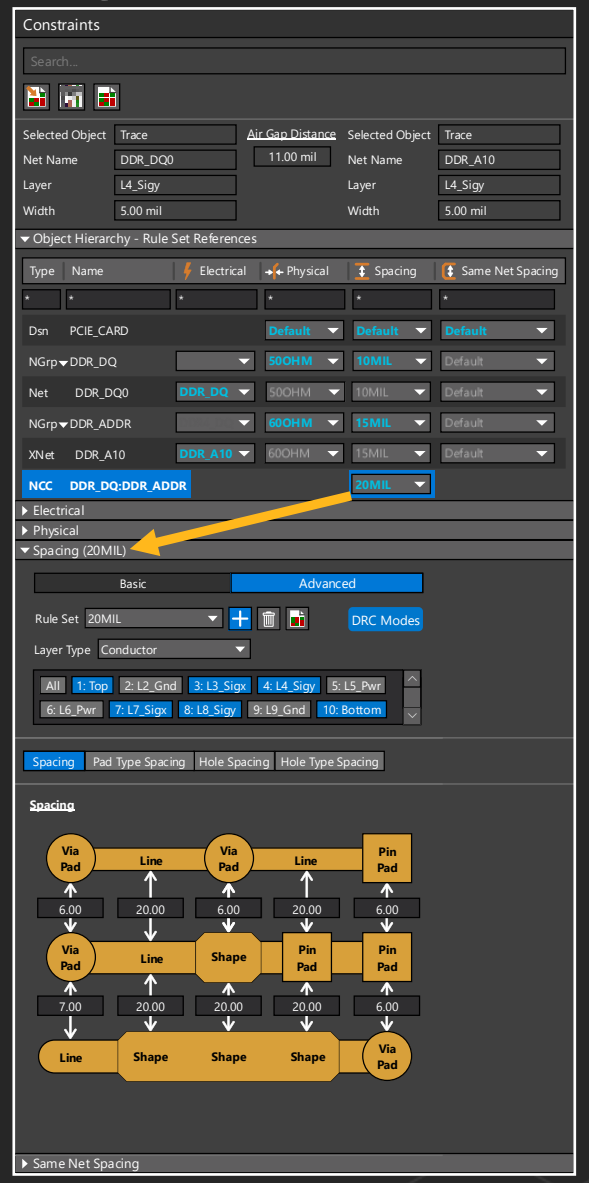
Constraint Panel – Gateway into Constraint Manager

- Select object(s) on canvas to display resolved constraints with associated Constraint Set assignment
  - Constraint Sets can be added at many levels, but it is important to understand the highest level will influence results on canvas
  - Focus on controlling constraints at an abstract level, instead of Net level, by assigning Constraint Sets to hierarchal groups (Net Group, Net Class, Diff Pair)
- Row and Constraint Set will be highlighted indicating resolved constraints with Constraint Sets driving rules activated under each domain for quick reference
  - Adjust Constraint Set or create a new Constraints Set for assignment
- Everything at your fingertips without opening Constraint Manager



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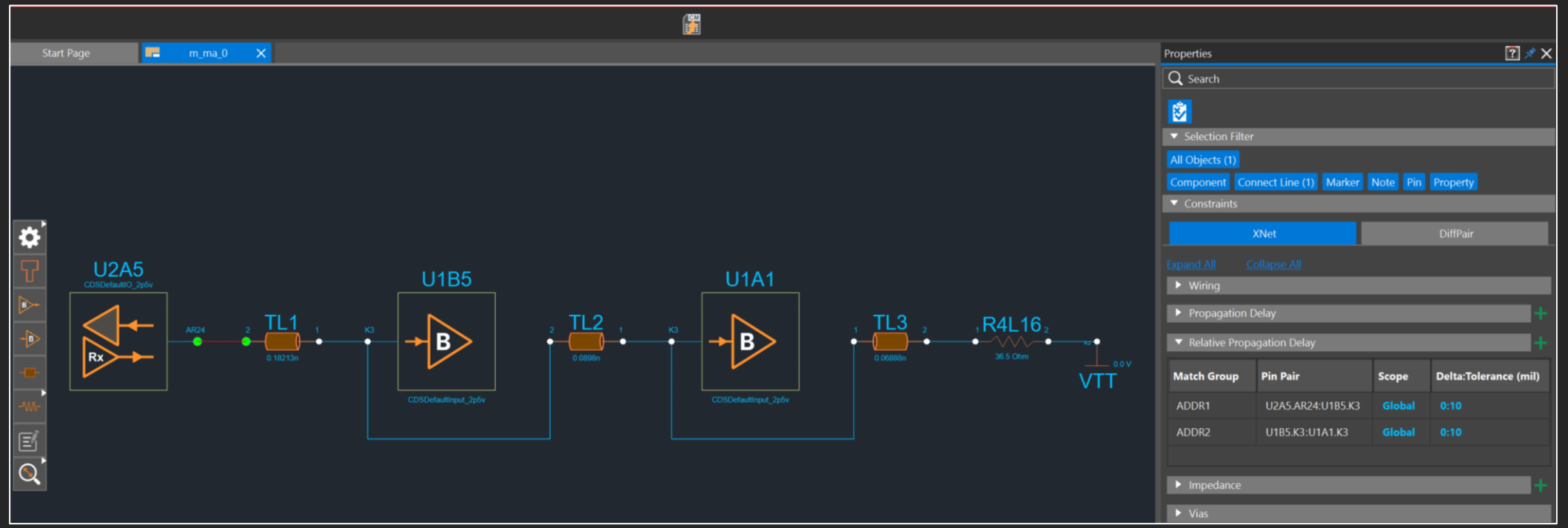
Topology Workbench – Topology-based Constraints

- Signal Explorer (SigXP) has been used to generate topology-based constraints, but we now have a next-generation topology editor called **Topology Workbench**
  - Topology Workbench offers similar functionality to SigXP, with an improved UI and a simpler use model
  - Re-schedule Net, drive constraints globally across the Net or create Pin Pair based constraints



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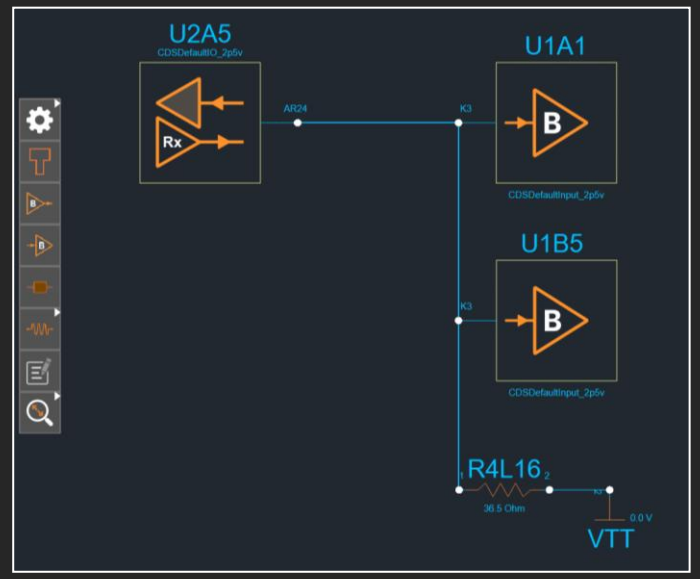
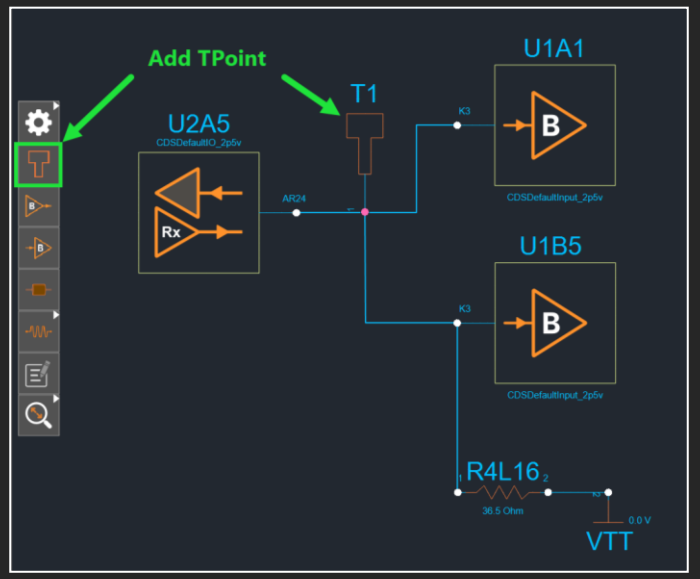
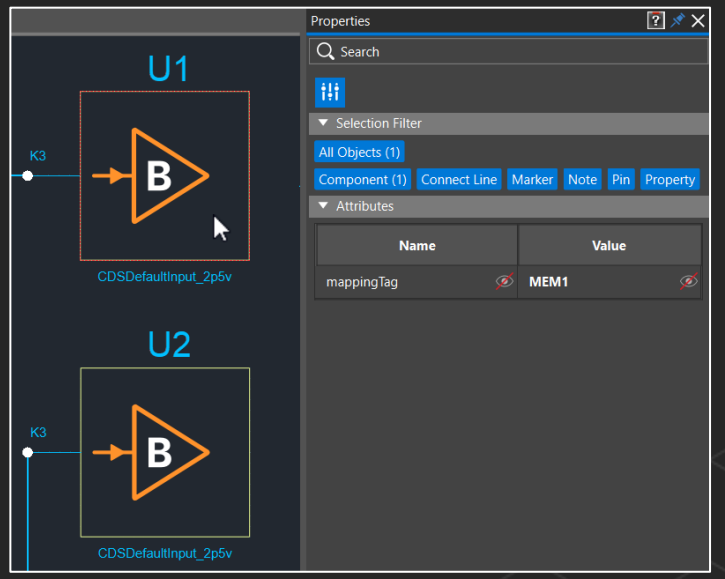
Topology Workbench – Topology-based Constraints

- Ideal Transmission Lines (TL*) are no longer required for Electrical CSet Topologies
  - ***RMB > Delete all Connections*** on canvas will delete all T-Lines so pins can be easily rearranged / reconnected
- New T-Point symbol can be placed to form a branch point to split route to different pins
  - Allows matching rules to be applied from T-Point to each component pin.
- Ambiguous pins, pins with same Pin Use, may not produce correct schedule order when applied
  - Applying a Mapping Tag in Topology and in the design will remove ambiguity resulting in correct routing schedule







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Manufacturing Output

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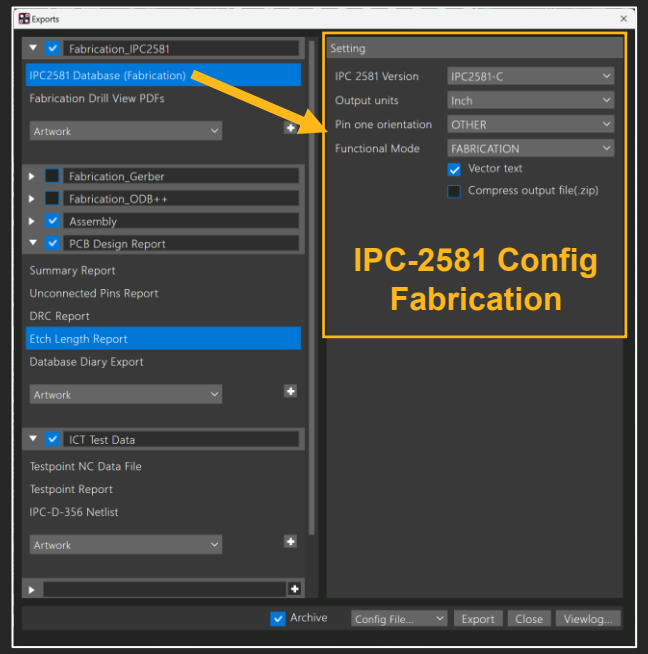
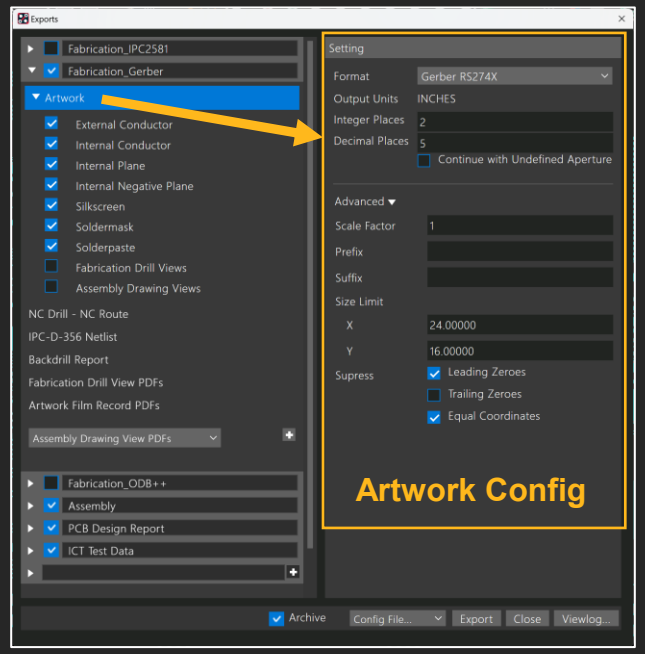
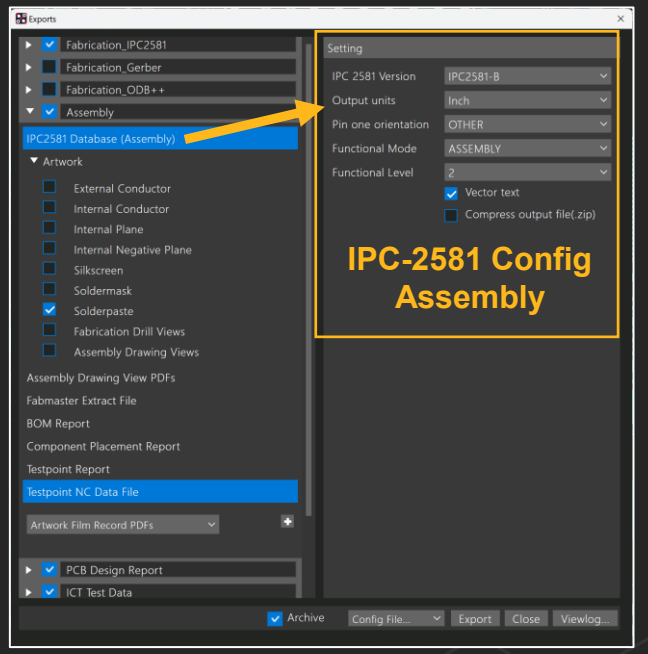
Manufacturing Output – Single-Click Export

- Avoid madness of jumping to different areas of tool to export each data type
  - Customers developed export automation, routine maintenance is a challenge, so functionality must be built-in
- Custom Export configuration used to ensure quick and complete export
  - Out-of-box configuration with standard outputs grouped by manufacturing focus that can be customized
  - Define Export configuration once and use it for all designs for a consistent can complete data export







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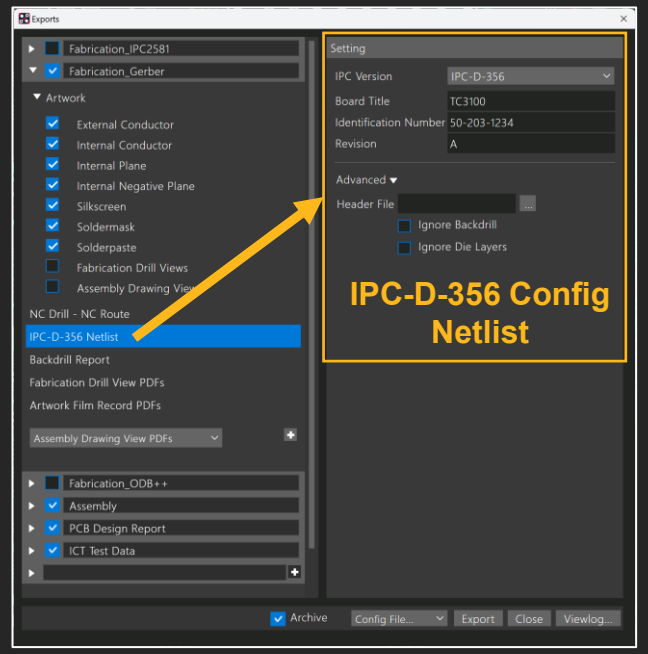
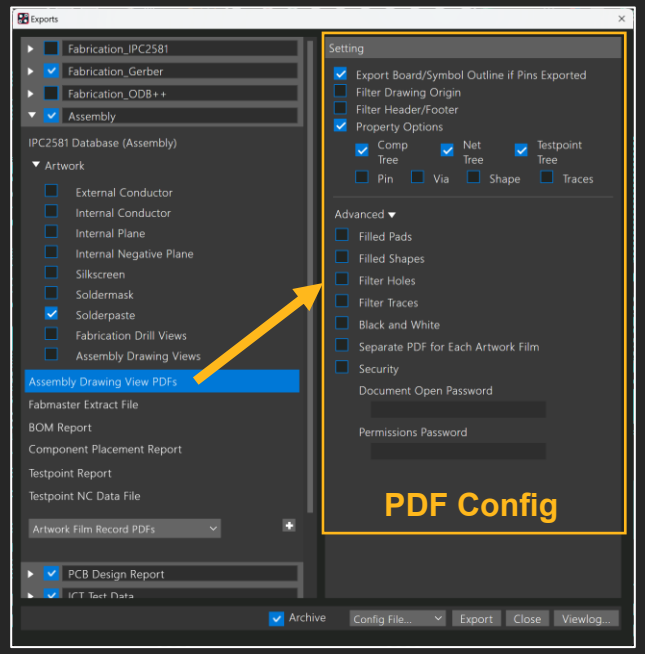
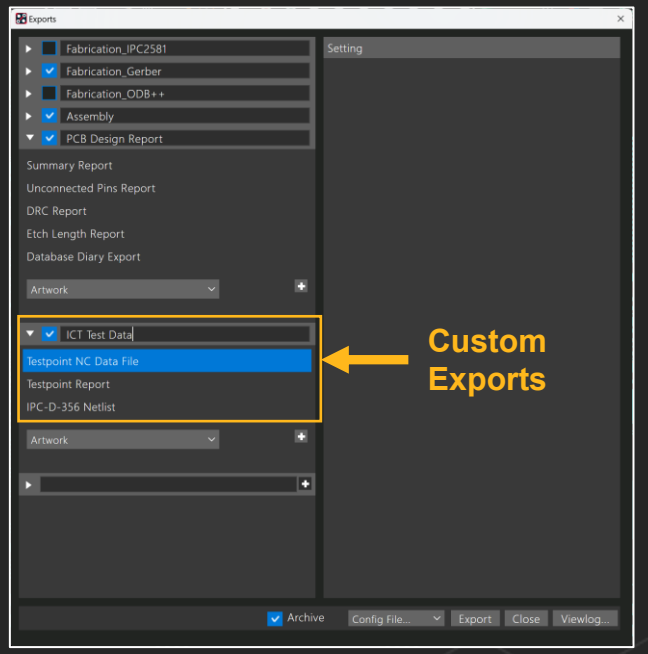
Manufacturing Output – Single-Click Export

- Each export can have its own parameters for quick access through Export form
  - IPC-2581, Artwork, NC Drill, etc.
- Create export groups for each manufacturing resource; no rearrange of output data manually
- Common configuration shared with 24.1 Artwork Film Record auto-generation for a complete and consistent manufacturing data package







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Upcoming Features in 25.1 ISR

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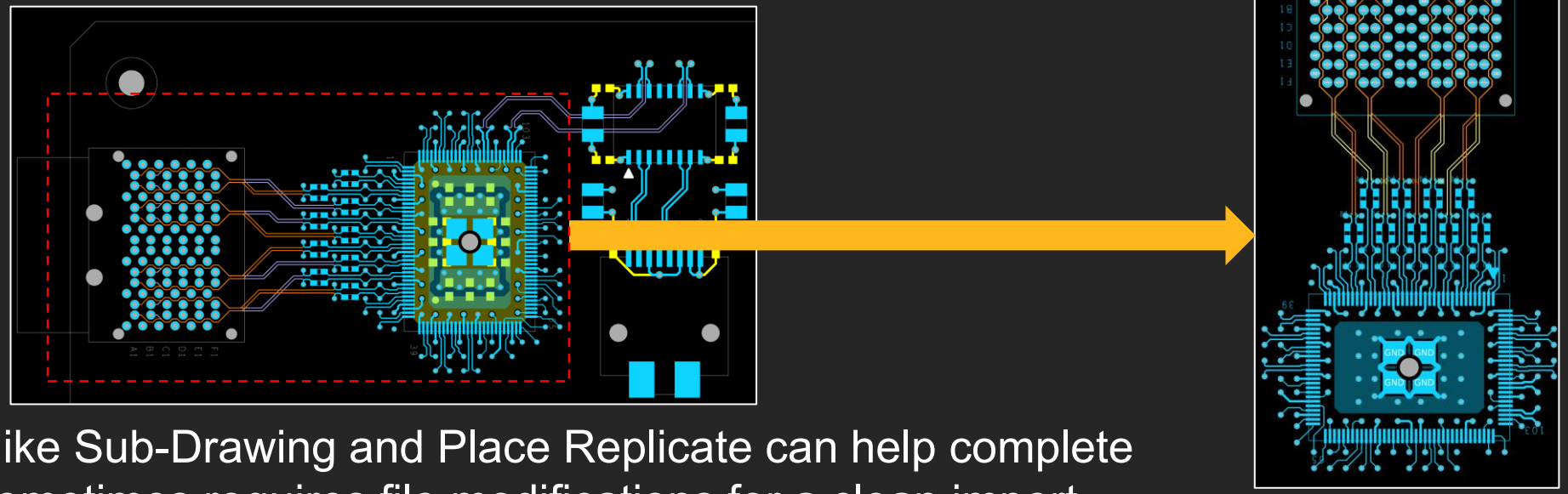
Copy / Paste Layout

- Reuse of sections from a previous layout can be a great time saver
  - Leverage placement and routing from a known good layout



- Functionality like Sub-Drawing and Place Replicate can help complete the task but sometimes requires file modifications for a clean import
- New Copy/Paste Layout allows copy of placement, routing, etc. from one design to another without saving or managing files
  - Open the source design and drag a window ***RMB > Copy Layout***
  - Open the destination design and ***RMB > Paste Layout***

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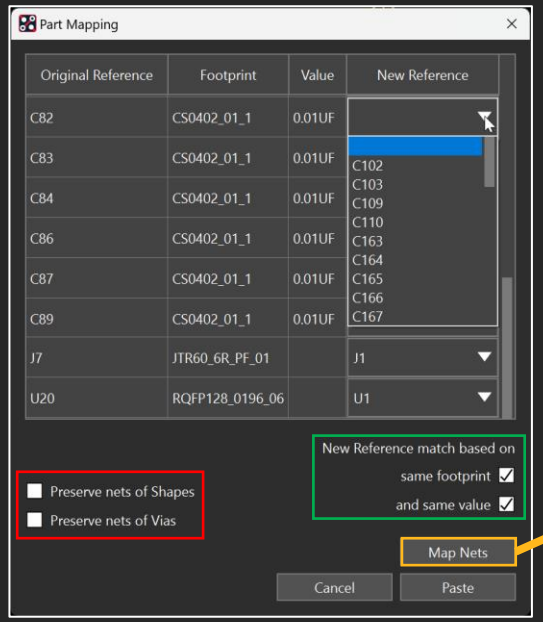
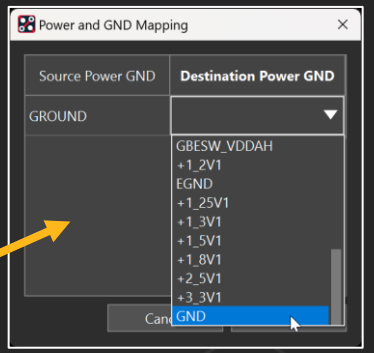
Copy / Paste Layout

- Pre-select objects from source design than copy data into buffer using ***RMB > Copy Layout*** or ***Edit > Copy Layout***
- Paste Layout into destination design using ***RMB > Paste Layout*** will present a Layer Mapping dialog to map layers between source–destination
  - Move layers one at a time or drag select multiple layers to move as a set
  - Source stack-up cannot have more layers than destination
- Mapping dialog to link source–destination Ref Des
  - New reference filtered by Footprint and/or Component Value
- Power and Ground Net Name mapping dialog allows mapping nets between source–designation
- Options to Preserve Net Names on Shapes and Vias





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