Carolina PCB Exposition

November 8th, 2023 Raleigh, NC

Optimizing Parasitic Capacitances in Power Substrates to Lower Common Interference

Presenter: Dr. Douglas C. Hopkins, DCHopkins@ncsu.edu
Co-Author: Sourish Sinha, SSinha5@ncsu.edu
NC State University

The Laboratory for Packaging Research in Electronic Energy Systems (PREES)

PROVIDING "CIRCUIT DESIGN BEYOND THE SCHEMATIC"





Floating and Fixed potential Shielding method on Low Impedance Power Modules

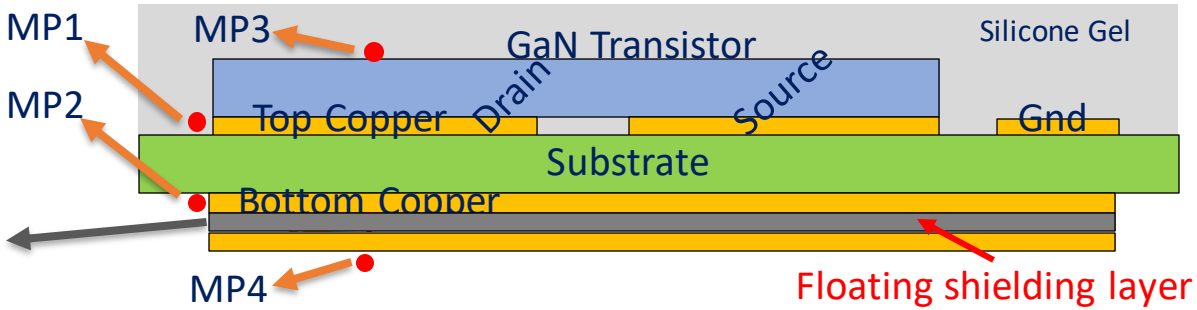
A case for Near Field Low Impedance Shielding Technique

ssinha5@ncsu.edu, dchopkins@ncsu.edu

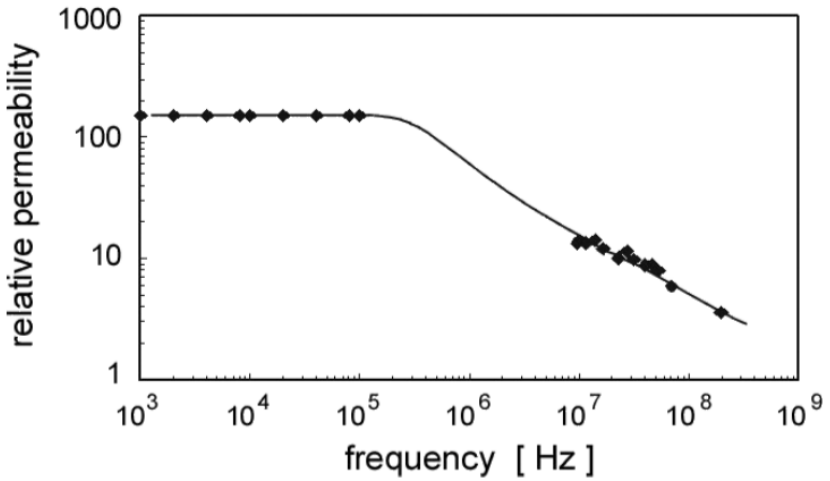
Novel Integrated Magnetic Field shielding in Power Module

Cu is non-ferromagnetic material: High-Freq. shielding (>100MHz)

Ferromagnetic material: Low-Freq. magnetic field shielding (<1MHz)



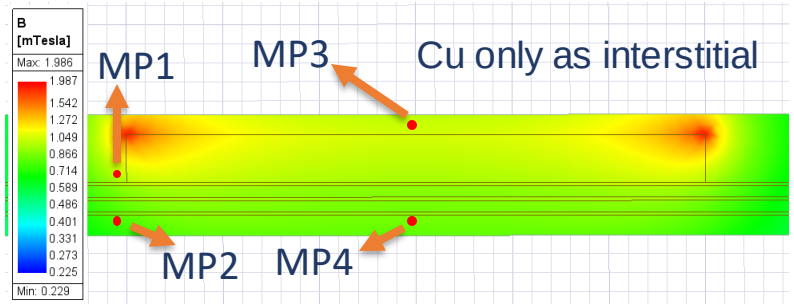
PERMEABILITY	
Steel (SAE 1045)	1000
Stainless Steel (304)	500
Nickel	100
Silver	1
Copper-annealed	1
Gold	1
Aluminum (soft)	1
Aluminum (tempered)	1
Zinc	1
Bras	1
Bronze	1
Tin	1
Lead	1



1. Roland S. TIMSIT, High Speed Electronic Connector Design: A Review of Electrical and Electromagnetic Properties of Passive Contact Elements-Part 1, IEICE Trans. on Electronics, 2008, Vol E91.C, Issue 8, p1178-1191, J-STAGE March 01, 2010.
2. M. Kącki, M. S. Rylko, J. G. Hayes and C. R. Sullivan, "Magnetic material selection for EMI filters," 2017 IEEE Energy Conversion Congress and Expo (ECCE), Cincinnati, OH, USA, 2017, pp. 2350-2356

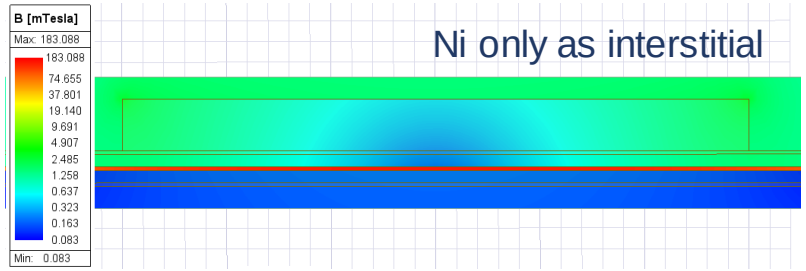
ssinha5@ncsu.edu, dchopkins@ncsu.edu

ANSYS MAXWELL Magnetostatic Simulation



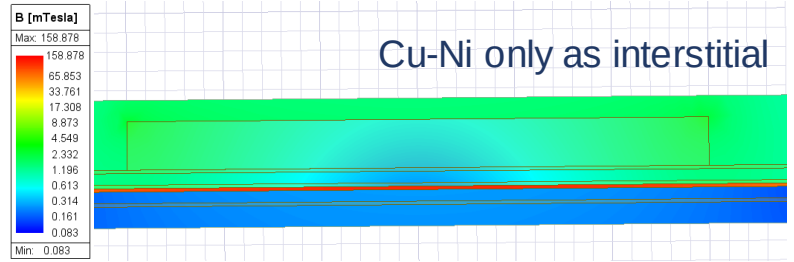
(<50MHz)

Magnetic Flux density (mT)			
MP 1	MP 2	MP 3	MP 4
1.05	0.83	1.18	0.82



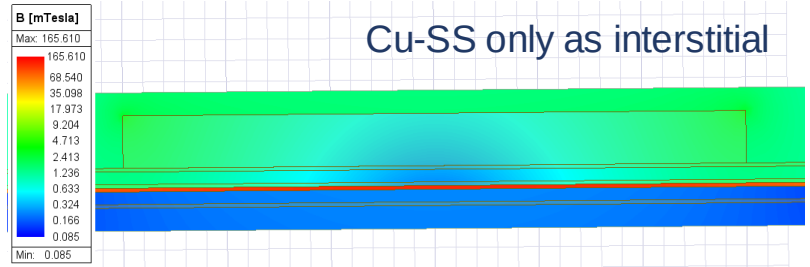
(<300kHz)

Magnetic Flux density (mT)			
MP 1	MP 2	MP 3	MP 4
9.75	0.10	4.91	0.09



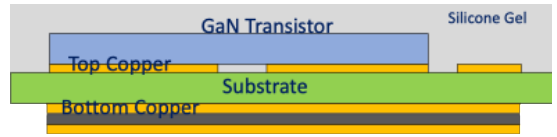
(<300kHz)

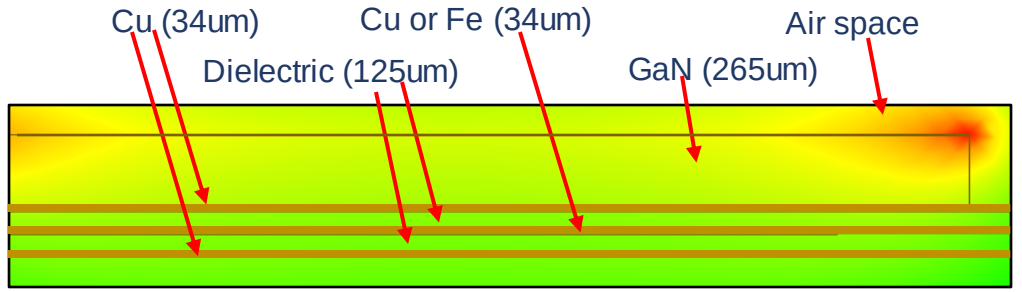
Magnetic Flux density (mT)			
MP 1	MP 2	MP 3	MP 4
9.12	0.24	4.15	0.29

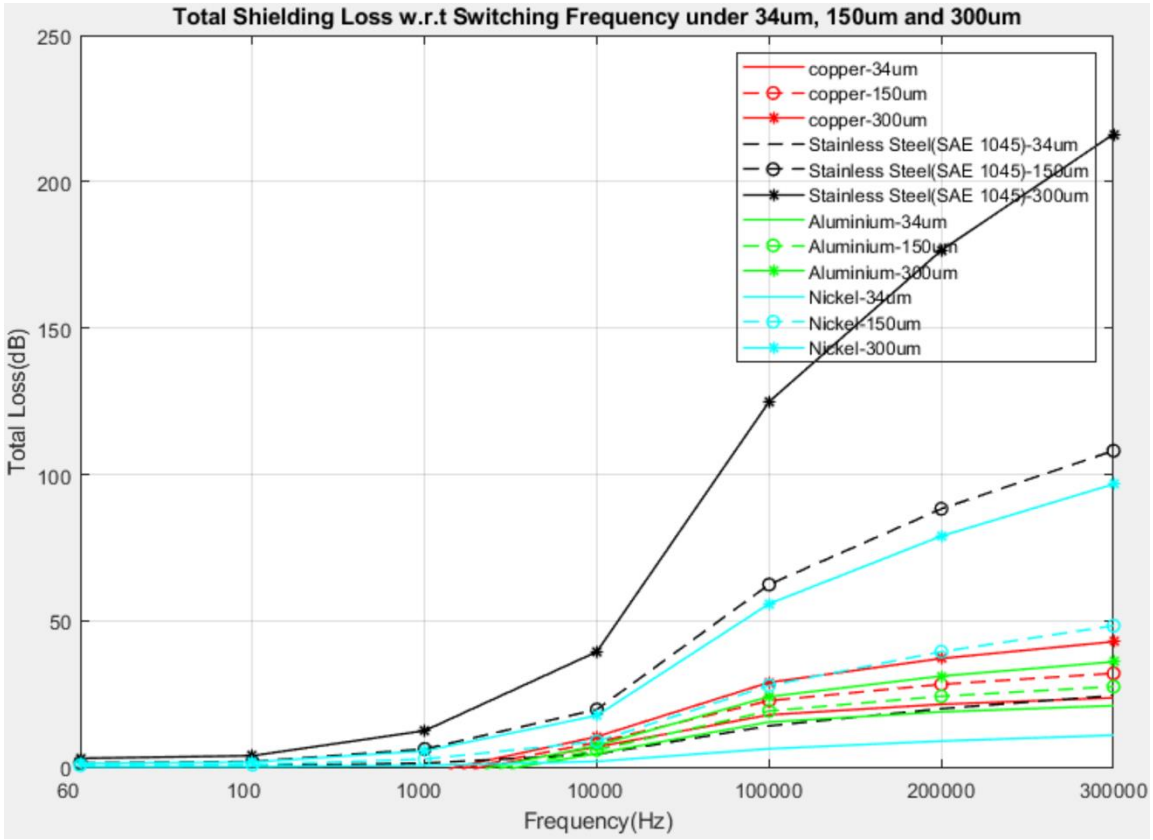


(<300kHz)

Magnetic Flux density (mT)			
MP 1	MP 2	MP 3	MP 4
9.62	0.31	4.72	0.22



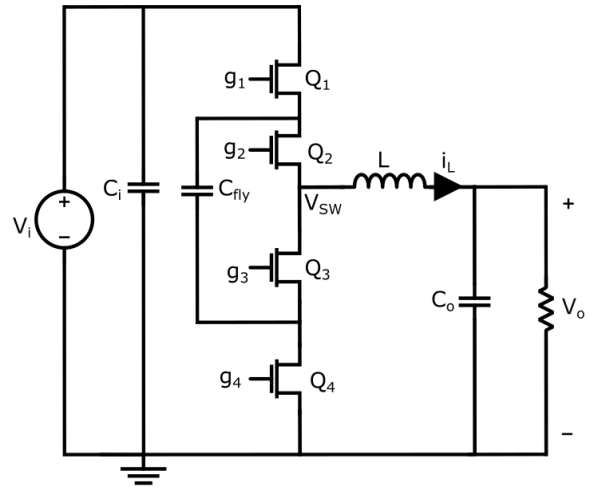




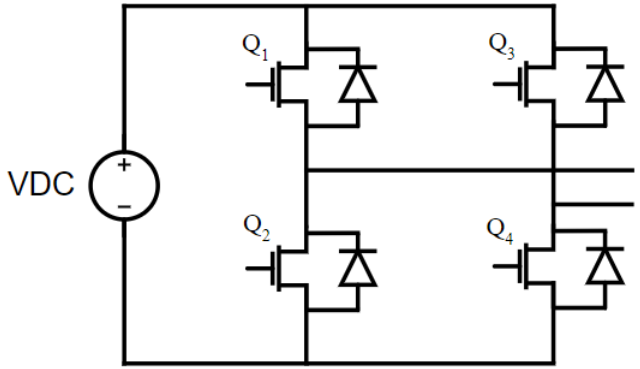
ssinha5@ncsu.edu, dchopkins@ncsu.edu

3D-Stacked Die Power Module
with enhanced EMI and Thermal Performance

Low Parasitics 3D Stacked Die Packaging for:
Single Switch Node Converter (SSNC)
Double Switch Node Converter (DSNC)



Single Switch Node
3-Level Converter



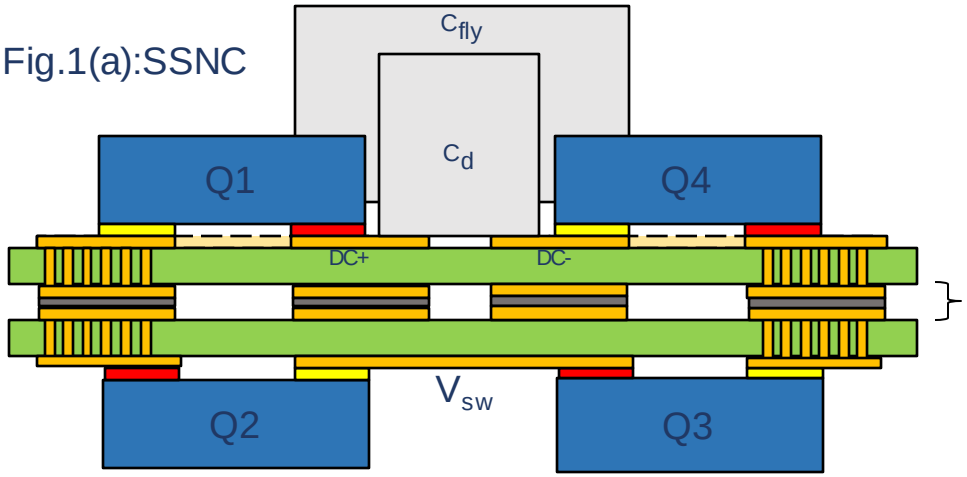
Double Switch Node
2-Level Converter

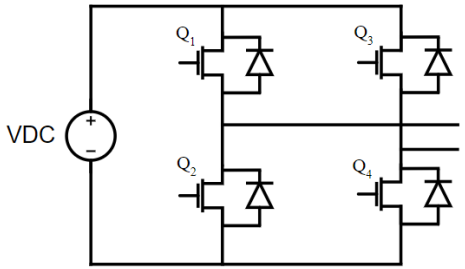
ssinha5@ncsu.edu, dchopkins@ncsu.edu

Magnetic and Electric Field Shielding for Sgl and Dbl Sw. Node Conv.

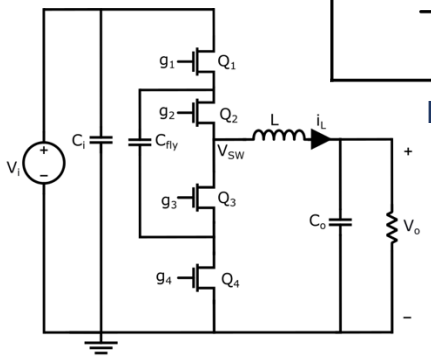
Combined Cu and Ferromagnetic materials provide electrostatic and electromagnetic shielding

Fig.1(a):SSNC





Double Switch Node Converter



Single Switch Node Converter

"Advanced Double-Sided Modules"

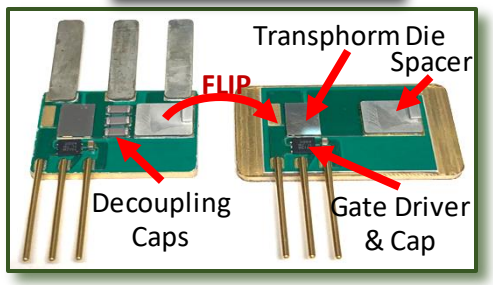


Fig.2(a):DSNC

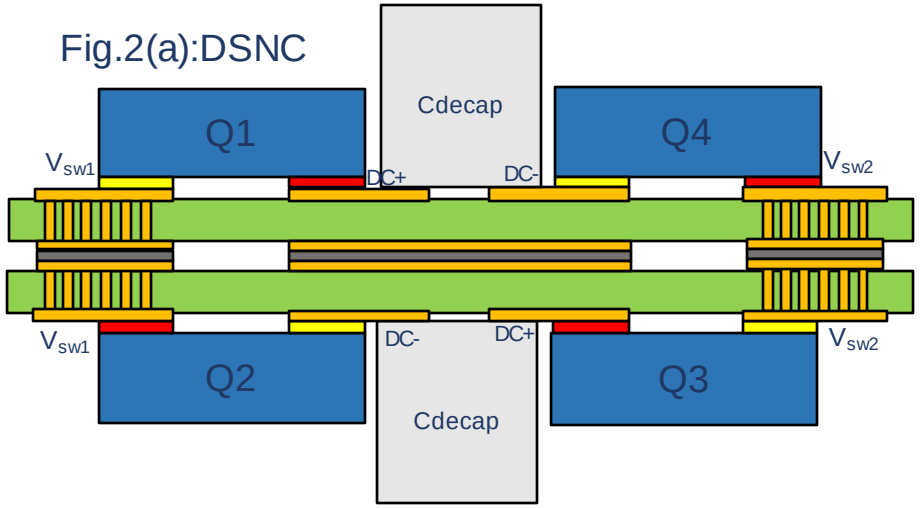
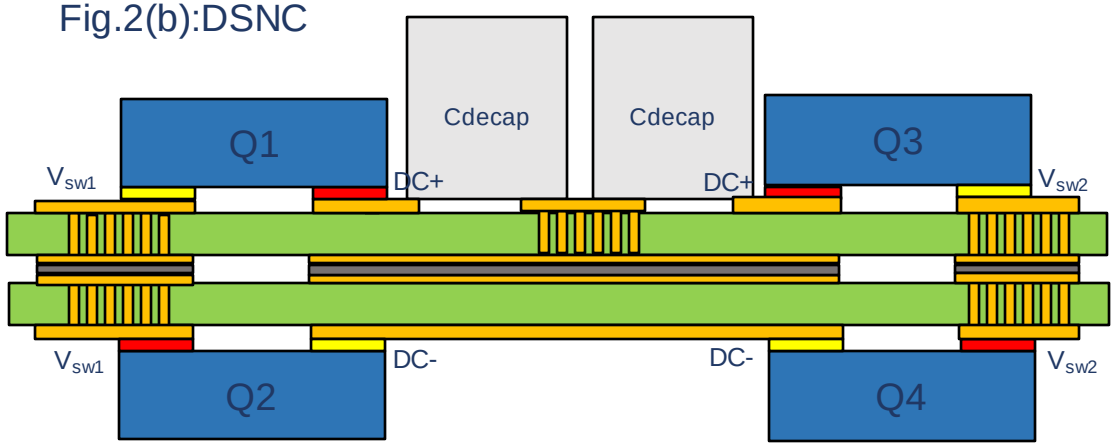


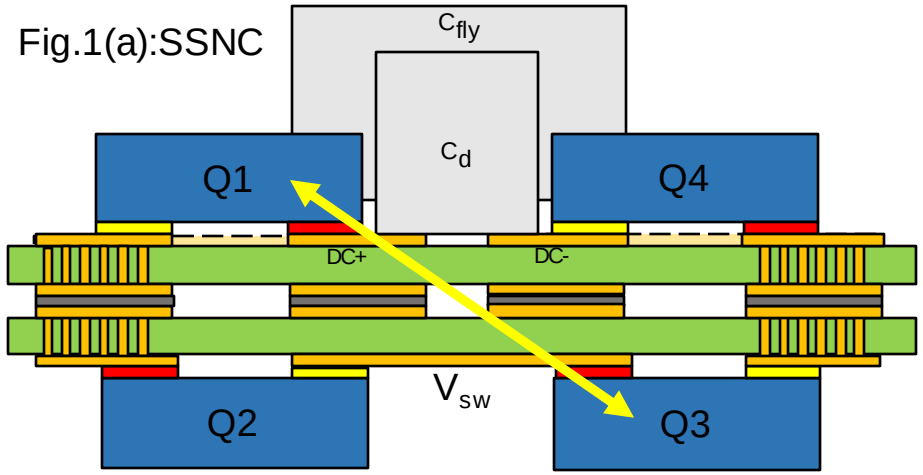
Fig.2(b):DSNC

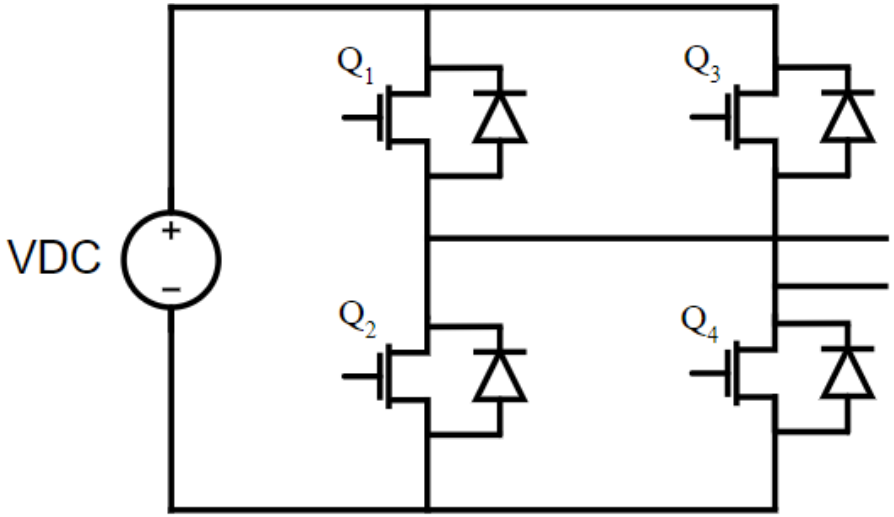


ssinha5@ncsu.edu, dchopkins@ncsu.edu

Thermal Balancing with Layout

Fig.1(a):SSNC

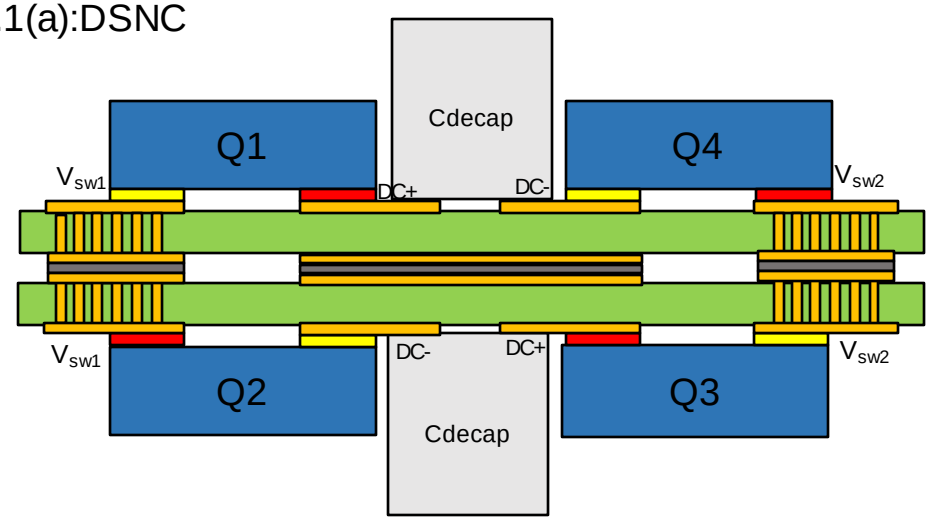




In double-sided power packaging it is critical that die junction temperature be limited to ≤125°C (or ≤150°C for WBG)

Placing dies diagonally that have the highest duty cycle of operation balances the thermal loading on the package and helps in mechanically balancing large stresses.

Fig.1(a):DSNC



ssinha5@ncsu.edu, dchopkins@ncsu.edu

Modifications to Minimize RMS and Peak CM Currents Through Capacitance Optimization

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Known Layout Modifications for Capacitance Optimization

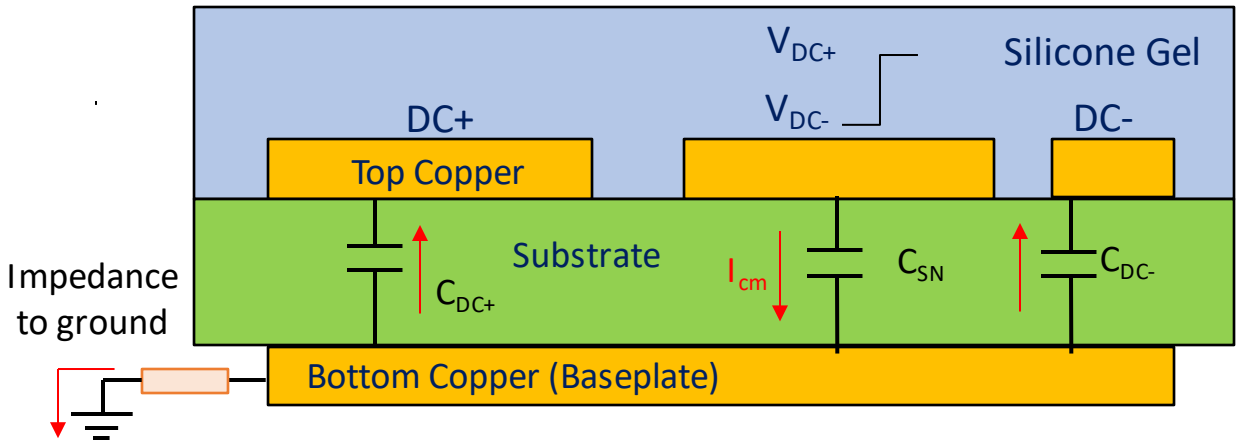
Both [1-2] suggest that C_{DC+} & C_{DC-} (DC+ & DC- power supply trace parasitic capacitances) should have a higher value than Switching Node parasitic capacitance, C_{SN}, to reduce CM current.

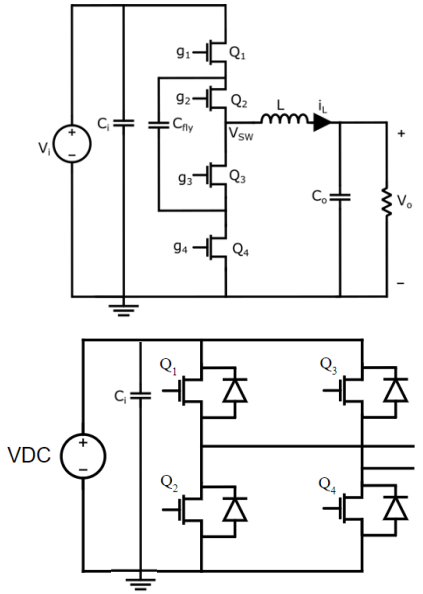
- This recirculates a portion of baseplate current back into the module.

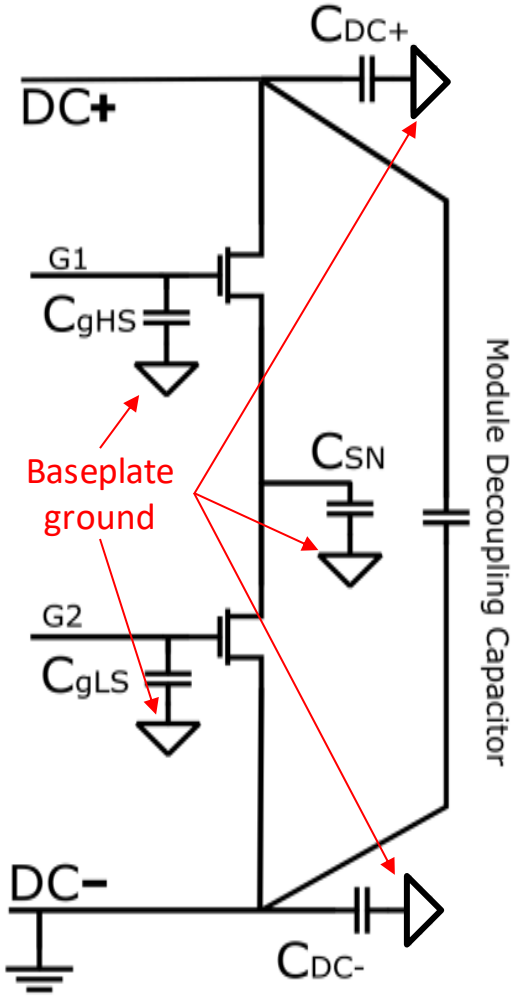
HOWEVER, this is valid when each ratio of $C_{DC+} : C_{SN}$ and $C_{DC-} : C_{SN}$ >1

The author (SSS) found that the increasing ratios do not show a monotonically decreasing trend to minimize RMS and peak CM currents.

- A frequency domain approach to optimization of capacitance distribution is used for advanced EMI improvement.







1. H. Lee, "Design and demonstration of SiC 3D stacked power module with superior electrical parasitics and thermal performances," in PhD Thesis, 2020.
2. A. Domurat-Linde and E. Hoene, "Analysis and Reduction of Radiated EMI of Power Modules," in 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), pp. 1–6, 2012.
3. N. Christensen, A. B. Jørgensen, D. Dalal, S. D. Sonderskov, S. Bęczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Common mode current mitigation for medium voltage half bridge SiC modules," in 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), pp. P.1–P.8, 2017.

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Optimized Capacitance Distribution: via Time Domain Waveforms

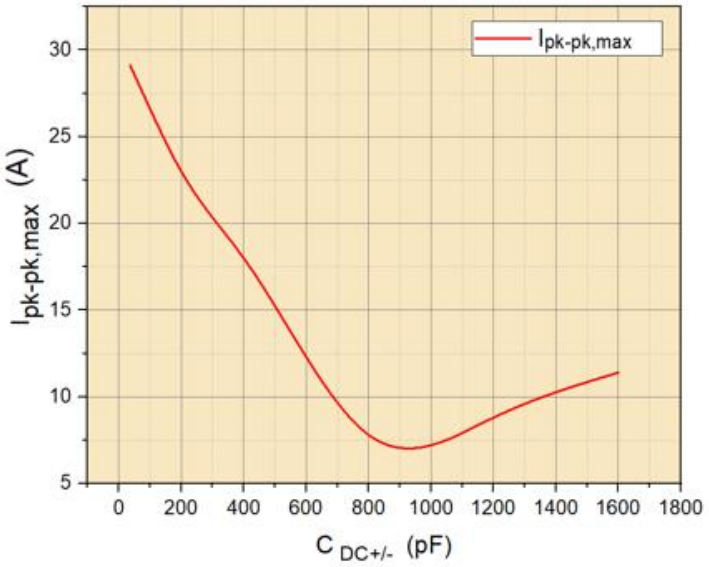
Simulations were performed varying C_{DC+} and C_{DC-} for a fixed C_{SN} as listed in Table 1.

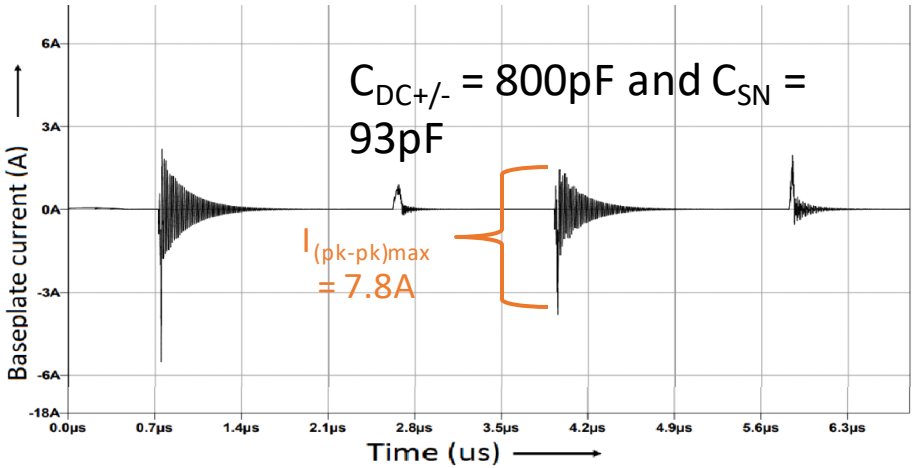
As the values of C_{DC+} and C_{DC-} increase from 37pF to 800pF the peak-to-peak substrate current through C_{SN} decreases from 29.1A to 7.8A.

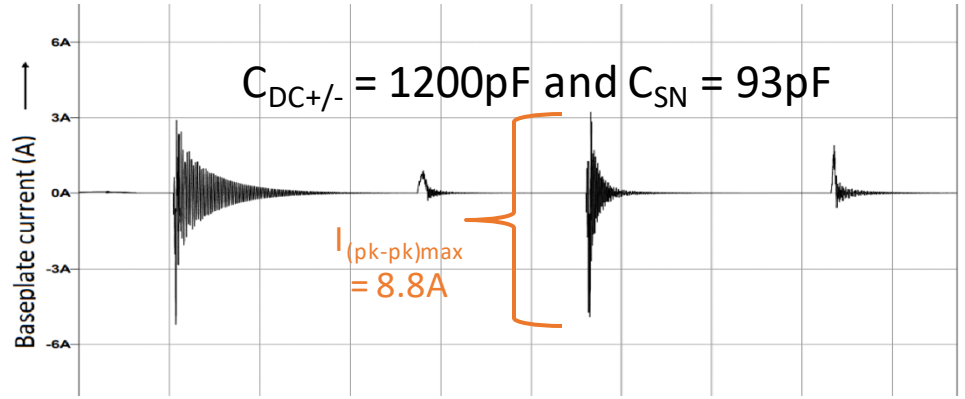
HOWEVER, after C_{DC+} and C_{DC-} cross 800pF the peak-to-peak substrate current increases to 8.8A. Hence, NOT A MONOTONIC change in current.

Table 1. Simulation Values and Resulting Baseplate Currents

PARAMETER	VALUES (pF,A)						
C_{DC+}, C_{DC-}	37	90	200	400	800	1200	1600
C_{SN}	93						
$I_{pk\text{-}pk,max}$ (A)	29.1	27.0	23.0	18.0	7.8	8.8	11.4





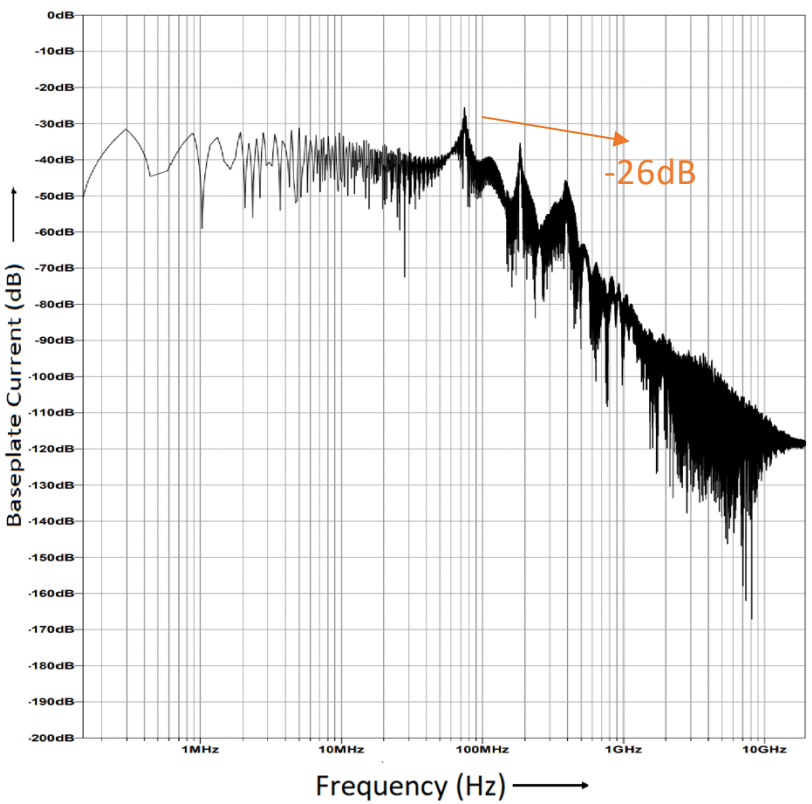


For square-wave switching it is more important to look at the "ENERGY" content of the loss. Hence, FDA is more insightful

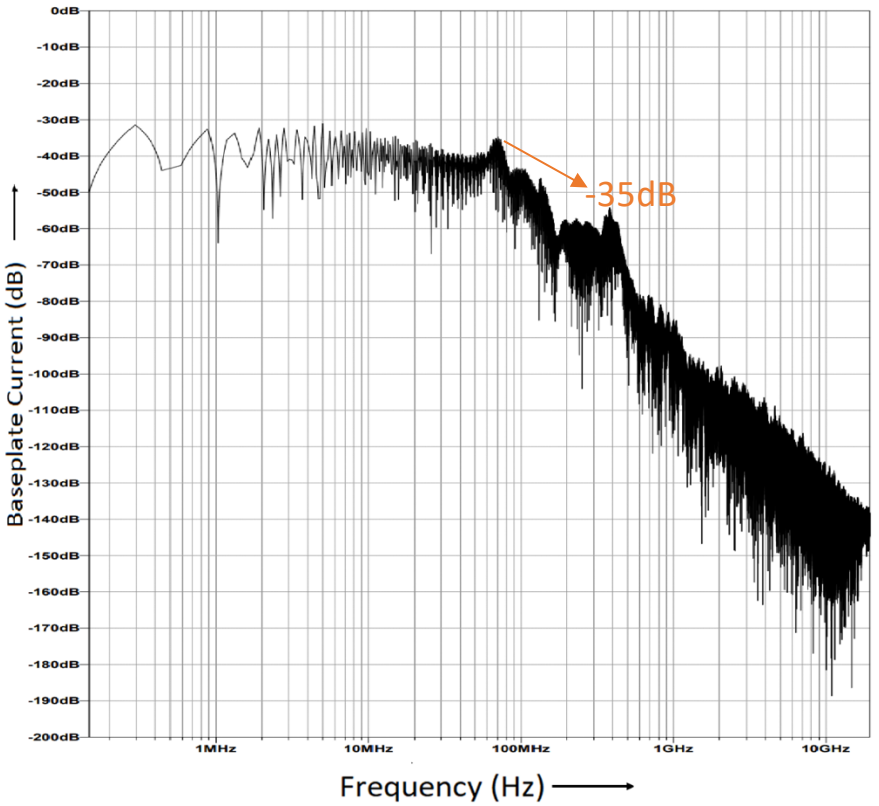
Sinha, Sourish S., Tzu-Hsuan Cheng, and Douglas C. Hopkins. 2023. "Double-Sided Integrated GaN Power Module with Double Pulse Test (DPT) Verification." Journal of Microelectronics and Electronic Packaging 20 (2): 71–81.

ssinha5@ncsu.edu, dchopkins@ncsu.edu

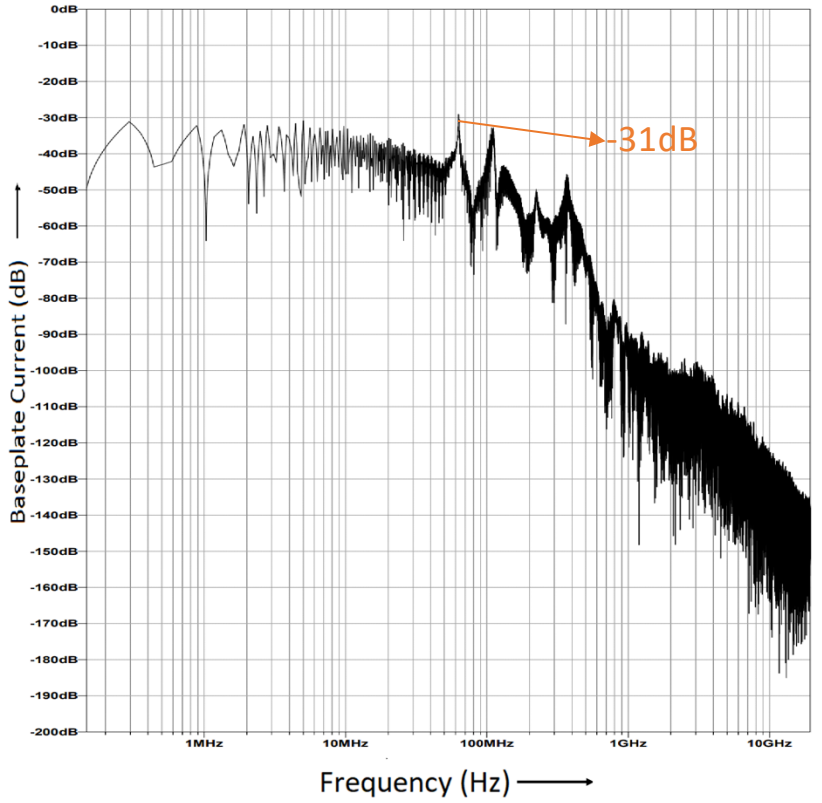
Optimized Capacitance Distribution for C_{SN} = 93pF



$C_{DC+/-}$ = 400pF and C_{SN} = 93pF



$C_{DC+/-}$ = 800pF and C_{SN} = 93pF

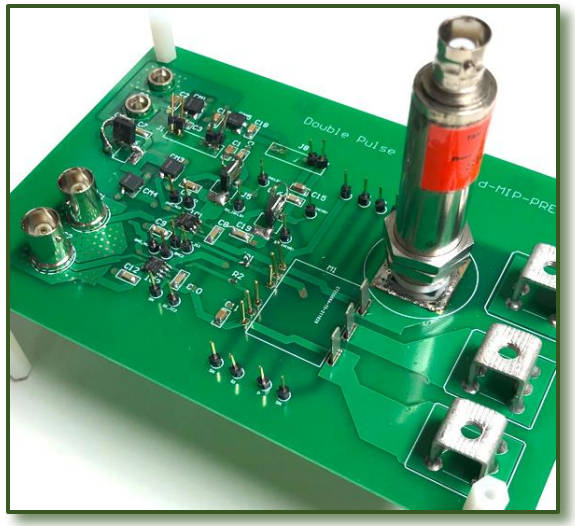


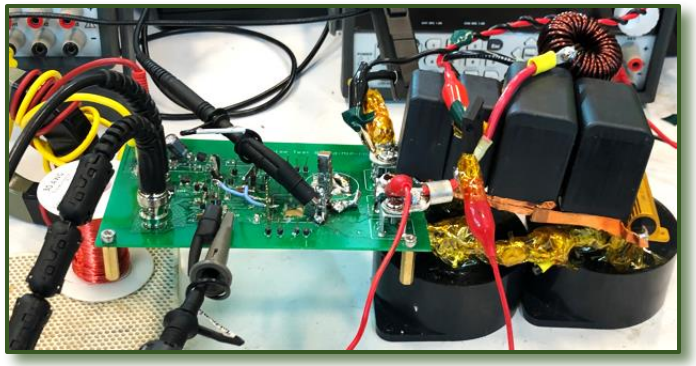
$C_{DC+/-}$ = 1200pF and C_{SN} = 93pF

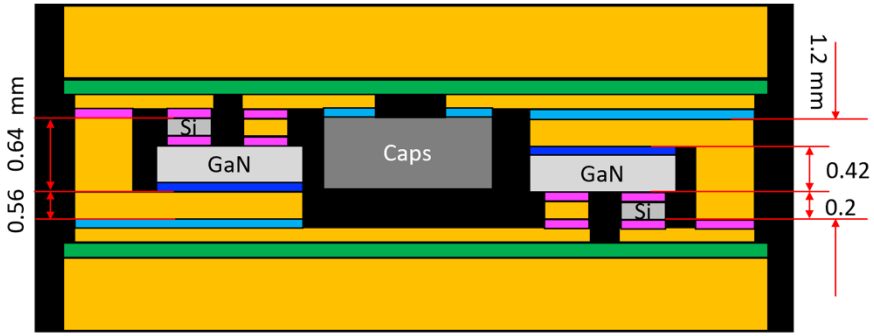
PARAMETER	VALUES (pF; I(dB))			
C_{DC+}, C_{DC-}	37	400	800	1200
C_{SN}	93			
I (dB)	-25	-26	-35	-31

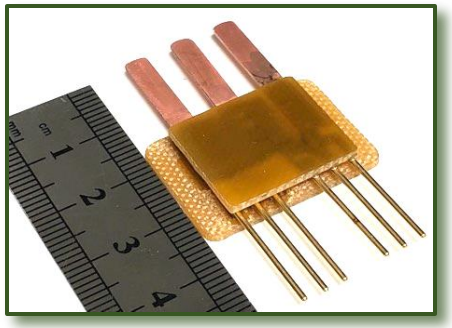
ssinha5@ncsu.edu, dchopkins@ncsu.edu

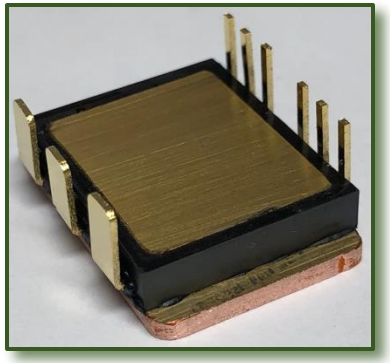
Test Evaluation Board with Module Mount and Fabrication of Module

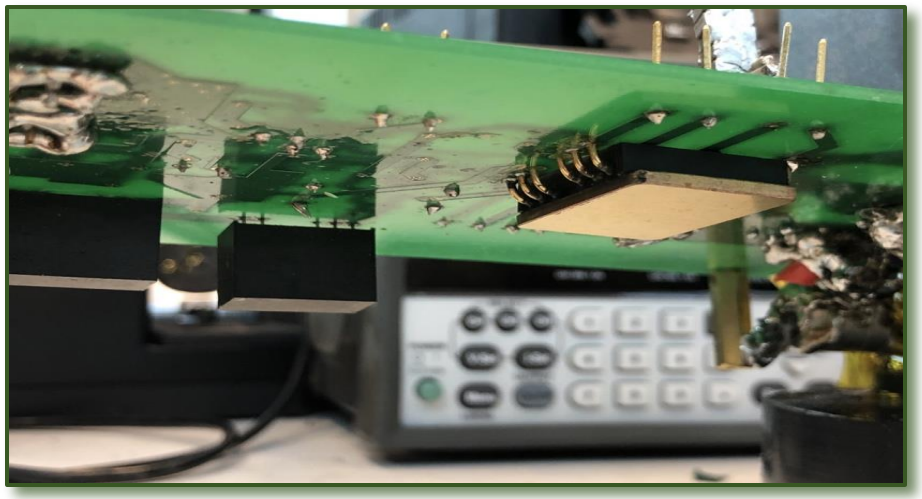


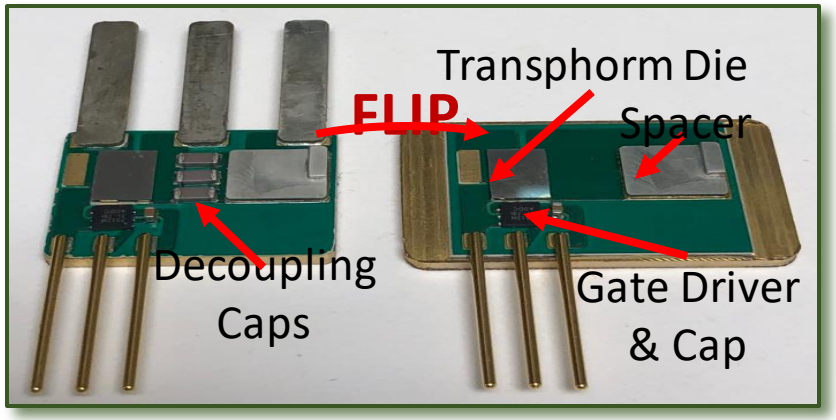










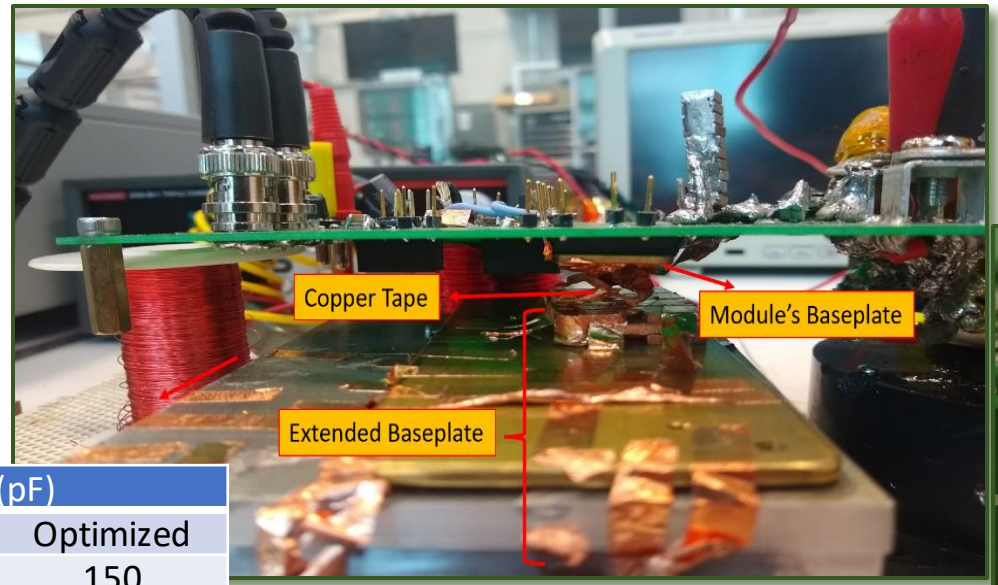


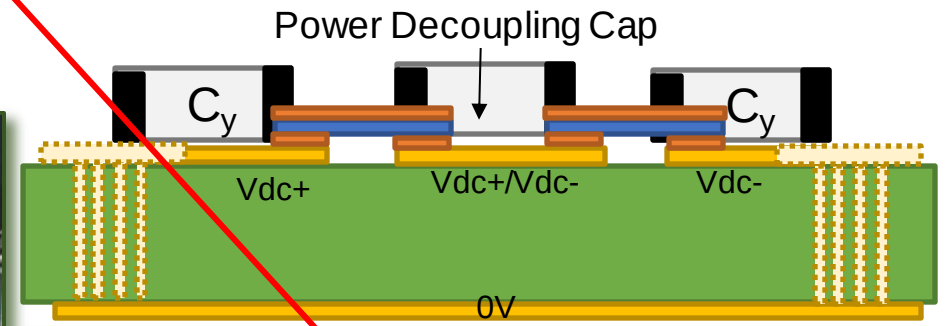
ssinha5@ncsu.edu, dchopkins@ncsu.edu

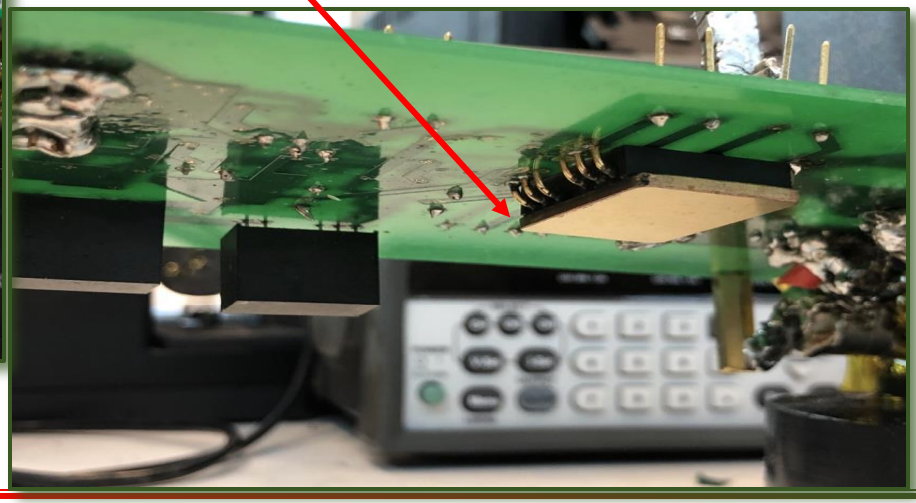
Experimental Results

- Experiments were conducted with two different ½-Bridge Modules (HBM): optimized and nonoptimized.
- Tests were performed with 400V DC bus with HBM mounted as shown.
- Both HBMs have two GaN Systems 650V/80A dies, three power decoupling capacitors of 4.7nF each, two gate drivers and two gate driver capacitors of 1uF.
- Board mounted power decoupling capacitors of 1.5uF in total were placed at the HBM terminals to boost decoupling action as close as possible to the device pads. The modules were run with 0Ω gate resistance which allowed the highest *dv/dt* operation of the GaN switches, and consequently the worst-case CM current to be generated.

Both HBMs use two GaN Systems 650V/80A dies, three power decoupling capacitors of 4.7nF each, two gate drivers and two gate driver capacitors of 1uF.





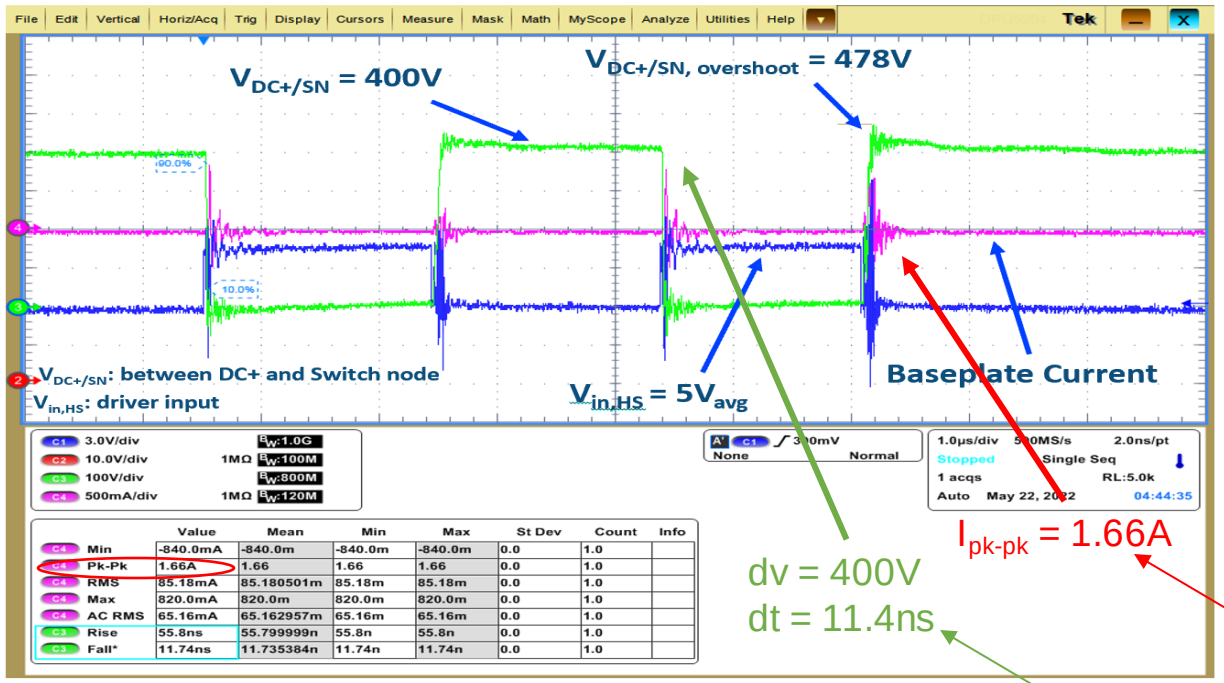


Parasitic Parameter	Values (pF)	
	Non-Optimized	Optimized
C_{DC+}	37	150
C_{DC-}	97	150
C_{SN}	93	

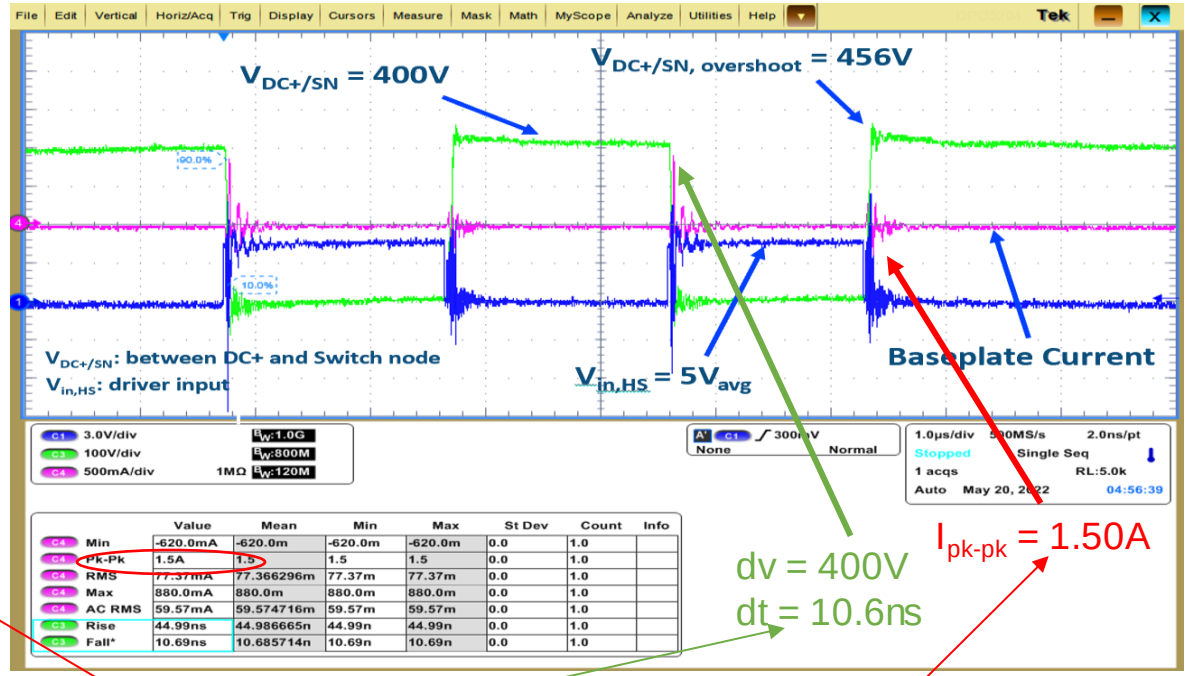
The magnitudes of parasitic capacitance for the non-optimized and optimized module

ssinha5@ncsu.edu, dchopkins@ncsu.edu

GaN Syst IPM: 400V/21A, Baseplate Floating, Substrate Current



(a) Non-Optimized Floating Baseplate



(b) Optimized Floating Baseplate

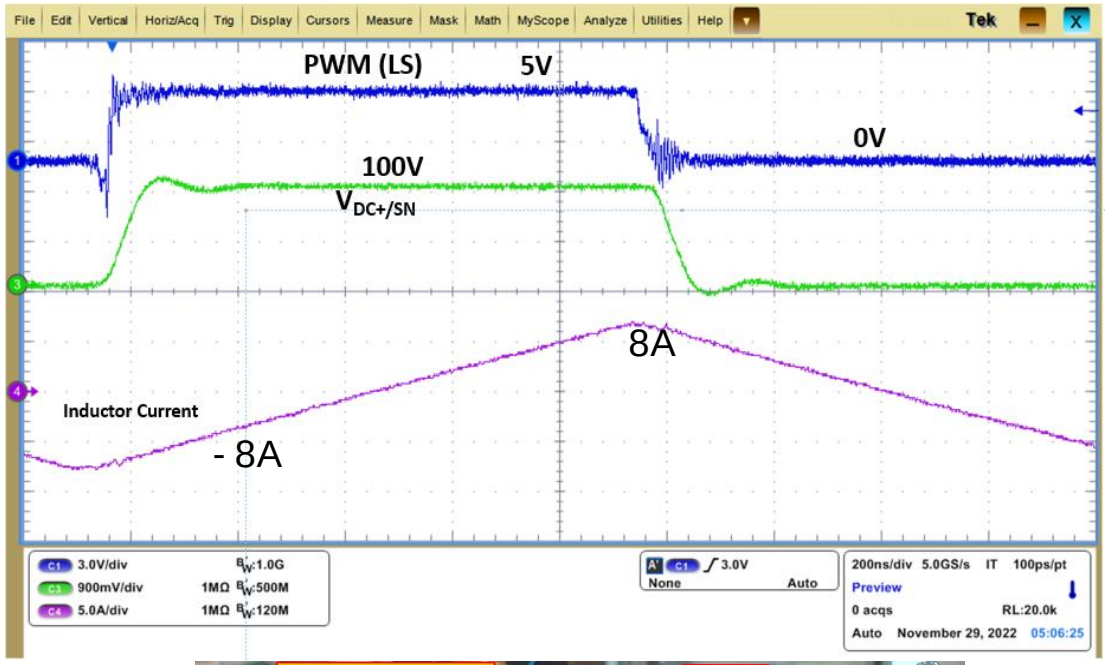
Δ = 0.08A (7% reduction)
dv/dt = 35V/ns

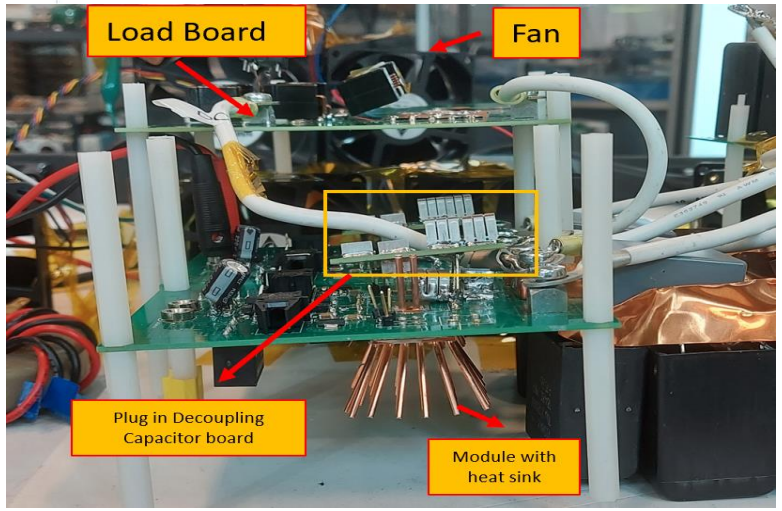
Δ = 0.16A (9.1% reduction)
dv/dt = 38V/ns

- **Sinha, Sourish S.**, Tzu-Hsuan Cheng, and Douglas C. Hopkins. 2023. "Double-Sided Integrated GaN Power Module with Double Pulse Test (DPT) Verification." Journal of Microelectronics and Electronic Packaging 20 (2): 71–81.

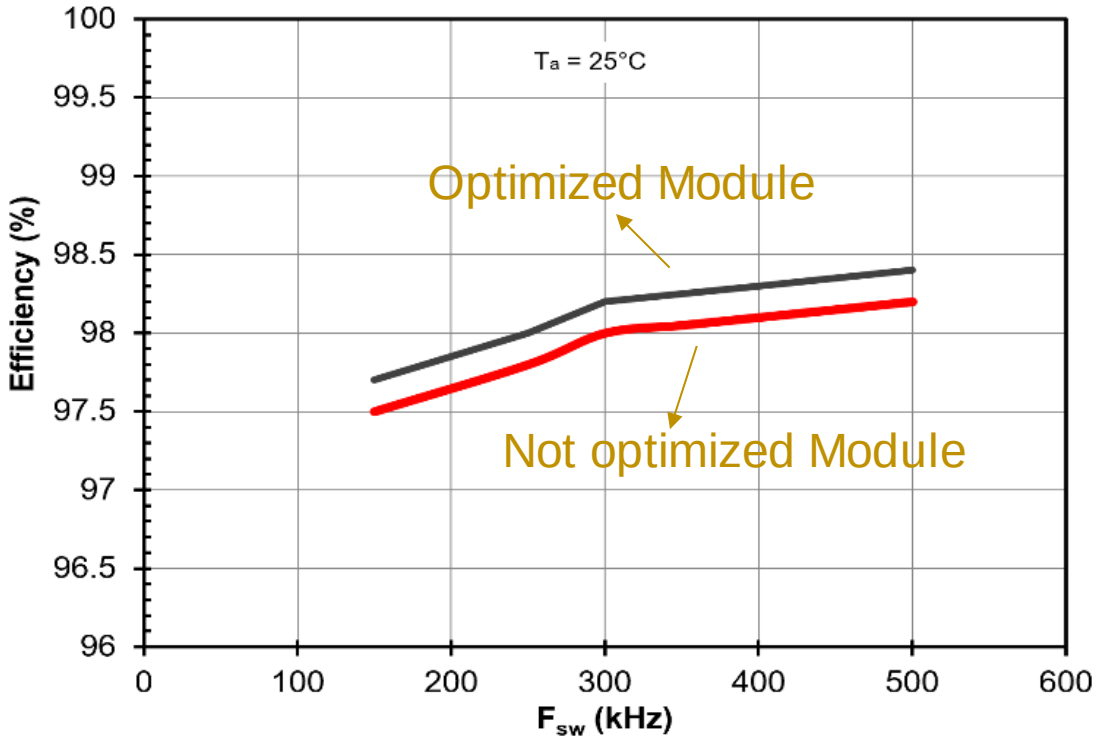
ssinha5@ncsu.edu, dchopkins@ncsu.edu

Full Bridge Converter Application under Zero Voltage Switching: 1kW





Converter Setup



S. S. Sinha, T. -H. Cheng, K. Parmar and D. C. Hopkins, "Advanced GaN IPM for High-Frequency Converter Applications Enabled with Thin-Substrates," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023.

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Sourish Sankar Sinha, ssinha5@ncsu.edu

Laboratory for Packaging Research in Electronic Energy Systems (PREES)

FREEDM Systems Center, North Carolina State University

1791 Varsity Drive, Suite 100; Raleigh, NC 27606-7571

Tele: 919-513-5929, Fax: 919-513-0405

www.prees.org

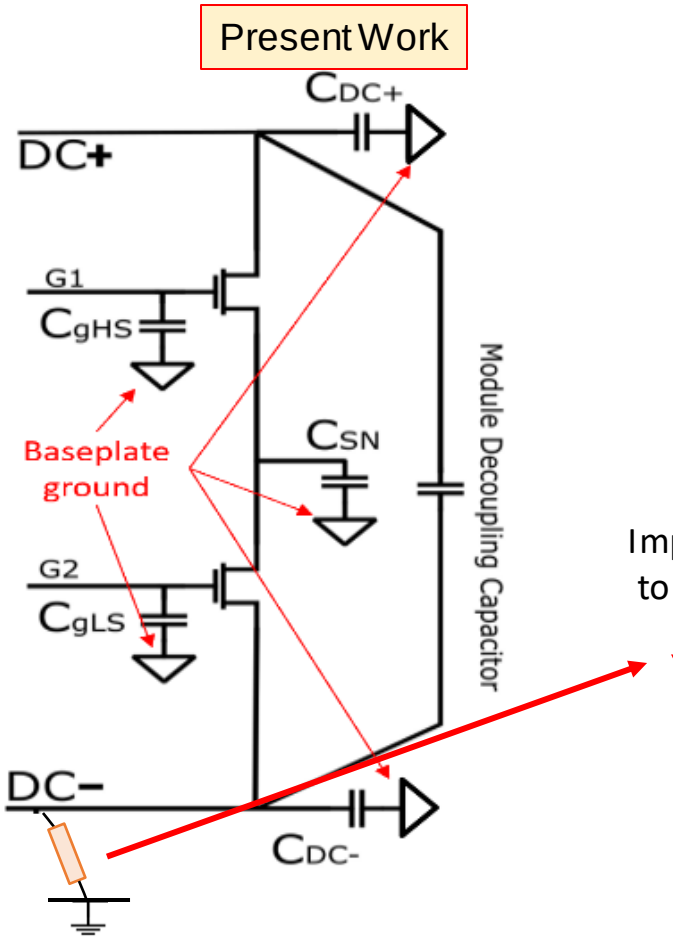
Common Mode Large Signal Model (CM-LSM) of Power Module with Gate Drives & GD Auxiliary Supplies

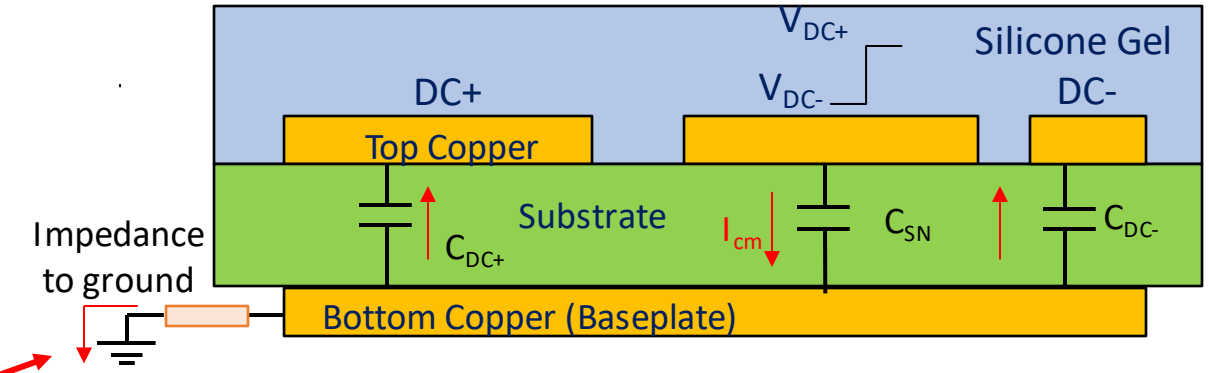
Derivation of Large Signal Model

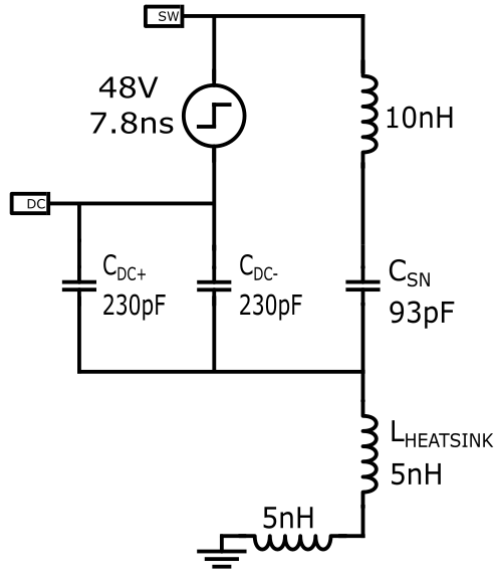
Comparison of results with a converter for direct use of values derived from the model in the converter.

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Simple Large Signal Model for CM current flow

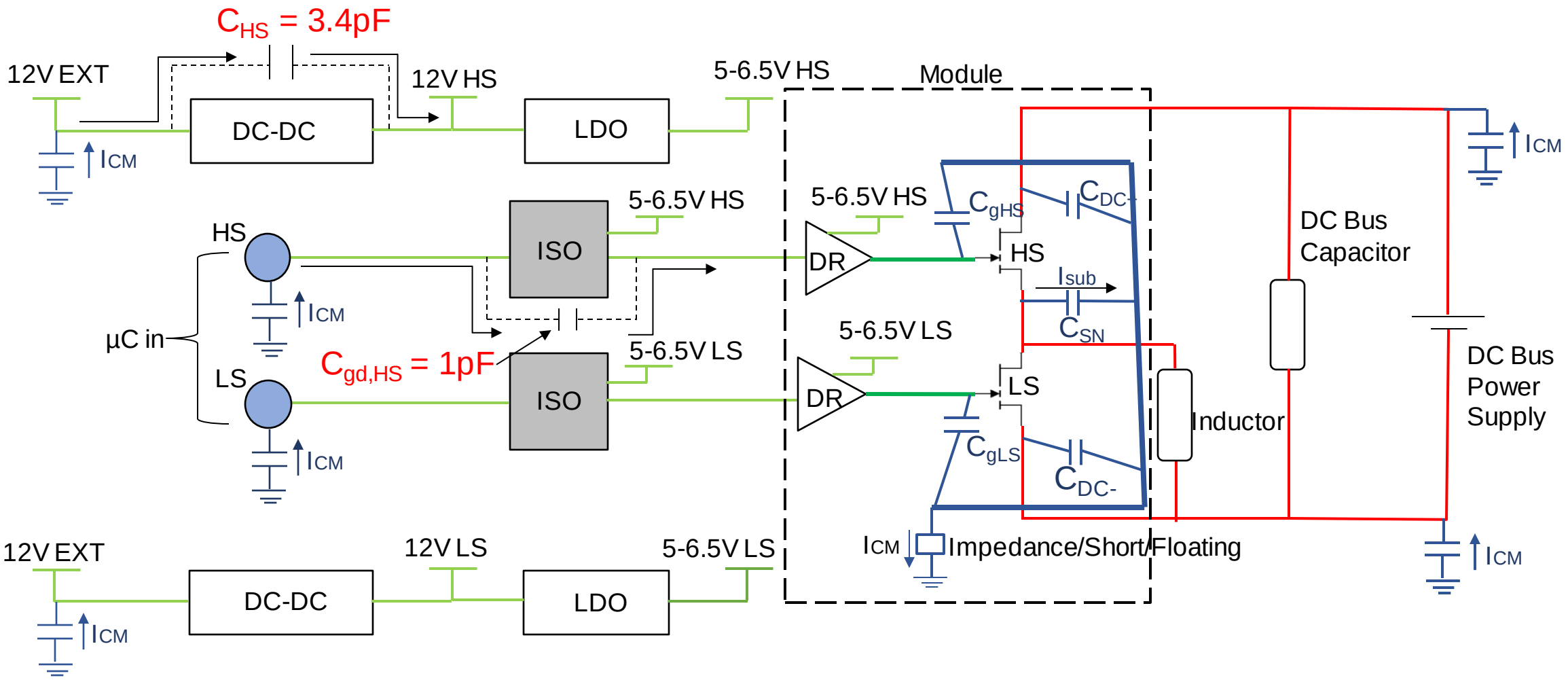






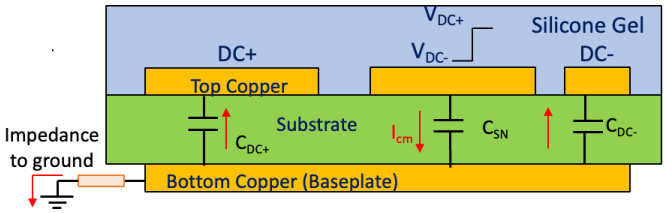
ssinha5@ncsu.edu, dchopkins@ncsu.edu

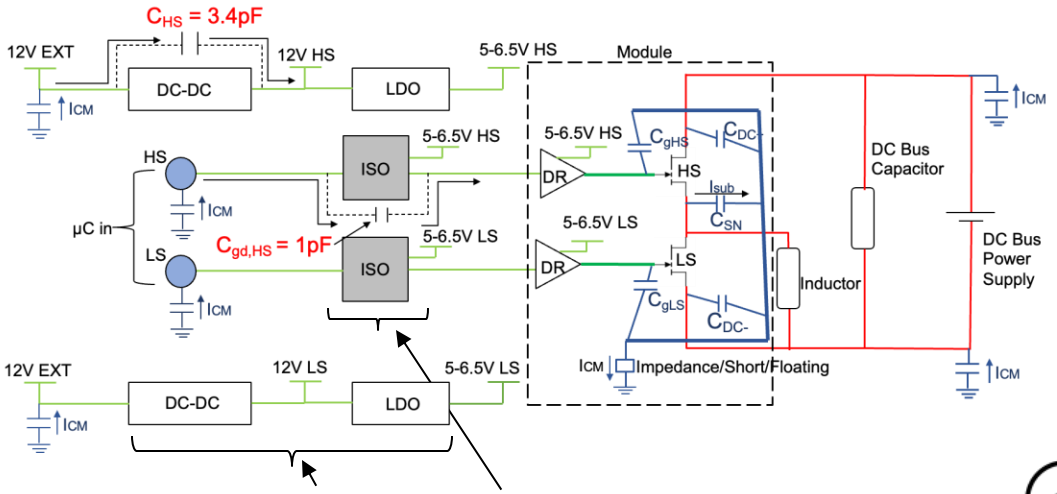
Full Converter Circuit with Gate Drives and Auxiliary Power Supply



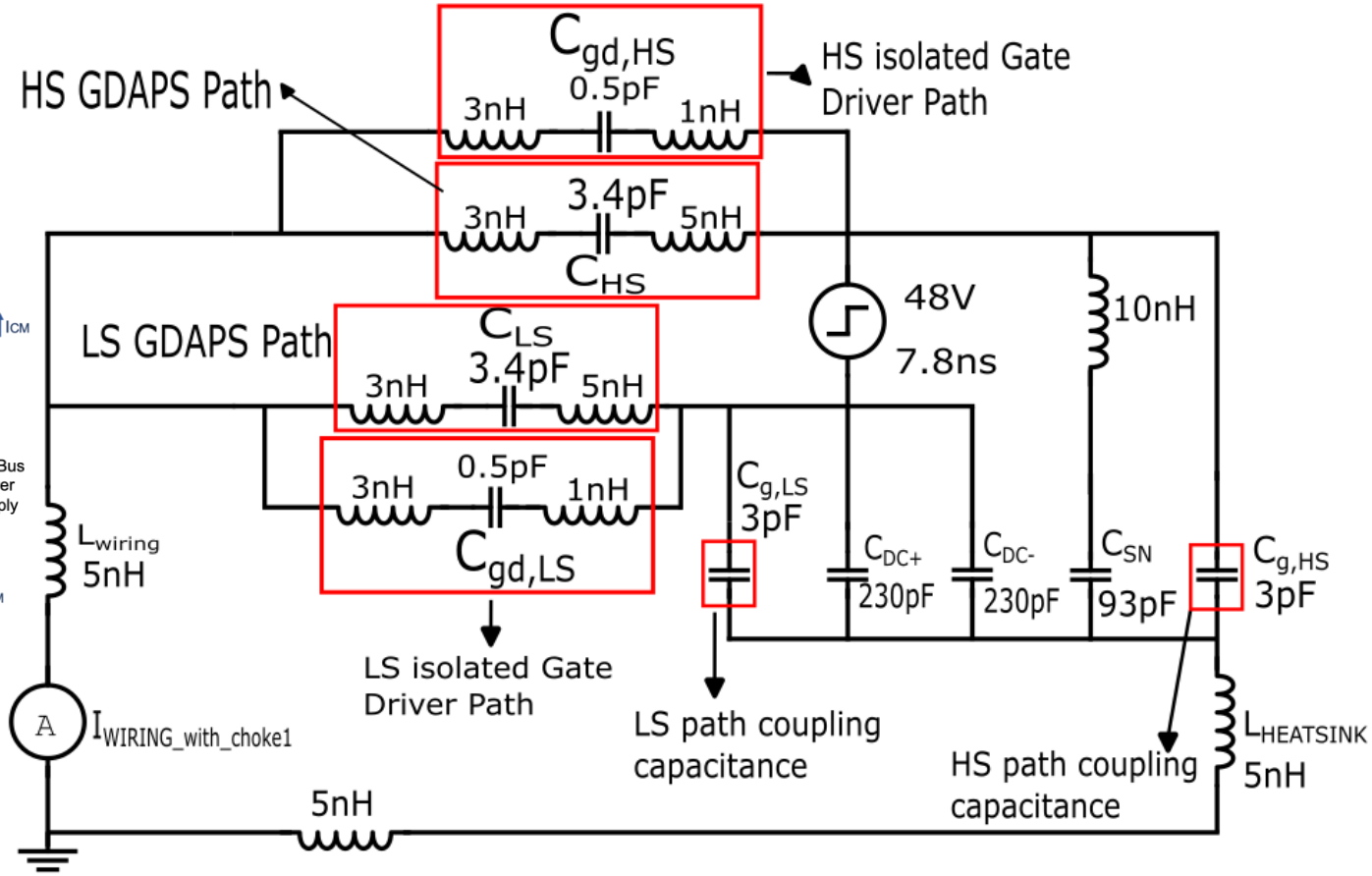
ssinha5@ncsu.edu, dchopkins@ncsu.edu

Full Large Signal Model for CM current flow



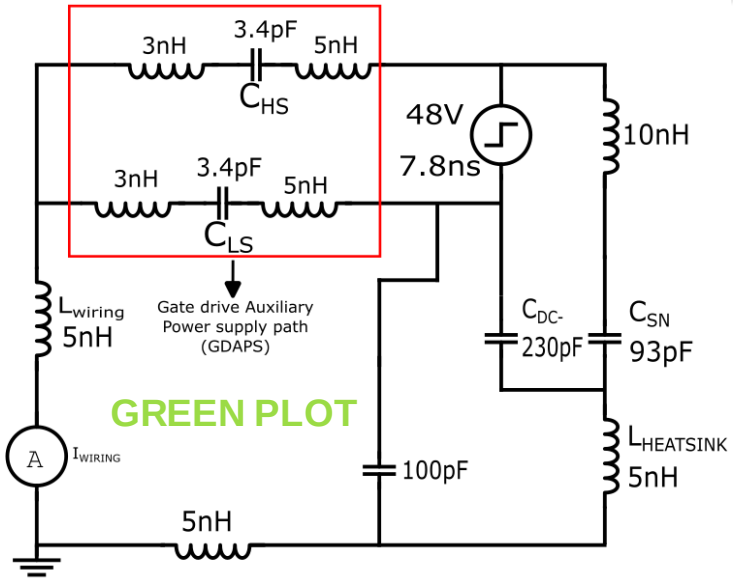


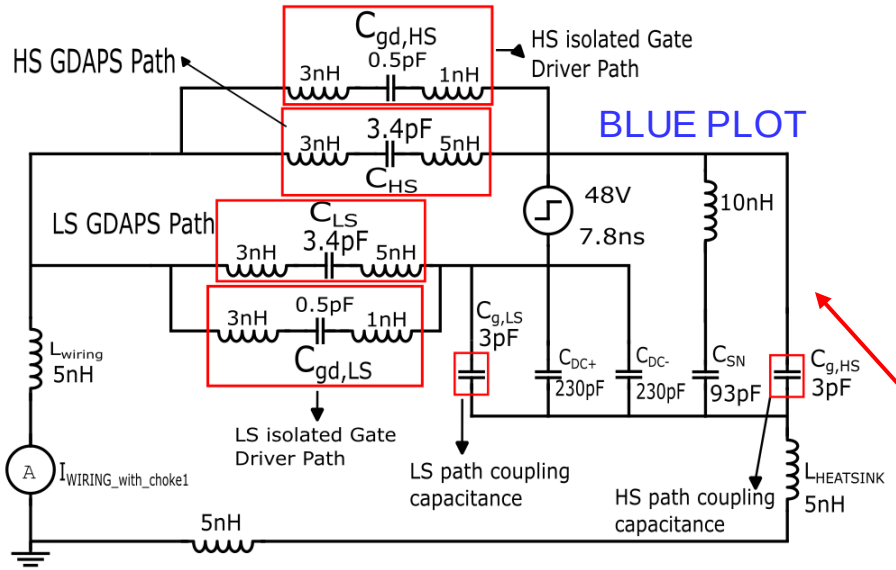
However, CM LSM Model should include the gate drive path too



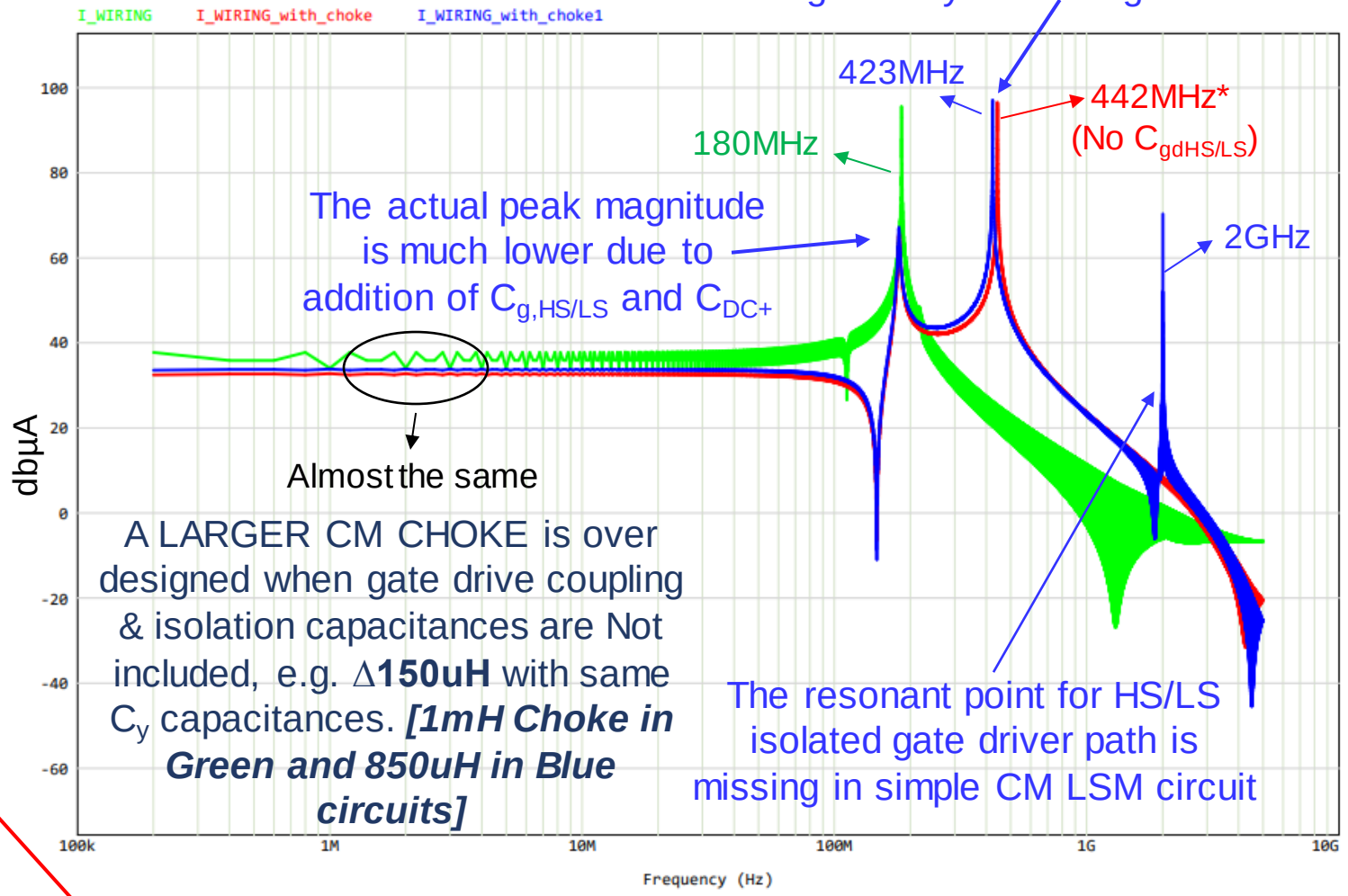
ssinha5@ncsu.edu, dchopkins@ncsu.edu

CM EMI Spectrum (I_{WIRING} Current)





These peak magnitude and frequency will vary too much once $C_{gd,HS/LS}$ starts to dominate. e.g., in case of magnetically isolated gate driver

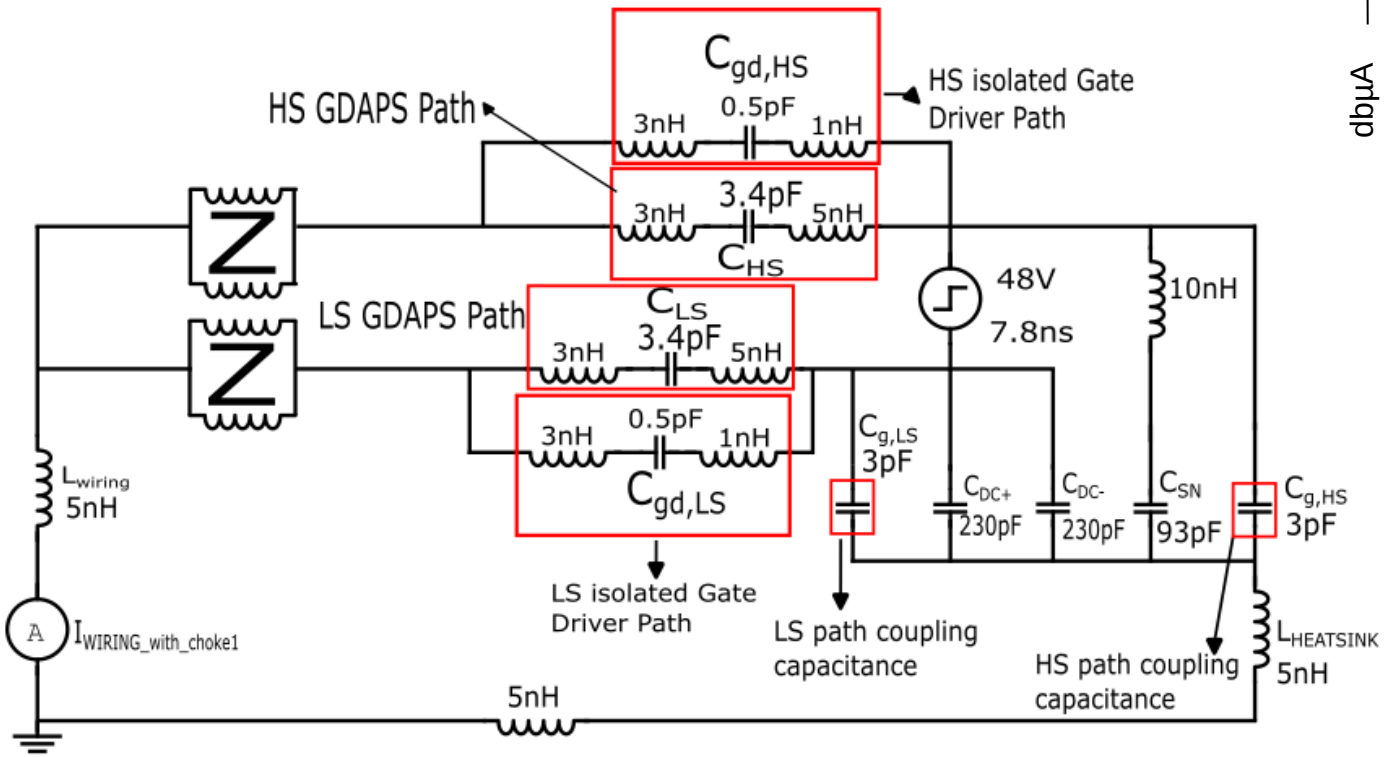


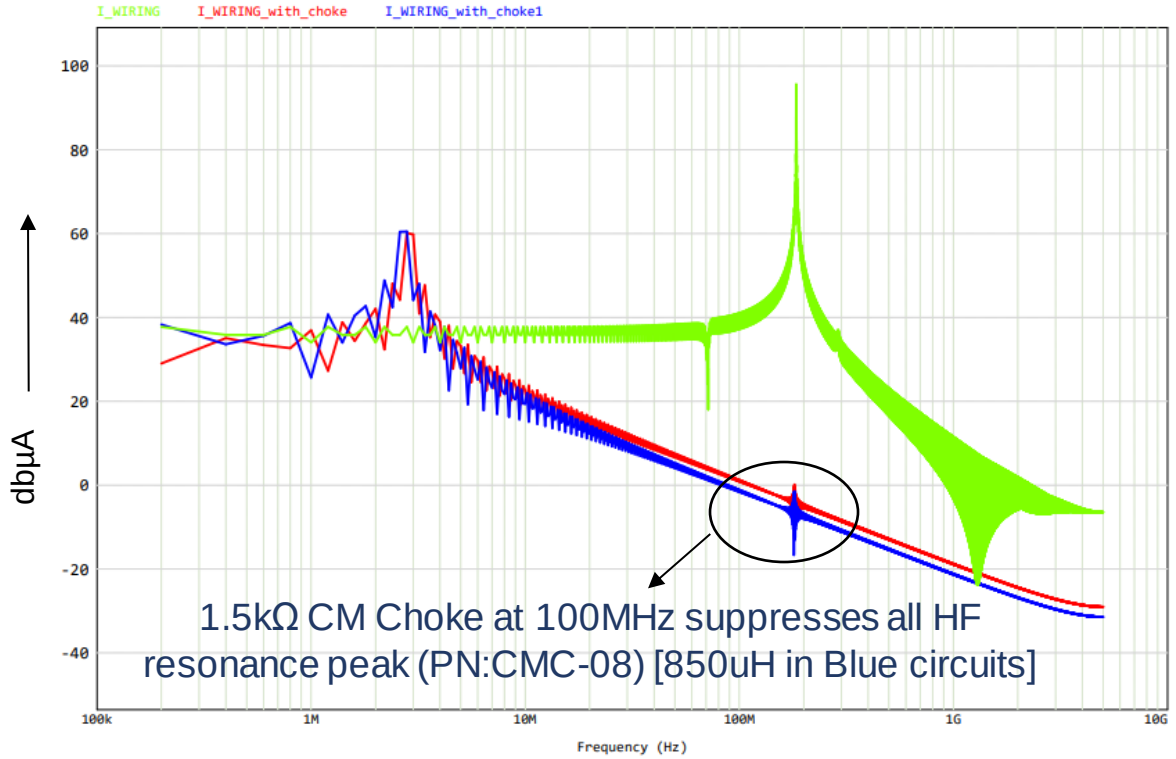
*Note: The red plot represents the circuit without $C_{gd,LS}$, and $C_{gd,HS}$ but with $C_{g,LS}$, C_{DC+}, C_{DC-} and $C_{g,HS}$

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Power Module Large Signal Model for CM current flow

Actual design values of CM Choke and gate driver isolation capacitance, auxiliary power supply (DC-DC) are available from LSM



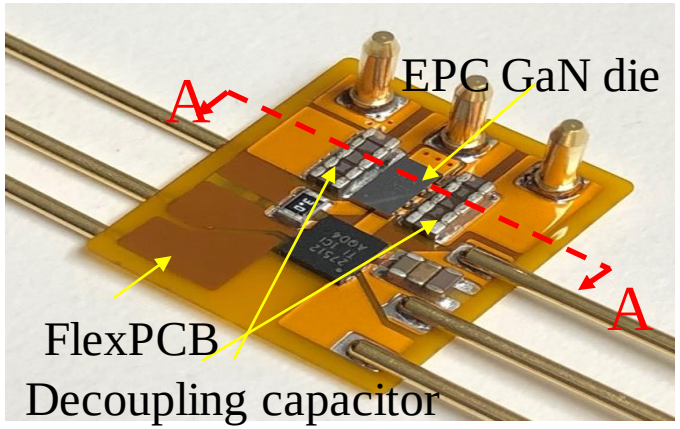


*Note: The red plot represents the circuit without $C_{gd,LS}$, and $C_{gd,HS}$ but with $C_{g,LS}$, C_{DC+}, C_{DC-} and $C_{g,HS}$

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Test for High Switching Transition Operation (Dr Cheng's)

GaN (EPC-2218) N_{off} 60V/25A/1.9ns

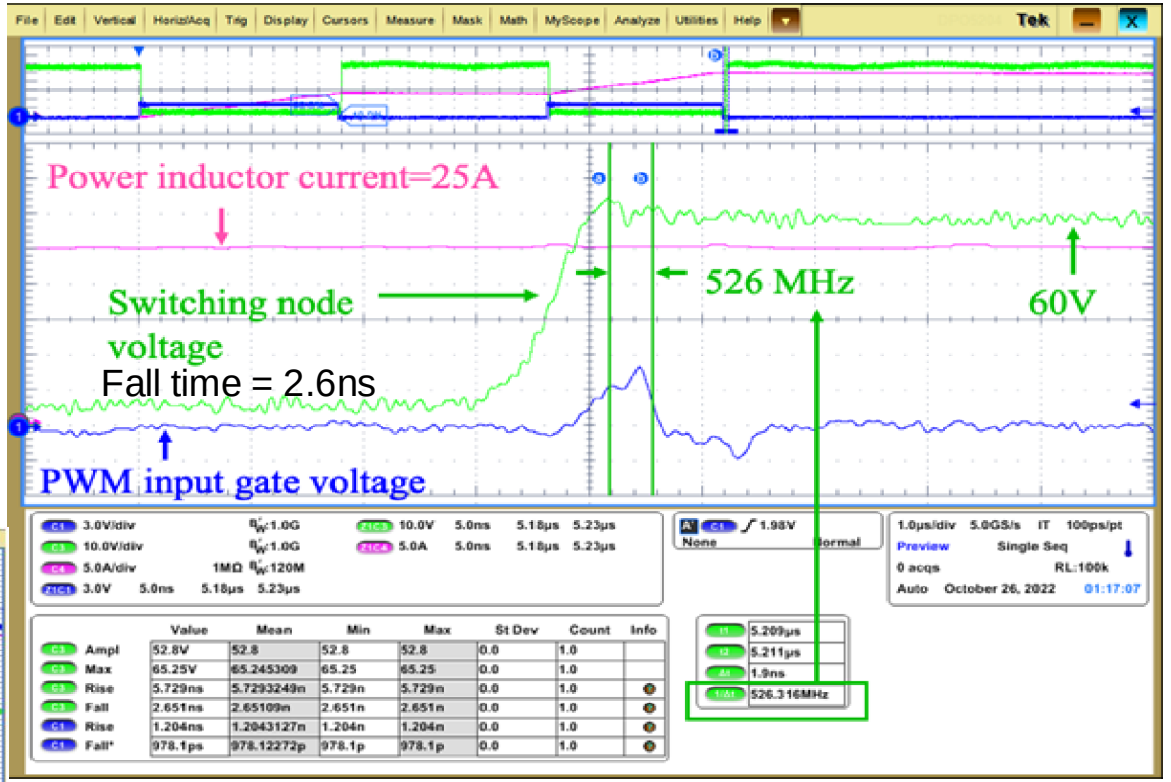


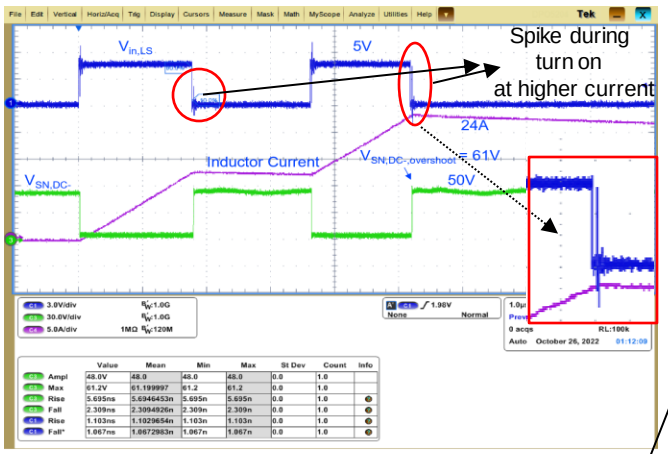
Power loop inductance

$$L_P = \frac{1}{4\pi^2 \times f_{ringing}^2 \times C_{oss}}$$

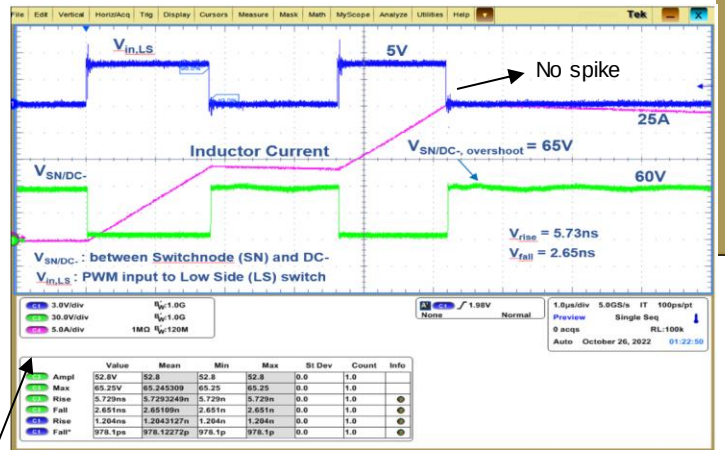
$$= \frac{1}{4\pi^2 \times (526MHz)^2 \times 562pF}$$

$$= 0.163\ nH$$





Non-Optimized CM choke and High Aux Pow er Supply C_{iso}



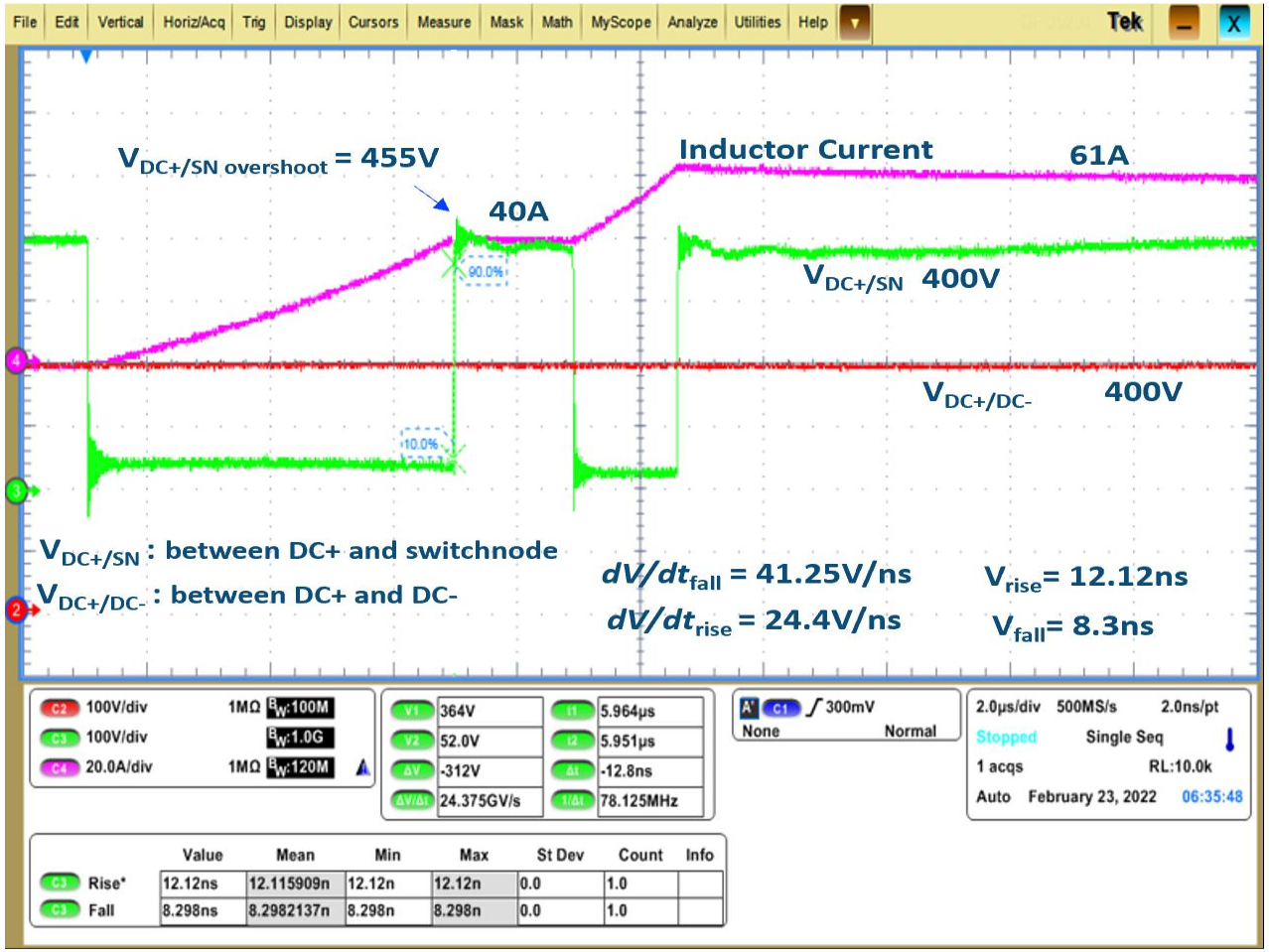
Optimized CM choke and Low Aux Pow er Supply C_{iso}

$C_{oss} = C_{oss,device} + C_{SN,baseplate} = (210+5)pF = 215pF$

No gate voltage spike at higher DC bus voltage for optimized layout-based module than in non-optimized module

ssinha5@ncsu.edu, dchopkins@ncsu.edu

DPT: 400V/61A GaN Systems Die Double Sided Module (80A/650V die: Large surface area)

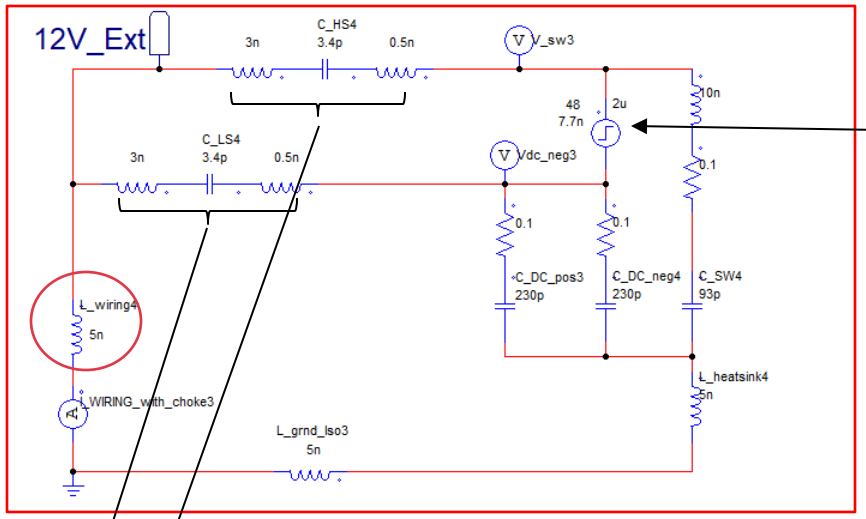


No spikes at 400V DC bus for confirming the compact layout for the non-optimized module does not lead to voltage isolation issues.

$C_{oss} = C_{oss,device} + C_{SN,baseplate} = (650+93)pF = 743pF$

ssinha5@ncsu.edu, dchopkins@ncsu.edu

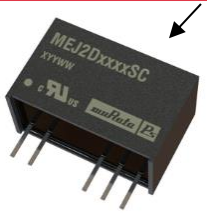
Transition speed effect due to proposed integrated Auxiliary Power (PS) Supply (through simulation)



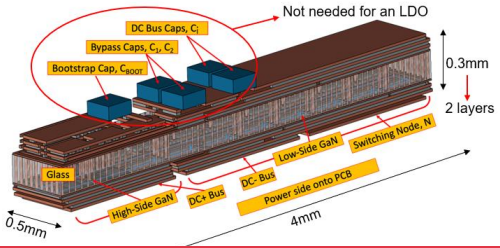
*CM Choke has been removed and L_wiring has been reduced to see the effect of just the effect of parasitic path inductance due to the auxiliary power supply

	Non integrated Auxiliary PS	integrated Auxiliary PS	integrated Auxiliary PS	integrated Auxiliary PS
Path inductance for Switch Node dv/dt of 48V/7.7ns (C_{iso} = 3.4pF)	25nH from 12V_Ext to DC-DC & 8nH from DC-DC to SN Large Auxiliary Power Supply Loop	3nH from 12V_Ext to DC-DC & 5nH from DC-DC to SN Integrated Auxiliary Power Supply	3nH from 12V_Ext to DC-DC & 2.5nH from DC-DC to SN Integrated Auxiliary Power Supply	3nH from 12V_Ext to DC-DC & 0.5nH from DC-DC to SN Integrated Auxiliary Power Supply
Peak resonant frequency in EMI spectrum for ground current in L_wiring	340MHz	433MHz	458MHz	473MHz

Present commercially available isolated Auxiliary PS



Need for



SMD high power density 3DHI power modules

Integrated auxiliary power supply

Peak resonant point is shifted almost by 133MHz improving the common mode transient immunity of the gate drive power supply path substantially

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Sourish Sankar Sinha, ssinha5@ncsu.edu

Laboratory for Packaging Research in Electronic Energy Systems (PREES)

FREEDM Systems Center, North Carolina State University

1791 Varsity Drive, Suite 100; Raleigh, NC 27606-7571
Tele: 919-513-5929, Fax: 919-513-0405
www.prees.org

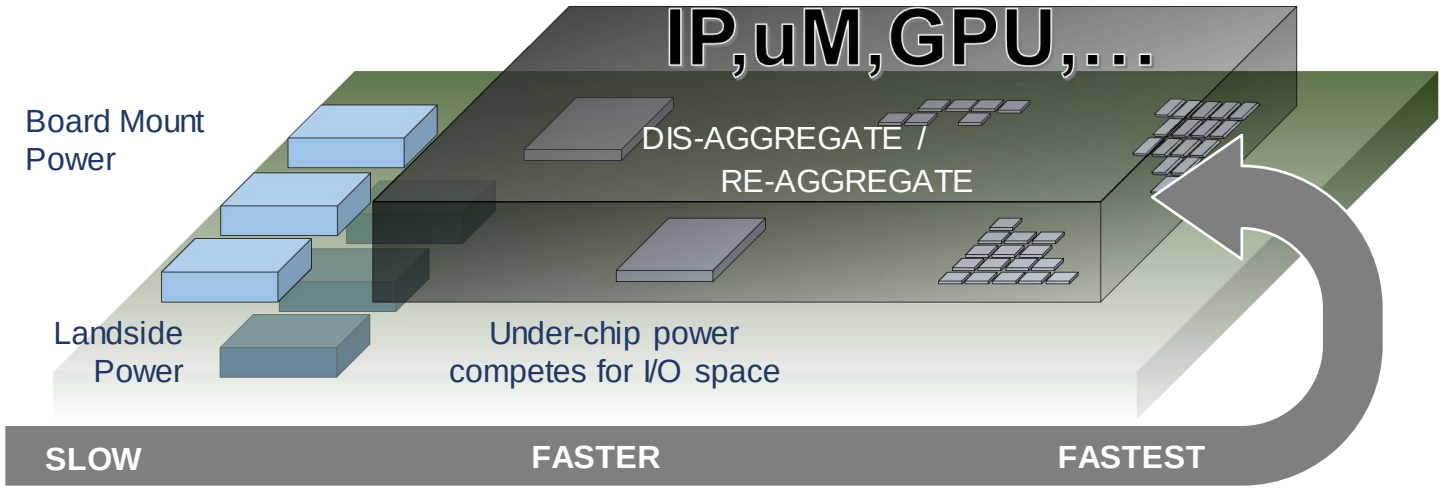
3D Heterogeneous Integration of Power Electronic MicroSystems: used as Auxiliary Power Supply

- Ultra low power and gate loop inductance
- High current density through multilayer interconnects

ssinha5@ncsu.edu, dchopkins@ncsu.edu

3D Heterogeneous Integration of Power Electronic MicroSystems

3DHI Power (3DHIP) MicroSystem



Large arrays of small, thin separately-manufactured 3DHIPs

How do we integrate power with the load?

DIS-AGGREGATE & RE-AGGREGATE

Electrical Circuit Topologies:

1. Switched Capacitor
2. Switched Inductor
3. Self-Resonant Converters
4. (Linear Topologies)

(Hybrid Topologies)

Physical Circuit Topologies:

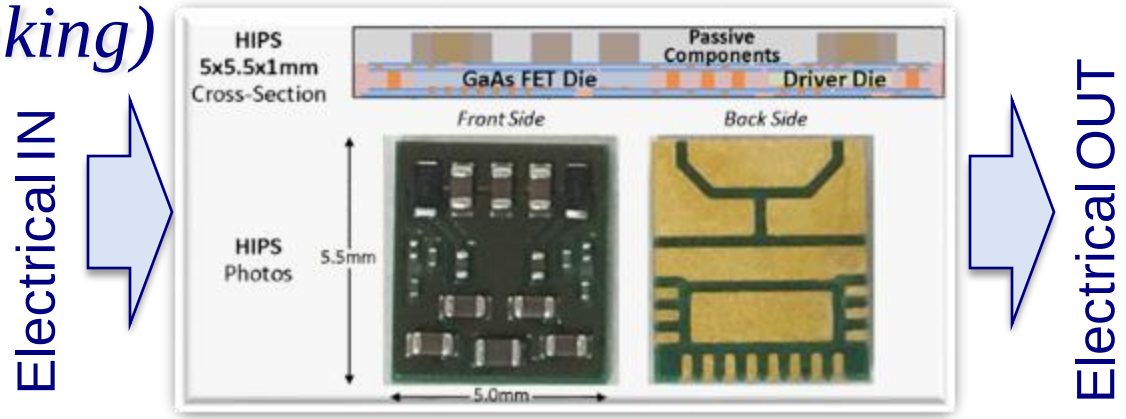
1. Standalone converters
2. Disaggregated components per converter
3. Clustered converters

ssinha5@ncsu.edu, dchopkins@ncsu.edu

EE Topology Approach (EE Thinking)

Key Challenges:

1. High currents (10A-20A/mm^2)
2. High bandwidth (ultralow inductances)
3. High Efficiency

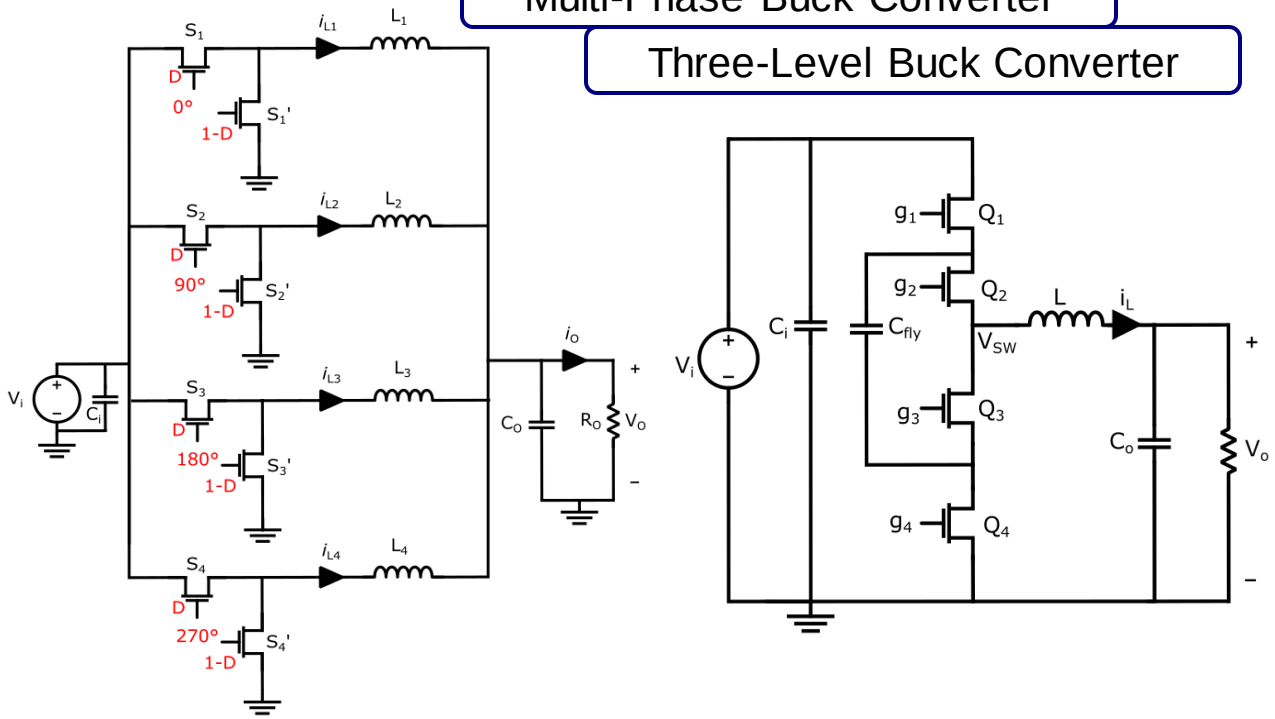


Source: Sarda Technologies (March, 2018 APEC)

Single Phase Buck Converter

Multi-Phase Buck Converter

Three-Level Buck Converter



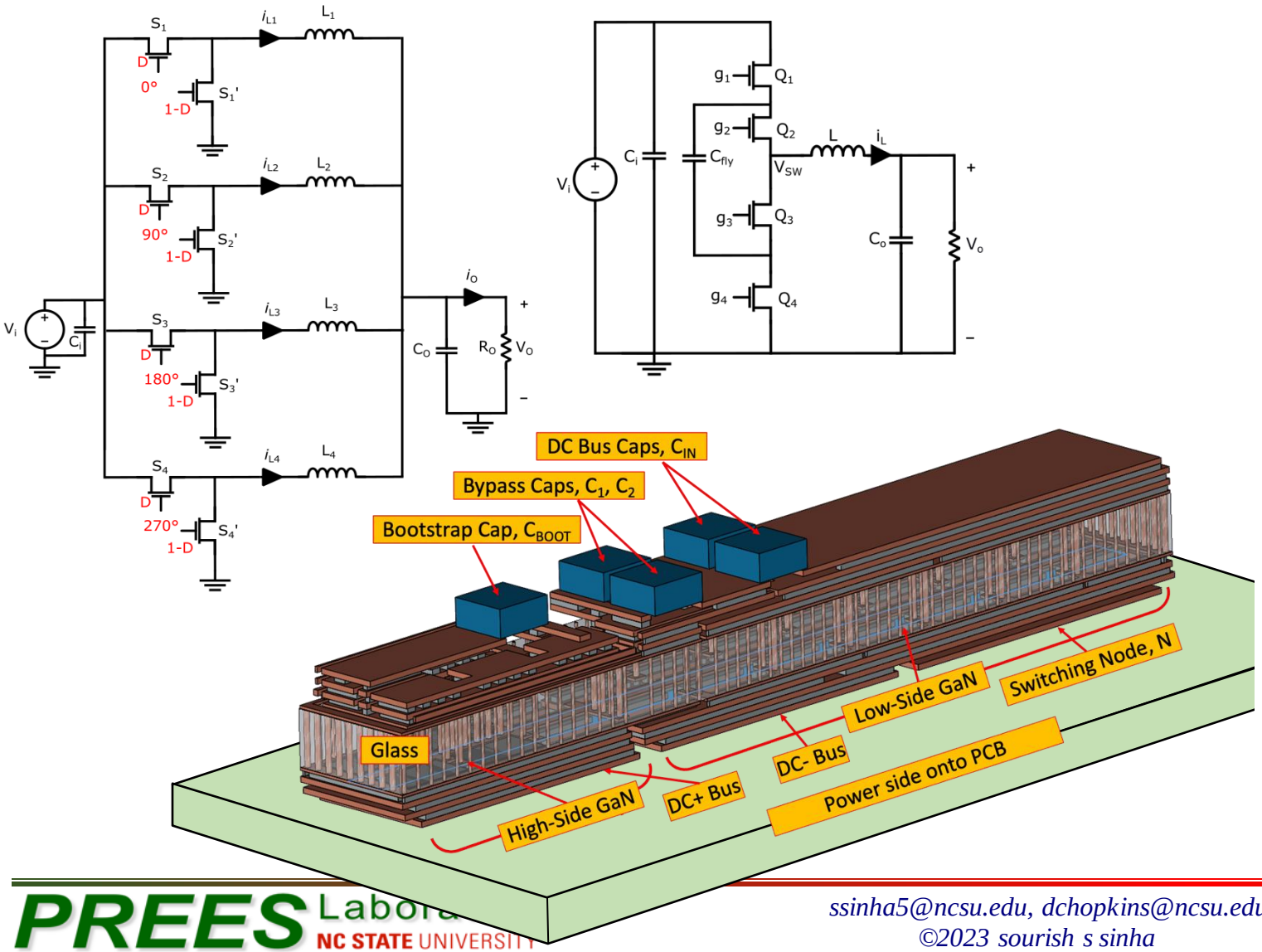
Each allows increased switching speed.

- Interleaved divides current through each die, L and associated interconnects per Ø.
  - Efficiency is increased and thermal stresses reduced
- The 3-Level provides a 2X frequency increase in the inductors, but not current
  - The 3-Level is often used to divide voltage across the semiconductor switches and might be considered for 340V:48V

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Exemplar: Topology Selection In Light Of Packaging

Re-evaluating the electrical topology



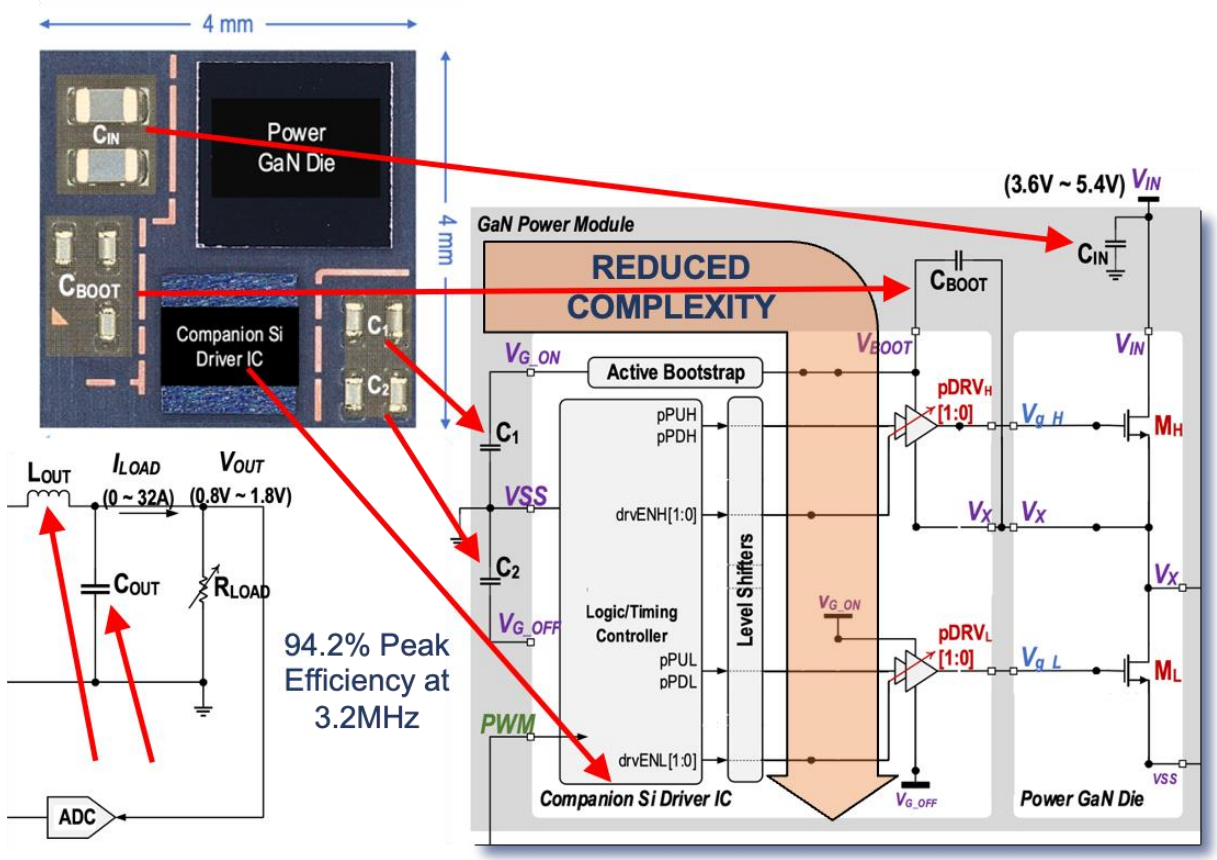
Exemplar Design Requirements	
Parameters	Values
V_i (Input DC Bus)	5V
V_o (Output)	1V
Efficiency	> 90%
Type	Interleaved Sync Buck
No. of Phases	4
Duty	0.21
I_o (average)	32A (8A per phase)
Peak L Ripple Current (per Ø)	6.4A (20% of I_o)
V_o ripple	0.1V (10% of V_o)

Key Challenges:

1. High currents (10A-20A/mm^2)
2. High bandwidth (ultralow inductances)
3. High Efficiency

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Exemplar Design Values for 5:1V/32A 4-Ph Interleaved Sync Buck



A. Component Values

- Decoupling Cap: C_{IN} = 100 x C_{oss} = 220pF (C_{oss} = 2.2pF)
- Bootstrap Cap Selection: [1] $C_{BOOT} \geq 10 \times C_{iss}$ = 100pF ($C_{iss} = C_{gs} + C_{gd}$ = 7.67pF)
- Bypass Cap Selection: $C_{BC} \geq 10 \times C_{boot}$ = **1nF**
- Phase Inductor: **12nH** @ 10MHz and 6.4A Inductor ripple

COMPONENT SELECTION

	Part No.	Value (nF)	Voltage (V)	SRF (GHz)	Thick (mm)	LXW (mm^2)
C_{BC}	MAASL063SB7-102MFCA01	1	10	>0.13	0.33	0.6X0.3
C_{BOOT}	0201ZA101JA-T2A	0.1	10	0.2	0.33	0.6X0.3
C_{IN}	MAASL063SB-7221MFCA01	0.22	10	1	0.33	0.6X0.3

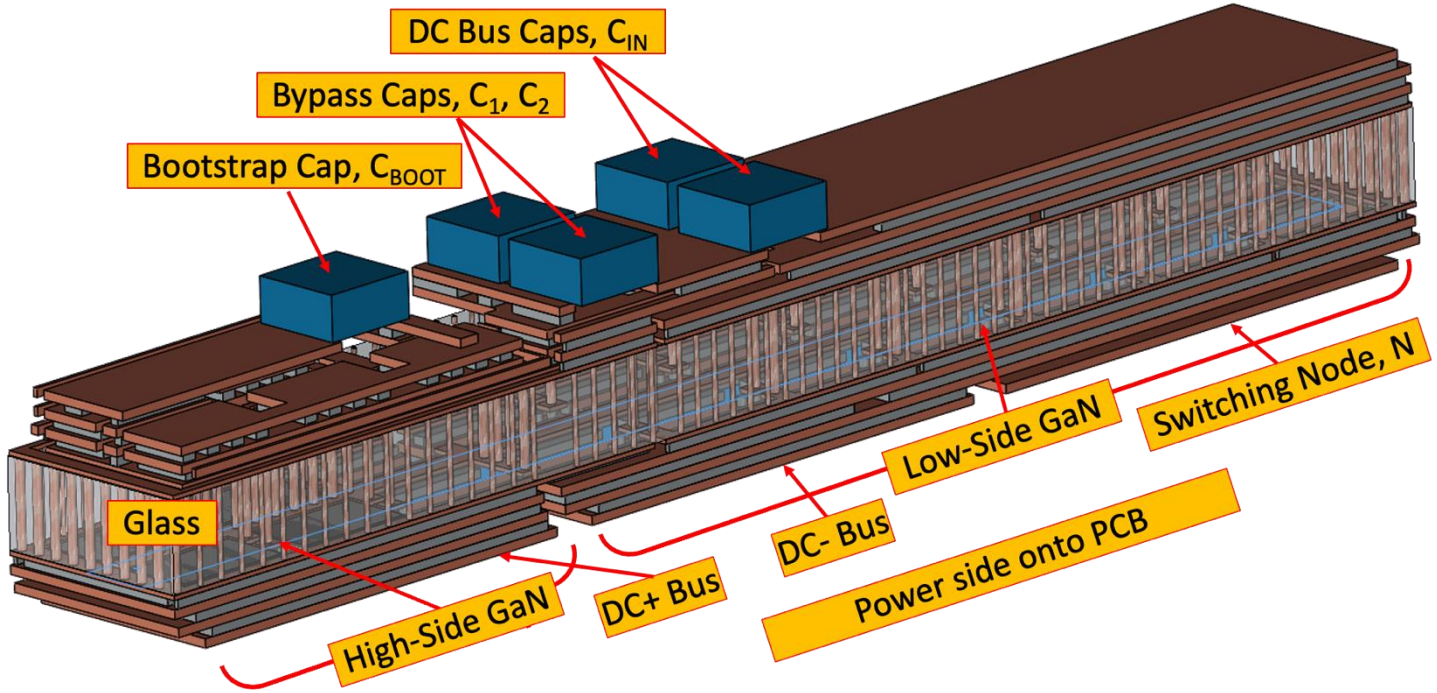
INDUCTOR SELECTION

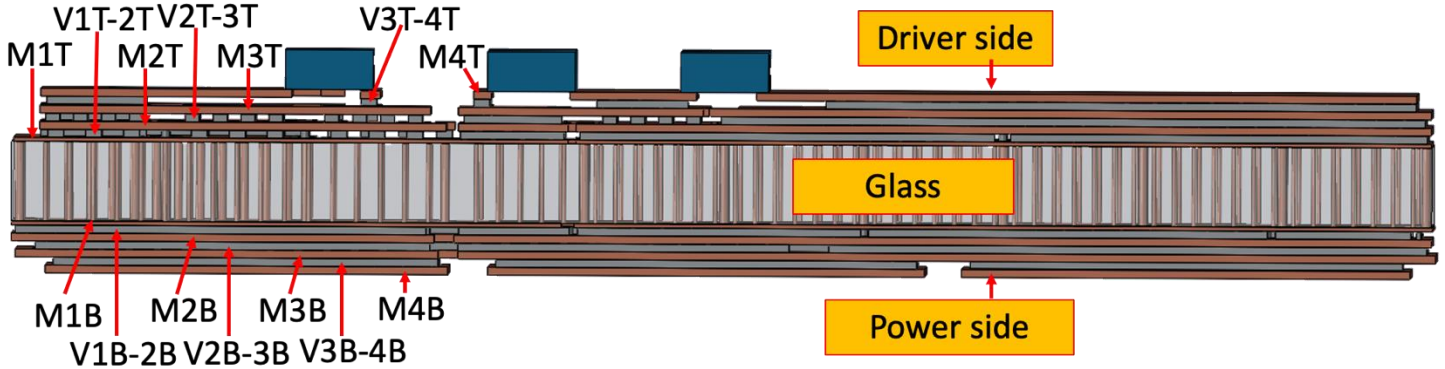
	Part No.	Value (nH)	Current (A)	SRF (GHz)	Thickness (mm)	L X W (mm^2)
L_{OUT}	Inductor	12	≥8	TBD	TBD	TBD

1. Application Report SLUA887, "Bootstrap Circuitry Selection for Half-Bridge Configurations", Texas Instruments.

ssinha5@ncsu.edu, dchopkins@ncsu.edu

Exemplar – 4-Phase Interleaved Buck 3DHIP Converter





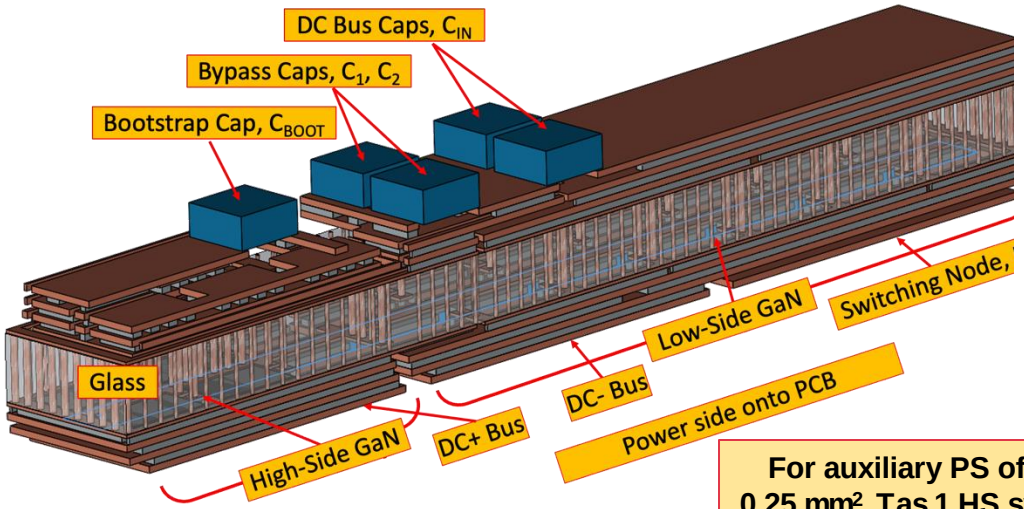
Half symmetry layout of 1-ph of a 4-ph interleaved Buck converter showing position of passives and power terminals

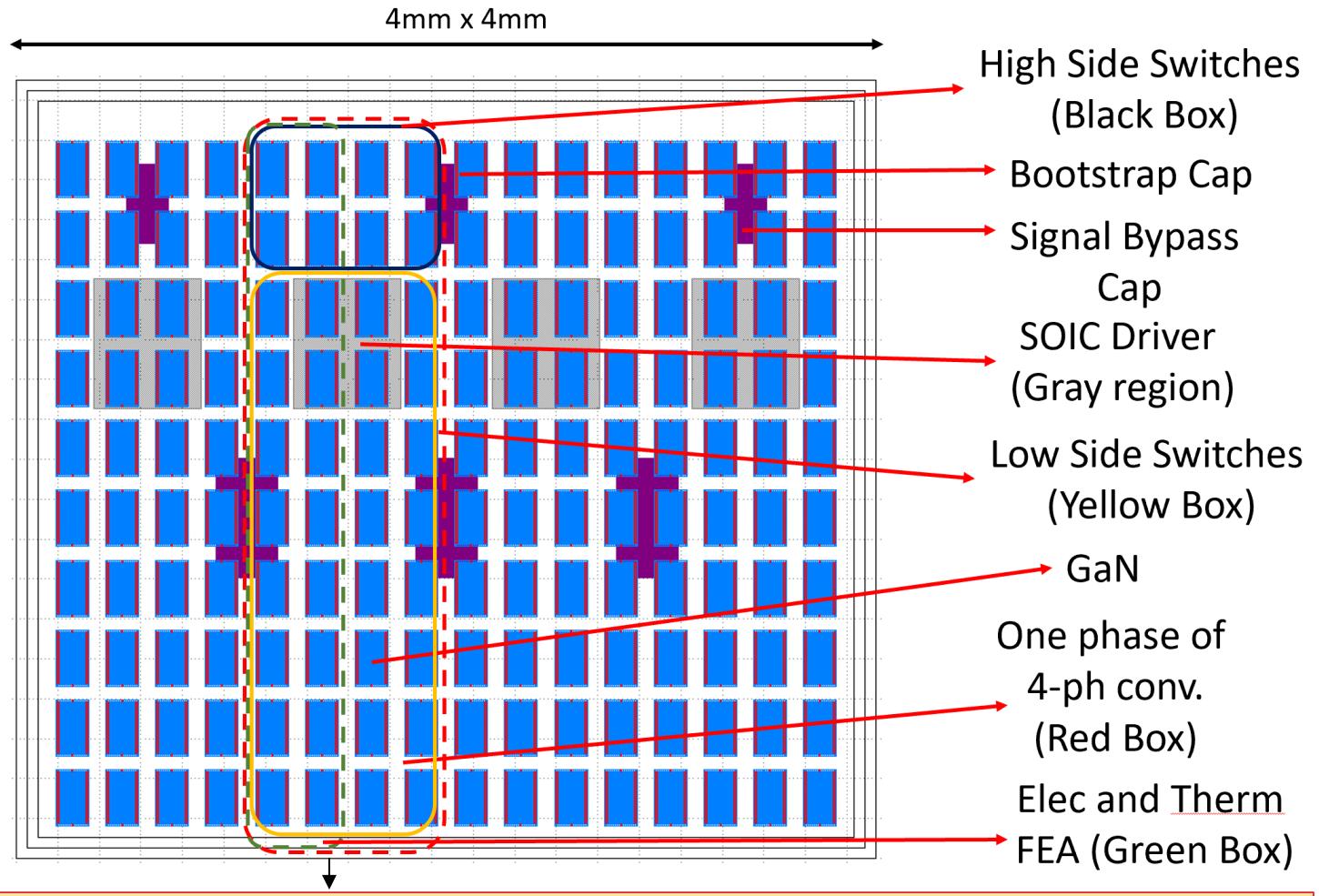
Layer Thicknesses	
M4B/M4T	20
V3B-4B/ V3T-4T	20
M3B/ M3T	20
V2B-3B/ V2T-3T	20
M2B/ M2T	20
V1B-2B/ V1T-2T	20
M1B/ M1T	10
Glass	200
Device	9.5
Adhesive	50-500nm

ssinha5@ncsu.edu, dchopkins@ncsu.edu

3DHIP Layout in Multiple Layers

- Glass interposer has 15µm vias on 30µm pitch (with proven reliable 40µm diameter and 80µm pitch).
- Multi layers of copper spread the current particularly at the die-interconnect interface.

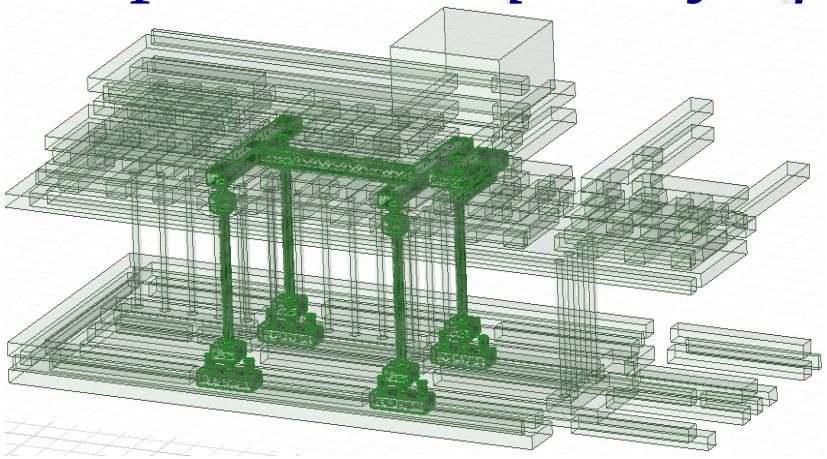


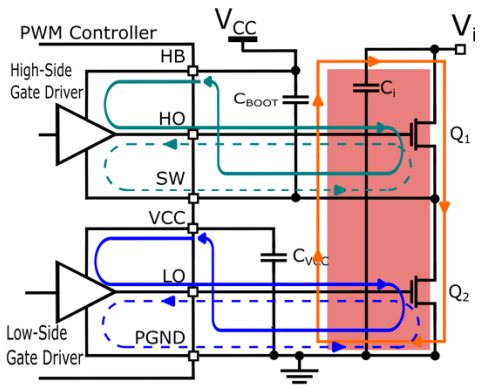


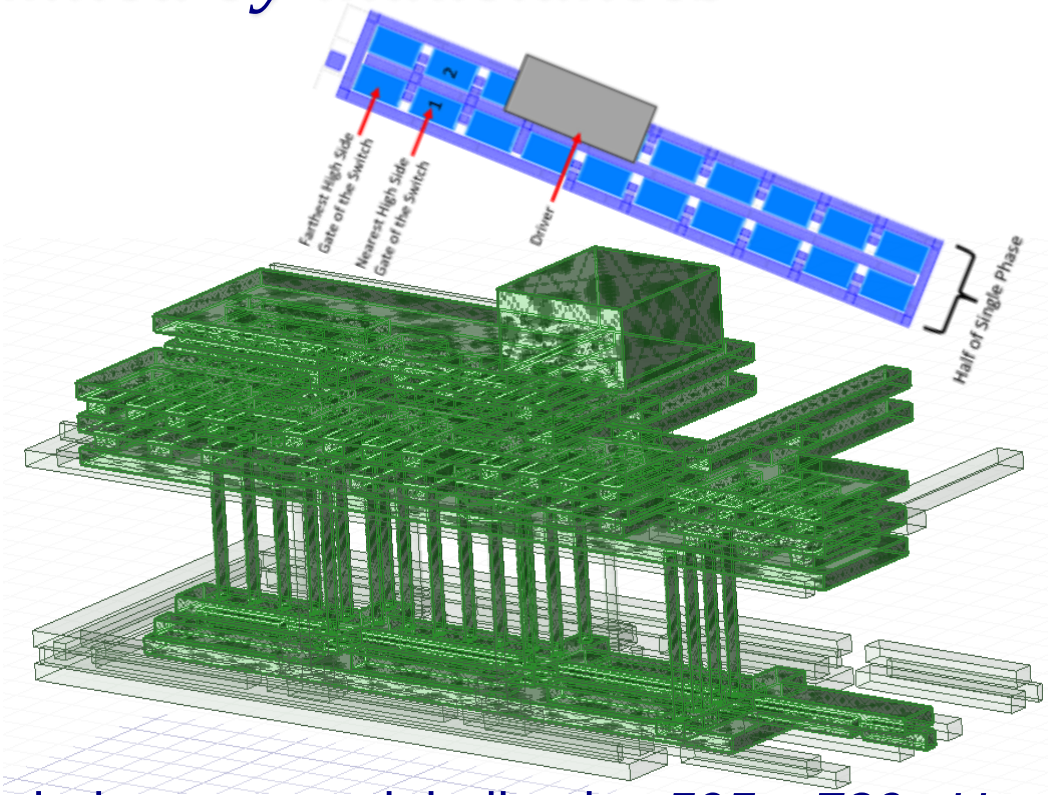
For auxiliary PS of power electronic converter gate drives, to carry 0.5A_{peak} the total area coverage will be merely 0.25 x 0.25 mm² Tas 1 HS switch and 1 LS switch will be required. Including isolations required by auxiliary PS and the secondary side of the converter. The size estimation is approximately 1 x 1mm². Compared to MURATA (12mm x 0.5mm) auxiliary PS of the same rating the size is almost 1/100th.

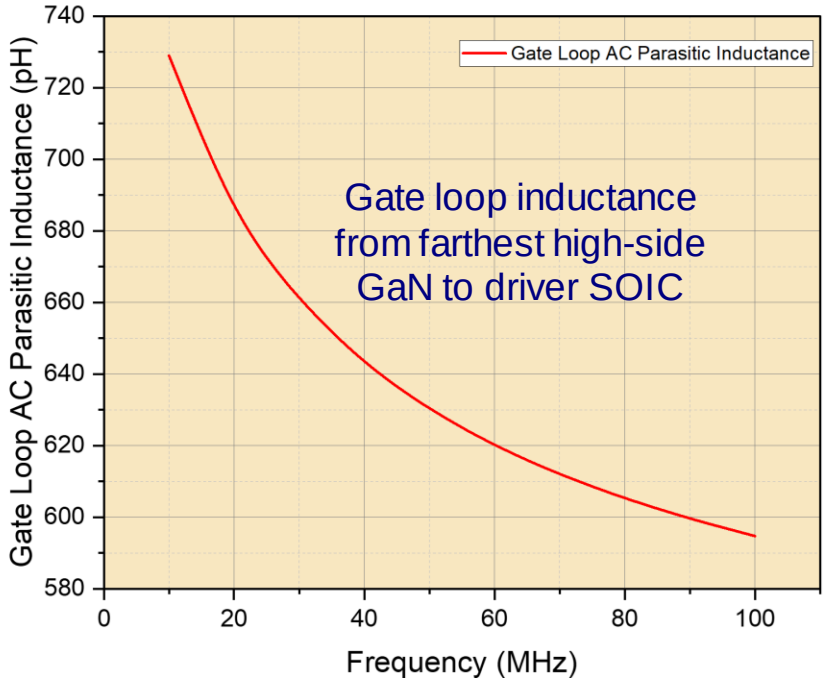
ssinha5@ncsu.edu, dchopkins@ncsu.edu

Exemplar – Frequency of Operation – Limited by inductances









Simulated Gate drive inductance path indicating *595 – 730 pH*.

Assuming a *600pH* path inductance at 20% duty cycle for the inverter, this ***implies a switching frequency of 83 MHz***

For a 5V/1A_{peak} GaN gate pulse with 600pH loop inductance with a 5% *dt* rise and fall, implies an edge response of 120ps each, or a 2.4ns pulse. At 20% duty cycle the switching frequency is 83.3 MHz (1/12ns), if GaN can respond.

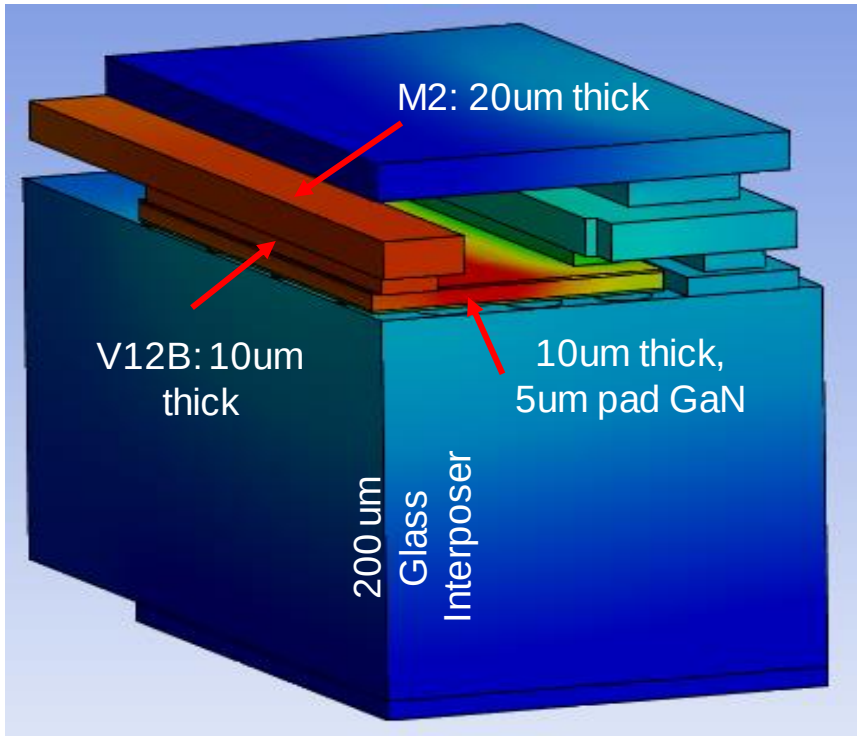
ssinha5@ncsu.edu, dchopkins@ncsu.edu

Thermal Profiling

- Primary GaN heat is into the PCB or Load and is an issue TBD by application
- Max Cu interconnect temperature (and GaN) is ***106°C*** with 27°C ambient.
- The 200um glass interposer with dense TGVs provides ~0.0 ΔT from SOIC to GaN
  - The 100um thick interposer performed the same
  - Thermal conductivity of Glass without thermal via is 1.3 W/m.K
  - Thermal conductivity of Glass with thermal via (40um diameter and 2D pitch) is 170 W/m.K.

- 3.2W loss distributed across all 96 GaN
  - 26.7mW per device
- PCB manages the 106°C
  - New ERCD laminate at 20W/mK should be considered

h coefficient	465 W/m^2.K (Top Surface)
h coefficient	5 W/m^2.K (Bottom Surface)
Ambient Temperature	27ºC



ssinha5@ncsu.edu, dchopkins@ncsu.edu

Interconnect Current Density – A challenge for 3DHIP

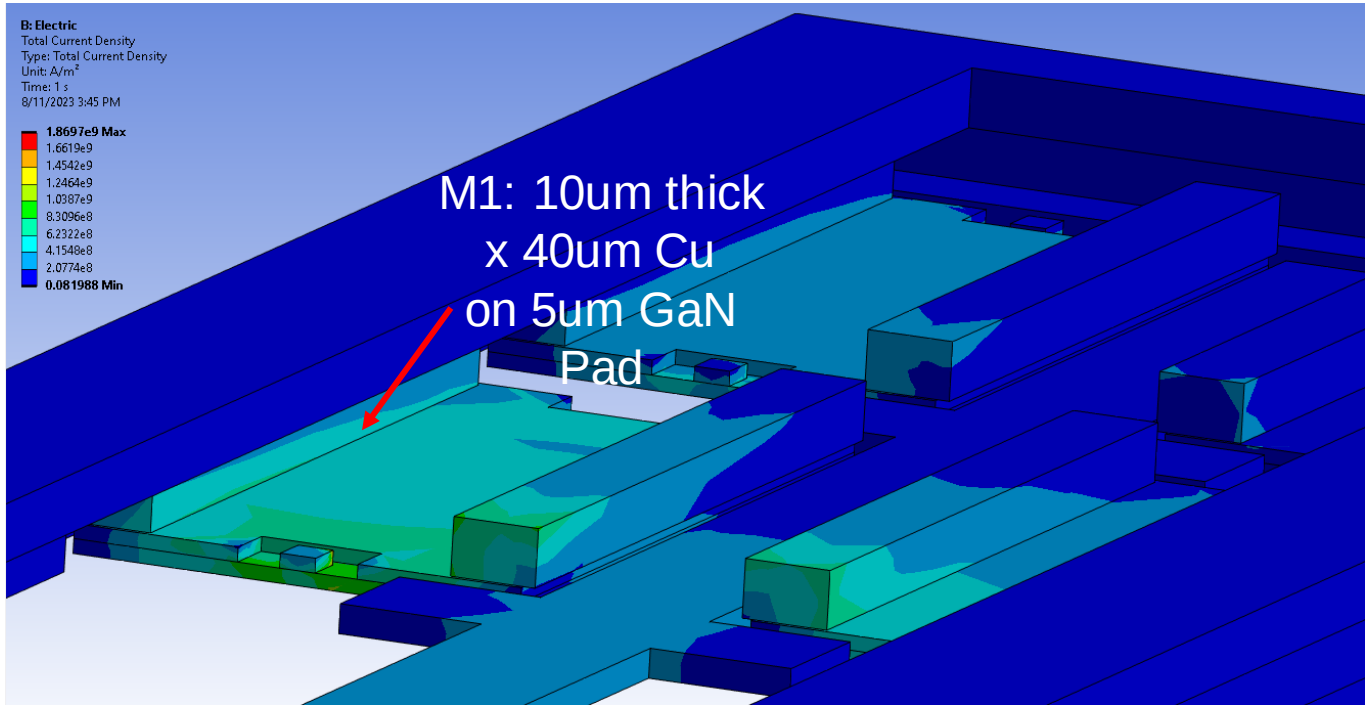
Die are 160um X 280um X 10um with 5um D-S pads along the 280um side

12 dies for upper switch and 28 dies for the lower switch per phase

Each phase (of four phases) carries 8A average (for 32A total)

Highest simulated current density was 830 A/mm² at the V12B interconnect & 5um GaN pad forcing GaN die redesign.

3DHP of the future will require GaN Semiconductors to be part of the Heterogeneous Design EcoSystem



ssinha5@ncsu.edu, dchopkins@ncsu.edu

Sourish Sankar Sinha, ssinha5@ncsu.edu

Laboratory for Packaging Research in Electronic Energy Systems (PREES)

FREEDM Systems Center, North Carolina State University

1791 Varsity Drive, Suite 100; Raleigh, NC 27606-7571
Tele: 919-513-5929, Fax: 919-513-0405
www.prees.org