Inductance of Capacitor Connections

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Using EMC test boards designed at University of Twente

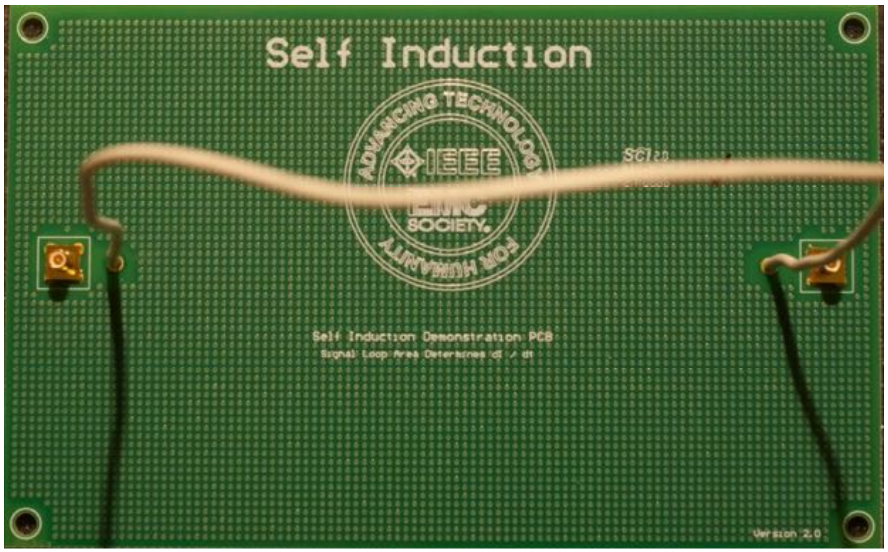
EMC Test Boards

10 PCBs designed by the University of Twente for EMC education

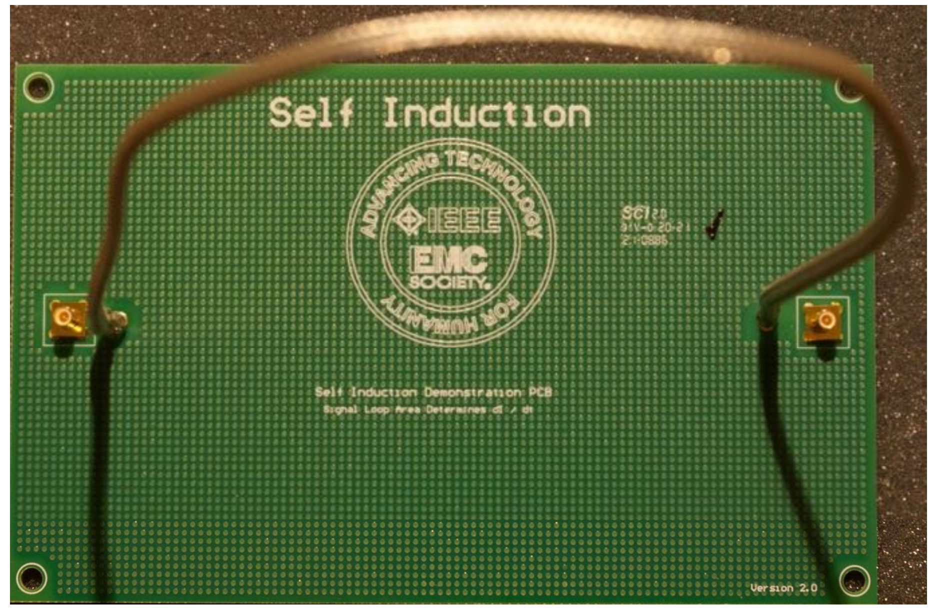
- (Self) Inductance of a Wire
- Inductance of Capacitor connection

(Self) Inductance of a Wire

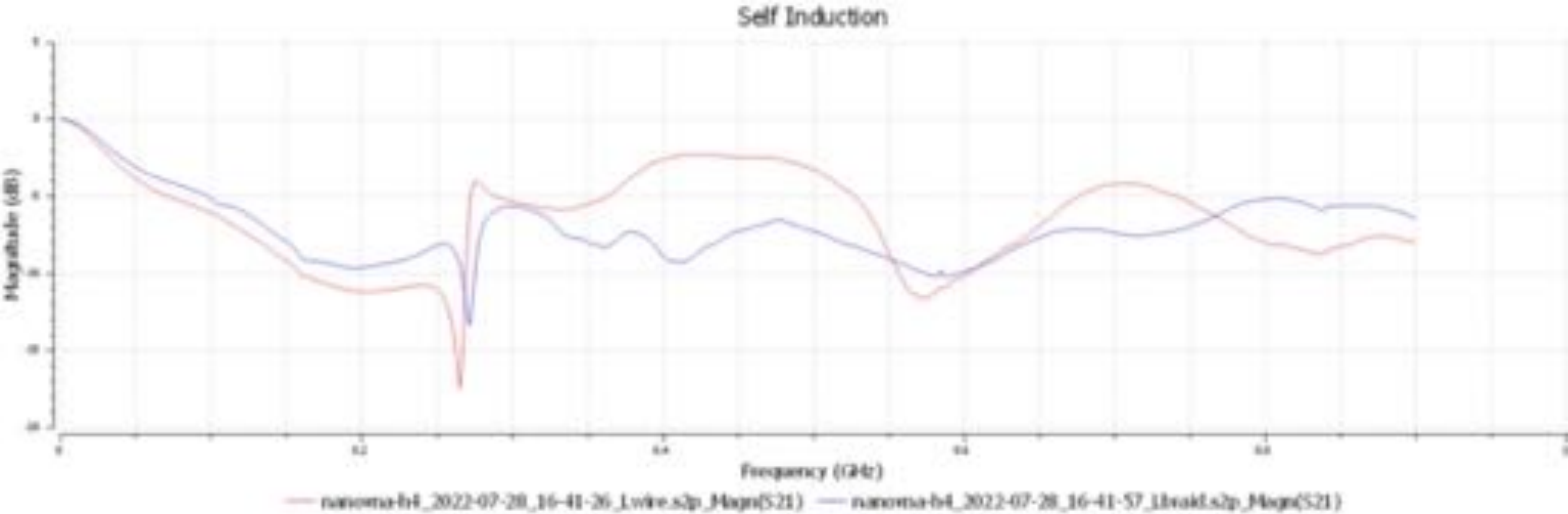
AWG 14 stranded wire



AWG 13.3 Tinned braid



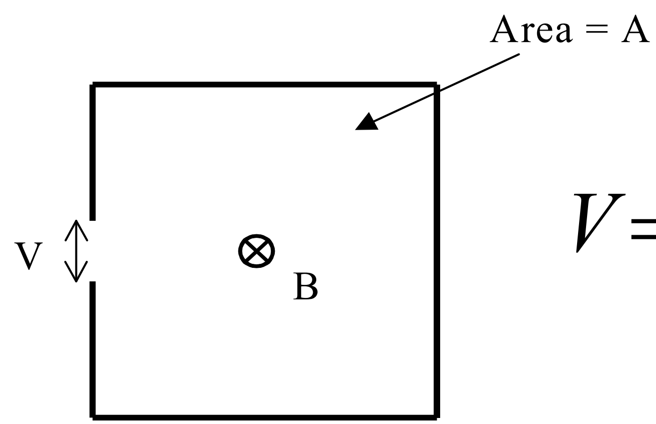
(Self) Inductance of a Wire



Inductance Definition

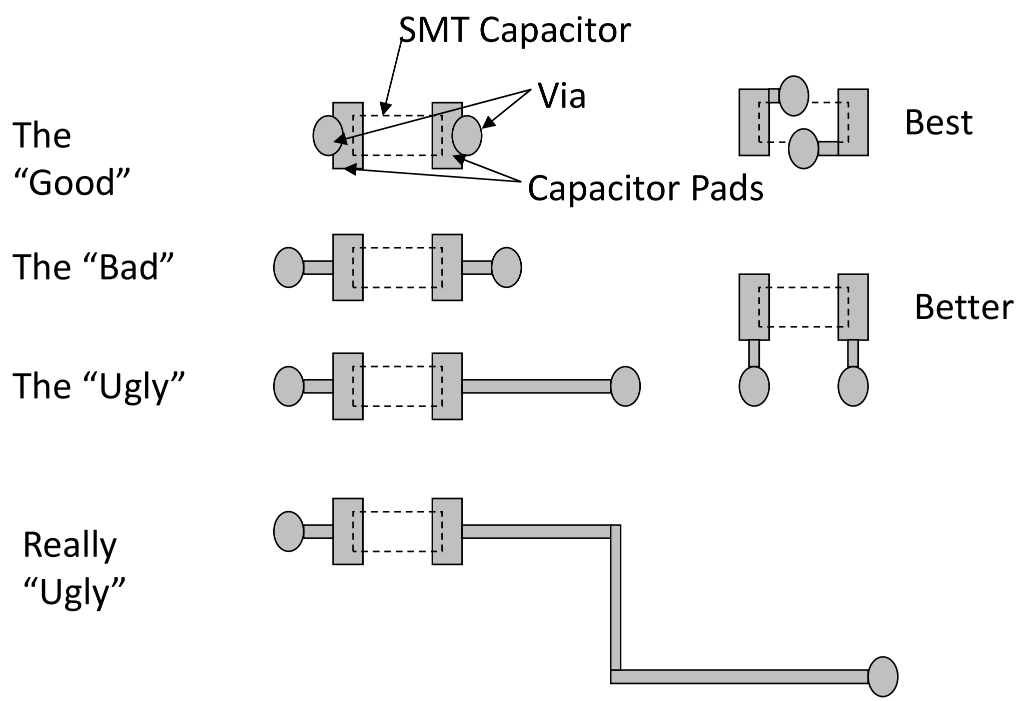
- Faraday's Law $$\oint \overline{E} \cdot dl = -\iint \frac{\partial \overline{B}}{\partial t} \cdot d\overline{S}$$

- For a simple rectangular loop



$$V = -A\frac{\partial B}{\partial t}$$

Via Configuration Can Change Inductance



Inductance of Capacitors

Cap. #1 – Vias and Value

All 1 nF

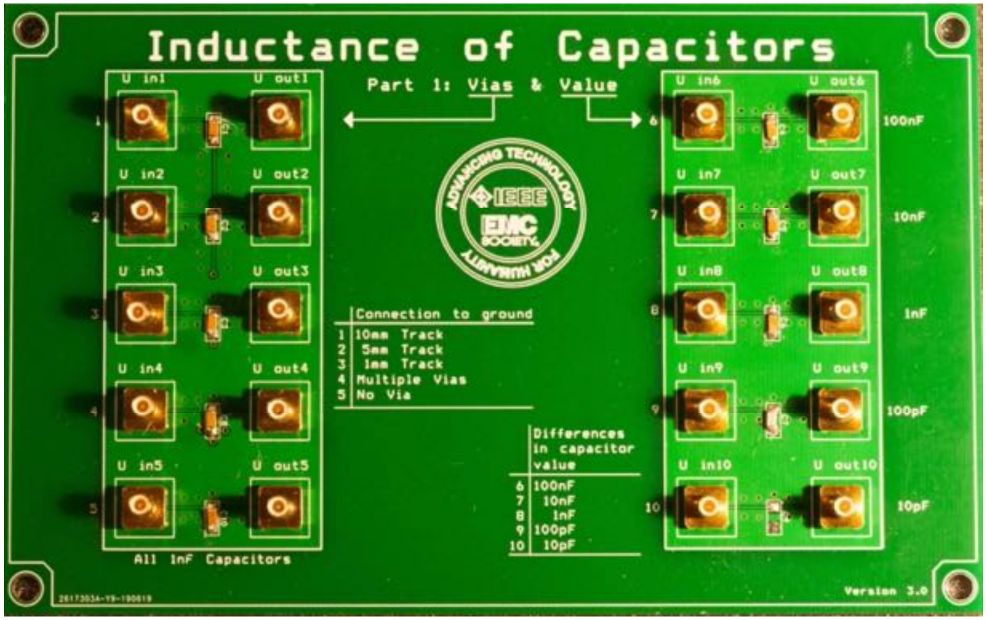
10 mm trace to via

5 mm trace to via

1 mm trace to via

Multiple vias

No via



100 nF

10 nF

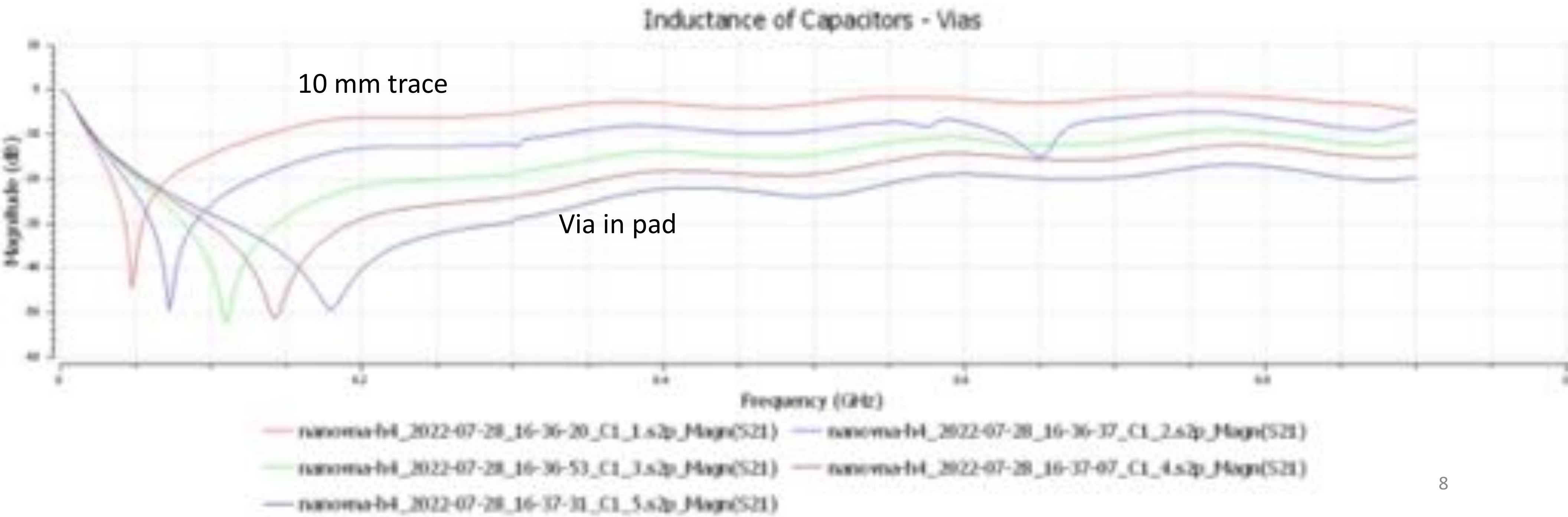
1 nF

100 pF

10 pF

Inductance of Capacitors

Cap. #1 – Distance to Via



Inductance

- Current flow through metal = inductance!
- Fundamental element in EVERYTHING
- Loop area first order concern
- Inductive impedance increases with frequency and is MAJOR concern at high frequencies

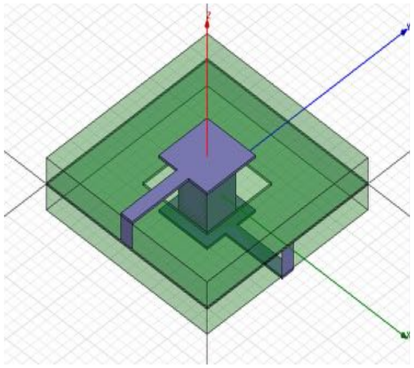
$$X_L = 2\pi f L$$

Given the Definition of Inductance

- Do these have inductance?

"Ground Strap"

SMT Capacitor



PCB Via

<u>Not until return path for current is identified!</u>

Current Loop = Inductance

Courtesy of Elya Joffe

Self Inductance

- Isolated circular loop

$$L \approx \mu_0 a \left(\ln \frac{8a}{r_0} - 2 \right)$$

a= loop radius
r_0= wire size radius

- Isolated rectangular loop

$$L = \frac{2\mu_0 a}{\pi} \left(\ln \frac{p + \sqrt{1+p^2}}{1+\sqrt{2}} + \frac{1}{p} - 1 + \sqrt{2} - \frac{1}{p}\sqrt{1+p^2} \right)$$

Note that inductance is directly influenced by loop ***AREA*** and less influenced by conductor size!

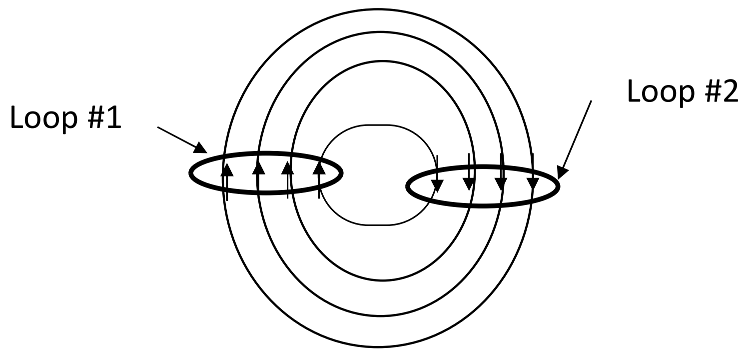
$$p = \frac{\text{length of side}}{\text{wire radius}}$$

Mutual Inductance

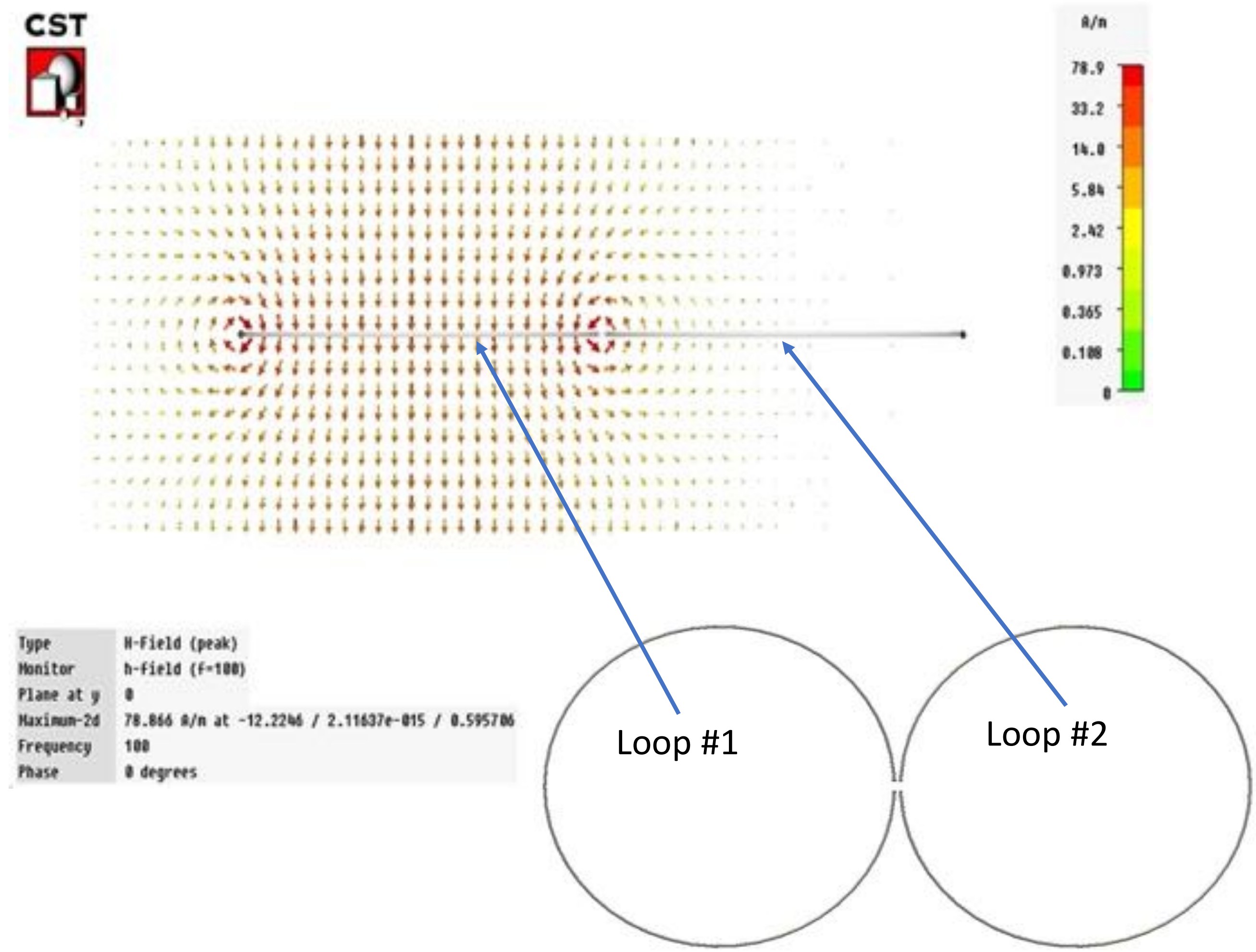
$$\Phi_2 = M_{21} I_1$$

$$M_{21} = \frac{\Phi_2}{I_1}$$

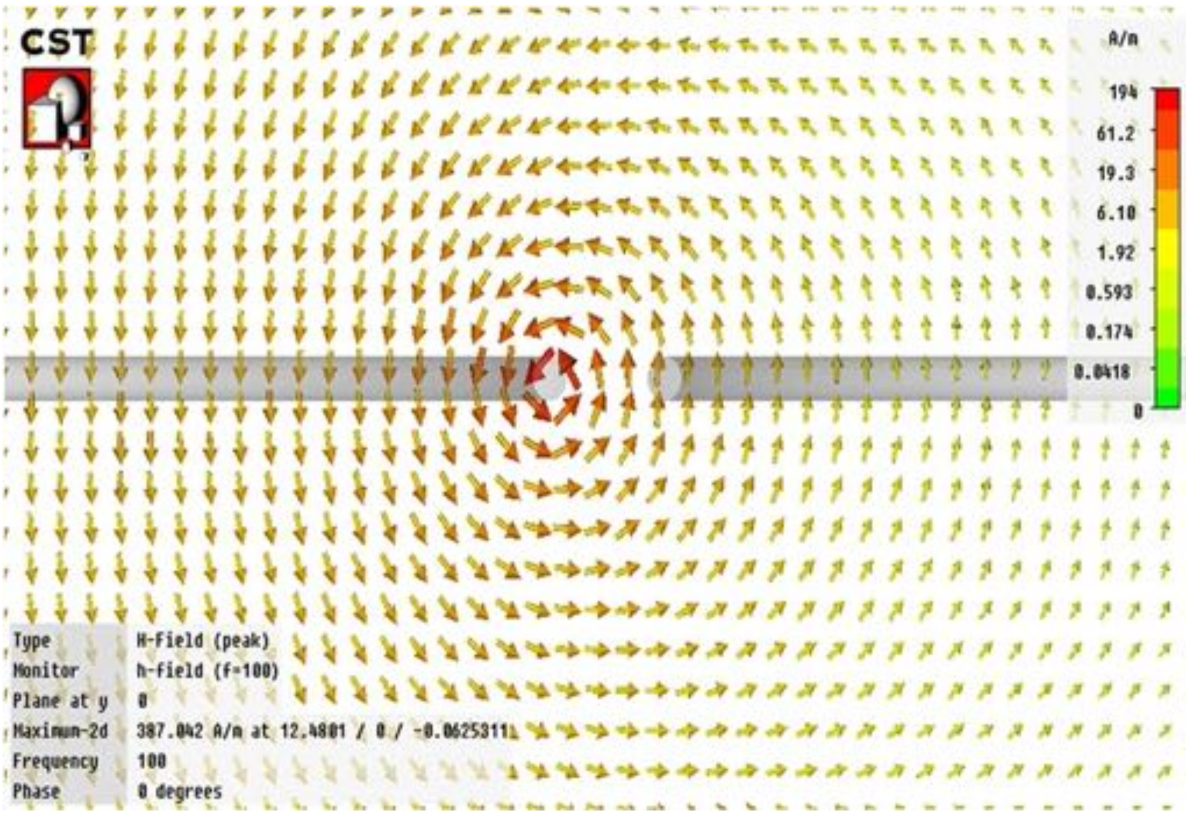
How much magnetic flux is induced in loop #2 from a current in loop #1?

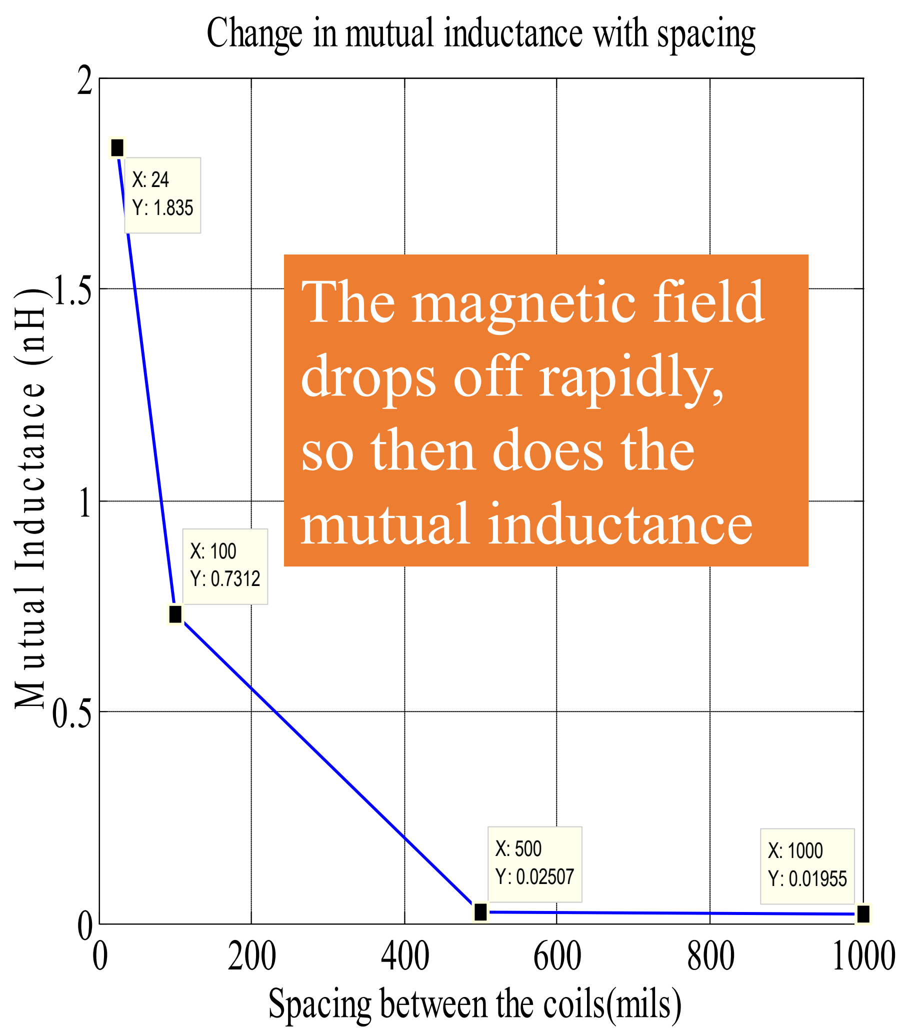


Flux from Current in Loop #1



Flux from Current in Loop #1

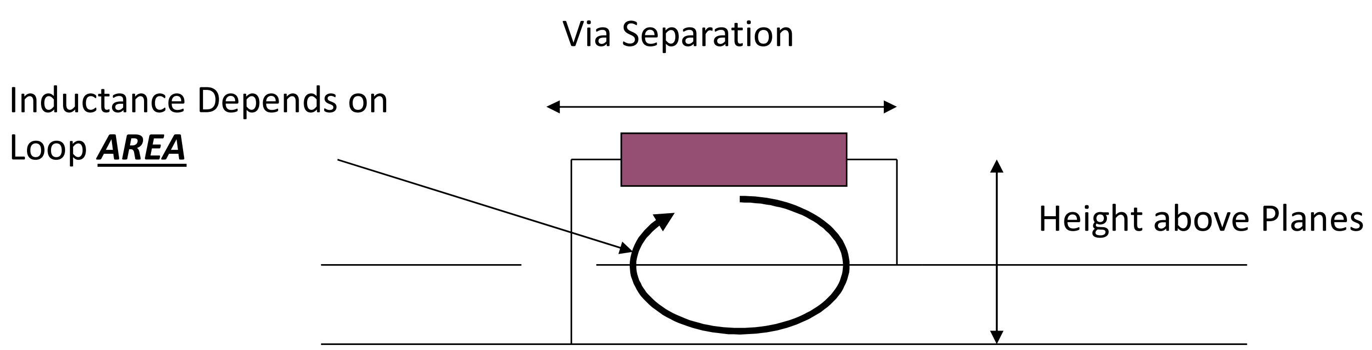



Change in mutual inductance with spacing
2
1.5
1
0.5
0
0
200
400
600
800
1000
Mutual Inductance (nH)
Spacing between the coils(mils)
X: 24
Y: 1.835
X: 100
Y: 0.7312
X: 500
Y: 0.02507
X: 1000
Y: 0.01955
The magnetic field drops off rapidly, so then does the mutual inductance

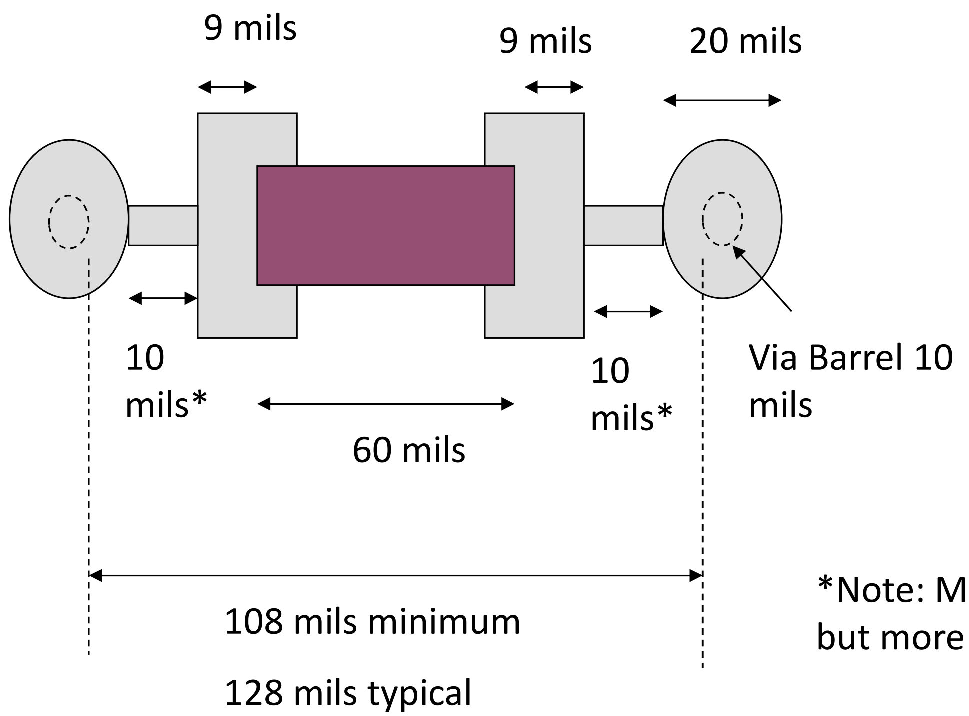
Example

Decoupling Capacitor Mounting

- **Keep vias as close to capacitor pads as possible!**

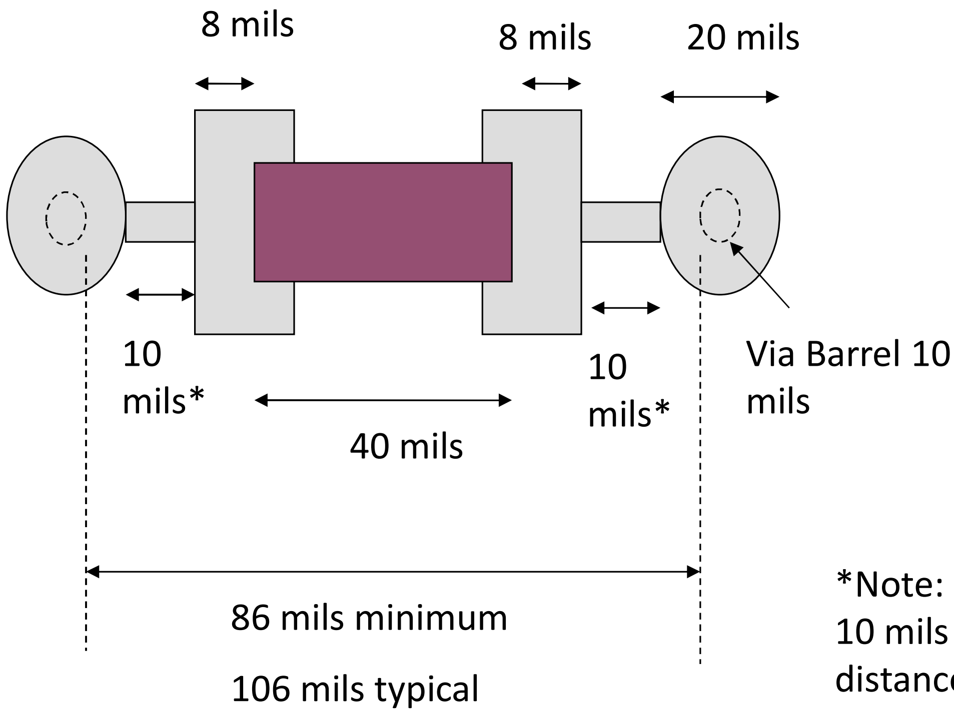


0603 Size Cap Typical Mounting



*Note: Minimum distance is 10 mils
but more typical distance is 20 mils

0402 Size Cap Typical Mounting



*Note: Minimum distance is 10 mils but more typical distance is 20 mils

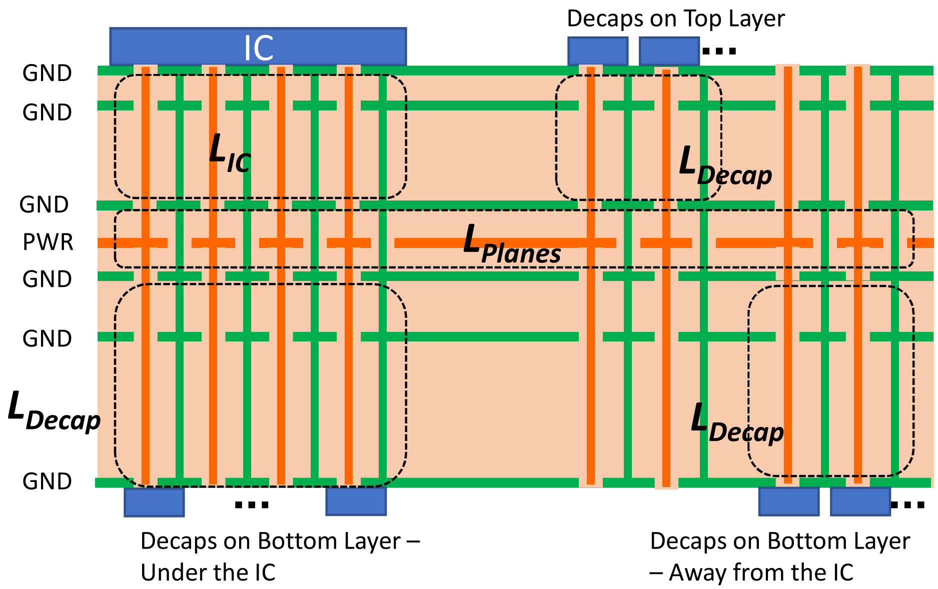
Connection Inductance for Typical Capacitor Configurations

Distance into board to planes (mils)	0805 typical/minimum (148 mils between via barrels)	0603 typical/minimum (128 mils between via barrels)	0402 typical/minimum (106 mils between via barrels)
10	1.2 nH	1.1 nH	0.9 nH
20	1.8 nH	1.6 nH	1.3 nH
30	2.2 nH	1.9 nH	1.6 nH
40	2.5 nH	2.2 nH	1.9 nH
50	2.8 nH	2.5 nH	2.1 nH
60	3.1 nH	2.7 nH	2.3 nH
70	3.4 nH	3.0 nH	2.6 nH
80	3.6 nH	3.2 nH	2.8 nH
90	3.9 nH	3.5 nH	3.0 nH
100	4.2 nH	3.7 nH	3.2 nH

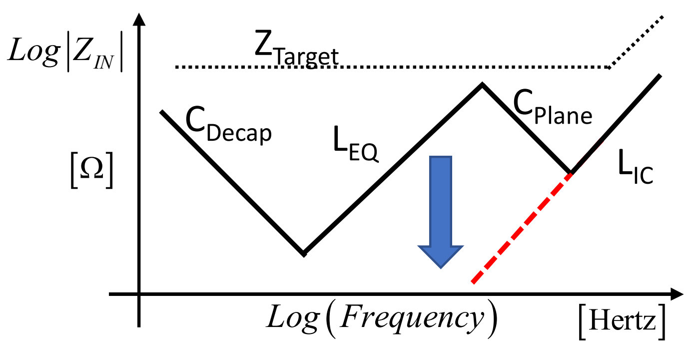
Connection Inductance for Typical Capacitor Configurations with 50 mils from Capacitor Pad to Via Pad

Distance into board to planes (mils)	**0805 (208 mils between via barrels)**	**0603 (188 mils between via barrels)**	**0402 (166 mils between via barrels)**
10	1.7 nH	1.6 nH	1.4 nH
20	2.5 nH	2.3 nH	2.0 nH
30	3.0 nH	2.8 nH	2.5 nH
40	3.5 nH	3.2 nH	2.8 nH
50	3.9 nH	3.5 nH	3.1 nH
60	4.2 nH	3.9 nH	3.5 nH
70	4.5 nH	4.2 nH	3.7 nH
80	4.9 nH	4.5 nH	4.0 nH
90	5.2 nH	4.7 nH	4.3 nH
100	5.5 nH	5.0 nH	4.6 nH

L_{Decap} L_{IC} definition

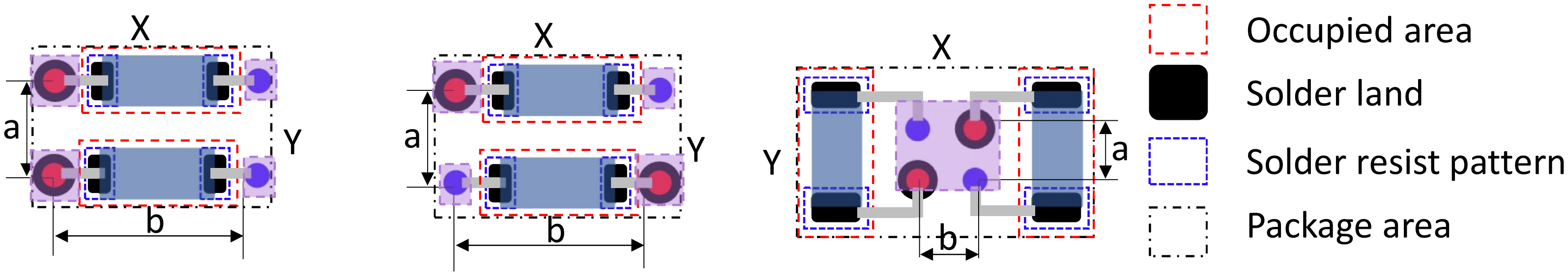


High-layer count PCB PDN geometry stack-up and L_{Decap} , L_{IC} definition.



$$L_{EQ} = L_{IC} + L_{Decap} + L_{Planes} + M_{IC.Decap}$$

Layout Options(mils, KEMET)

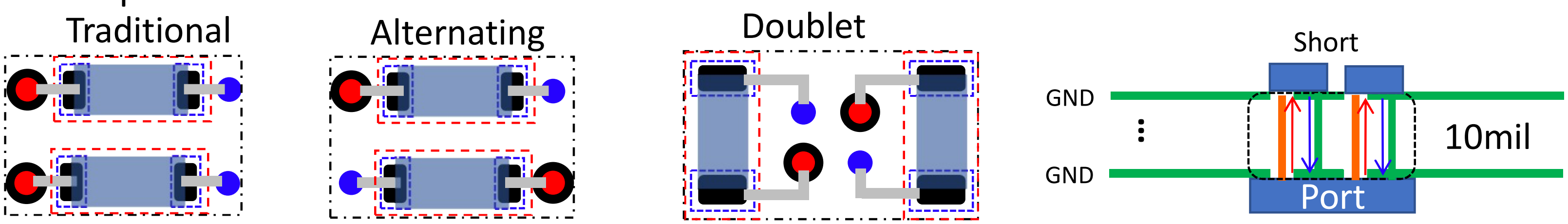


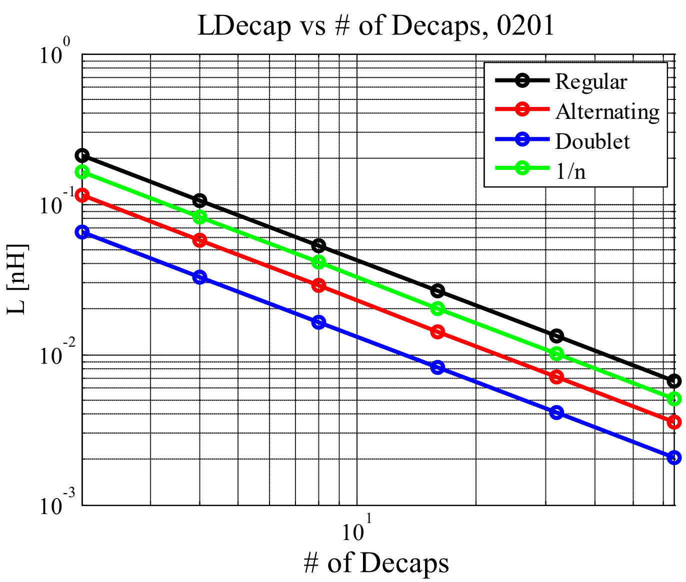
traditional alternating doublet

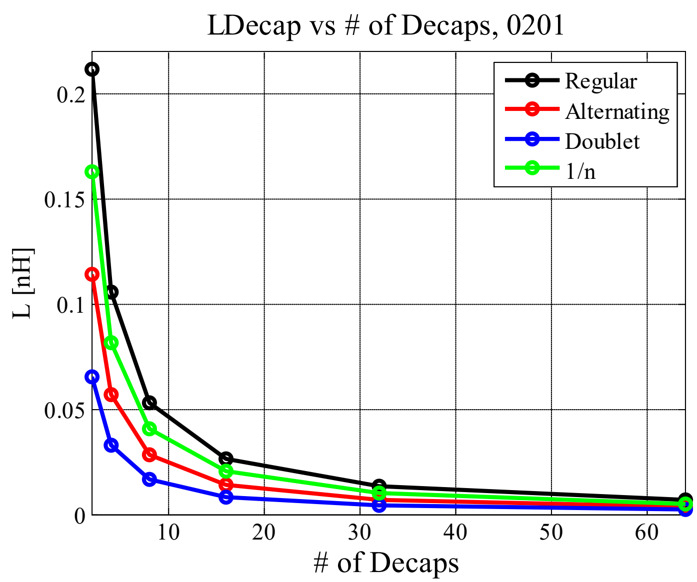
Drill size: 8mils, anti-pad size: 25.5mils, pad: 16mils, min Space :5mils

Decap layout	Decap size	X	Y	Keep out region
Alternating / Regular	0201	132	85	2*(antipad+minSpace)^2 2*(pad+minSpace)^2 => 2* 930 mil^2 + 2* 441 mils^2 = 2742 mils^2= 1.76mm^2
	0402	148	101	
	0603	219	171	
	0805	235	211	
Doublet	0201	96.5	71	(1.5*antipad_D+pad_R+minSpace)^2 => 2627 mils^2= 1.69mm^2
	0402	104.5	87	
	0603	139.5	158	
	0805	159.5	174	

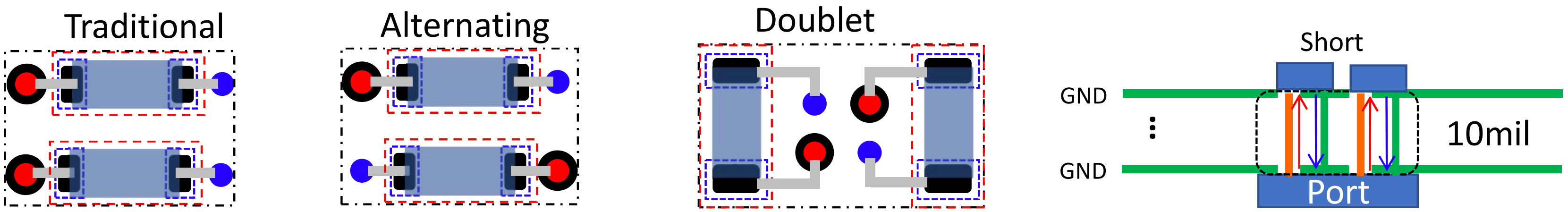
L_{Decap} comparison (h=10mils, 0201) Normalized

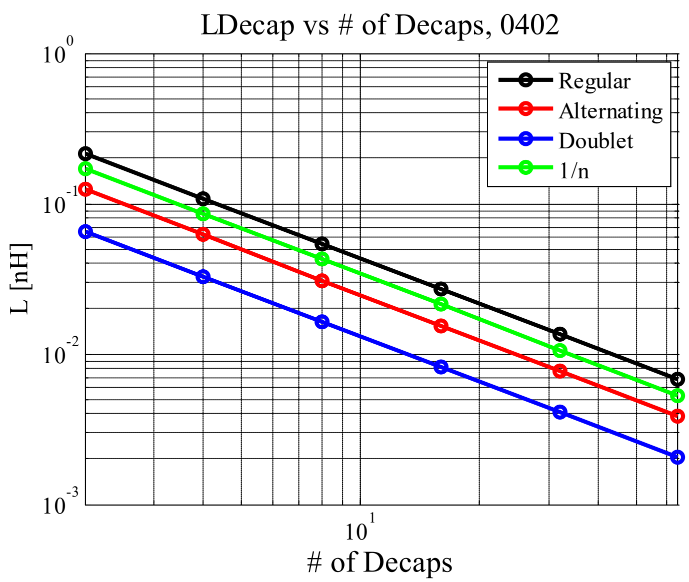


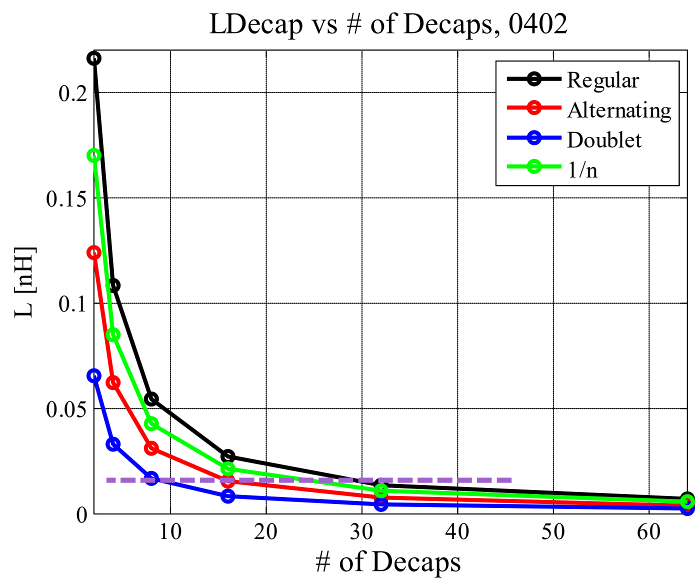




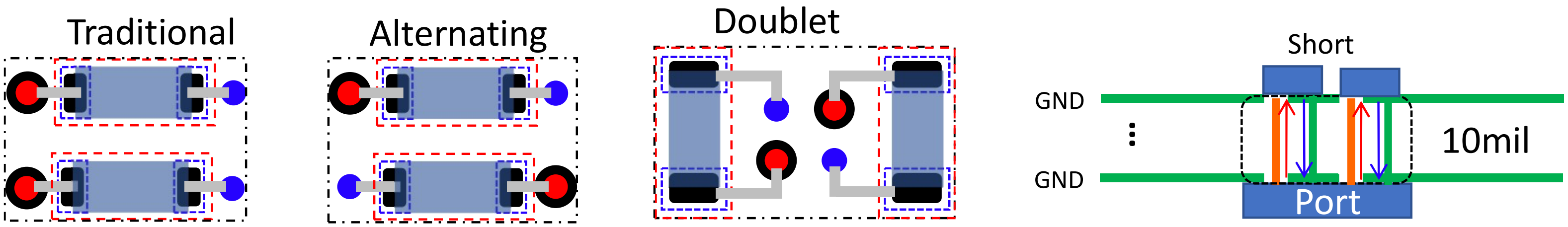
L_{Decap} comparison (h=10mils, 0402) Normalized

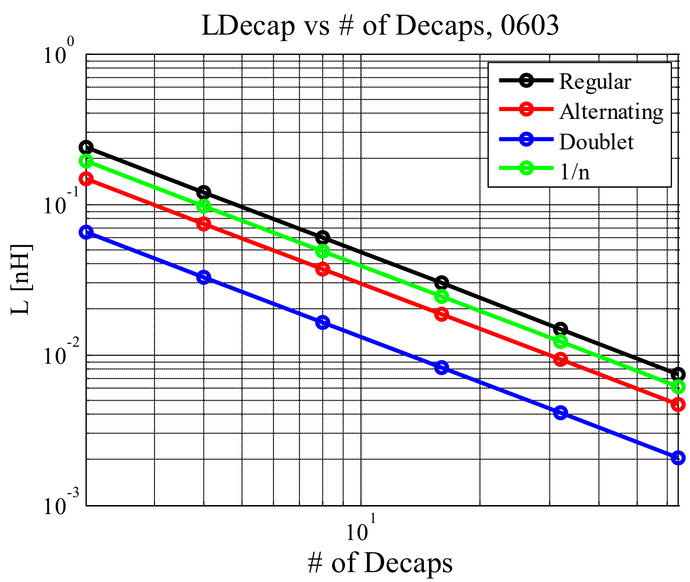


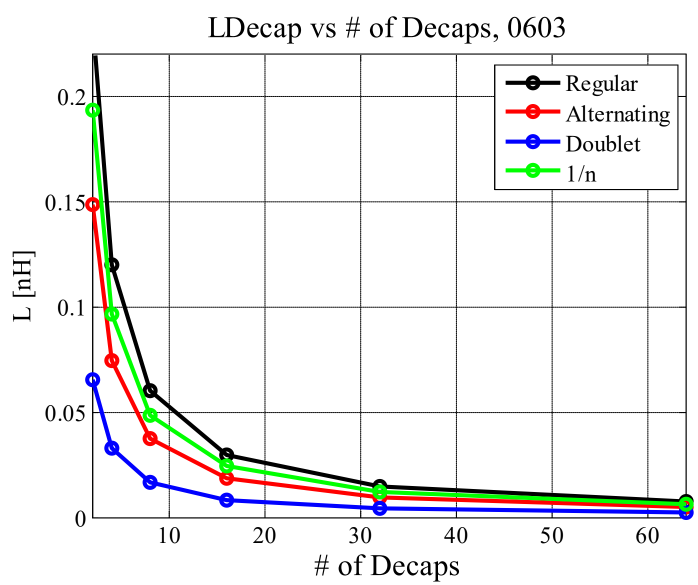




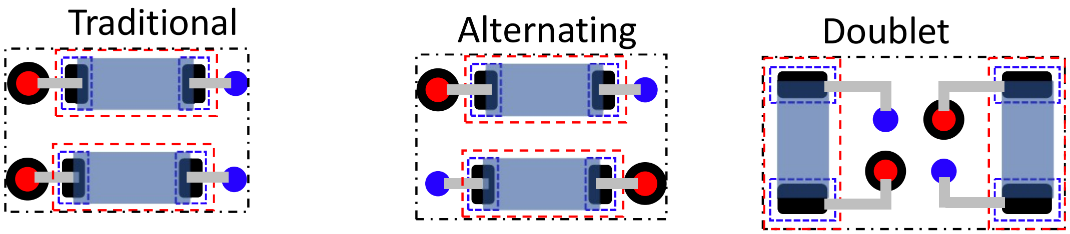
L_{Decap} comparison (h=10mils, 0603) Normalized

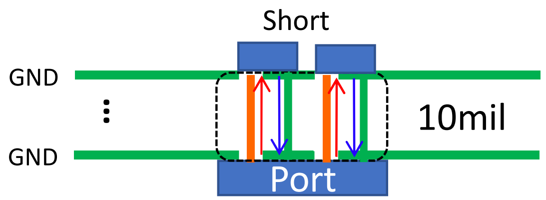


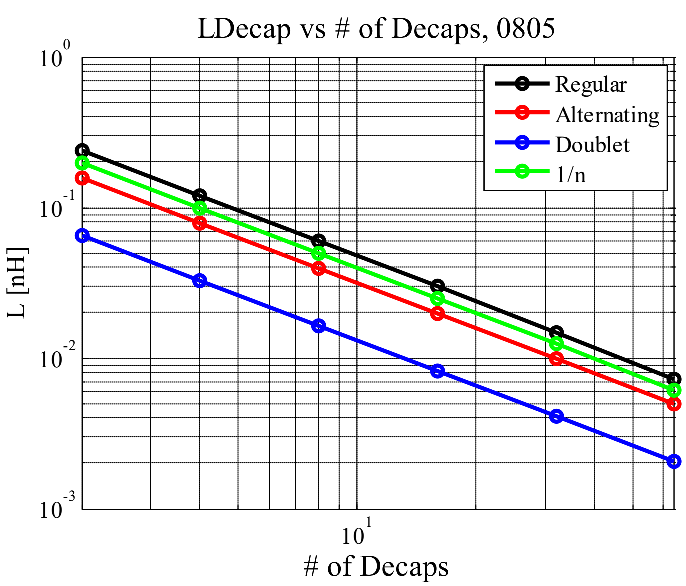


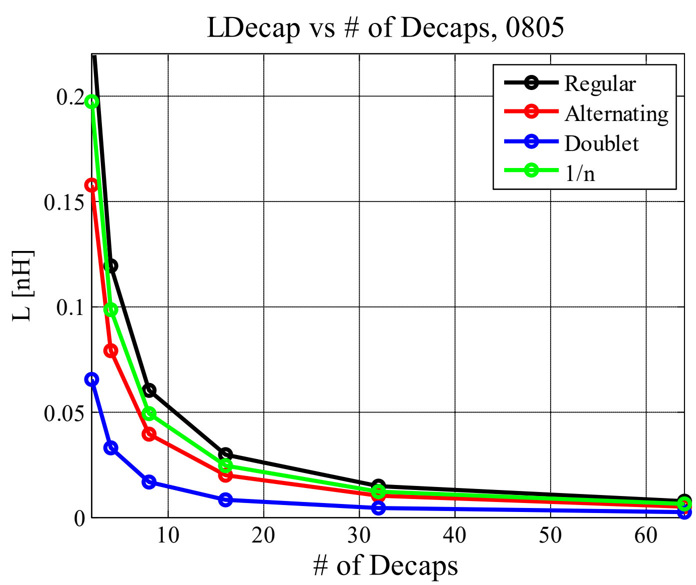


L_{Decap} comparison (h=10mils, 0805) Normalized









Summary

- Loop area is most important
- Via distance to capacitor pad MATTERS
- Wire size is a minor factor
- Capacitor physical size matters