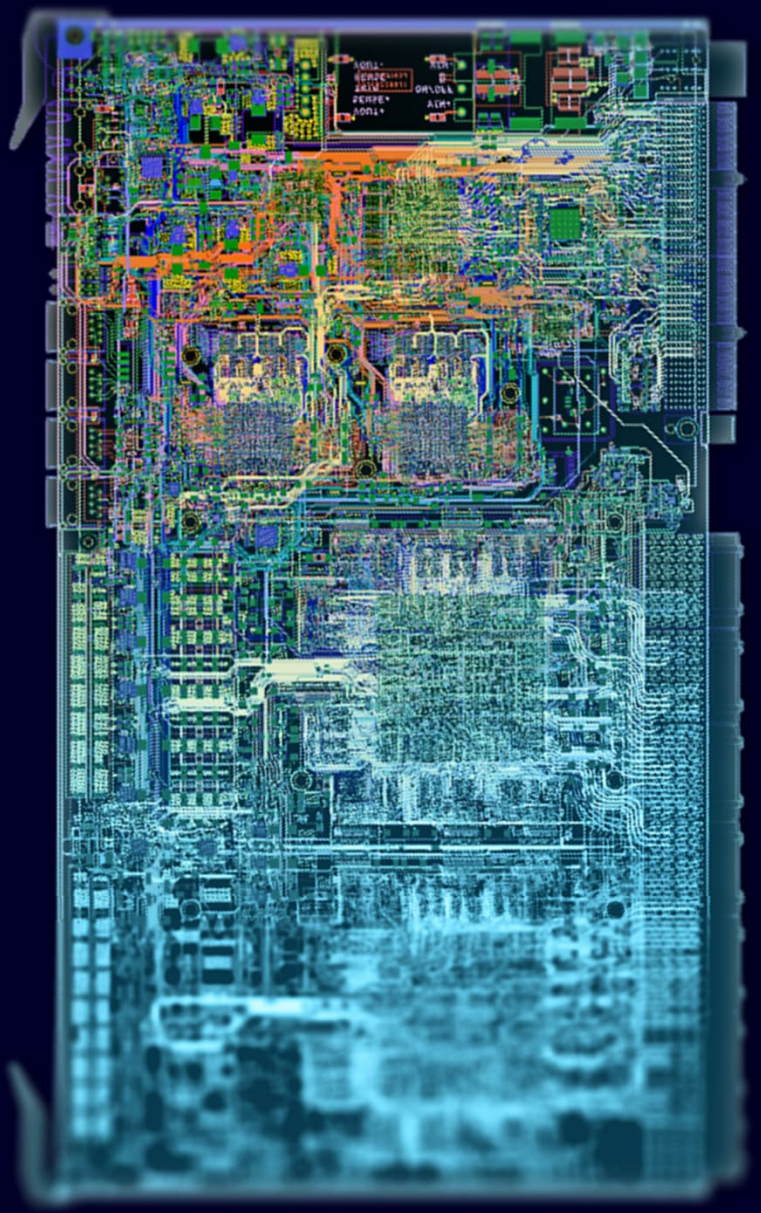
# Optimizing Engineering to Manufacturing Efficiencies



Stephen V. Chavez, MIT, CPCD, CID+

November 2025

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# Introduction - Bio

30+ years of industry experience: PCB Design SME, Educator, Author, Podcast Host, Blogger and Entrepreneur

- Co-Founder and Chairman – Printed Circuit Engineering Association (PCEA)
- Co-Author and Master Instructor of PCEA Training (CPCD Certification)
- IPC Certified Master Instructor (MIT) – PCB Design Certification (CID/CID+)
- Advanced PCB Design certifications: CID+ and CPCD
- Committee Member IPC-2221/2222, IPC-6019, and IPC-2229 Standards
- Published Author: Technical White Papers, Articles, Columns, Blogs
- Host of The Printed Circuit Podcast
- A.S. Degree in Mathematics
- Military Veteran – U.S. Marine Corps – Avionics Technician

LinkedIn Profile:

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Printed Circuit Podcast: https://blogs.sw.siemens.com/podcasts/category/printed-circuit/
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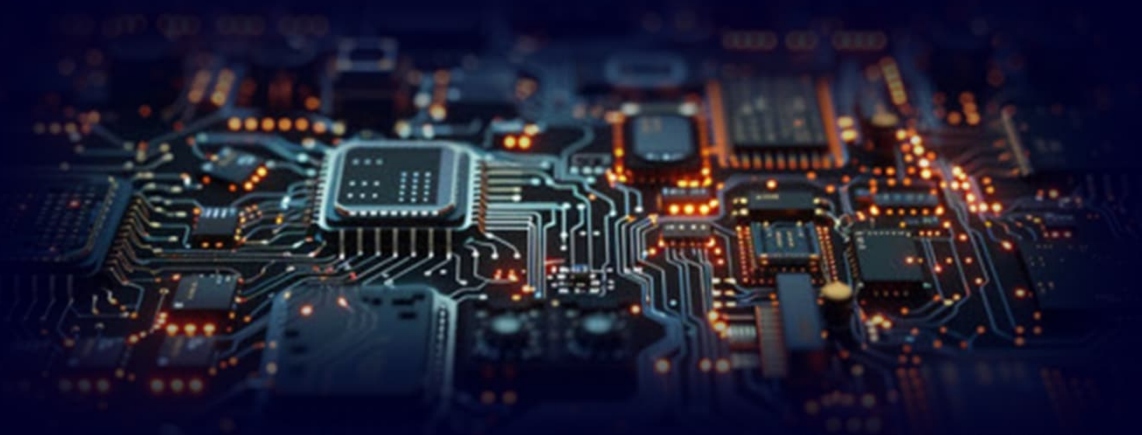

(Images courtesy of Iconnect007)

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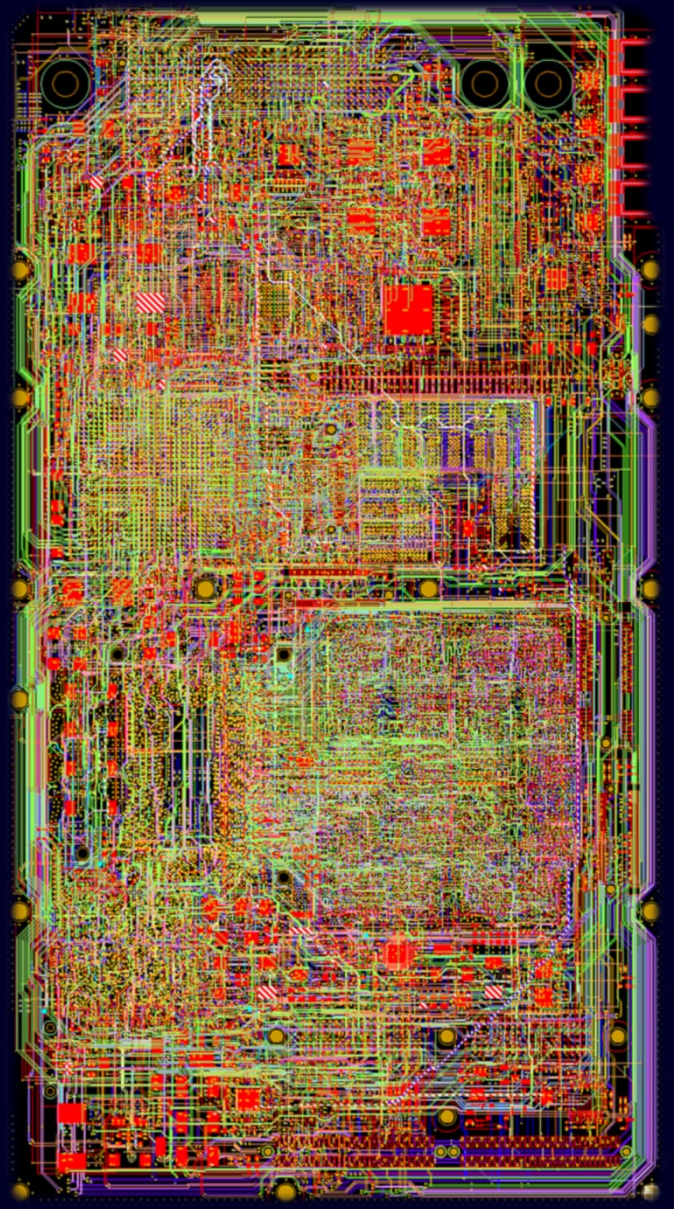
# The state of design in electronics



Design teams **must deliver more complex products** on **even more compressed schedules**, but they **lose valuable time** with unproductive tasks. **Connect them** through all **engineering disciplines** and give them **best-in-class solutions** to thrive with a **collaborative** approach to **Electronic Systems Design**.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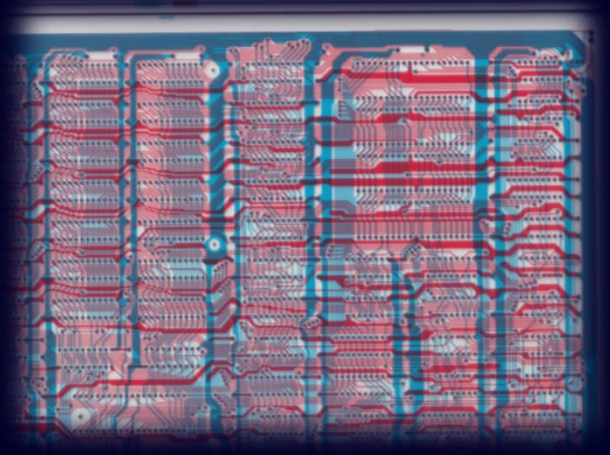
# Complexity in PCB Design has evolved...

Designing PCBs in 1984

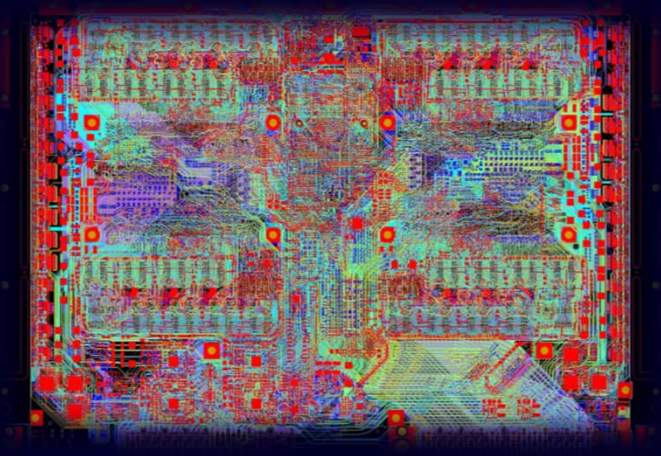
Image from *Rick Hartley at 39yrs old laying Red and Blue tape on 6mil (0.15mm) thick mylar. Blue tape formed the copper features on the top layer of the board, Red tape was the bottom layer.*

2 Layer PCB - 1984



1984 2-layer PCB Design – Rick Hartley

18 Layer PCB - 2022



2022 XTIA Winner – ABACO Systems

100Gbps High-speed Design – Military & Aerospace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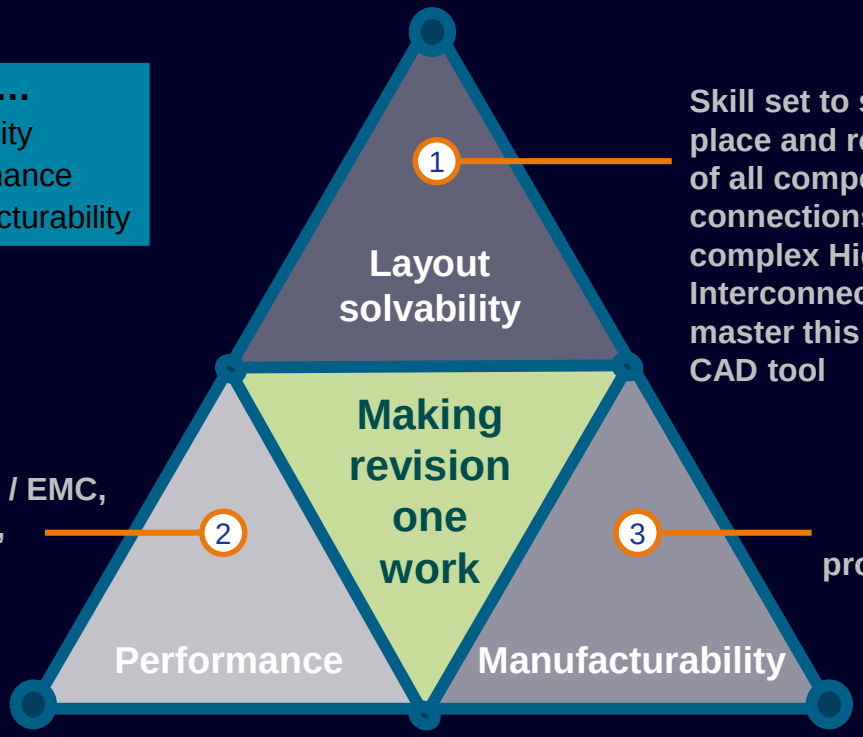
# Three Key Perspectives of Success in PCB Design

Today's circuit engineer must meet three competing perspectives for success

**Design for…**
- **DFS**olvability
- **DFP**erformance
- **DFM**anufacturability




Skill set to solve the place and route of all components and connections often with complex High-Density Interconnect (HDI)…and master this on your CAD tool

Signal Integrity / EMC, Power Delivery, Thermal

DFX (DFM) all considerations producing high yield and lower cost

## IPC-22XX 1.X. Definition for Printed Circuit Engineering Layout Professional

**The result** provides for maximum component placement/routing density achievable, optimum electrical performance and efficient, high yield, defect free manufacturing.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## Manufacturing (DFM)

**Problem!**

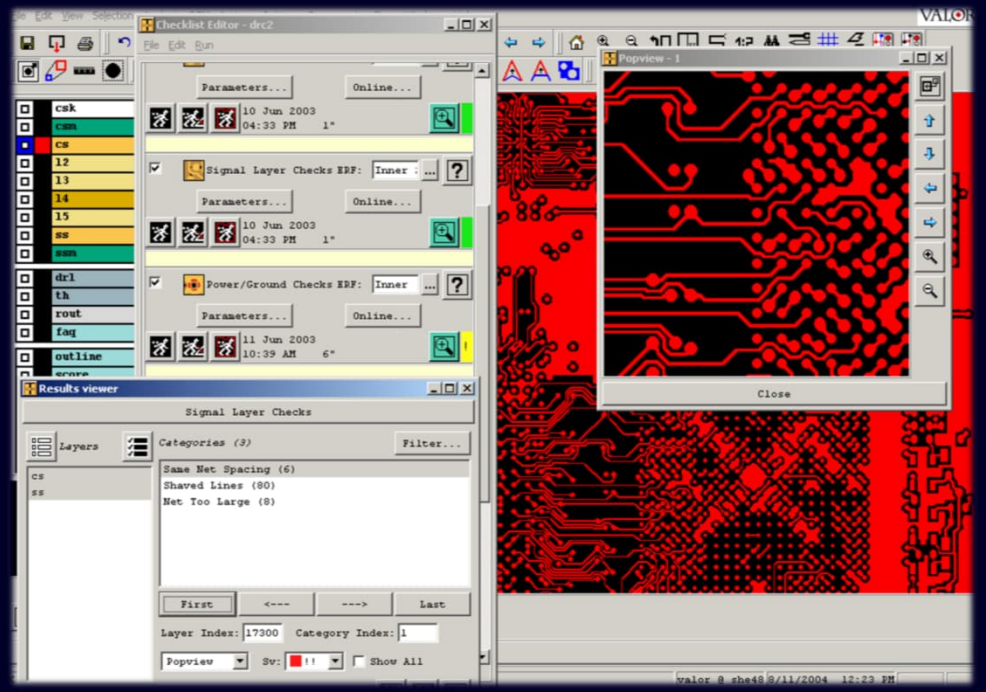
# Manufacturing is a after thought or worse…not accounted for

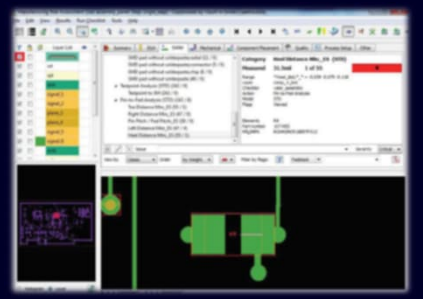
**Roadblocks!**

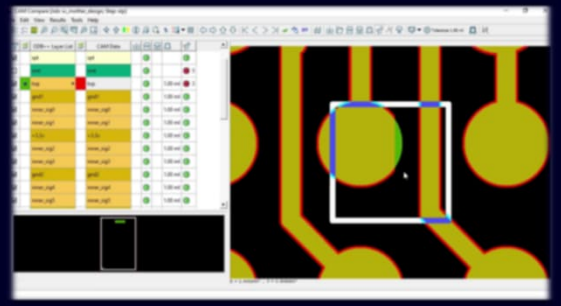
- Component Placement (to close, no routing channels, etc.)
- Mixed technology (TH/SMT, via types, material, etc.)
- Component library creating not to industry standard (IPC, Best practices, etc.)
- Best practices not implemented (placement/routing)

**Best Practice**

- Implement DFM from beginning
- Implement industry best practices
- Collaborate with your supplier(s)



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## Manufacturing – DFM & Producibility

**Problem!**

# Data not addressing producibility or manufacturability passed to manufacturing

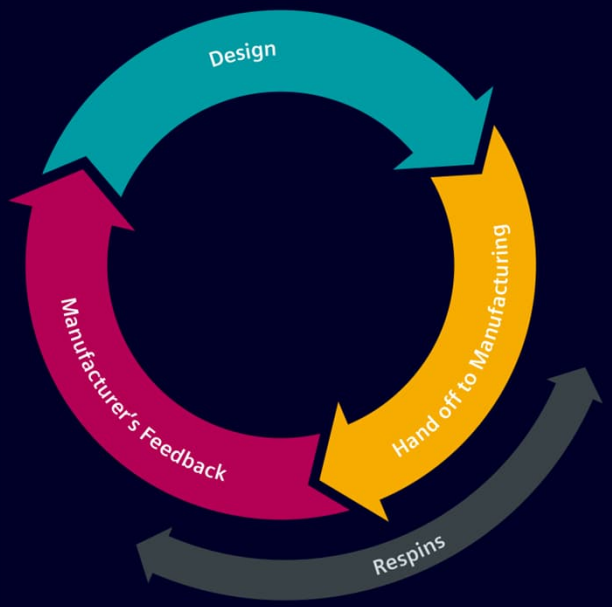
**Roadblocks/Inhibitors!**

- Competitive pressure on Fab house to accept poor data
- No time to run DFM analysis

Best Practice

- Optimize integration between design and MFG
- Enable lessons learned in MFG to influence designs (enable feedback loop)
- Perform DFM Analysis – Don't skip this step!
- Utilize intelligent data format (ODB++, IPC-2581)

*Traditional iterative design flow*




*Concurrent DFM*



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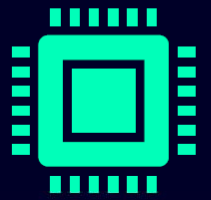
# Manufacturing – Design for Manufacturing Study

## Volume and Speed of PCB Design Processes

**+2.9**

On average, a PCB design undergoes 2.9 respins at an average material cost of $28k per respin

**+$28k**



**⬆49%**

Companies using DFM software produce 49% more PCB designs per year compared to non-users

**⬇12%**

Companies using DFM software take 12% less time to develop PCB designs from the completion of schematic to manufacturing release

- On average, a PCB design undergoes 2.9 respins before going to volume production.
- These respins can often be avoided and are often due to manufacturability issues.
- When a design has to be reworked it takes an average of 2 weeks to complete at an average material cost of more than $28K per respin.
- You have likely heard of manufacturing scrap as material waste resulting from a production error.
- Design respins can be seen as engineering scrap - avoidable costs sunk into designs.
- DFM ensures that projects achieve quality goals, meet target costs, and are completed on time.

Source: Aberdeen, May 2023

DFM software users are able to design faster and have more productive PCB design processes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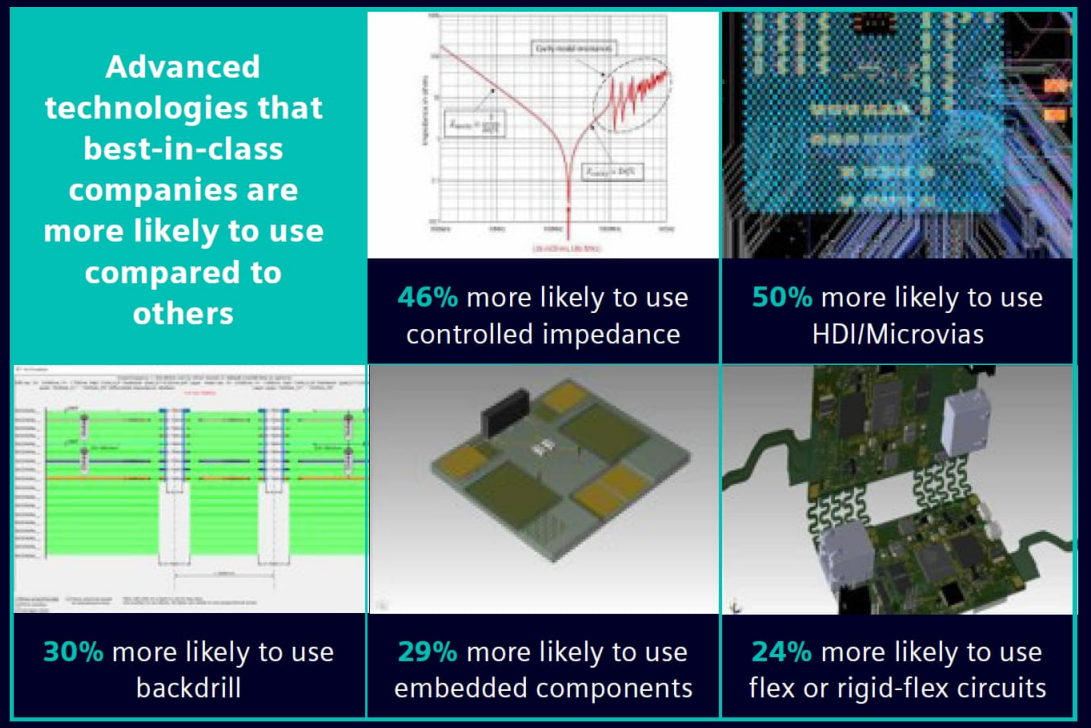
# Manufacturing - Design for Manufacturing Study

## Complex Designs Necessitate Best Practices

- Best-in-class companies are far more likely to be designing with advanced technologies.
- From controlled impedance to HDI via technologies, DFM software as part of an overall best practices mindset helps to ensure that PCB designs meet the necessary fabrication and assembly requirements.
- DFM software enables Best-in-Class companies to design more complex PCBs with more advanced technologies.




Source: Aberdeen, May 2023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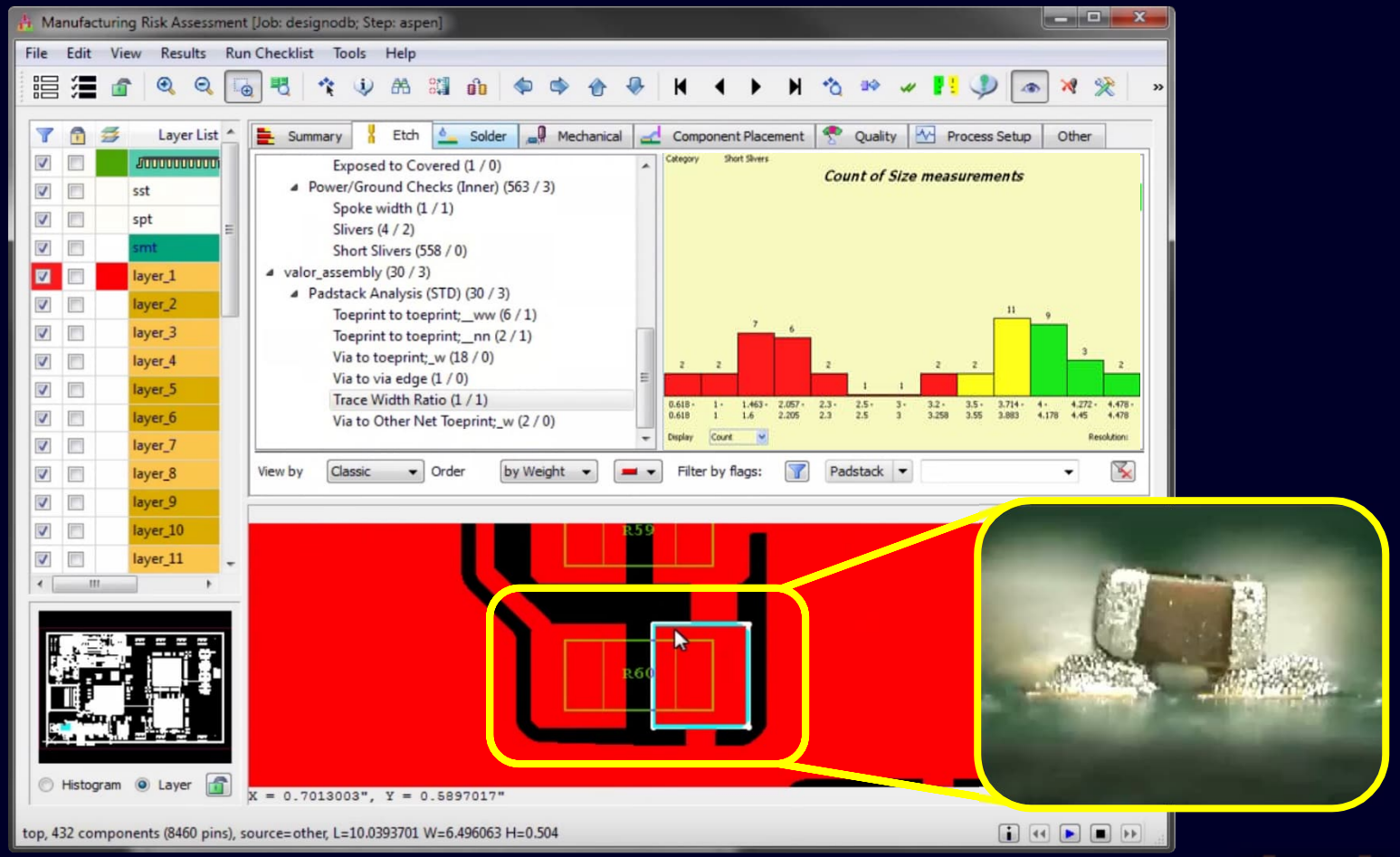
# Design For Manufacturing  “DFM – Assistive Technology”




- Simulation of the PCB Fabrication and Assembly process in order to identify manufacturability issues in advance, saving time and money. Don’t ship the DFM Analysis step in the process!
- DFM is assistive technology with the objective of preventing “catastrophic failures” – like Lane Assist in a car.
- Just as Lane Assist is more important when you’re going 80 miles per hour, DFM is more critical when using complex technologies such as HDI or UHDI.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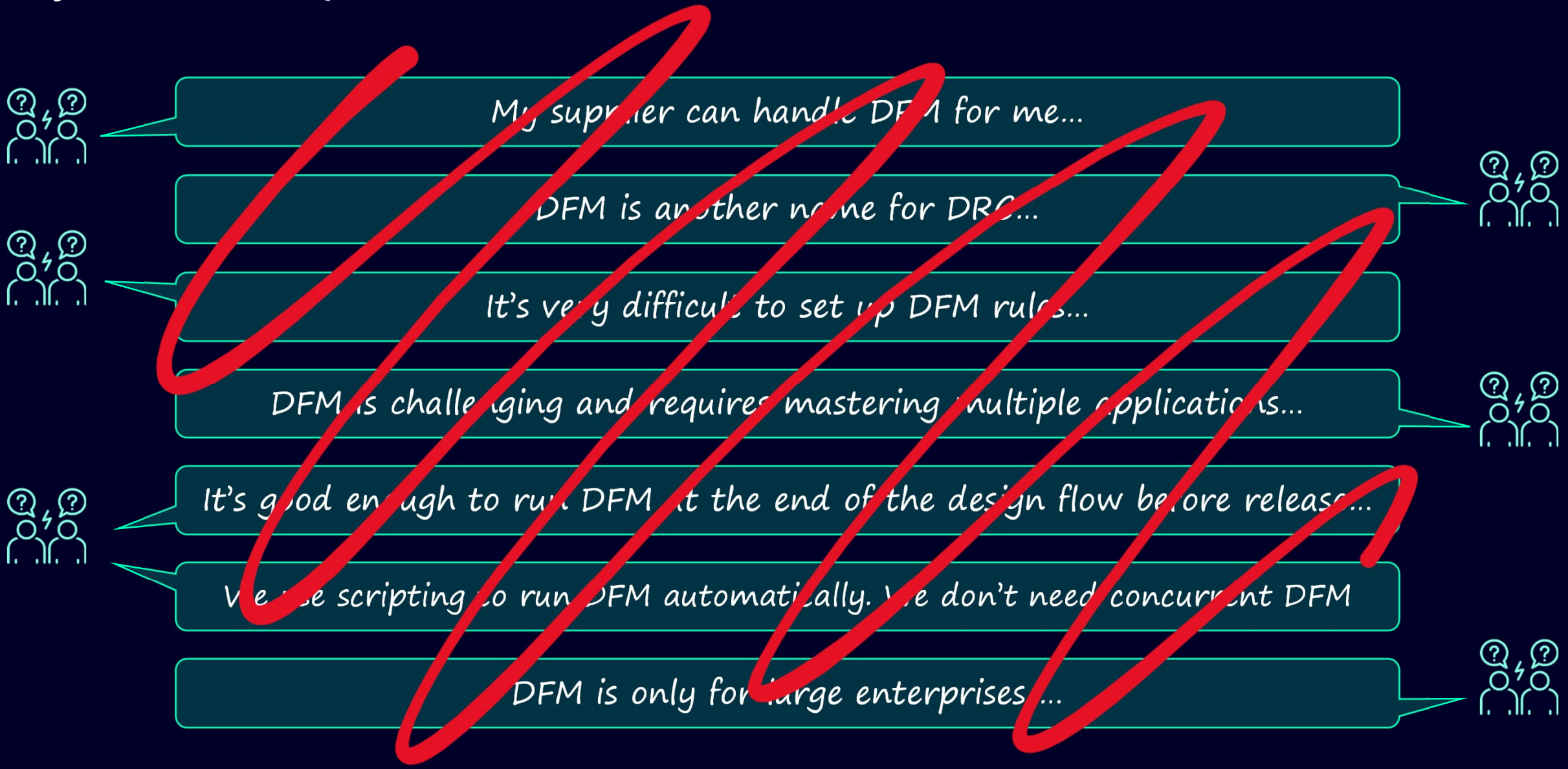
# Key DFM Misconceptions ……





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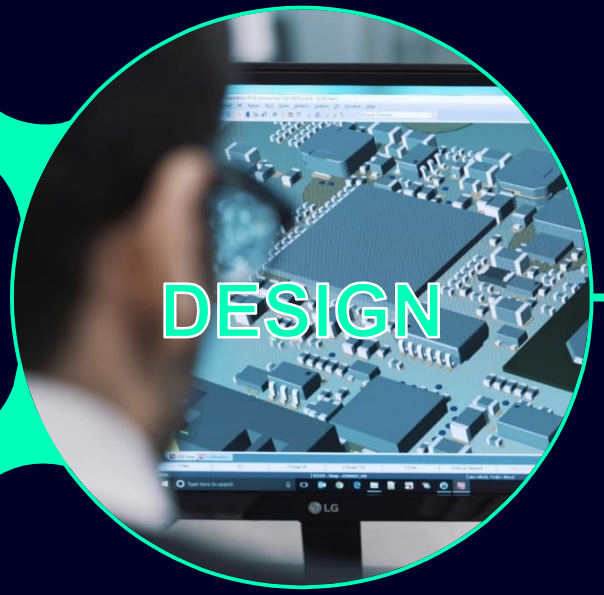
# DFM adds value to both sides of the PCB Design and Manufacturing flow

Prevent manufacturing violations

Eliminate re-spins (time & cost)





Optimize manufacturing process

Ensure manufacturing continuity

Protect margins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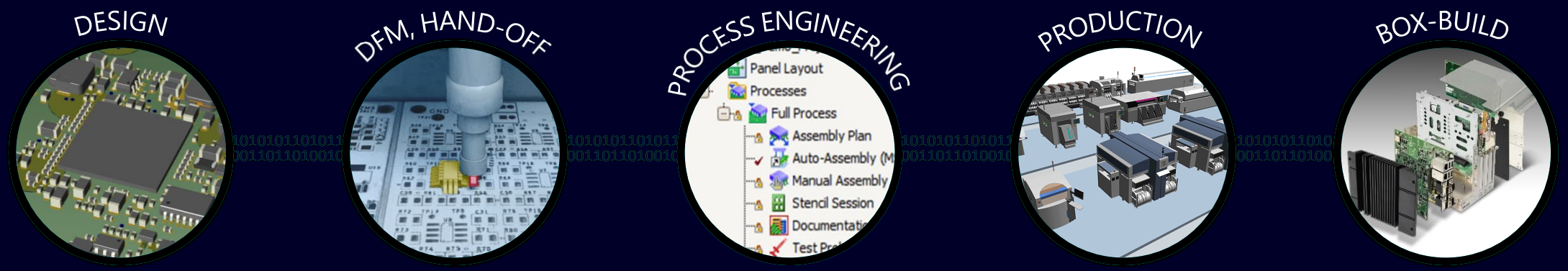
# DFM is essential to improve NPI with advanced technologies

Companies need to make manufacturing decisions early in the design process




*Can I Design it Better in advance?*

*Can I Manufacture It?*

*How to Manufacture it?*

*Can I Manufacture it Better?*

Design Oriented – DFM Analysis

Process Oriented – DFM Analysis

Manufacturing Oriented – DFM Analysis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# DFM complements DRC

~~DFM is another name for DRC...~~

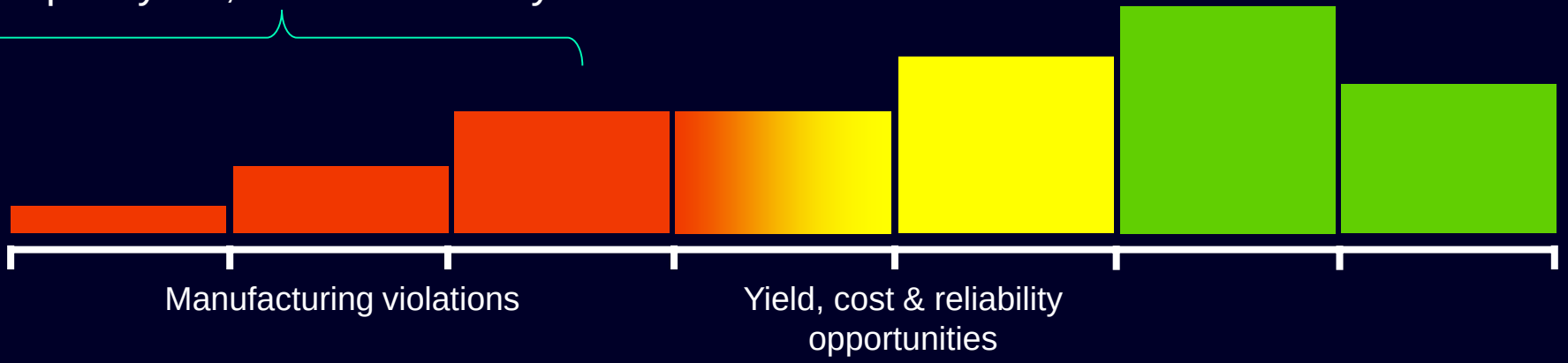
## DFM

DFM enables you to optimize your design for volume manufacturing during initial release

DFM is manufacturing facing - Check the design for issues that can impact manufacturing using rules aligned with your supplier's capabilities for chosen manufacturing processes

## DRC

An issue can pass DRC but still impact yield, cost or reliability.




**For example:**
Close spacing over an extended length affects yield and therefore costs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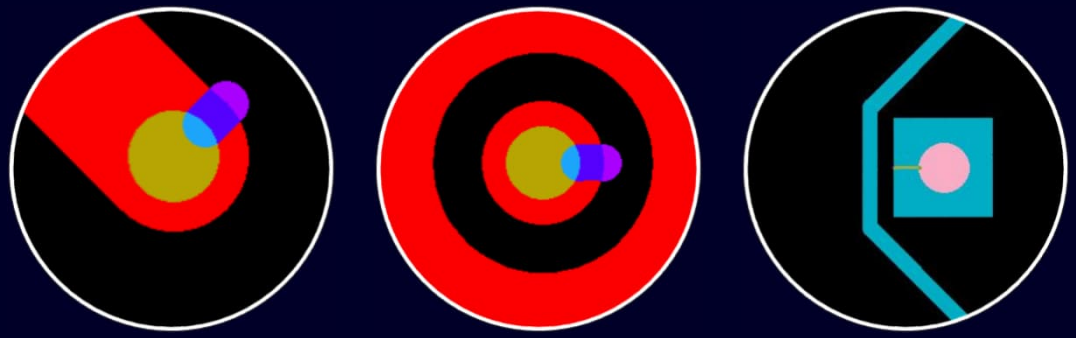
# DFM complements DRC

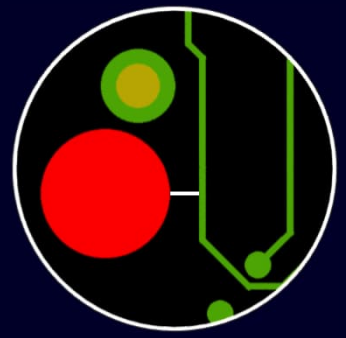
~~DFM is another name for DRC...~~

## Different manufacturing processes requires more specific checks



### Annular Ring

- DRC uses a minimum annular ring
- DFM analyzes annular ring size based on manufacturing process (Laser drilled via / Mechanically drilled TH / Backdrill)



### Drill to Copper Spacing

- DRC has drill to copper spacing
- DFM analyzes drill to copper spacing based on manufacturing process - PTH can be closer to trace than NPTH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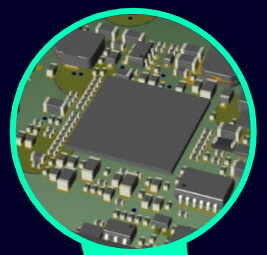
# Manufacturing Driven Design

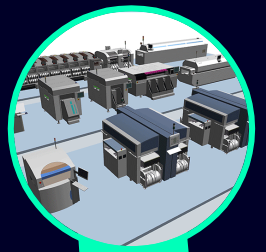
~~It's very difficult to set up DFM rules...~~



## 1. DESIGN FACTORS

**Use design technology to determine which DFM checks need to run**

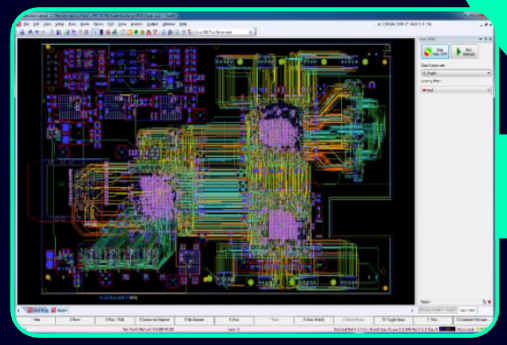
- Layer Types
- Spacing Intent
- Conductor width Intent
- Copper Weight
- Number of Layers
- etc.



## 3. MANUFACTURING CONSTRAINTS

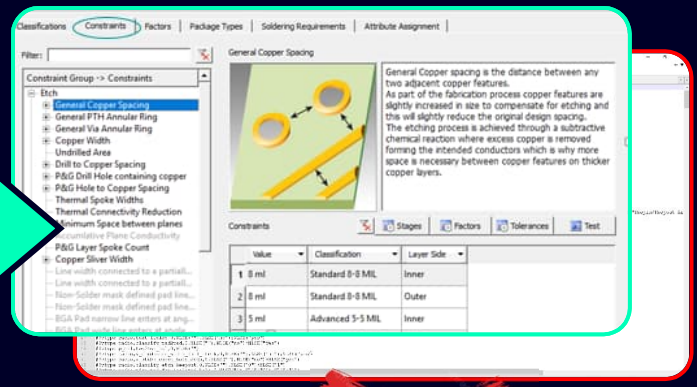
**Understand the manufacturing partner's capabilities & limitations**

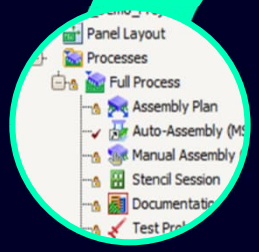
- Copper Spacing
- Annular Ring
- Plane Spacing
- Solder Mask Coverage
- Silk Screen Spacing
- Solder Volume
- Component Spacing
- Component Shadowing
- Test Access
- etc.



DESIGN

**INTELLIGENT DFM RULE DEFINITION**




## 2. DESIGN CLASSIFICATION

**Use process definition to determine applicable DFM rules**

- Technology Levels (Standard, Advanced, Micro-electronics)
- Single Sided SMT, Double Sided SMT
- Ground systems, Airborne systems
- IPC Class 1, 2, or 3
- Board characteristics such as typical line width
- etc.

~~Legacy ERF~~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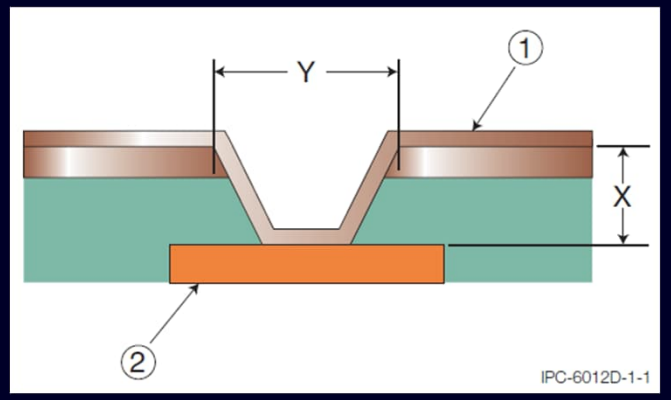
# Manufacturing Driven Design

~~It's very difficult to set up DFM rules...~~

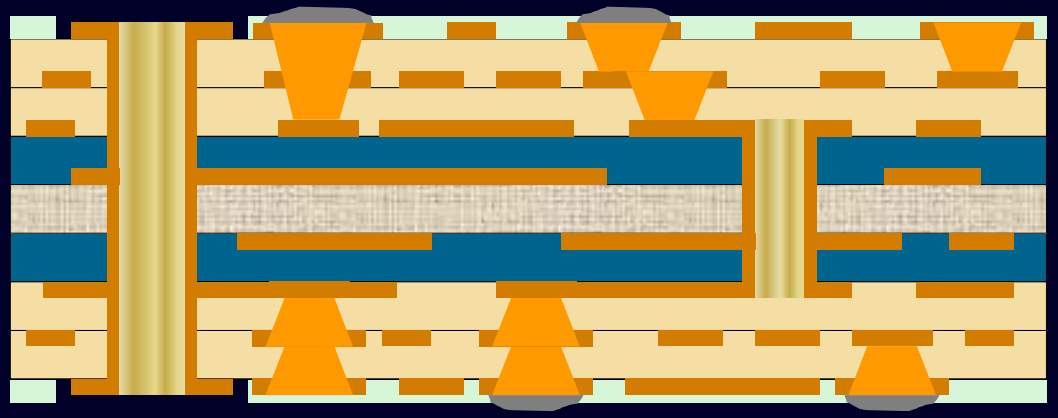
Using our manufacturing knowledge to automatically determine which DFM checks and rules to apply




## Example: Microvia

Determination is based on IPC standard

If Aspect Ratio <= 1.0 and Depth <= 9.84 mils,
then Microvia Analysis is automatically performed.



## Example:HDI

If Microvias are present and at least one layer is designated as buildup layer,
HDI DFM analysis is automatically executed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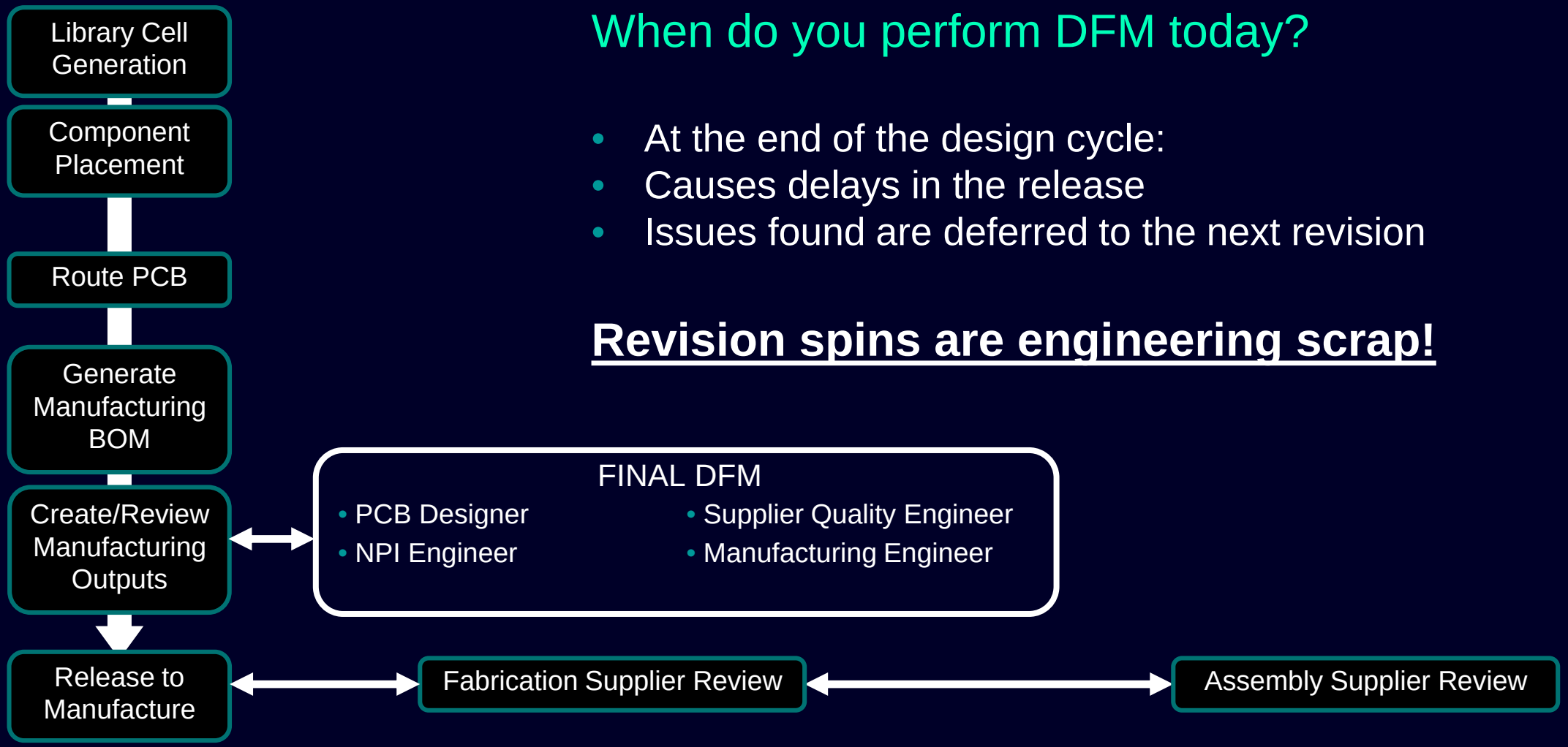
# Review and Release Process Today

~~It's good enough to run DFM at the end of the design flow before release...~~




## When do you perform DFM today?

- At the end of the design cycle:
- Causes delays in the release
- Issues found are deferred to the next revision

**Revision spins are engineering scrap!**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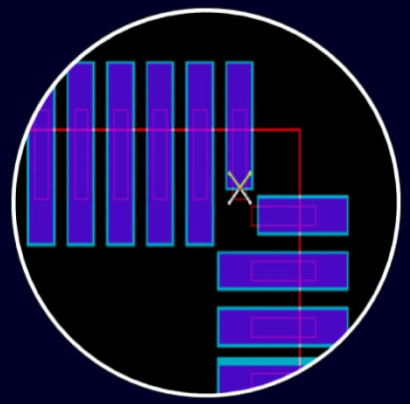
# Review and Release Process with Valor NPI

~~It's good enough to run DFM at the end of the design flow before release...~~

- Library Cell Generation
- Component Placement
- Route PCB
- Generate Manufacturing BOM
- Create/Review Manufacturing Outputs
- Release to Manufacture

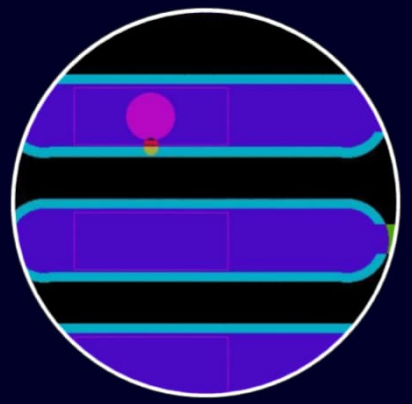
## Library Cell Review

- Cell validation of new library parts is a manual, time-consuming process
- Valor Parts Library can be used with manufacturing rules to validate cells



Pin overhanging soldermask can cause solder bridging


If orientation mark is wrongly placed, the component will be placed incorrectly



Pins too wide for pads can lead to insufficient side fillets of solder joints

Gangmask is required for fine-pitch devices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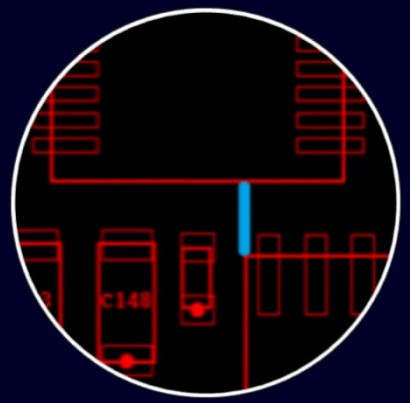
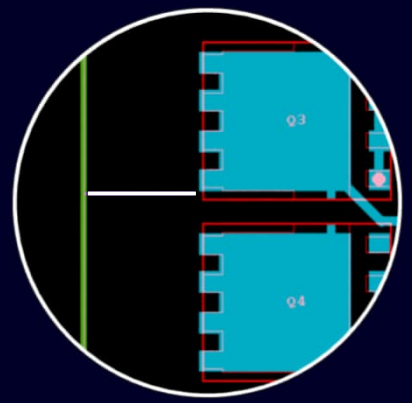
## Component Placement Review

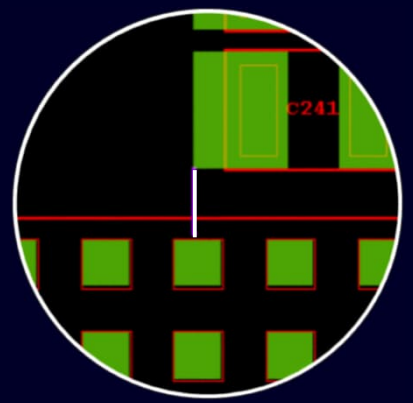
- Lock in placement for manufacturability before you start routing copper
- Validates placement against assembly processes

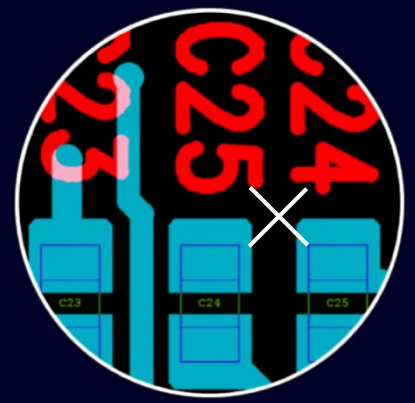



Component clearance requirements vary by type, orientation and placement machine




Toeprint too close to conveyed edge can be damaged by SMT gripper





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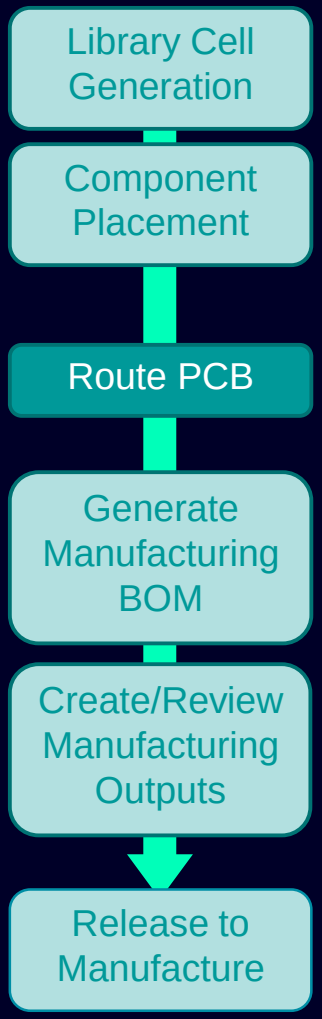


## Route Review

- Running DFM concurrent with PCB design accelerates the release process
- Common fabrication issues are identified and addressed immediately by the Designer

Slivers can cause repeat defects due to photo-resist flaking

Starved thermals prevent proper heat containment, affecting quality of via solder connection

Undetected copper slivers can cause net shorts

Circuits close to a pad must be fully covered by mask to avoid solder bridging during the assembly process


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# Review and Release Process with Valor NPI

~~It's good enough to run DFM at the end of the design flow before release...~~

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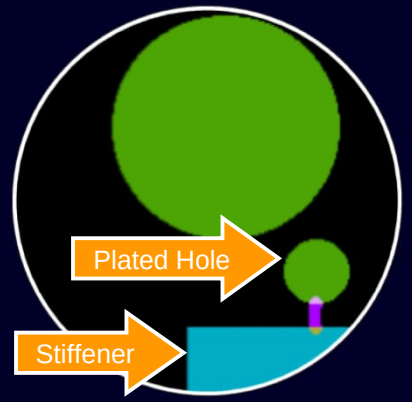
## Route Review

Flex and rigid-flex

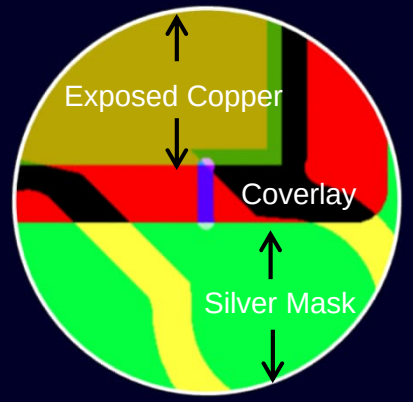
- Flex and rigid-flex circuits have their own manufacturing requirements
- Unique checks are required to identify potential issues

Conductors should be perpendicular across the entire bend area




Plated holes too close to a stiffener can lead to cracks in the barrel

Rigid area copper close to interface area can cause copper to crack




Silver mask must remain clear of exposed copper to avoid EMI issues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# Review and Release Process with Valor NPI

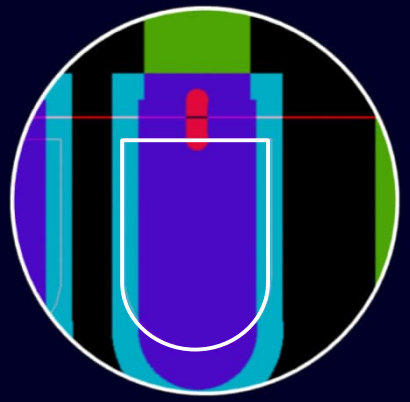
~~It's good enough to run DFM at the end of the design flow before release...~~

- Library Cell Generation
- Component Placement
- Route PCB
- **Generate Manufacturing BOM**
- Create/Review Manufacturing Outputs
- Release to Manufacture

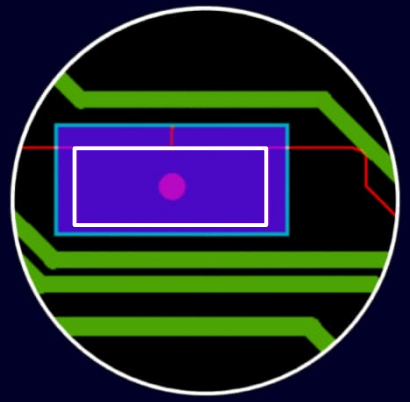
## Manufacturing BOM Review

CAD/manufacturing BOM validation

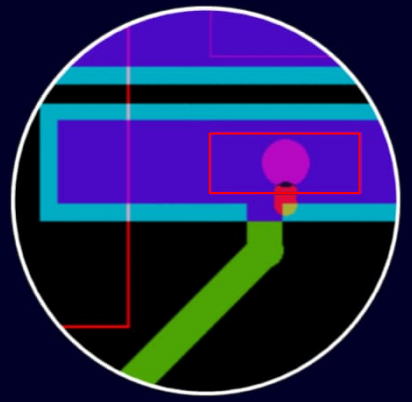
- Assures there are no refdes or quantity mismatches
- Validates sufficient solder joints for selected and qualified parts



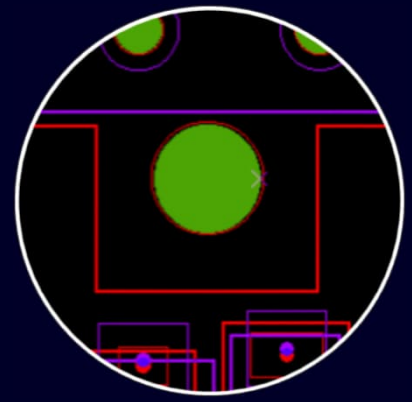
Insufficient heel distance will lead to a weak solder joint



Insufficient toe distance and even the ratio of heel/toe affect the quality of a solder joint



Side solder fillets are also a factor in the quality of a solder joint



Actual component body (red) covers mounting hole that CAD package (purple) didn't detect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# Review and Release Process with Valor NPI

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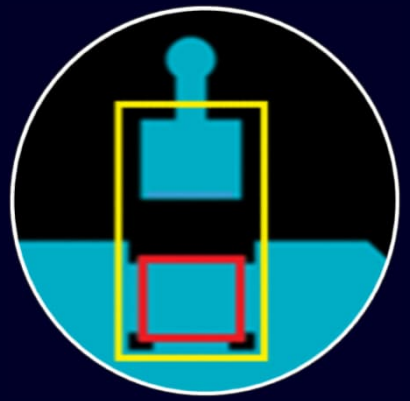
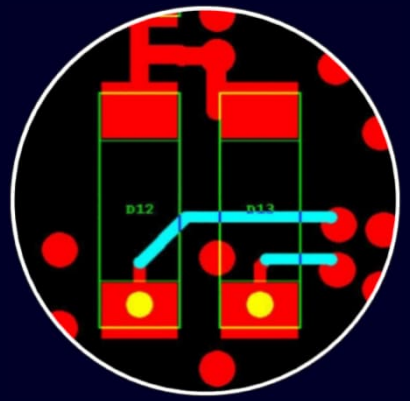
- Create/Review Manufacturing Outputs
- Release to Manufacture

## Manufacturing Package Review

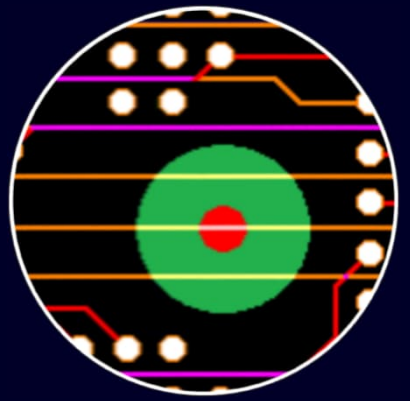
- Final review brings all elements together (CAD, BOM, Netlist)
- Validate no issues have been edited into design



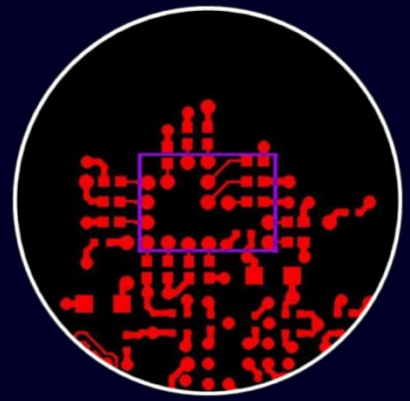
Different trace widths connecting pads can cause the component to tombstone during reflow




Traces under a zero-offset device may cause the component to rock, causing a poor solder joint



Adjacent layer copper makes it difficult for SMT equipment to identify local fiducials



Too many testpoints within an area will stress the PCB, potentially affecting the solderjoints in the area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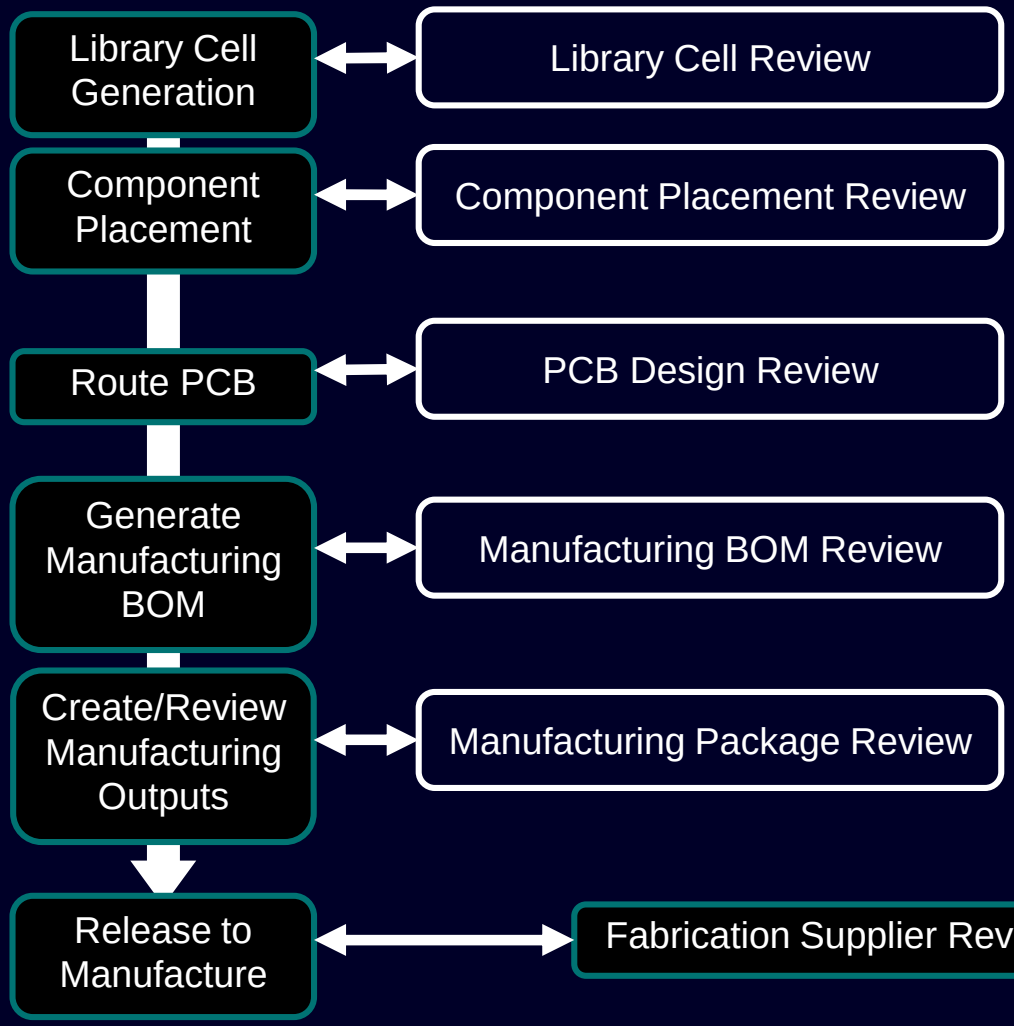
It's good enough to run DFM at the end of the design flow before release...

# Review and Release Process with Embedded DFM




- Embed DFM as part of design flow and review
- Find critical issues early on
- Run only applicable checks in every stage
- Very limited burden/hassle for designer
- All rules can be managed centrally for the group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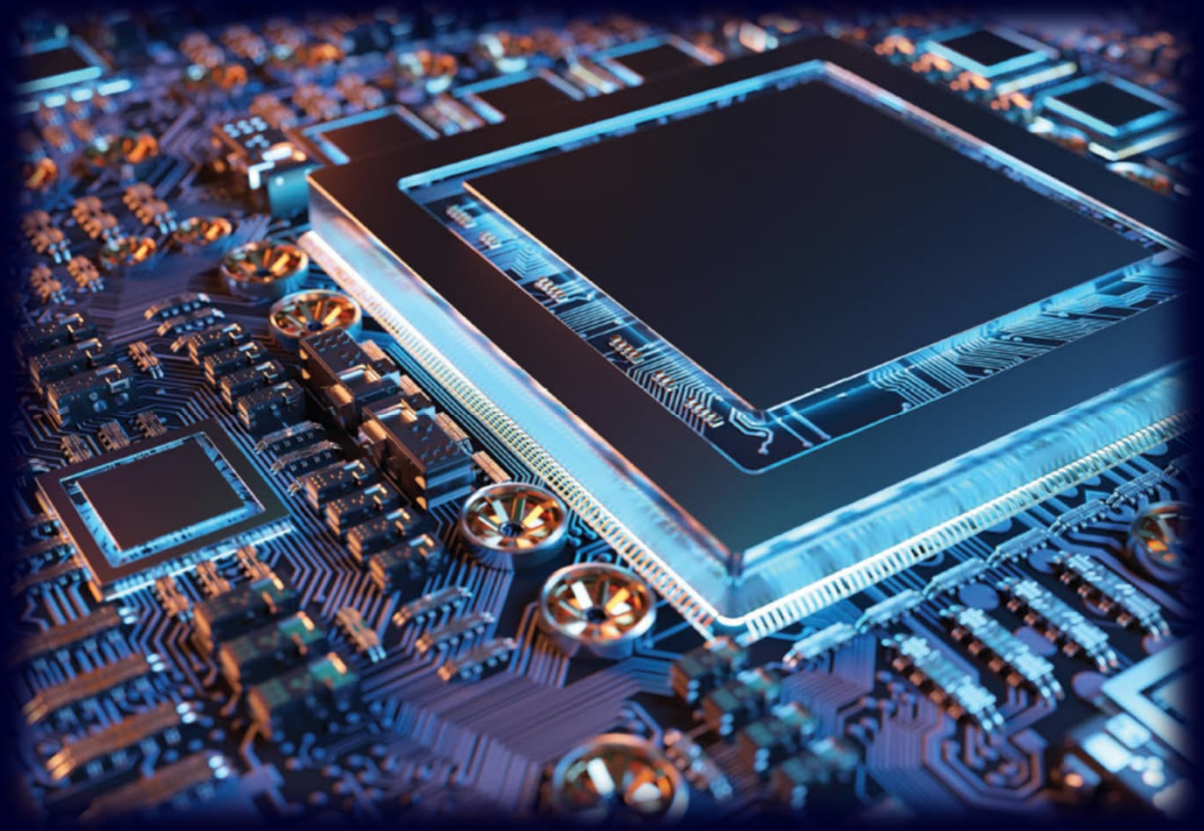
# Summary

## Optimizing Engineering to Manufacturing Efficiencies

- Design teams must deliver more complex products on even more compressed schedules, and with less resources
- Must address the three perspectives of PCB design
- Perform DFM Analysis – Don’t skip this step!
- Implementing best practices have huge benefits and increased ROI
- Understand the impact of decisions made upstream and their effects down stream in manufacturing
- Multidiscipline and multidomain collaboration and integration is key (this includes external suppliers)
- Utilize today’s EDA tool automation and horsepower to your advantage
- Be open to new methodologies, AI, ML and Cloud-based connectivity

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# Questions?

# Thank You!

Link to: Electronic Systems Design

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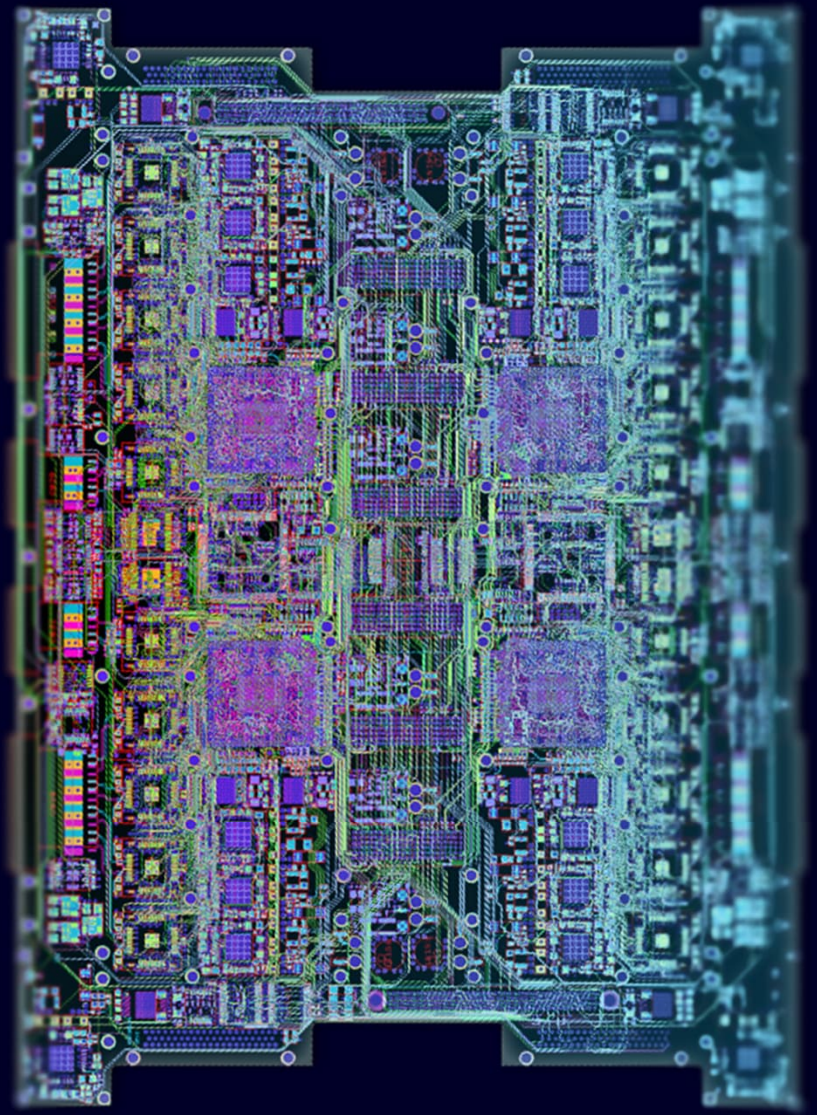


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