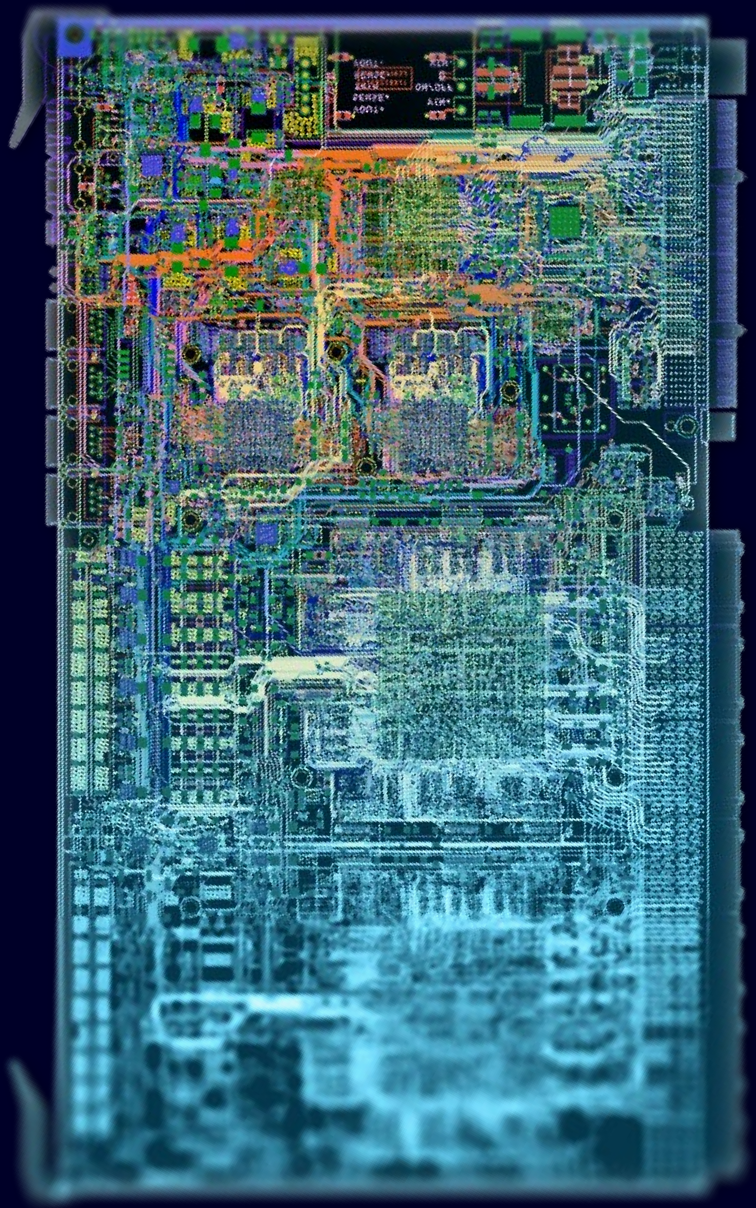
Designing Complex PCBs

Key Considerations, Methodologies, and Emerging Trends

Stephen V. Chavez, MIT, CID+, CPCD

October 2024



Introduction - Bio

30+ years of industry experience: Educator, Author, PCB Design SME, Podcast Host, Blogger and Entrepreneur

- Co-Founder and Chairman – Printed Circuit Engineering Association (PCEA)
- Co-Founder/Author/Instructor of PCE-Edu CPCD Curriculum - Now known as PCEA Training
- IPC Certified Master Instructor (MIT) – PCB Design Certification (CID/CID+)
- Advanced PCB Design certifications: CID+ and CPCD
- Committee Member IPC-2221/2222 Standard
- Published Author: Technical White Papers, Articles, Columns, Blogs
- Host of The Printed Circuit Podcast
- A.S. Degree in Mathematics
- Military Veteran – U.S. Marine Corps – Avionics Technician

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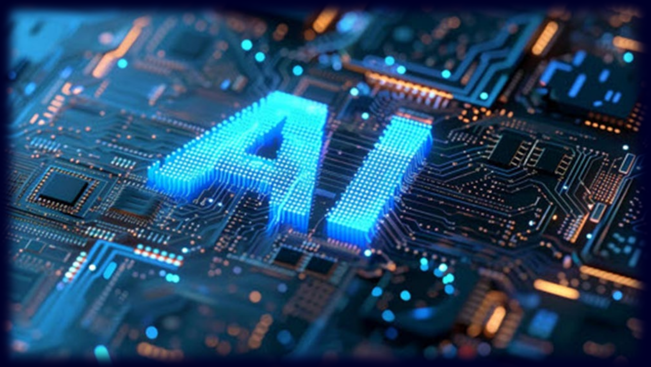
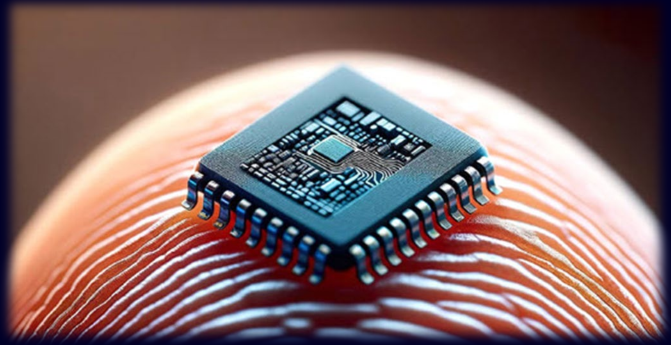
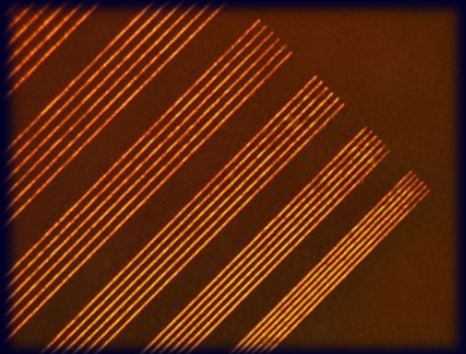
Blogs: https://blogs.sw.siemens.com/electronic-systems-design/

Emerging Trends and Future Directions

- Adoption of ML and AI for automated design optimization.
- Cloud-based environments and connectivity.
- 3D printing and additive manufacturing for rapid prototyping.
- Novel materials with improved electrical, thermal, and mechanical properties.
- Standardization for UHDI design and verification.
- Collaboration between academia, industry, and research to tackle challenges and drive innovation.



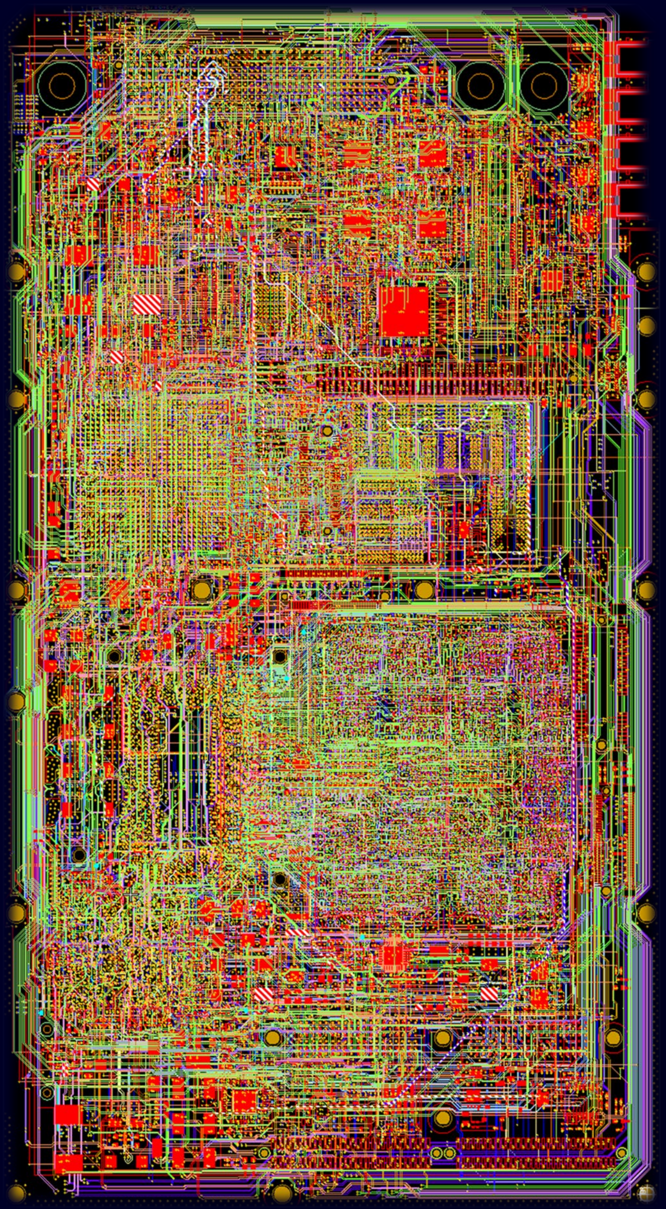




25-micron feature sizes and below – with Ultra HDI
(images courtesy of ASC & Iconnect007)

The state of design in electronics

Design teams **must deliver more complex products** on **even more compressed schedules**, but they **lose valuable time** with unproductive tasks. **Connect them** through all **engineering disciplines** and give them **best-in-class solutions** to thrive with a **collaborative** approach to **Electronic Systems Design**.



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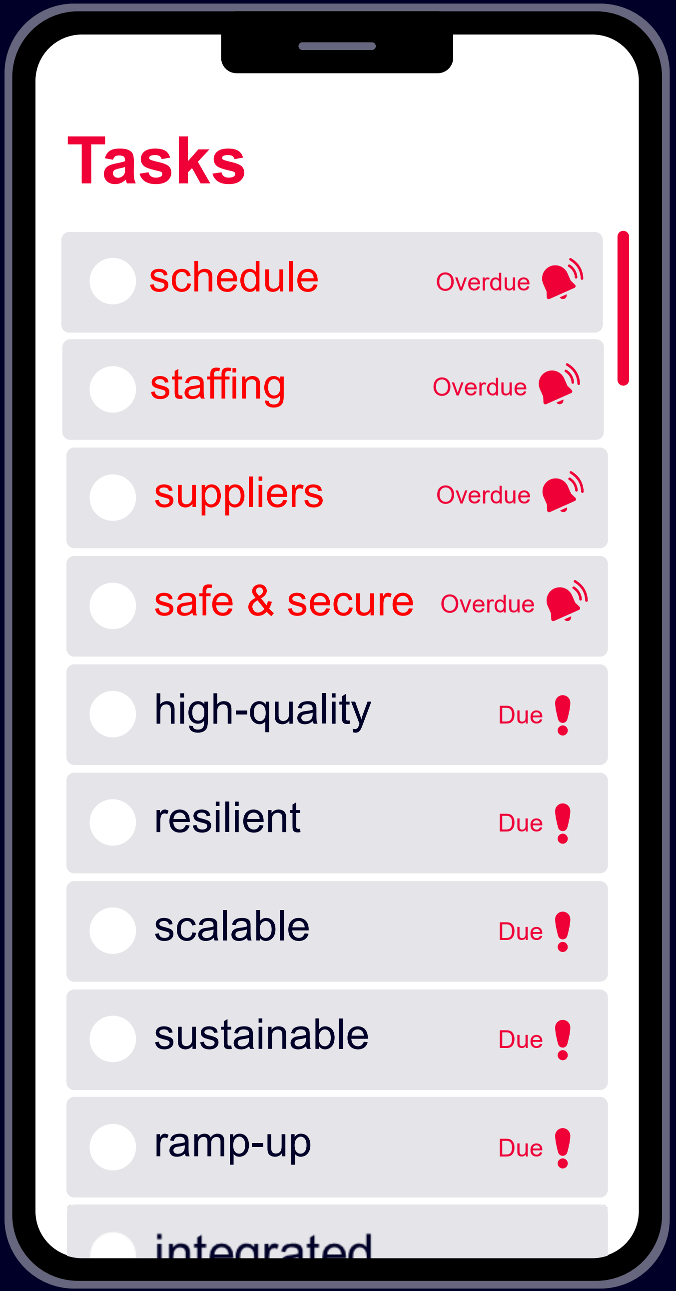
Goals

keep pace with accelerating innovation

speed up product delivery

Challenges

Resource Constraints	Competitive Pressures	Market Volatility



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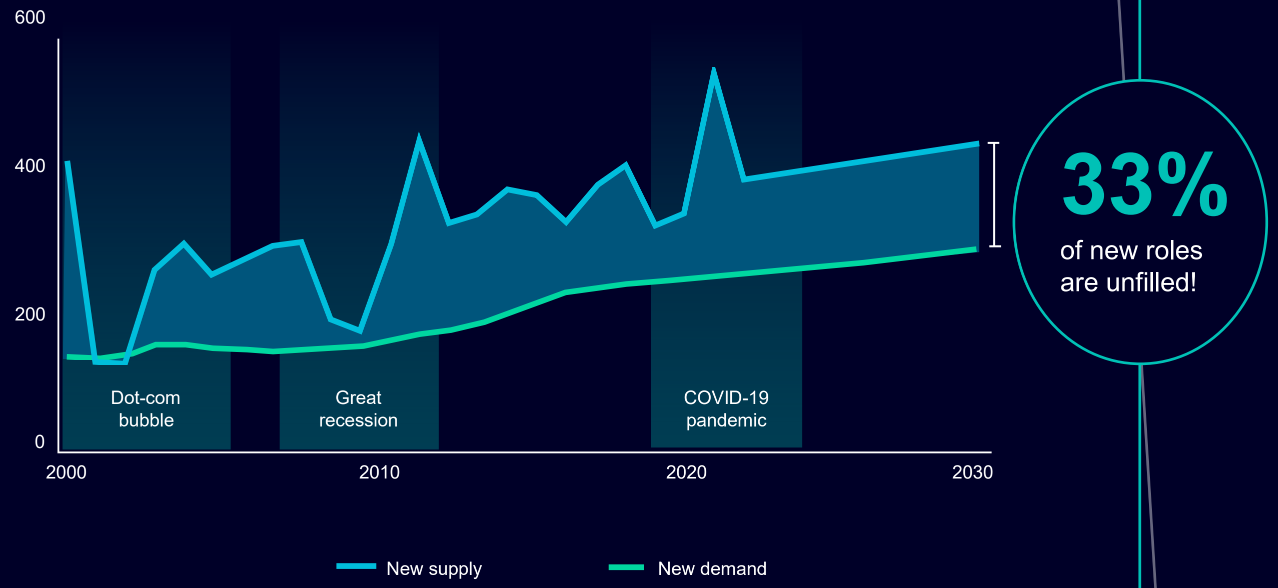
Workforce changes and resource management are straining engineering organizations across all geographies.

One in three engineering jobs goes unfulfilled in the United States



Boston Consulting Group 2023

BCG analysis based on US bureau of statistics; National Sciences Foundation, American Society of Engineering Education, US Citizen and Immigration Services

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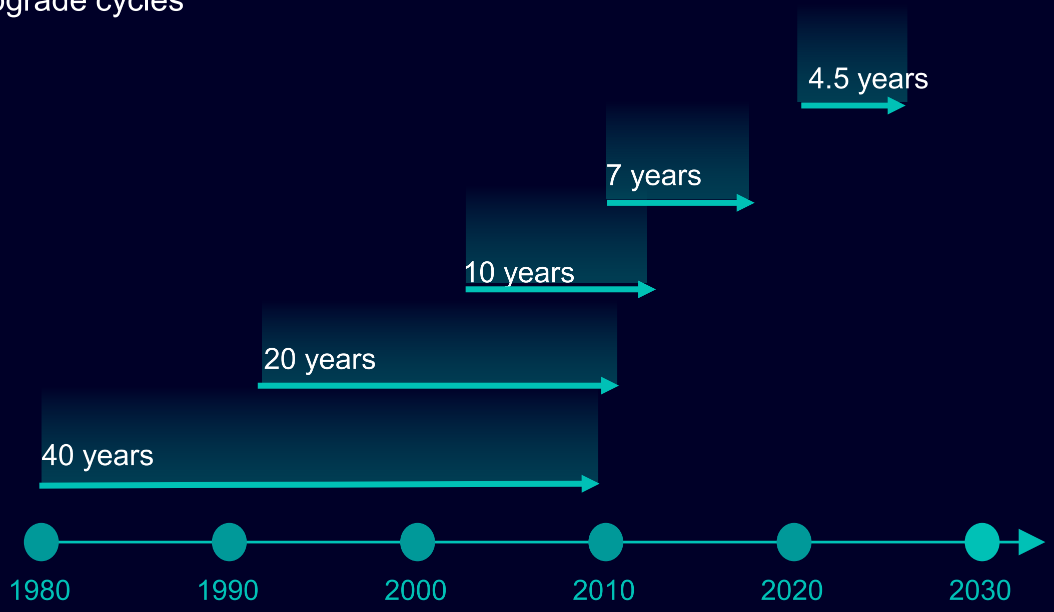
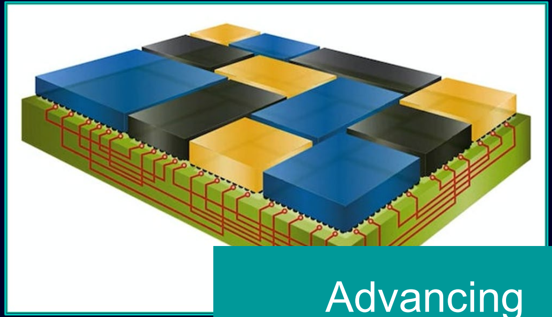
Electronic systems innovation is accelerating, product release cycles are measured in months, not years.

Innovation, connectivity, emerging economies, and more consumer options are driving product replacement and upgrade cycles



Expected Lifecycle of Electronic Devices
Pew Research

Unpredictability is the new normal, and there is no end in sight requiring resilience across organizations.



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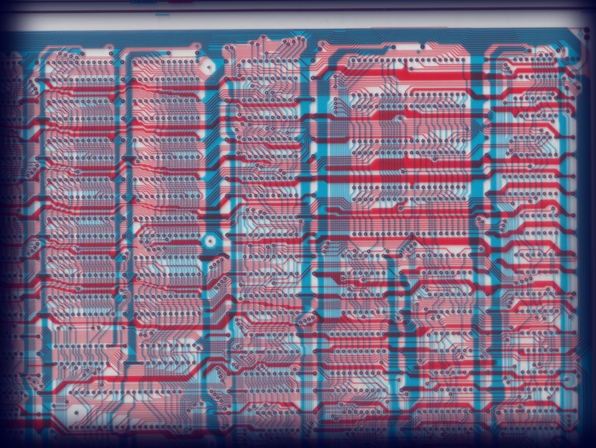
Complexity in PCB Design has evolved...

Designing PCBs in 1984

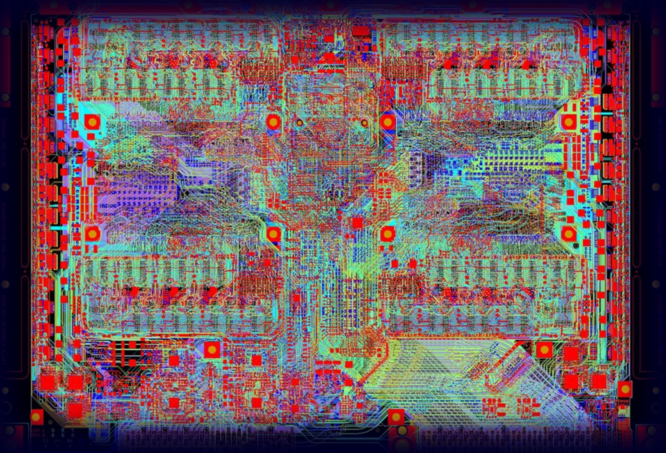
Image from *Rick Hartley at 39yrs old laying Red and Blue tape on 6mil (0.15mm) thick mylar. Blue tape formed the copper features on the top layer of the board, Red tape was the bottom layer.*

2 Layer PCB - 1984



1984 2-layer PCB Design – Rick Hartley

18 Layer PCB - 2022



2022 XTIA Winner – ABACO Systems
100Gbps High-speed Design – Military & Aerospace

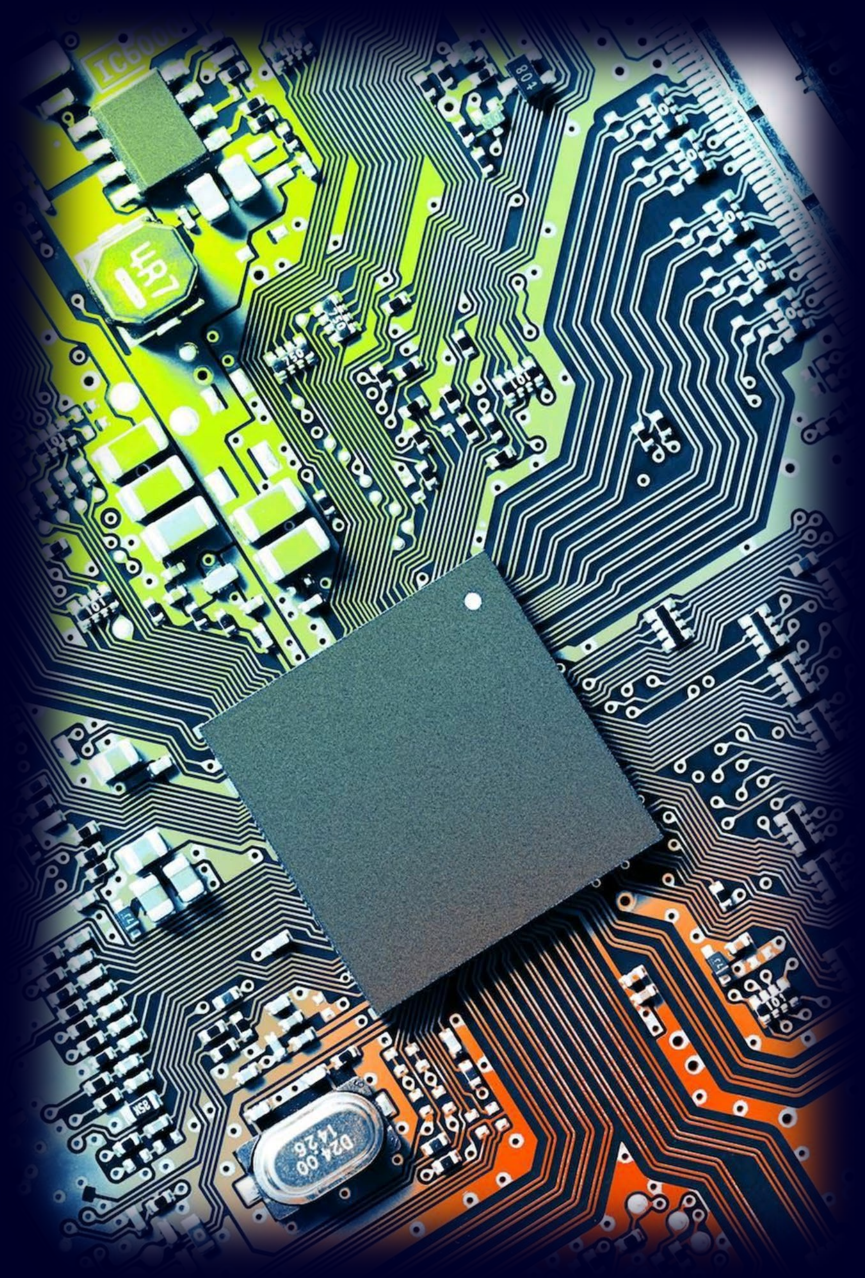
Complex (complicated) - Definition

Definition per Merriam-Webster

A whole made up of complicated, intricately combined, or interrelated parts. Hard or difficult to separate, analyze, or solve.

What is considered complex in PCB Design?

- High layer count…HDI…UHDI?
- Via technology (Blind, Buried, micro, Via-in pad)
- Material / Flex / Rigid-Flex
- High pin count BGAs, connectors, etc.
- Physical board envelope to components, ratio?
- Design constraints (physical/electrical)
- Optimized component placement
- Signal routing of critical & non-critical nets
- Establishing a good PDN
- Project schedule (resources & budget)



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Common challenges in Complex PCB Design

Problem!

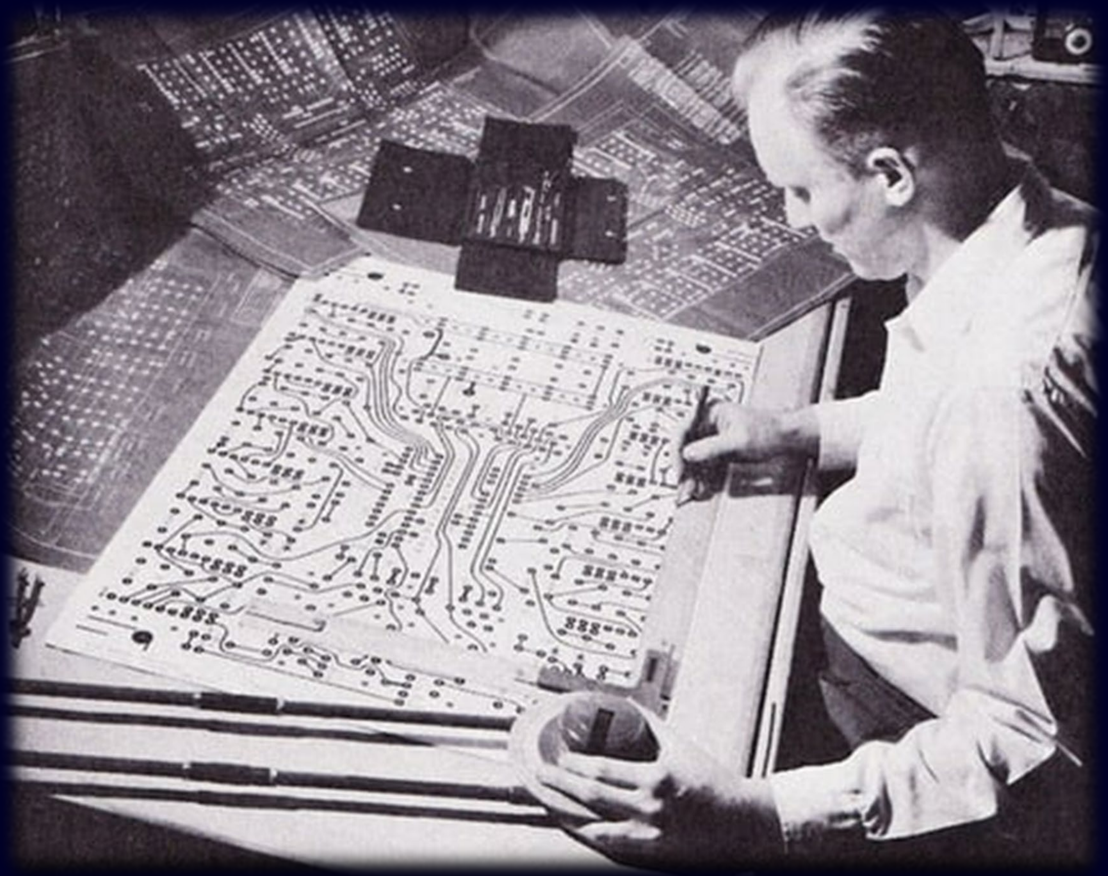
“Using legacy methodologies to design today’s complex PCBs!”

Roadblocks!

- Lack of PCB design knowledge and or experience
- Don’t trust today’s EDA tools / no time to learn
- Design requirements / unrealistic schedules
- Internal company culture resistance to change

Best Practice

- Constantly evolve education, skillset, and network
- Keep up-to-date with today’s EDA tool capabilities, functionalities, and automation
- Collaboration with suppliers from the beginning



Drawing a PCB with tape and mylar before EDA arrived

Image from *A Manual of Engineering Drawing for Students and Draftsmen, 9th Ed.,* by French & Vierck,1960, p. 487.

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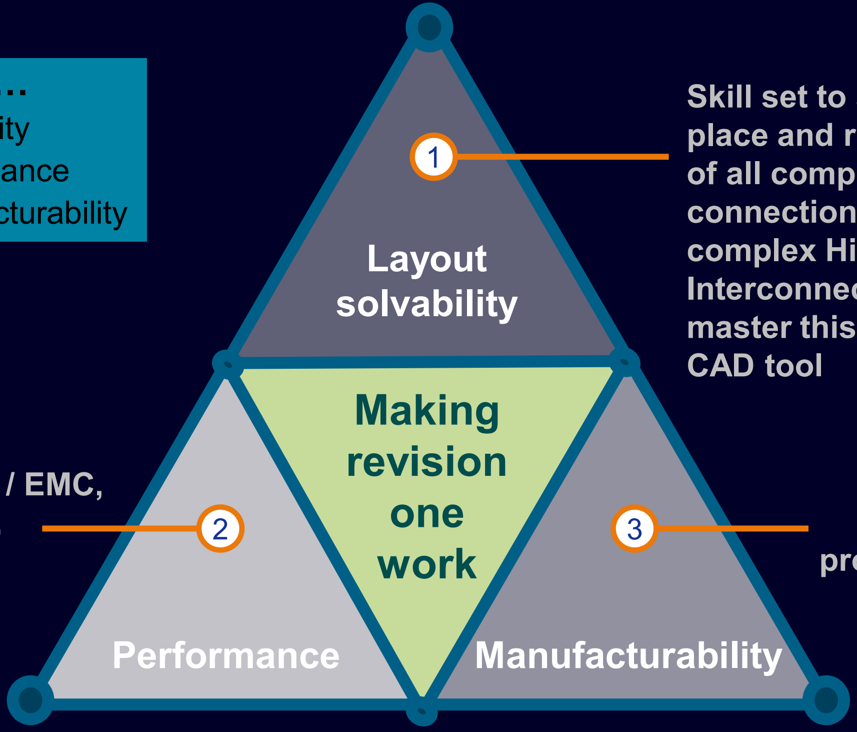
Three Key Perspectives of Success in PCB Design

Today's circuit engineer must meet three competing perspectives for success

Design for…

- **DFS**olvability
- **DFP**erformance
- **DFM**anufacturability



Skill set to solve the place and route of all components and connections often with complex High-Density Interconnect (HDI)…and master this on your CAD tool

Signal Integrity / EMC, Power Delivery, Thermal

DFX (DFM) all considerations producing high yield and lower cost

IPC-22XX 1.X. Definition for Printed Circuit Engineering Layout Professional

The result provides for maximum component placement/routing density achievable, optimum electrical performance and efficient, high yield, defect free manufacturing.

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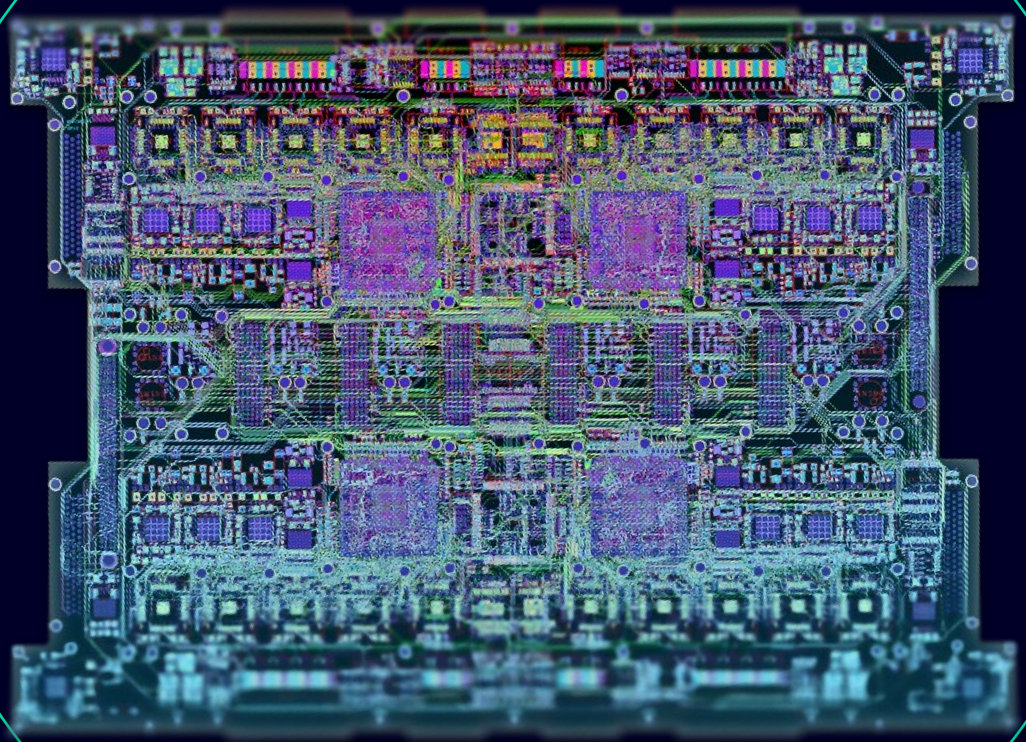
Critical Aspects of Complex PCBs



- Layout Solvability
- Performance (SI, PI, EMI/EMC, Thermal)
- Manufacturing (DFM)
- Supply-chain Resilience
- Process Optimization

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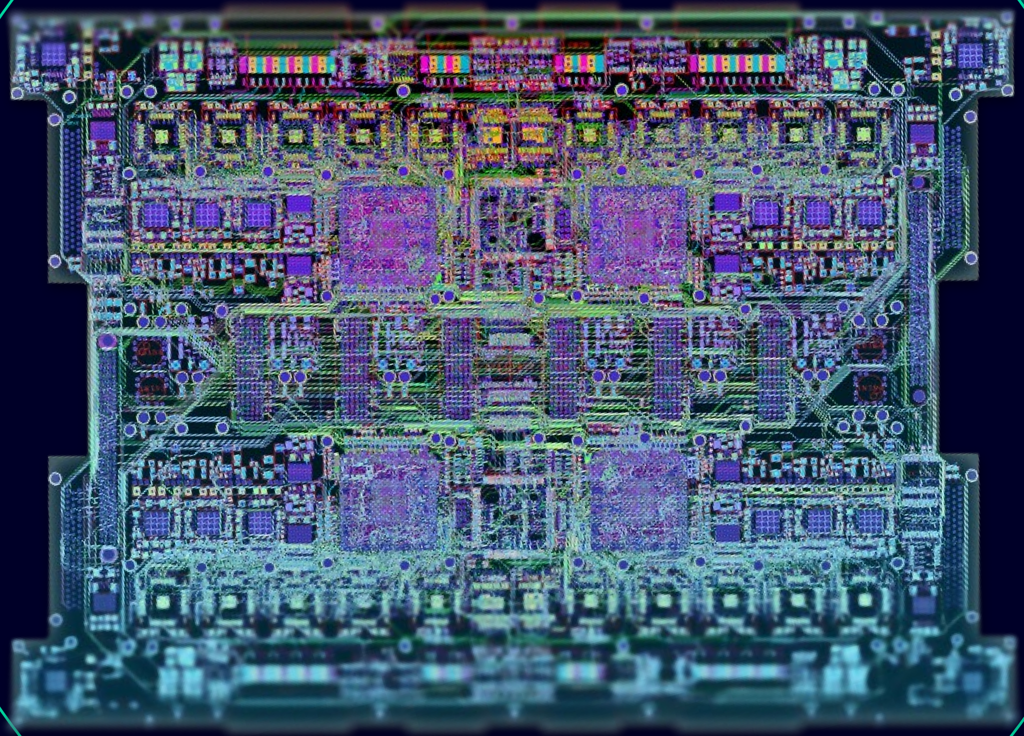
Critical Aspects of Complex PCBs



Layout Solvability

Performance (SI, PI, EMI/EMC, Thermal)

Manufacturing (DFM)

Supply-chain Resilience

Process Optimization

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Solvability – Component Placement

Problem!

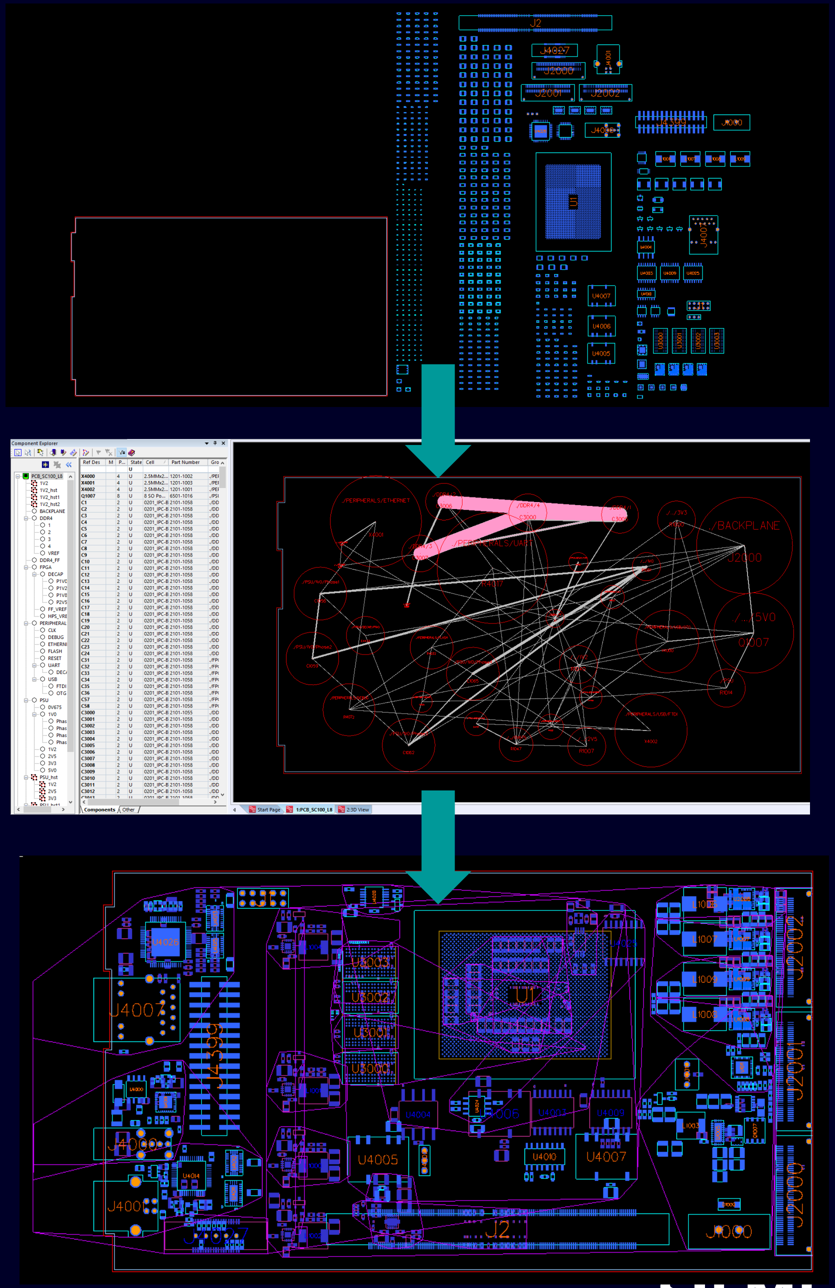
Not all components will fit within the mechanical envelope

Roadblocks!

- No Real-estate analysis / Area Study
- Inefficient component placement
- Poor mechanical / physical definition

Best Practice

- Perform Real-estate Analysis / Area Study
- Assign and place parts by groups/clusters
- Look at methodologies that enables context-based, incremental collaboration between domains, and adopt latest exchange formats (IDX).



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Solvability – Power Distribution Network (PDN)

Problem!

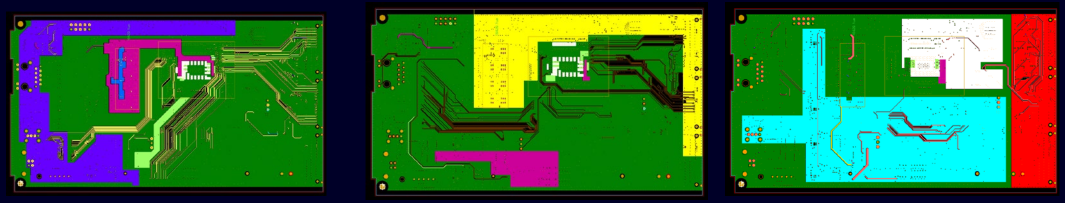
Poor and or inadequate power delivery

Roadblocks!

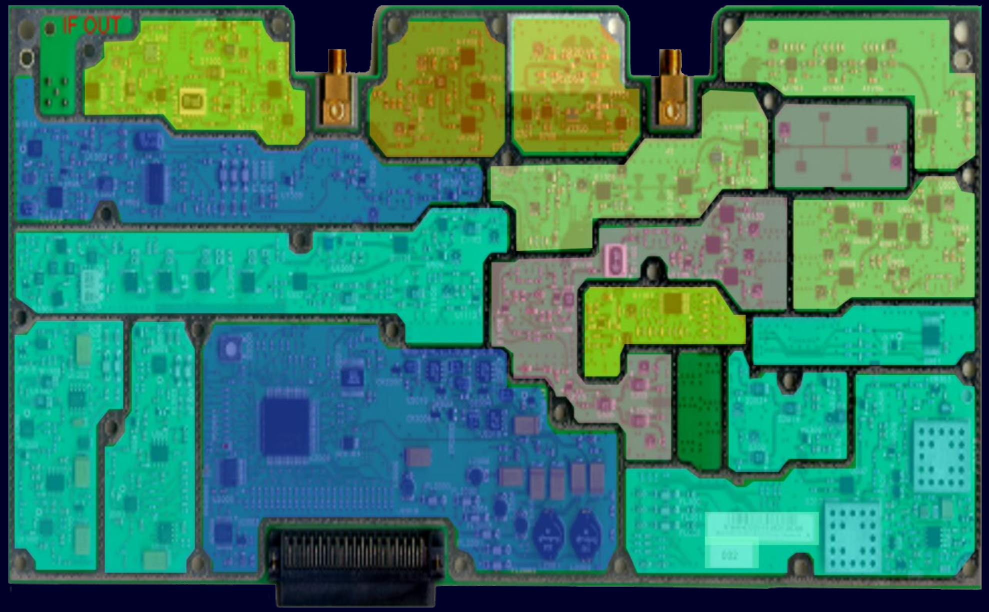
- Poor PDN definition
- Non-optimized Component placement
- PCB stackup (layer count/structure)
- Over constrained design

Best Practice

- Establish a good PDN per requirements
- Establish an optimal PCB stackup
- Establish an overall Birds-eye view of signal/power flow map



Example of Simple PDN Design



Example of Complex PDN Design

Solvability – Signal Routing

Problem!

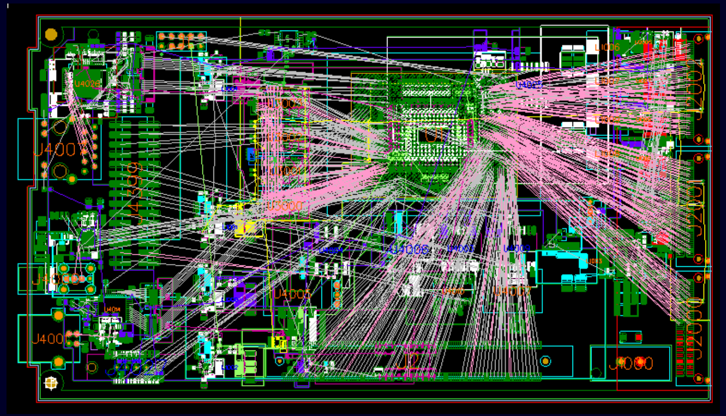
Difficult to complete all routing connections

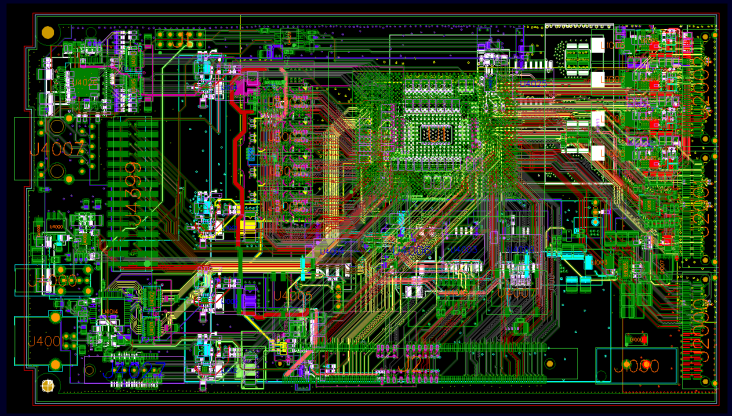
Roadblocks!

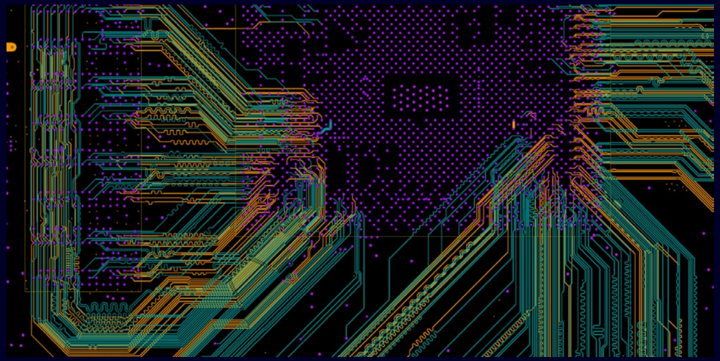
- None-optimal component placement
- No routing strategy employed (constraints, rule areas, rooms etc.)
- High pin count BGAs, connectors, etc.
- Small pin-pitch components
- Over constrained design

Best Practice

- Establish a signal flow map and a thorough PDN that optimizes a good component placement.
- Define/utilize constraints to meet requirements.







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Solvability – Manufacturing (DFM)

Problem!

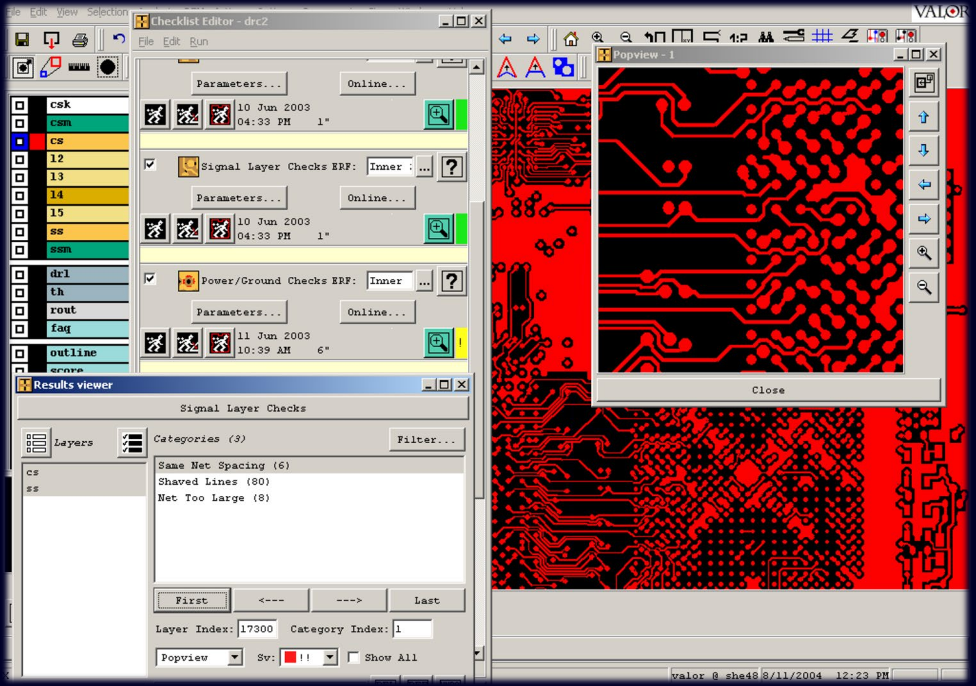
Manufacturing is a after thought or worse…not accounted for

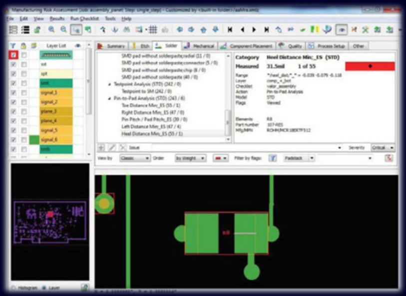
Roadblocks!

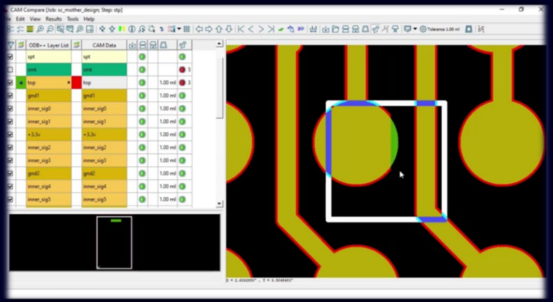
- Component Placement (to close, no routing channels, etc.)
- Mixed technology (TH/SMT, via types, material, etc.)
- Component library creating not to industry standard (IPC, Best practices, etc.)
- Best practices not implemented (placement/routing)

Best Practice

- Implement DFM from beginning
- Implement industry best practices
- Collaborate with your supplier(s)







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Solvability – Test

Problem!

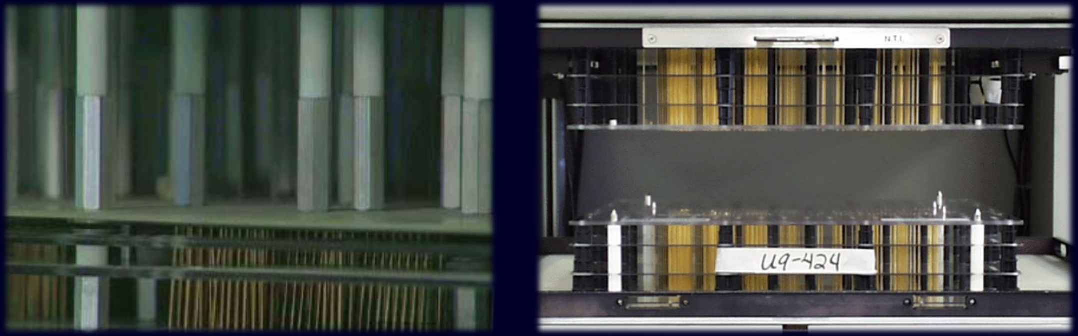
Not accounting for testability of your design

Roadblocks!

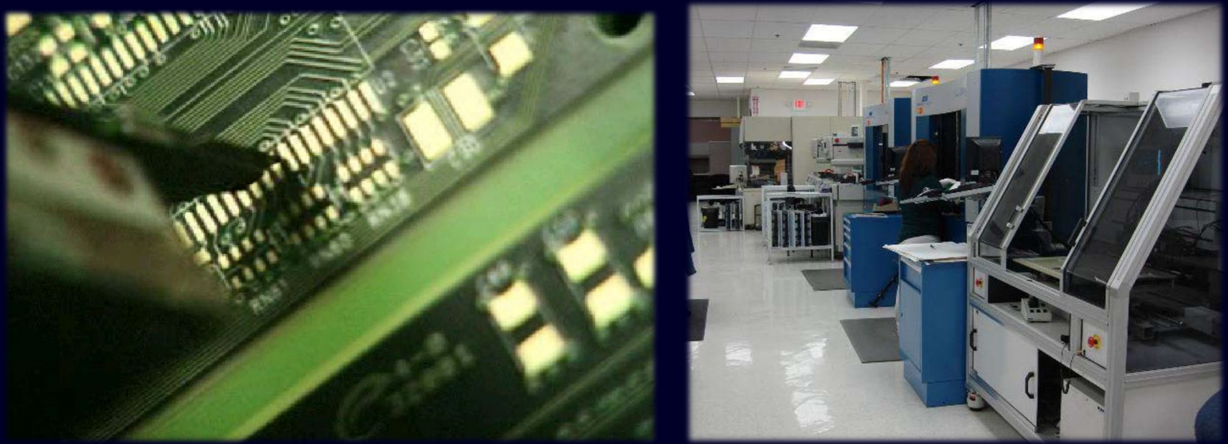
- Test is not initially accounted for
- Inefficient component placement (too close)
- Not all nets accessable for test
- Testability requirements (not clearly or defined)
- Too expensive to implement

Best Practice

- Account for Test front the beginning
- Establish a test plan & methodology
- Collaborate with your supplier(s)



Clam Shell / Bed of Nails Test



Flying Probe Tester

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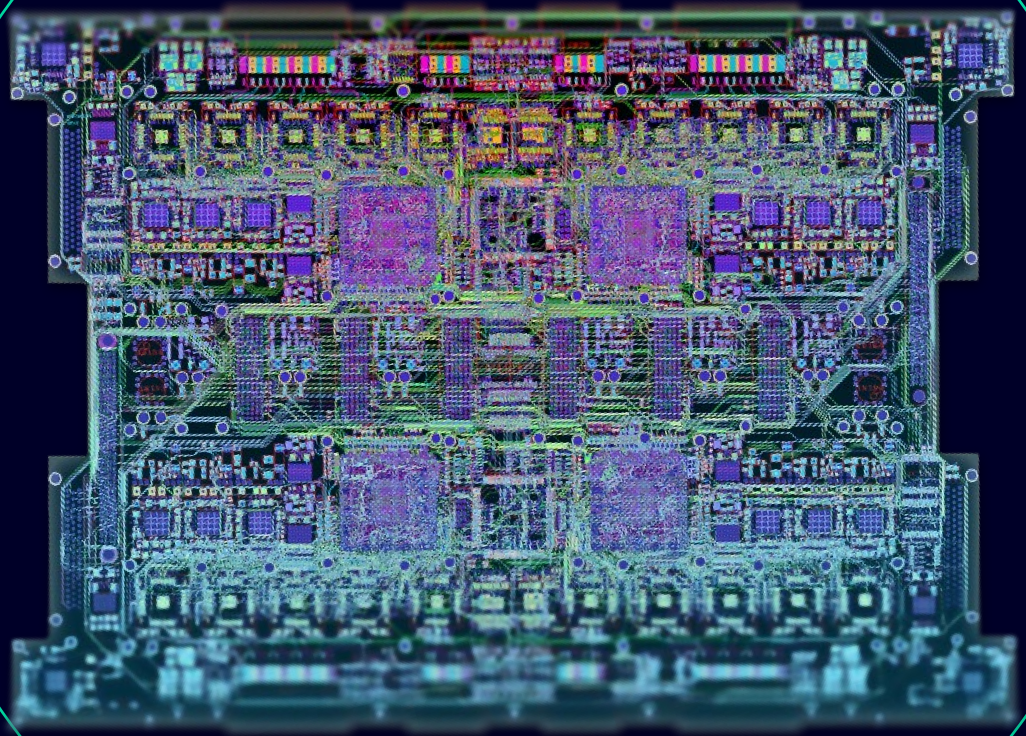
Critical Aspects of Complex PCBs



- Layout Solvability
- Performance (SI, PI, EMI/EMC, Thermal)
- Manufacturing (DFM)
- Supply-chain Resilience
- Process Optimization

Performance – Shift Left – Analysis

Problem!

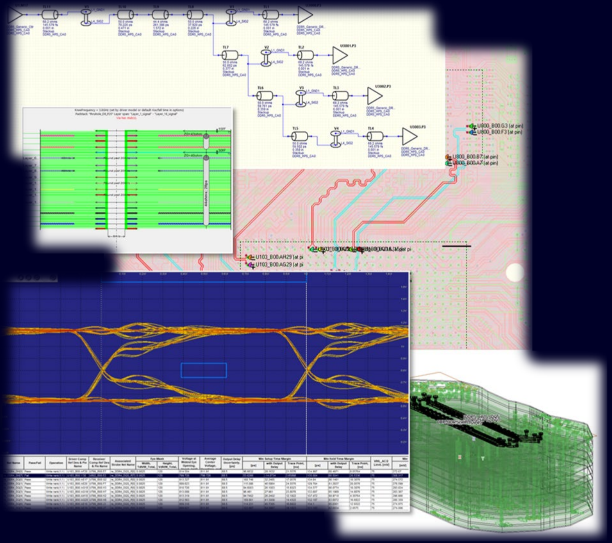
Re-spins are normalized due to analysis not being run

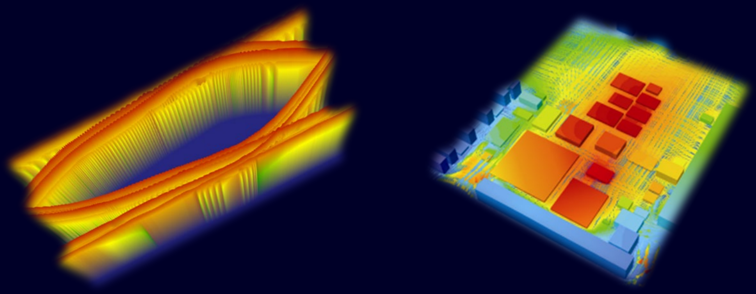
Roadblocks!

- Multiple re-spins already planned in schedule
- "No time to complete analysis" mentality
- Too much overhead to setup/implement/maintain

Best Practice

- Account for analysis in the initial project schedule
- Don’t eliminate analysis in trying to reduce project schedule and cost
- Shift left multidiscipline analyses of Schematic, Thermal, SI/PI, AMS, DFM, Specialist/Design Author, HASS/HALT, DFT to eliminate errors





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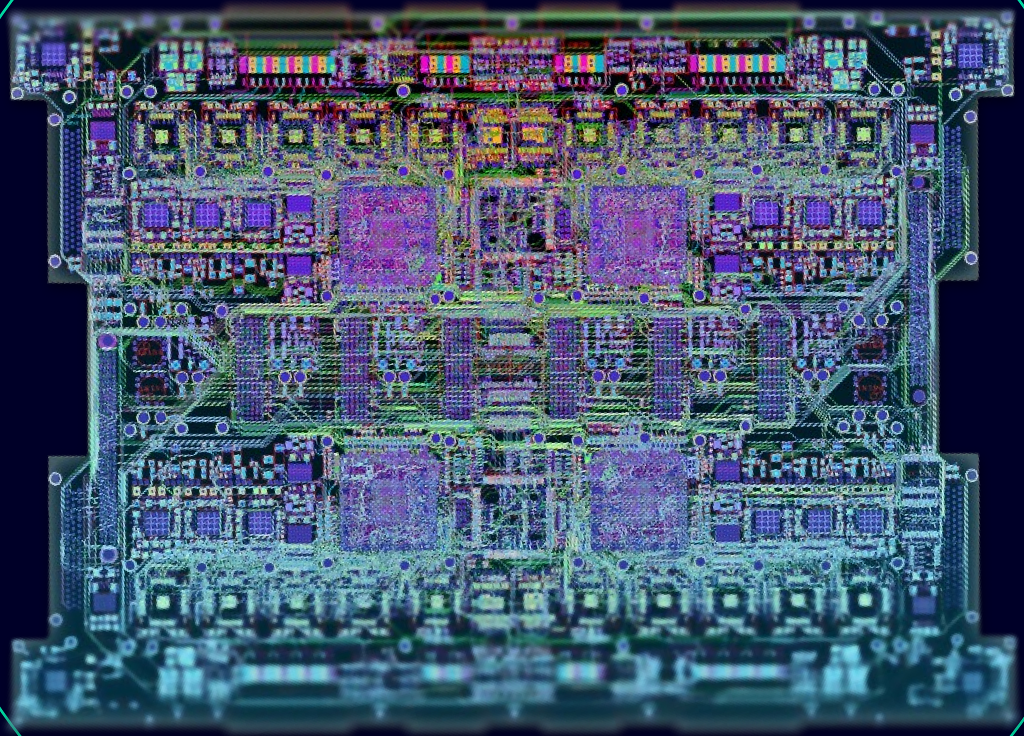

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Manufacturing - DFM

Problem!

Data not addressing producibility or manufacturability passed to manufacturing

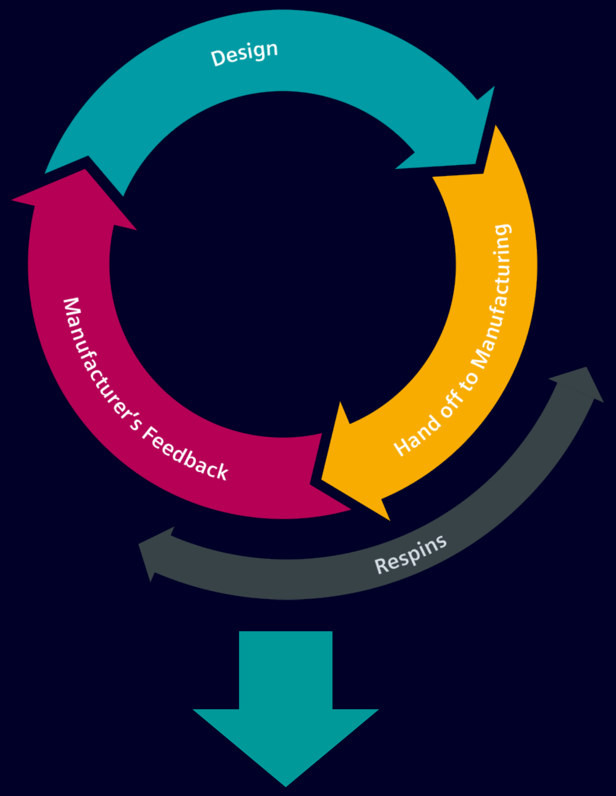
Roadblocks/Inhibitors!

- Competitive pressure on Fab house to accept poor data
- No time to run DFM analysis

Best Practice

- Optimize integration between design and MFG
- Enable lessons learned in MFG to influence designs (enable feedback loop)
- Utilize intelligent data format (ODB++, IPC-2581)

Traditional iterative design flow



Concurrent DFM

Manufacturing – Design for Manufacturing Study

Volume and Speed of PCB Design Processes

+2.9

+$28k

On average, a PCB design undergoes 2.9 respins at an average material cost of $28k per respin

↑49%

Companies using DFM software produce 49% more PCB designs per year compared to non-users

↓12%

Companies using DFM software take 12% less time to develop PCB designs from the completion of schematic to manufacturing release

- On average, a PCB design undergoes **2.9 respins** before going to volume production.
- These respins can often be avoided and are often due to manufacturability issues.
- When a design has to be reworked it takes an average of **2 weeks to complete** at an average material cost of more than **$28K per respin**.
- You have likely heard of manufacturing scrap as material waste resulting from a production error.
- Design respins can be seen as engineering scrap - avoidable costs sunk into designs.
- DFM ensures that projects achieve quality goals, meet target costs, and are completed on time.

Source: Aberdeen, May 2023

DFM software users are able to design faster and have more productive PCB design processes

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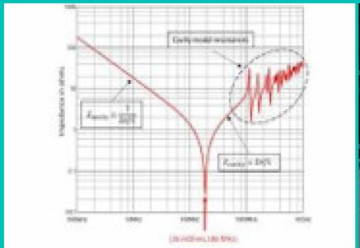
Manufacturing - Design for Manufacturing Study

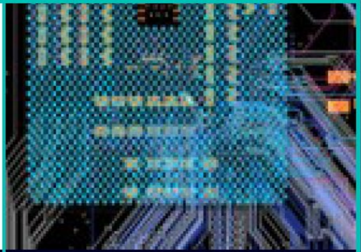
Complex Designs Necessitate Best Practices

- Best-in-class companies are far more likely to be designing with advanced technologies.
- From controlled impedance to HDI via technologies, DFM software as part of an overall best practices mindset helps to ensure that PCB designs meet the necessary fabrication and assembly requirements.
- DFM software enables Best-in-Class companies to design more complex PCBs with more advanced technologies.

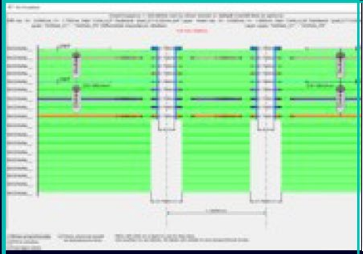
Advanced technologies that best-in-class companies are more likely to use compared to others



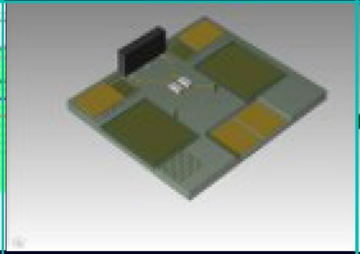
46% more likely to use controlled impedance



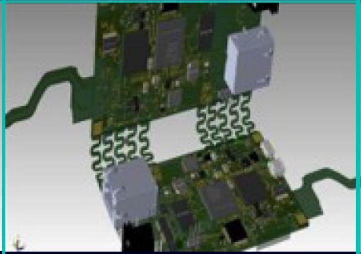
50% more likely to use HDI/Microvias



30% more likely to use backdrill



29% more likely to use embedded components



24% more likely to use flex or rigid-flex circuits

Source: Aberdeen, May 2023

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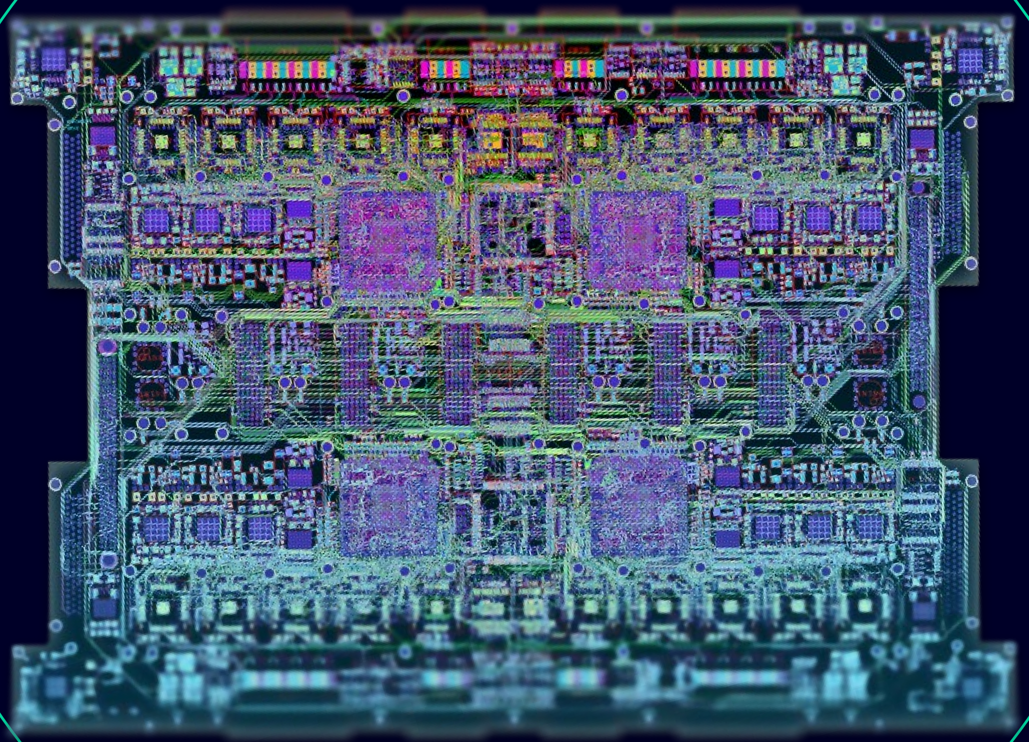
Critical Aspects of Complex PCBs



- Layout Solvability
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- Supply-chain Resilience
- Process Optimization

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Design for Resilience

Problem!

Siloed teams, legacy processes and ineffective risk management

Roadblocks!

- Just-in-time approach current mode of operation
- Not sure how to address supply chain issues
- Too much overhead to setup/implement/maintain

Best Practice

- Implement outside-in approach with supply-chain intelligence by shifting left best-known part availability, BOM validation, and validation of alternates at point of design
- Remove barriers from siloed teams and optimize operations and communications

+

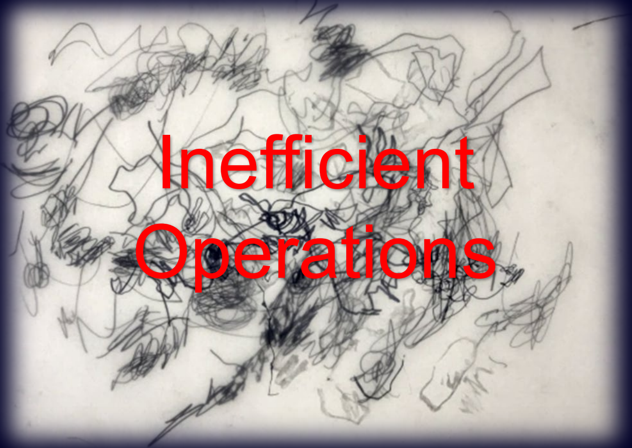
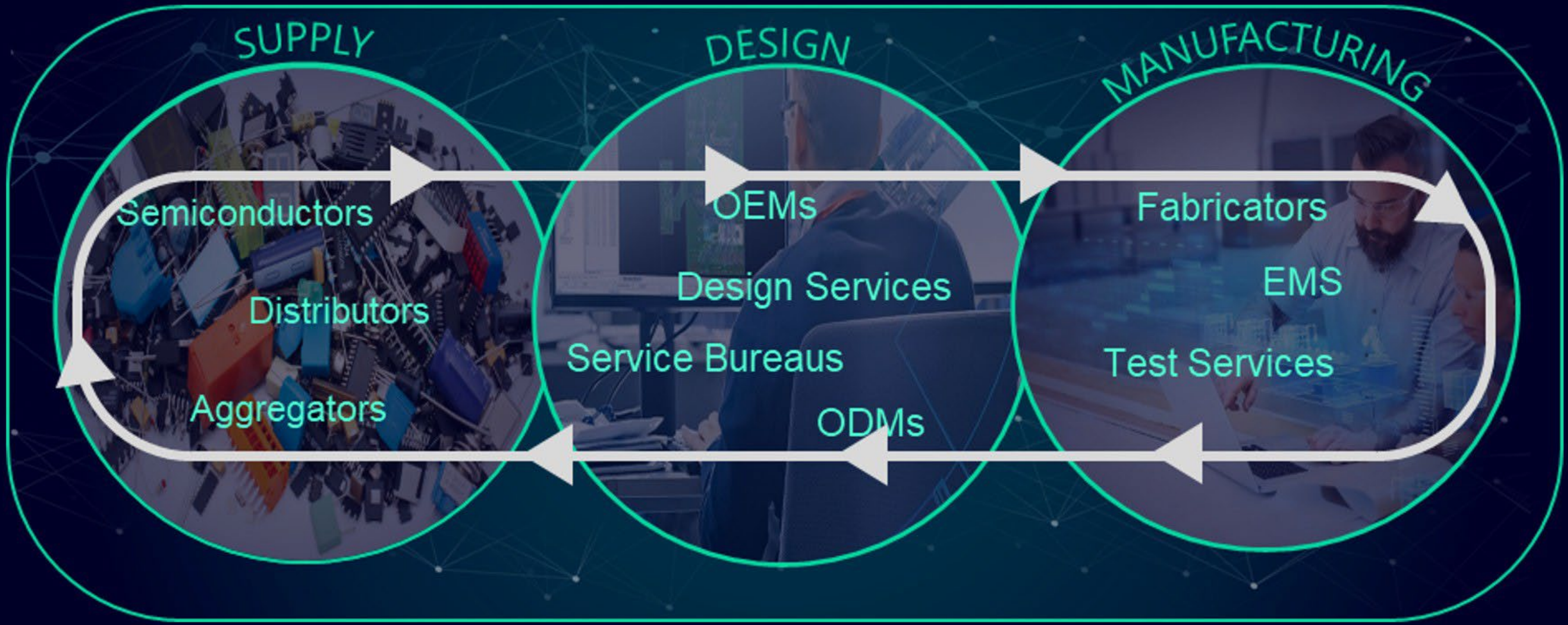


Image: Inefficient Mapping by Linda Knight

Design for Resilience



The foundation of supply-chain resilience

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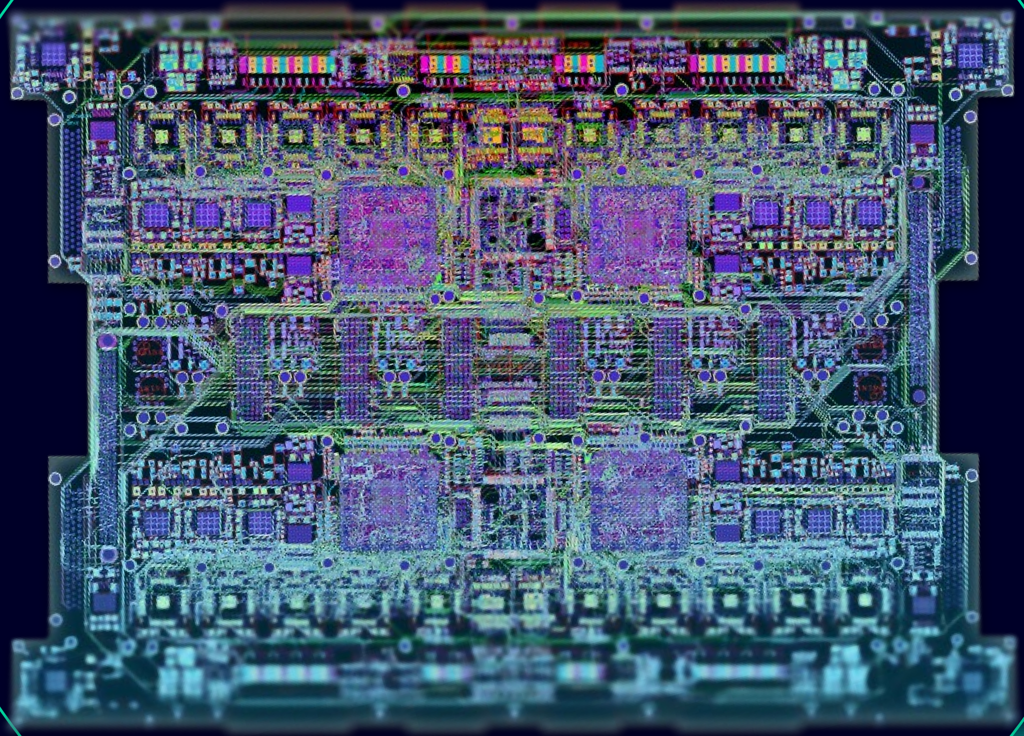
Critical Aspects of Complex PCBs



Layout Solvability

Performance (SI, PI, EMI/EMC, Thermal)

Manufacturing (DFM)

Supply-chain Resilience

Process Optimization

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Process Optimization – Library and Data Management

Problem!

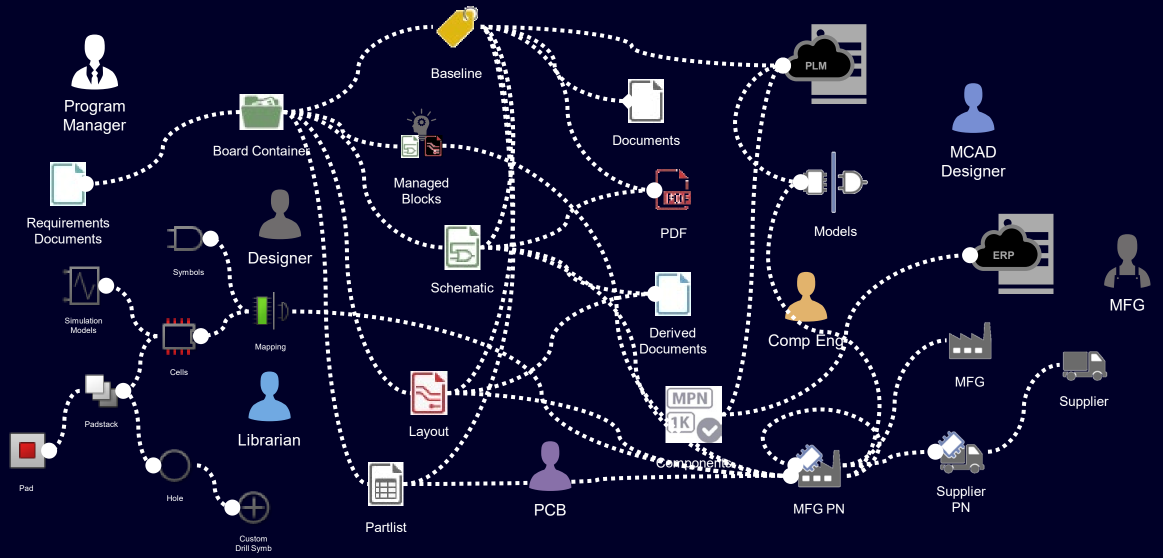
Ineffective collaboration across teams

Roadblocks!

- Product/organizational/process complexities
- Too much overhead to maintain
- No experience/specialist

Best Practice

- Establish internal guidelines & processes
- Utilize industry standards
- Organize and control your library and data



Process Optimization – Multi-board Design

Problem!

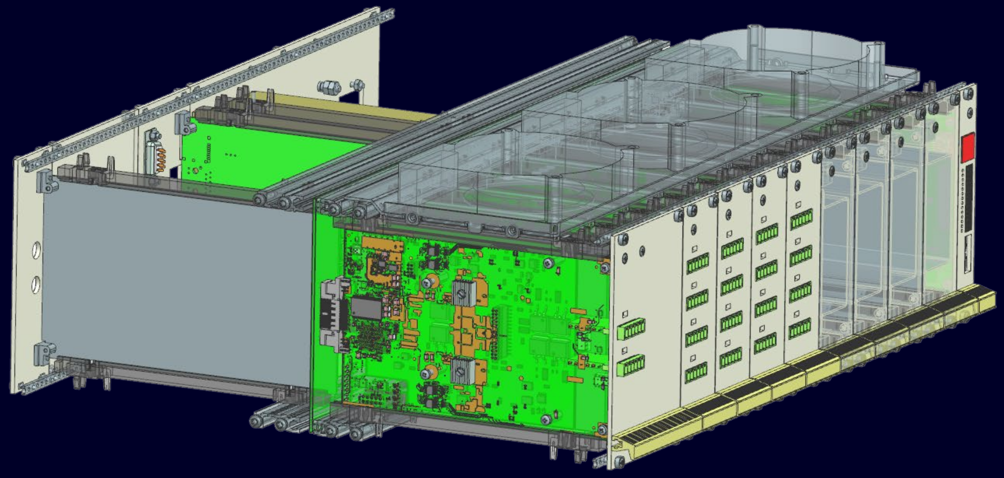
Full systems design done in a vacuum, and by siloed team members

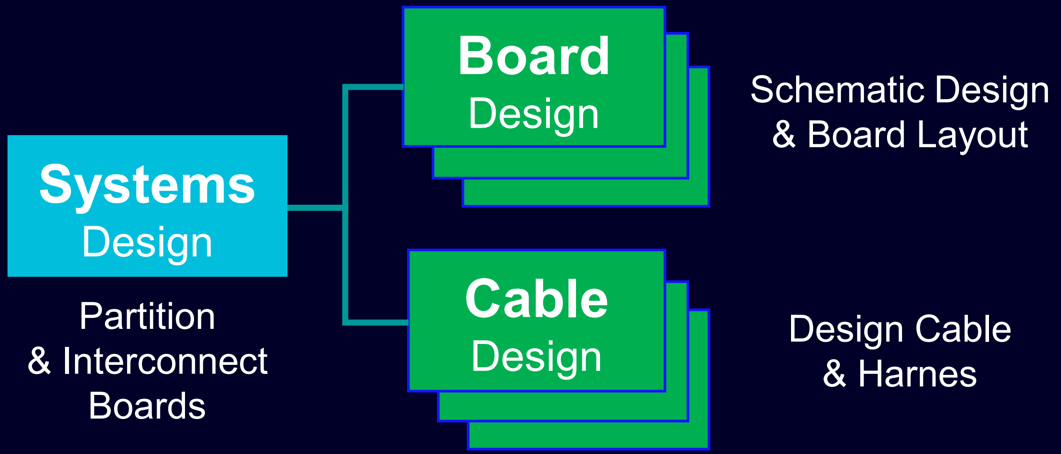
Roadblocks!

- Not familiar/proficient with tool
- Too much overhead to setup/implement/maintain
- Too expensive to implement

Best Practice

- Implement multi-board model-based engineering for cross-system optimization options (size / performance)
- Remove siloed engineering approach





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Process Optimization – Analog/Digital/RF Co-design

Problem!

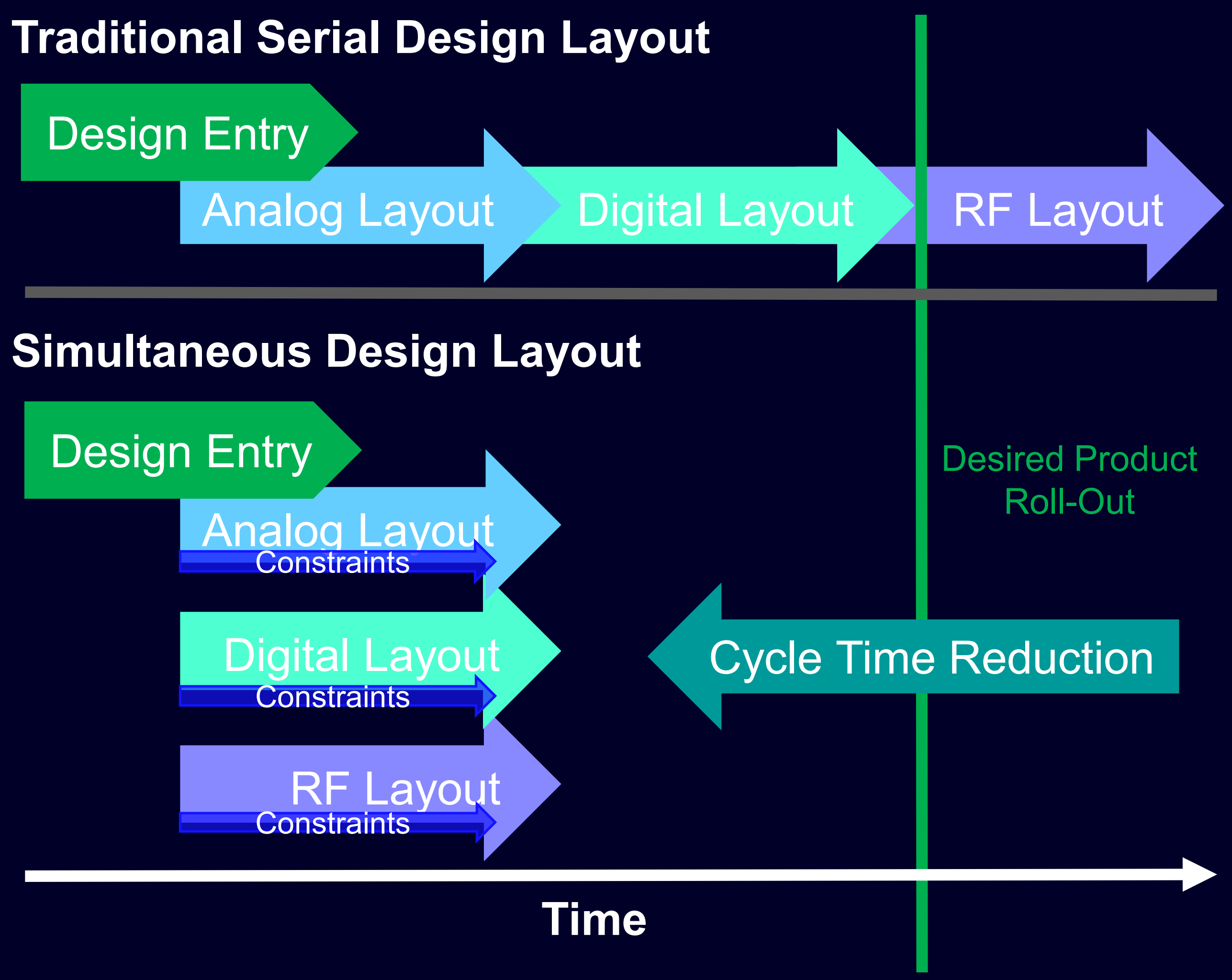
RF circuits are not optimally integrated into the design

Roadblocks!

- Disparate disciplines working in isolation
- Outsource to specialist or SME
- Siloed organizations/specialists

Best Practice

- Implement co-design and integration between Analog/Digital/RF engineers
- Integrate RF circuitry concurrently in design
- Adopt latest exchange formats



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Process Optimization – Concurrent Design – Schematic / Layout

Problem!

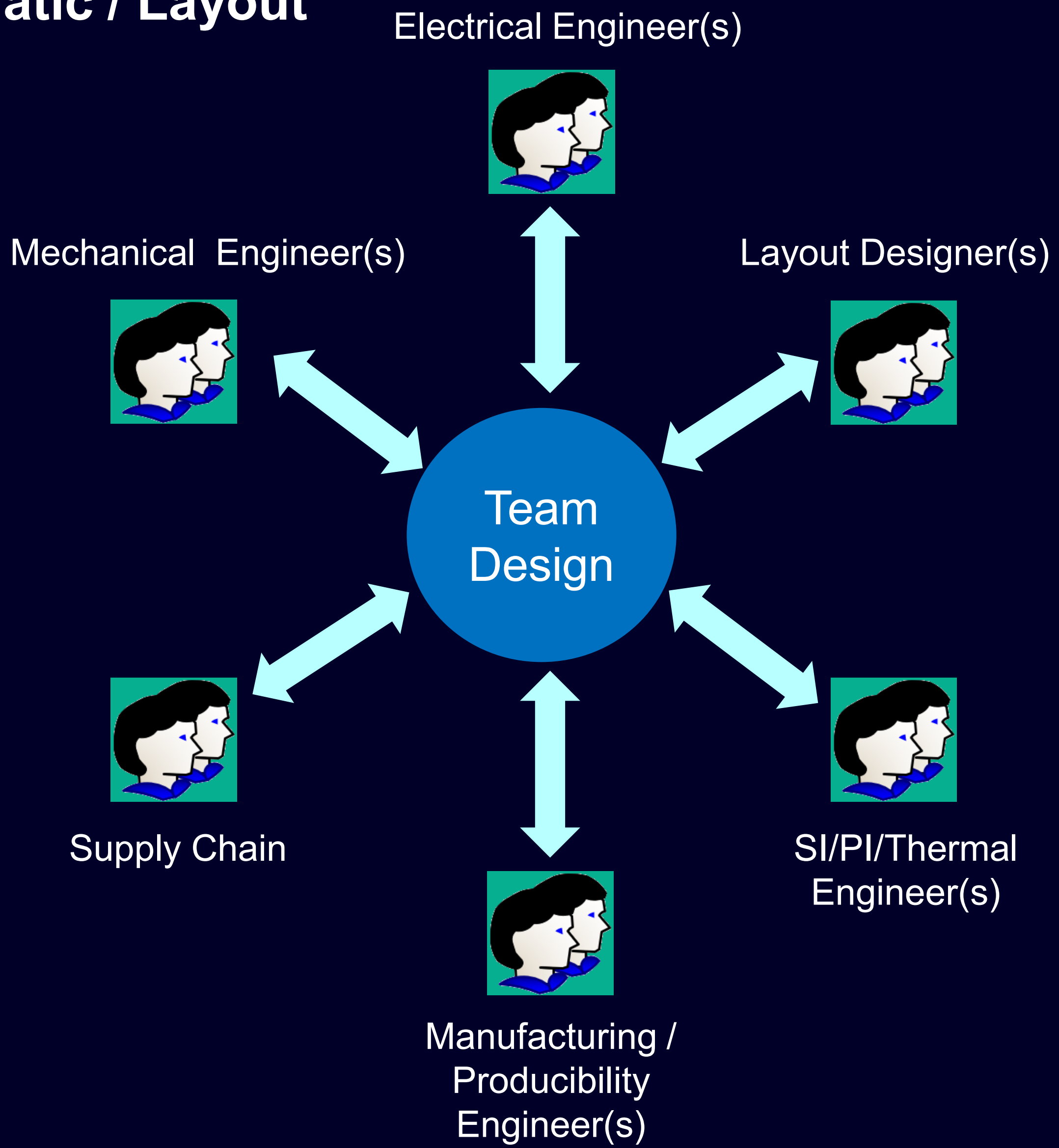
Legacy serial approach is inefficient

Roadblocks!

- Not wanting others to touch/modify their work
- Inefficient work distribution / working in silo's
- No incentive to change

Best Practice

- Utilize advanced capabilities - schematic/layout
- Optimize multidiscipline integration in database
- Optimize team utilization



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Process Optimization – Work-in-progress Design Management

Problems!

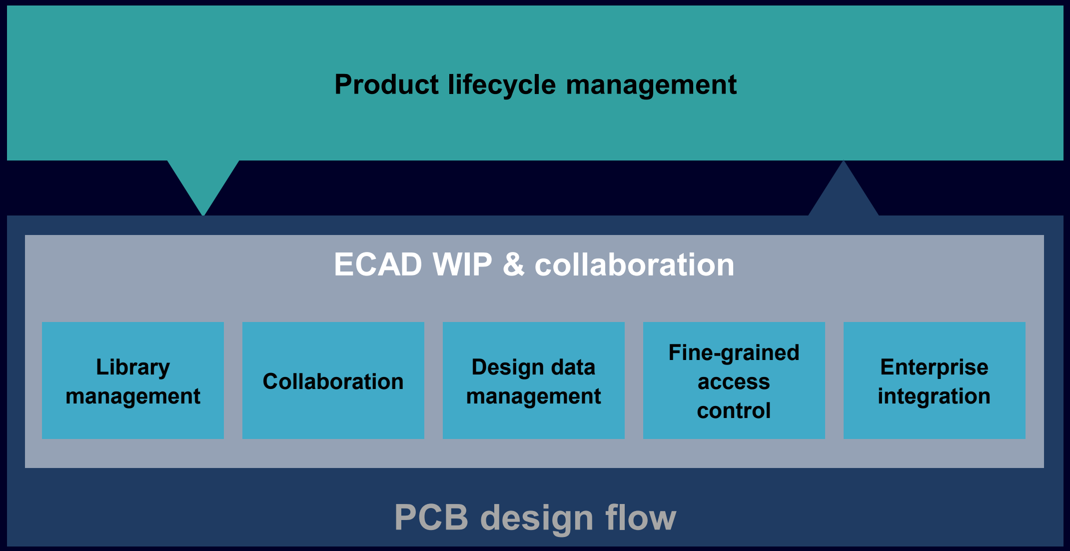
In-process status visibility not adequately shared across functions

Roadblocks!

- Home grown manual processes in place
- Too much overhead to maintain / complexities
- Unaware of opportunities to be better optimized

Best Practice

- Deliver instant status updates and visibility
- Facilitate team integration & optimization
- Attack multi-domain roadblocks instantly and on the fly



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Process Optimization – Constraint Driven Design

Problem!

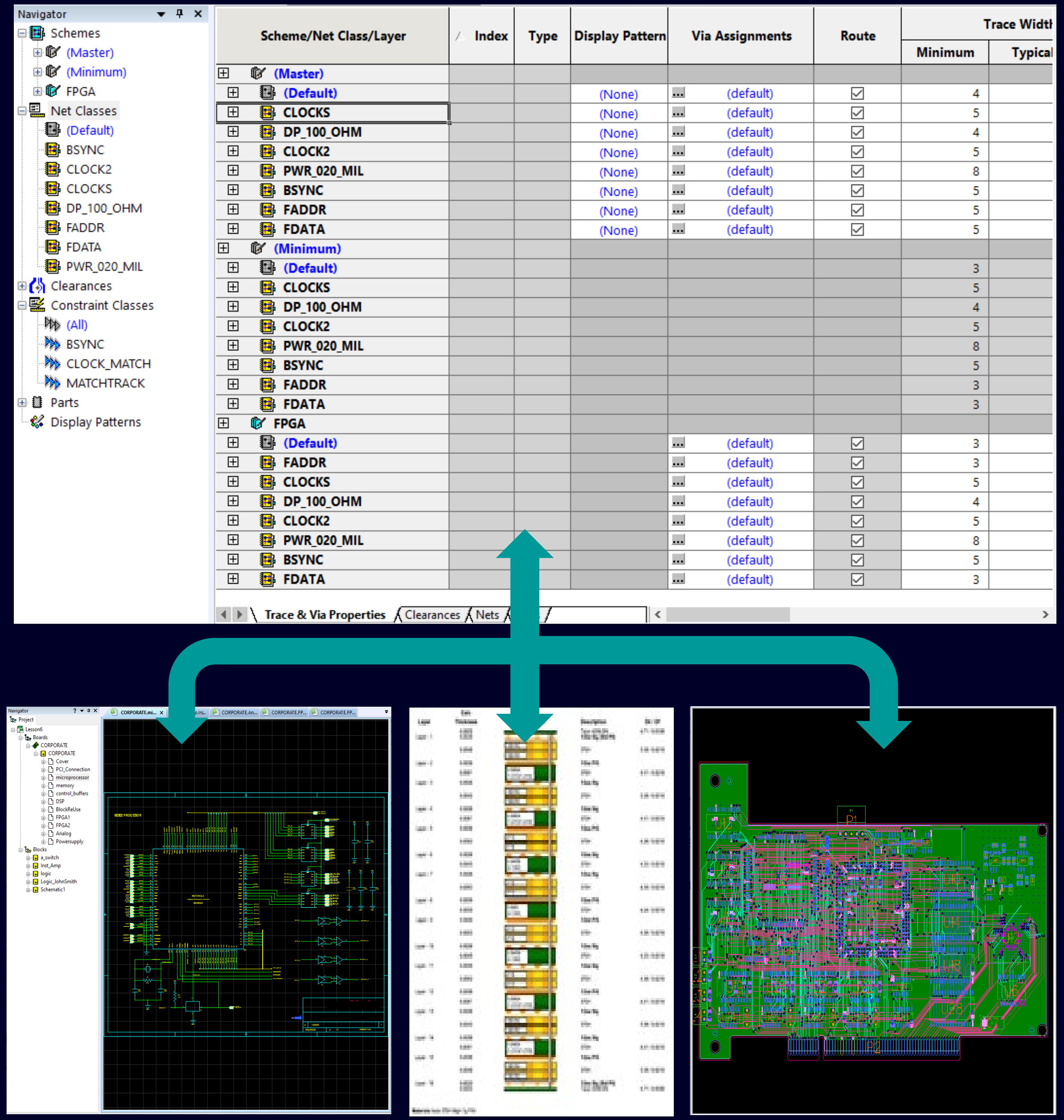
Inefficient implementation of design rules

Roadblocks!

- Too much overhead to setup/implement/maintain
- Takes too long to implement
- Not familiar/proficient with tool

Best Practice

- Establish constraint management process
- Utilize automation to control, meet, and verify requirements were implemented



Scheme/Net Class/Layer	Index	Type	Display Pattern	Via Assignments	Route	Trace Width Minimum	Typical
(Master)							
(Default)			(None)	(default)	☑	4	
CLOCKS			(None)	(default)	☑	5	
DP_100_OHM			(None)	(default)	☑	4	
CLOCK2			(None)	(default)	☑	5	
PWR_020_MIL			(None)	(default)	☑	8	
BSYNC			(None)	(default)	☑	5	
FADDR			(None)	(default)	☑	5	
FDATA			(None)	(default)	☑	5	
(Minimum)							
(Default)						3	
CLOCKS						5	
DP_100_OHM						4	
CLOCK2						5	
PWR_020_MIL						8	
BSYNC						5	
FADDR						3	
FDATA						3	
FPGA							
(Default)				(default)	☑	3	
FADDR				(default)	☑	3	
CLOCKS				(default)	☑	5	
DP_100_OHM				(default)	☑	4	
CLOCK2				(default)	☑	5	
PWR_020_MIL				(default)	☑	8	
BSYNC				(default)	☑	5	
FDATA				(default)	☑	3	

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Process Optimization – Automation (Placement, Route, Outputs)

Problem!

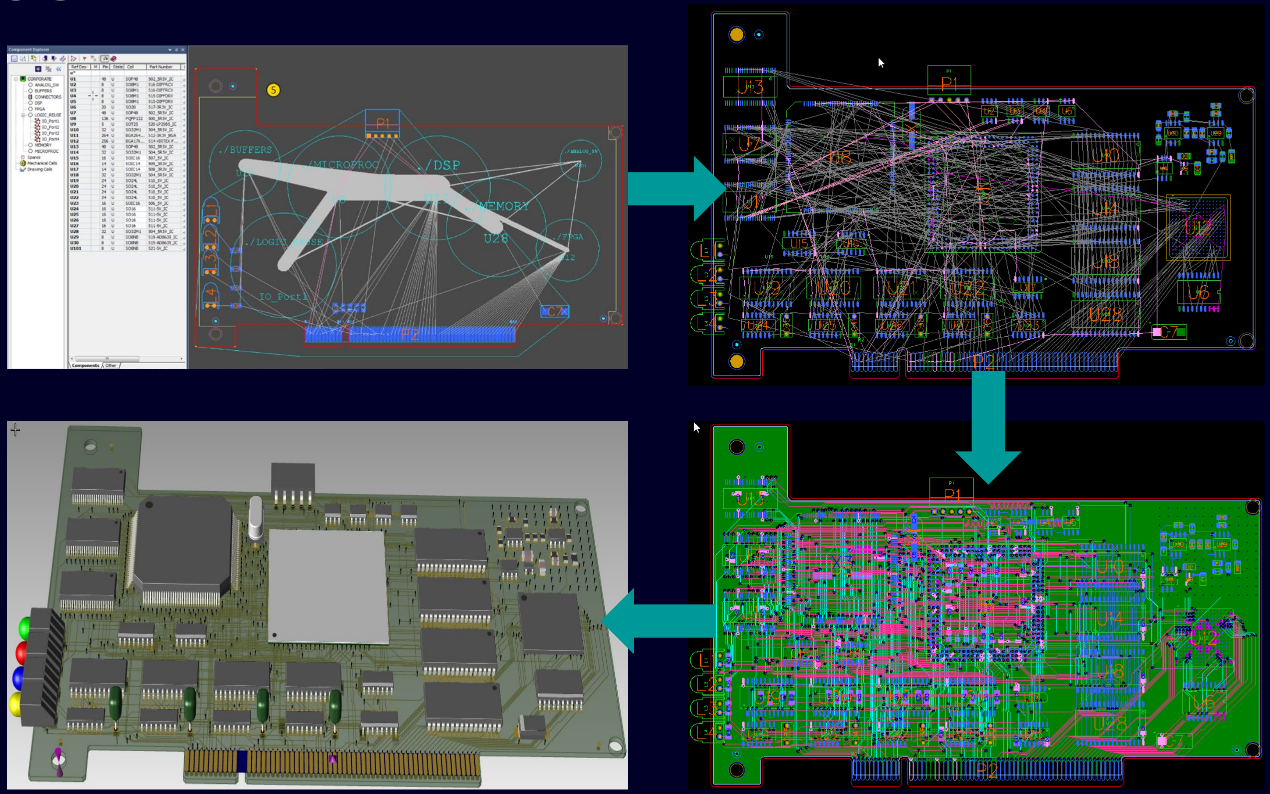
Legacy methodologies can't meet today's design complexities

Roadblocks!

- Unfamiliar with automated functions in tool
- Feeling of less control of design, don't trust
- Legacy practices are the standard

Best Practice

- Assign parts to groups/clusters
- Route using a combination of interactive and automated routing
- Generate outputs utilizing built-in automation functionality



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Process Optimization – Design Reuse

Problem!

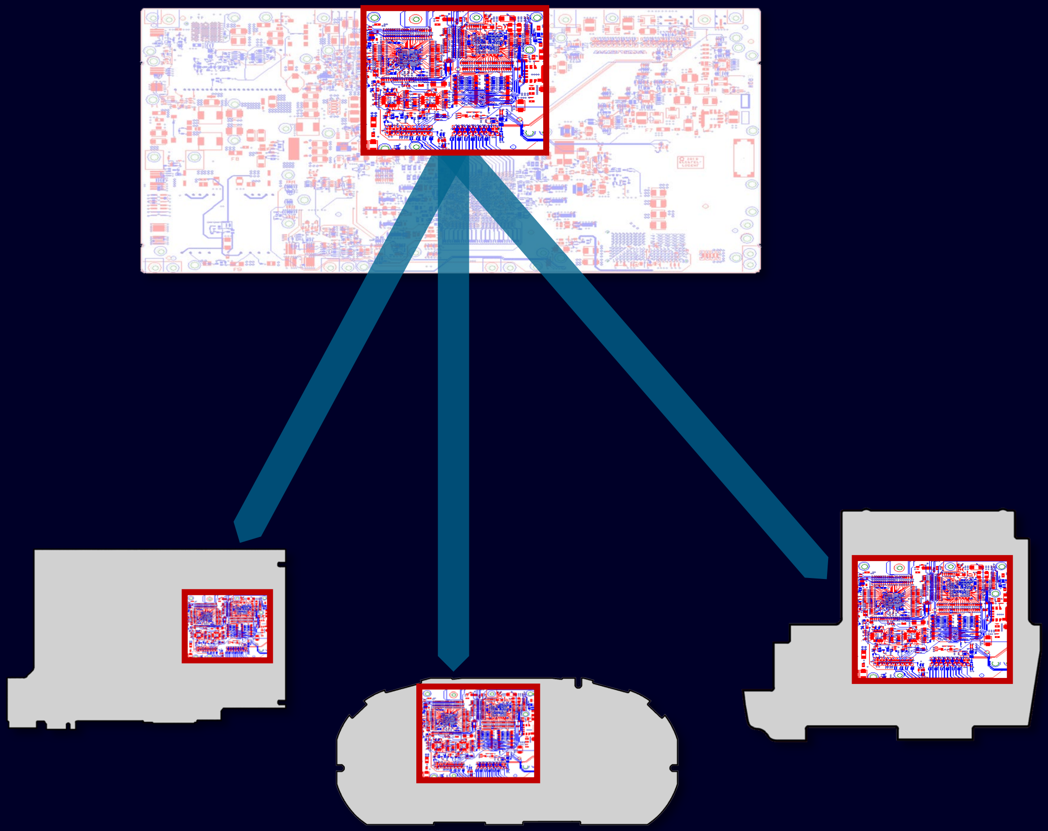
Re-inventing the wheel and poor enterprise utilization

Roadblocks!

- Inefficient process for sharing data
- Don’t trust another engineer’s circuit/layout
- No pressure to improve current methodology

Best Practice

- Utilize proven circuitry and layouts – lower risk
- Manage modules same as individual components
- Share validated HW IP throughout enterprise



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Process Optimization – FPGA/PCB Optimization

Problem!

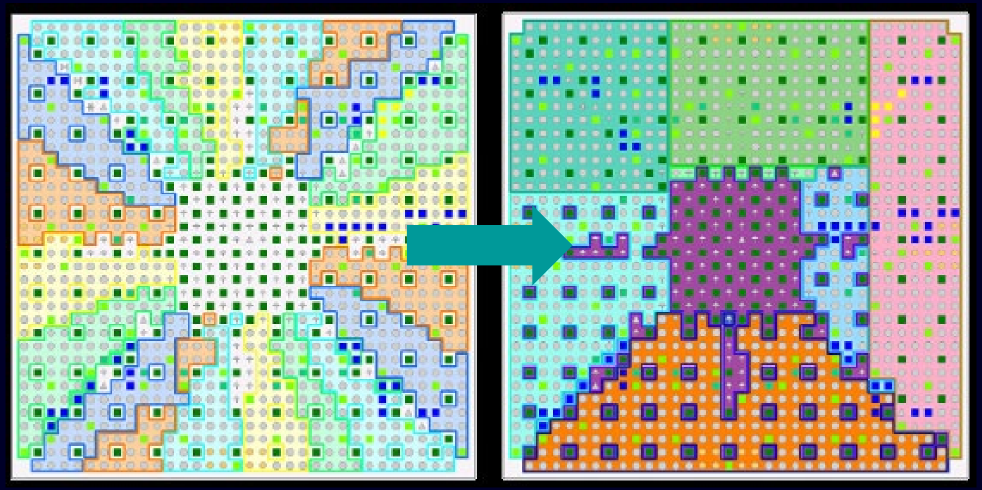
FPGA design methodology is inefficient in its ability to optimize FPGA pin-out configurations

Roadblocks!

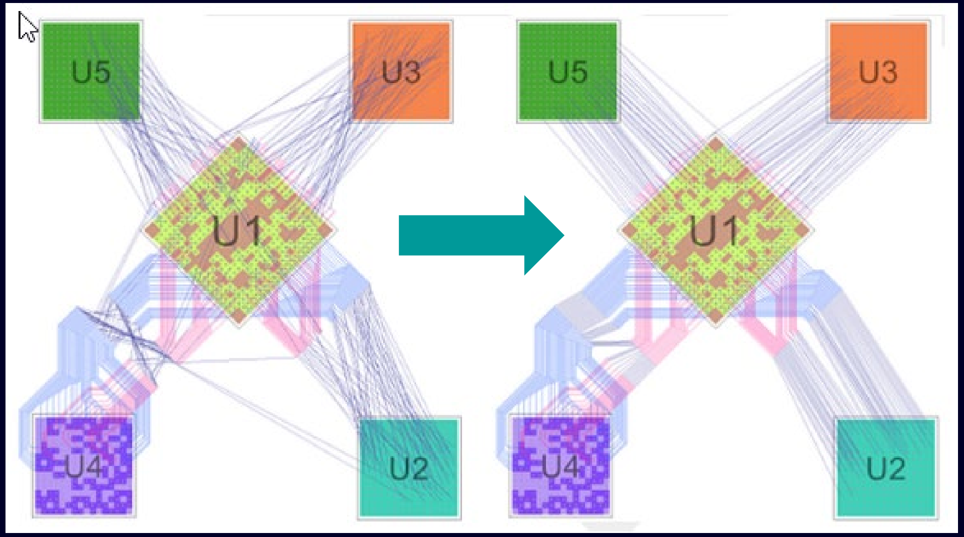
- Too much overhead to setup/implement/maintain
- FPGA tools good enough (even if they don't consider layout)

Best Practice

- Utilize FPGA/PCB integration
- Configure FPGA pin-out for routing optimization
- Enable efficient FPGA pin-swapping capability



Ten banks partitioned into seven custom pins groups



Connectivity needs to be optimized across multiple devices

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Process Optimization – High Density Interconnect (HDI)

Problem!

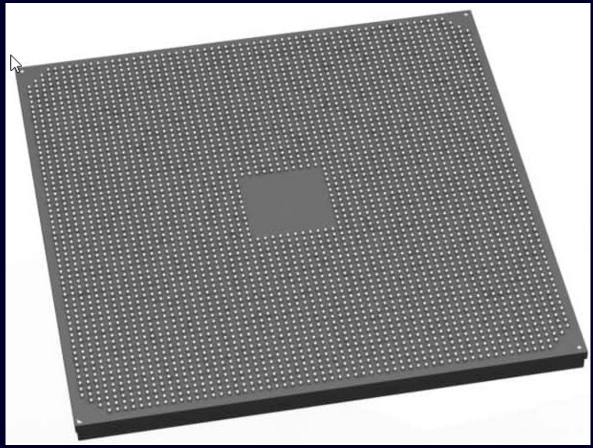
Implementing traditional via structures results in delays/cost

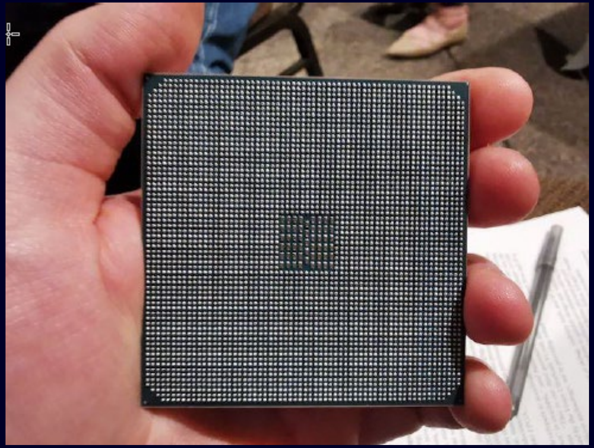
Roadblocks!

- Not familiar/proficient with tool and or subject
- Inefficient processes reduce opportunities to use HDI

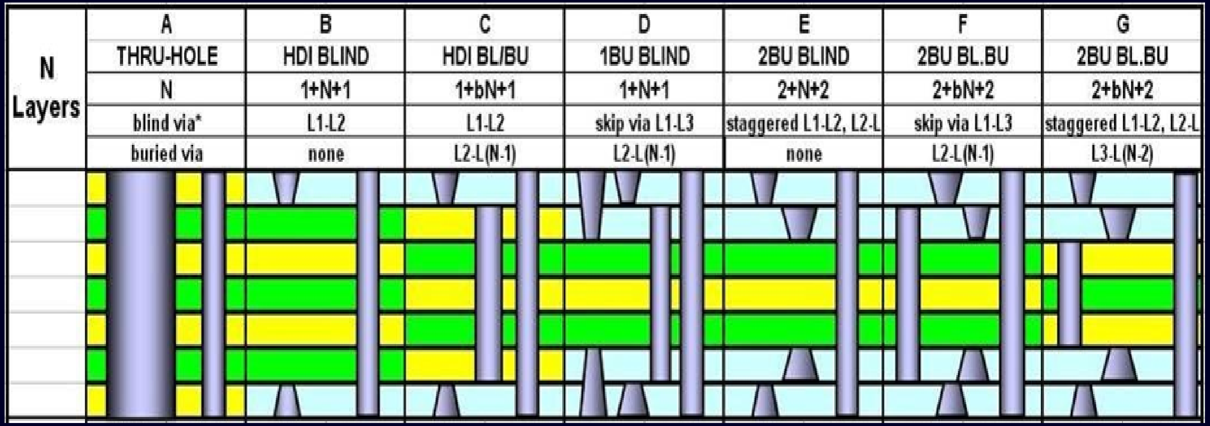
Best Practice

- Capabilities are commonly available in most tools… stop doing work-arounds!





AMD Xilinx - IC FPGA VIRTEX-UP 3824FCBGA (65x65)



Examples of HDI constructions types and methodologies

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Process Optimization – Rigid-flex

Problem!

Rigid-flex design using rigid structures is inefficient and error prone

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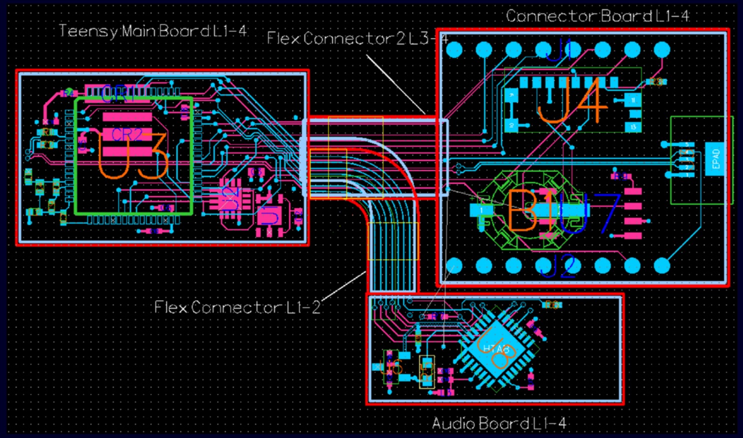
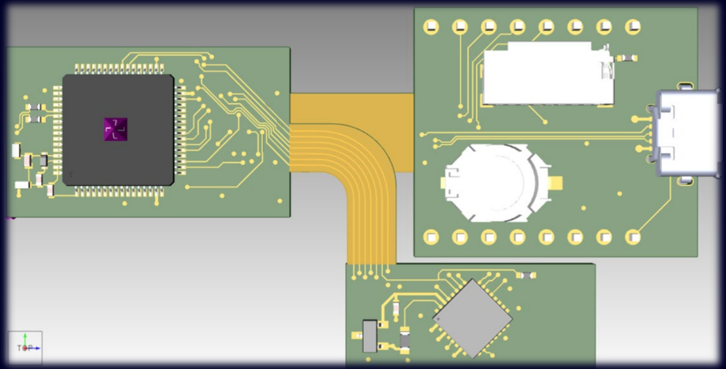
Roadblocks!

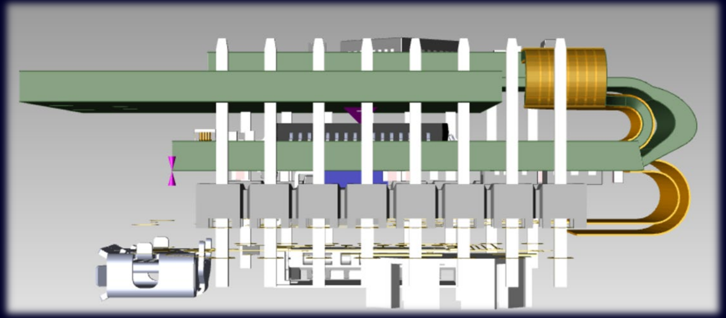
- Not familiar/proficient with tool and or subject
- Use standard rigid PCB approach for everything
- Requires specialist/SME

Best Practice

- Utilize updated rigid-flex design methodology to efficiently define board outlines, stack-ups, and regional constraints







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Process Optimization – IC/Package/PCB

Problem!

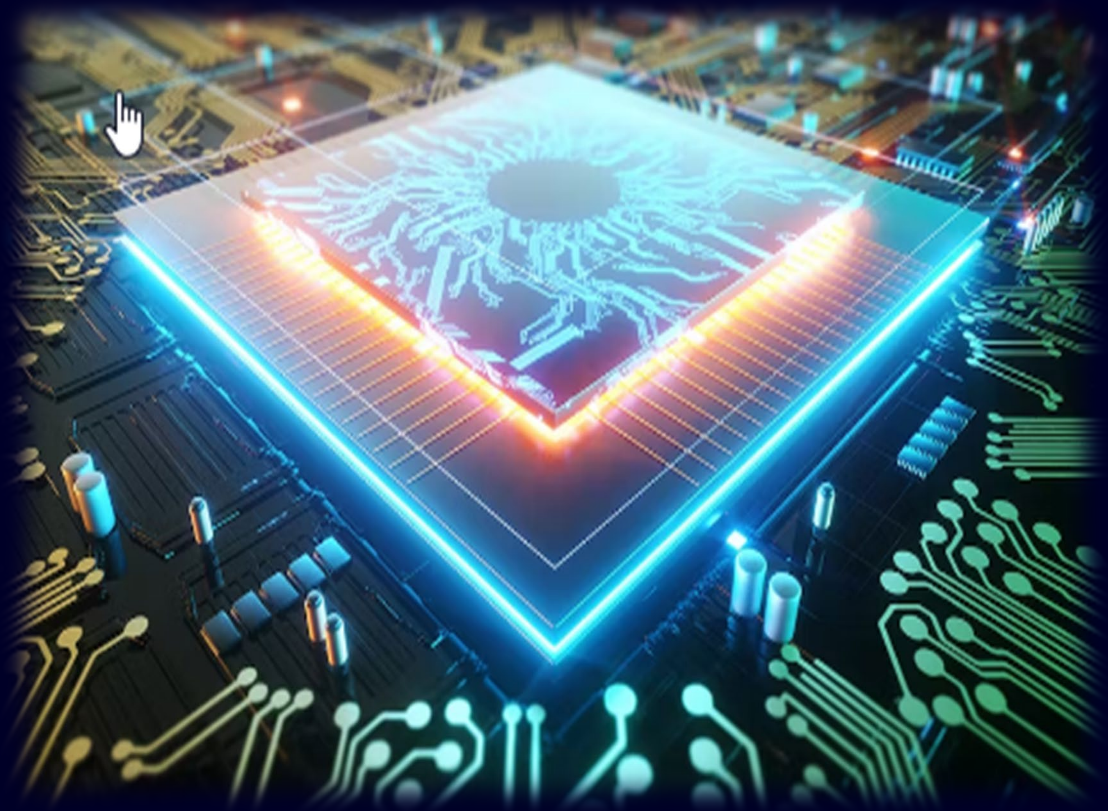
Inefficient IC/package/PCB optimization, not considering all "fabrics" simultaneously

Roadblocks!

- Not familiar/proficient with tool
- Too much overhead to setup/implement/maintain
- Too expensive to implement

Best Practice

- Utilize Systems-Level Model Based Engineering
- Optimize the system IO
- Enable digital twin



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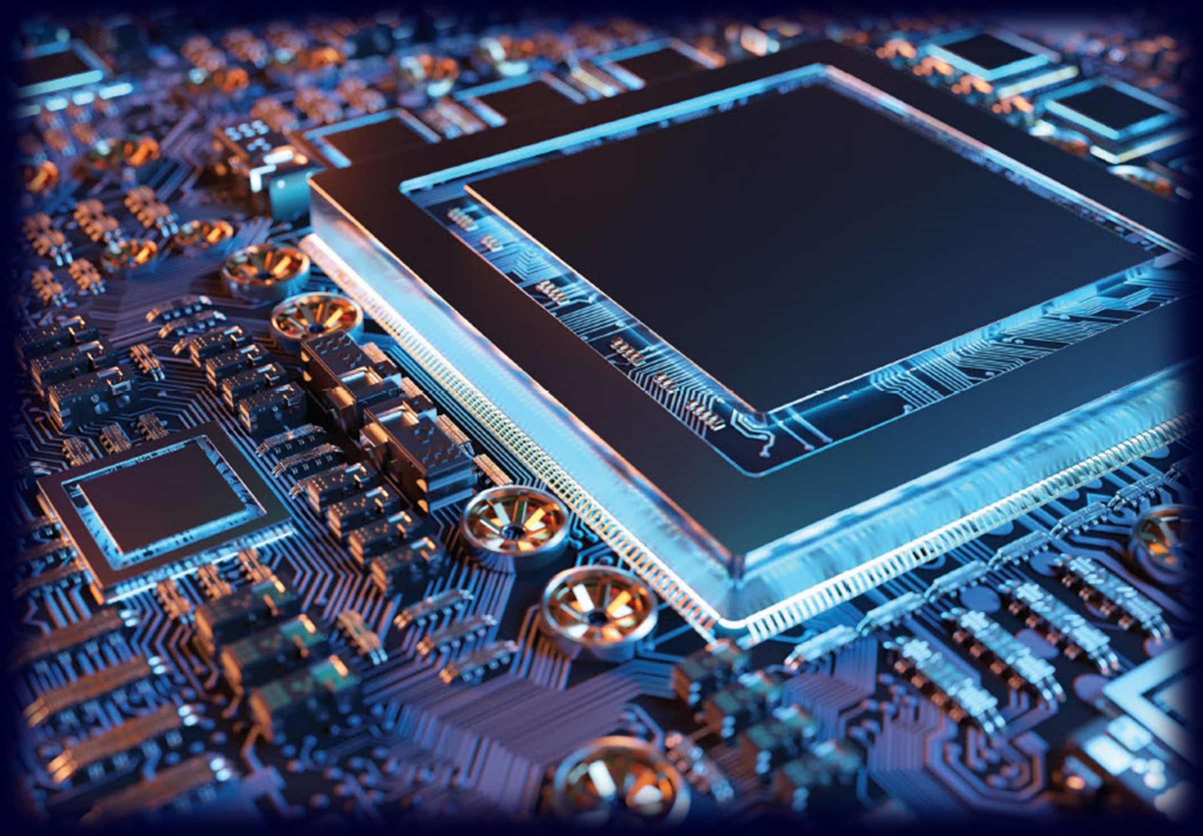
Summary
Designing Complex PCBs

- Must address the three perspectives of PCB design
- Implementing best practices have huge benefits and increased ROI
- Understand the impact of decisions made upstream and their affects down stream in manufacturing
- Multidiscipline and multidomain collaboration and integration is key (this includes with your suppliers)
- Utilize today's EDA tool automation and horsepower to your advantage
- Know the true cost of doing nothing (remaining status que)
- Be open to new methodologies, AI, ML and Cloud-based connectivity
- Know that company culture can be the ultimate roadblock



Questions?

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Transforming electronic systems design

- **Intuitive user-experience** to speed time-to-ramp
- **AI-infused** to accelerate productivity
- **Cloud-enabled** to enable development across the electronics design chain
- **Integrated** to support multi-discipline co-design
- **Secure** to protect critical IP and export compliance

image courtesy of Iconnect007

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Thank You!

[Link to Building an effective PCB design flow - 36 video series](#)

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