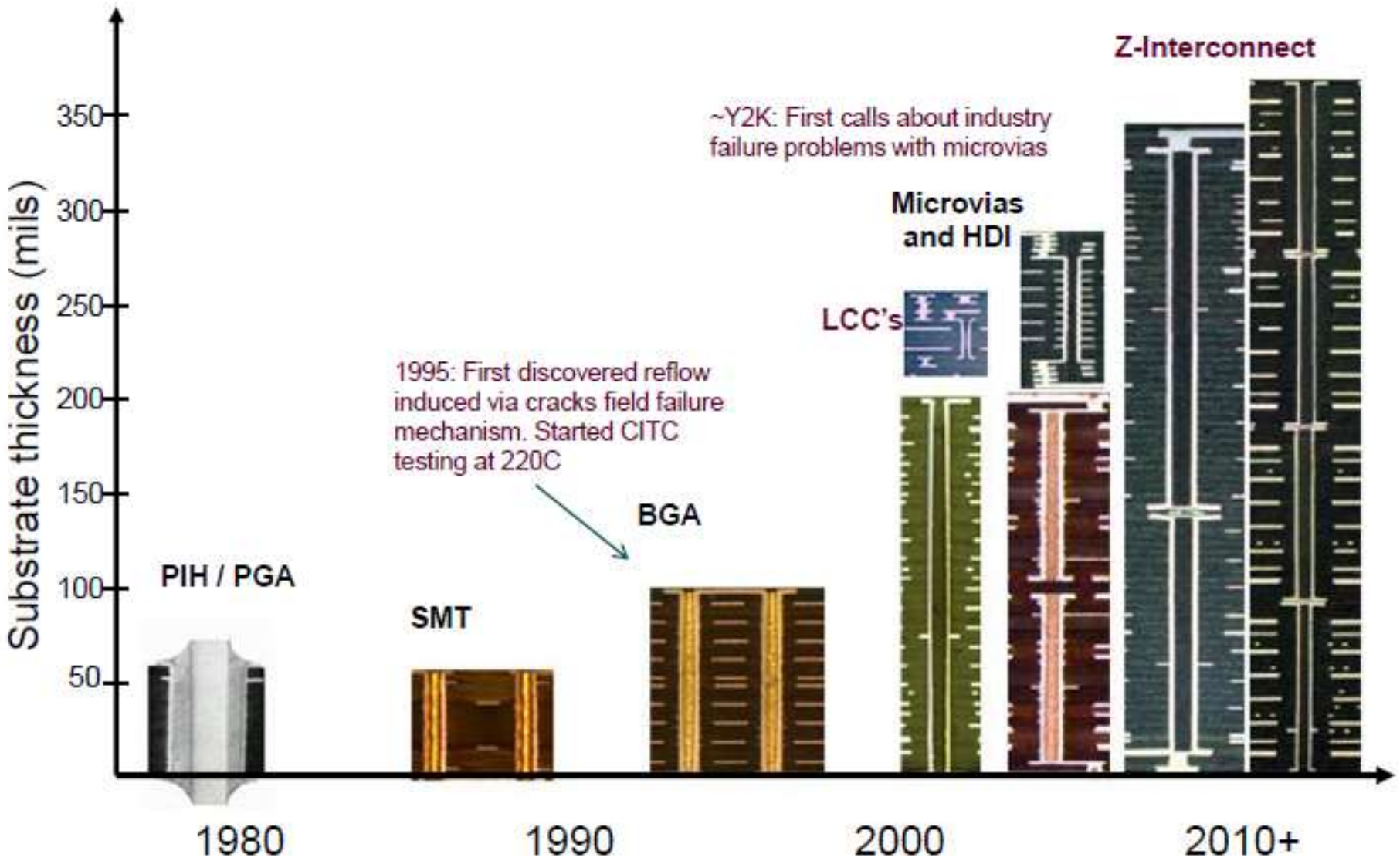
Advanced Materials and Processing

Paul Cooke

Director of Engineering

The PTH Yesterday and Today

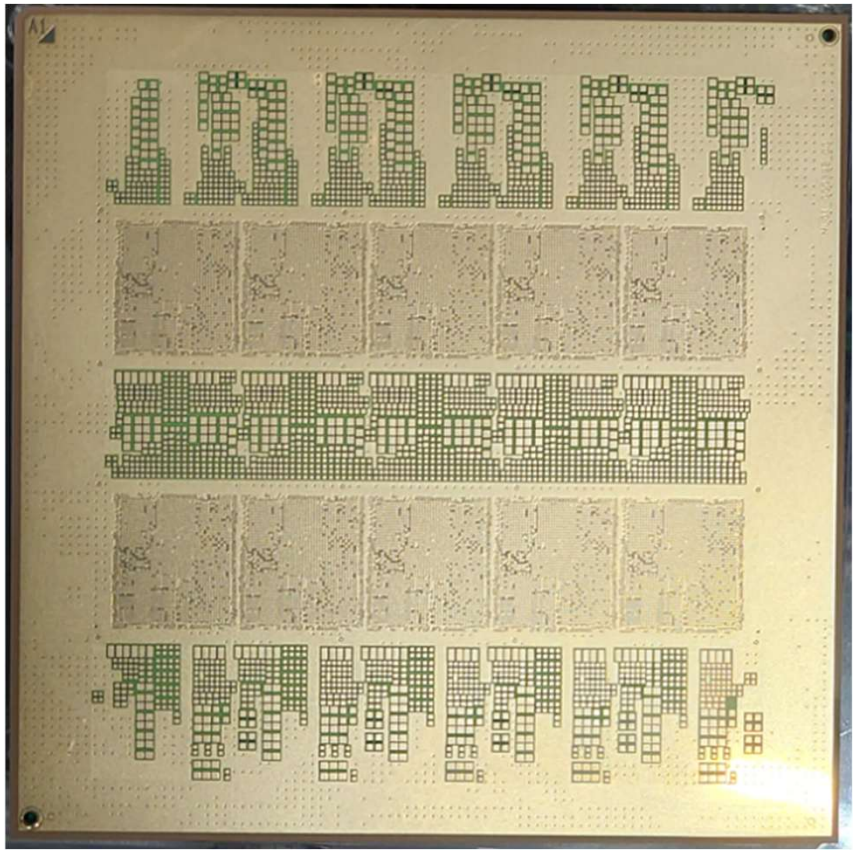


Probe card customer 14-24-14 MLO (2022 Fab)

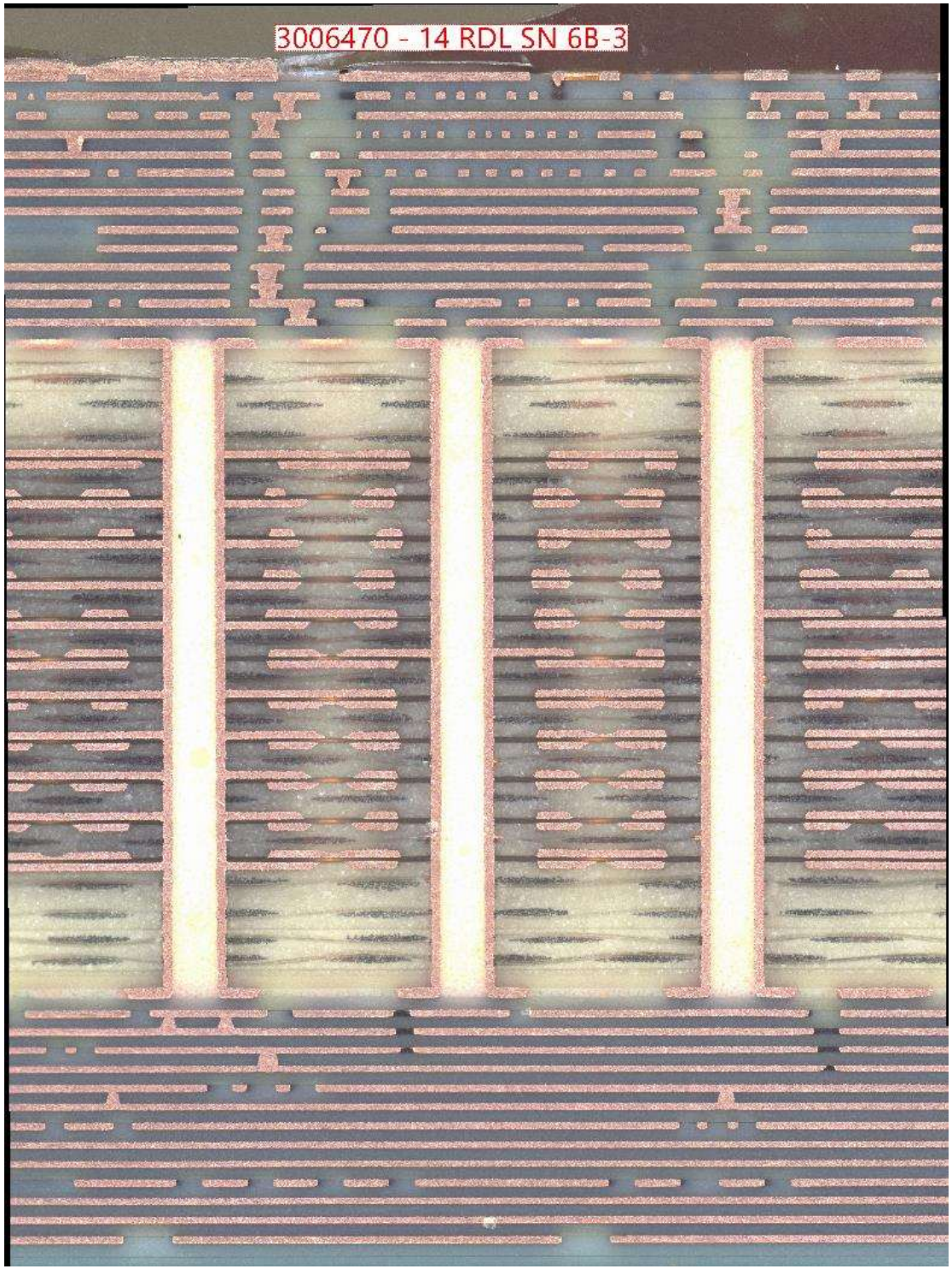
Die Pitch – 90um #of Die Pads ~ 86K (Total for 10 Dies)- 1421601 (~1.4 Million vias connection thru 12 RDLs Top and Bottom)

BGA Pitch - .55mm #of BGA Pads ~ 16K

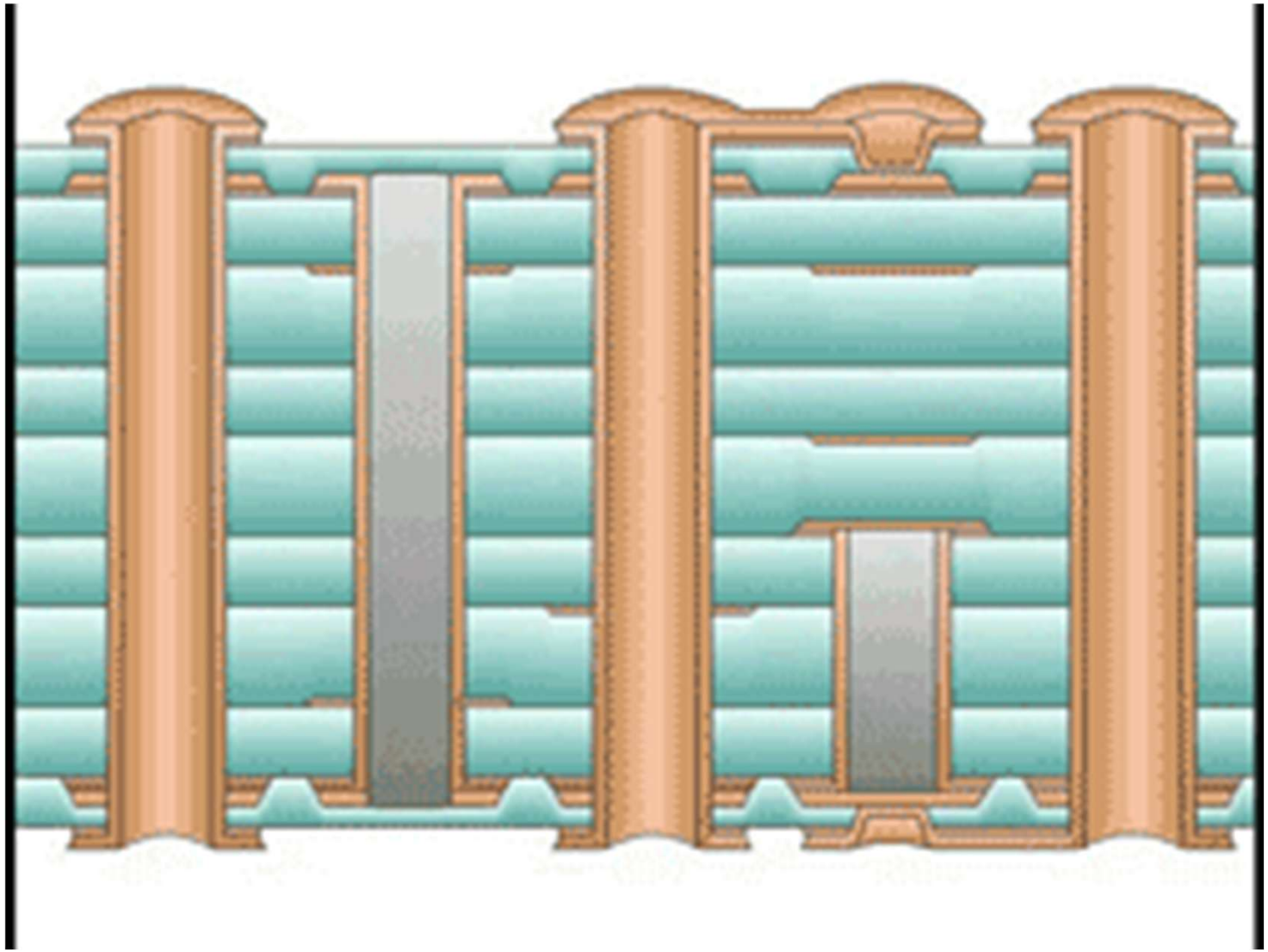
Board Size – 72x72 mm(2.8”x2.8”), Thickness – 3mm (.118”) - 1up 6”x6”



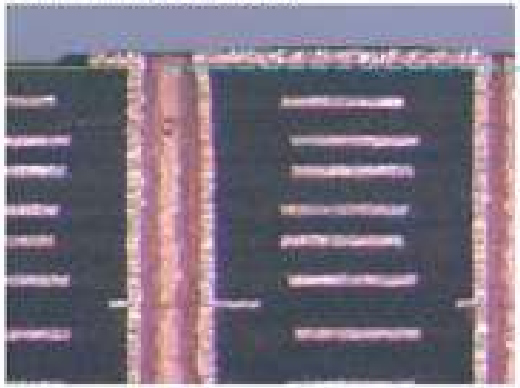
Coplanarity			
C4 Pad (Dut 1) Z-Height	25 µm Max.	16.2 µm	✓
C4 Pad (Dut 2) Z-Height	25 µm Max.	9.6 µm	✓
C4 Pad (Dut 3) Z-Height	25 µm Max.	10.6 µm	✓
C4 Pad (Dut 4) Z-Height	25 µm Max.	5.8 µm	✓
C4 Pad (Dut 5) Z-Height	25 µm Max.	13.3 µm	✓
C4 Pad (Dut 6) Z-Height	25 µm Max.	16.4 µm	✓
C4 Pad (Dut 7) Z-Height	25 µm Max.	9.2 µm	✓
C4 Pad (Dut 8) Z-Height	25 µm Max.	6.8 µm	✓
C4 Pad (Dut 9) Z-Height	25 µm Max.	8.1 µm	✓
C4 Pad (Dut 10) Z-Height	25 µm Max.	16.7 µm	✓
Overall C4 Side Z-Height	100 µm Max.	58.1 µm	✓
Overall BGA Side Z-Height	100 µm Max.	52.1 µm	✓


3006470 - 14 RDL SN 6B-3

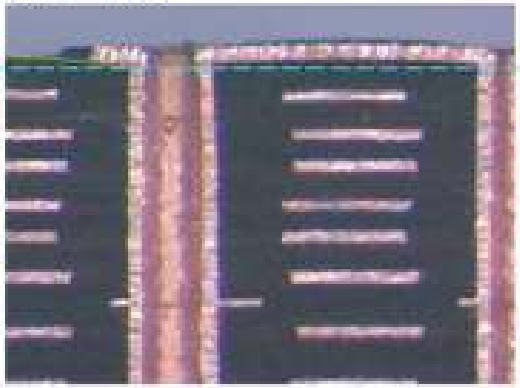
Thermal Expansion



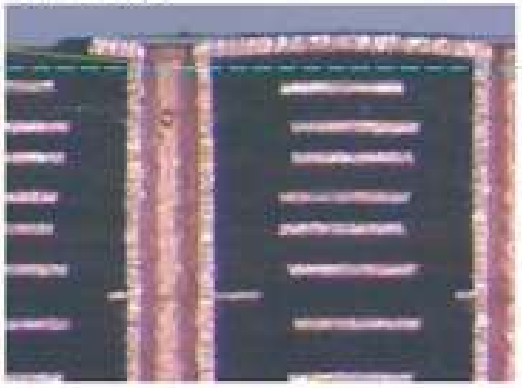
a) T=Ambient (start)



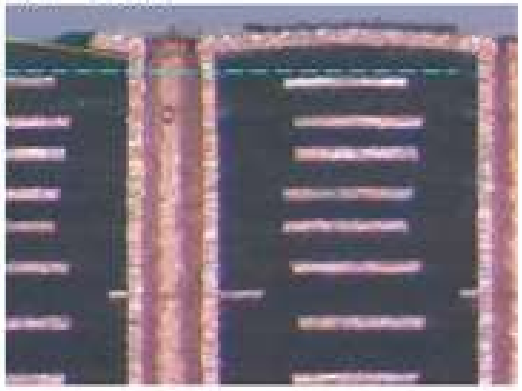
b) T=175C

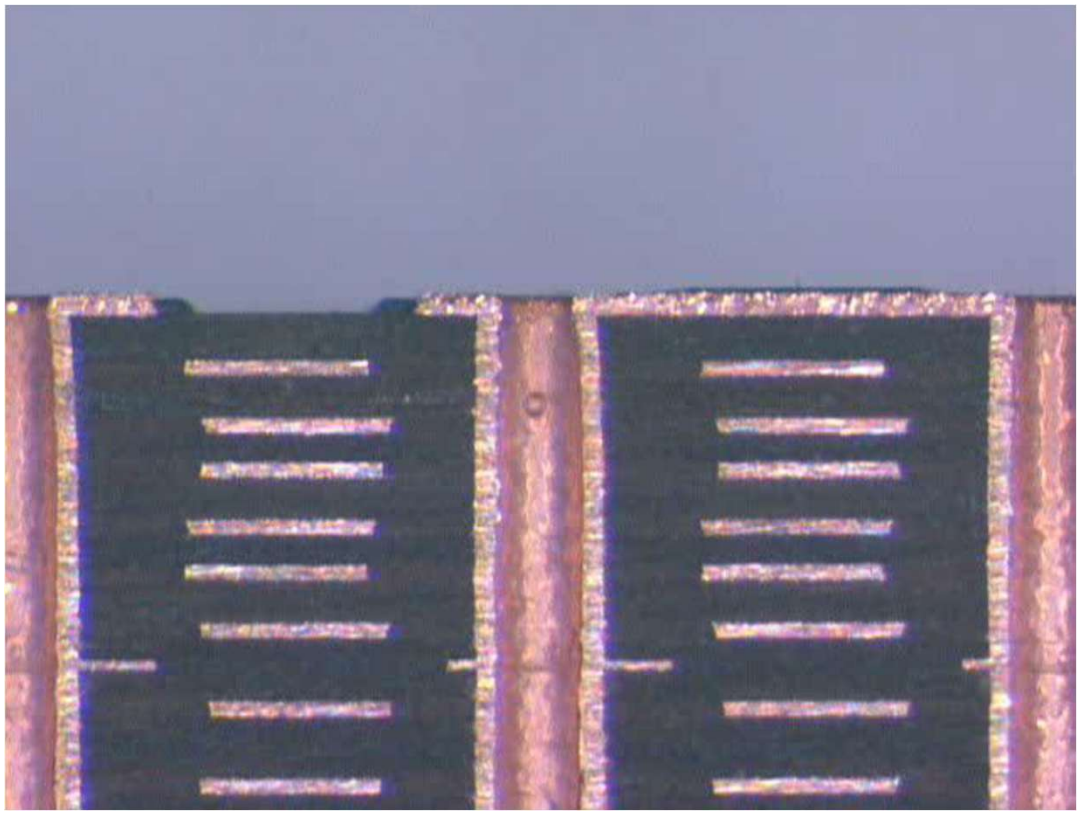


c) T=220C



d) T=260C

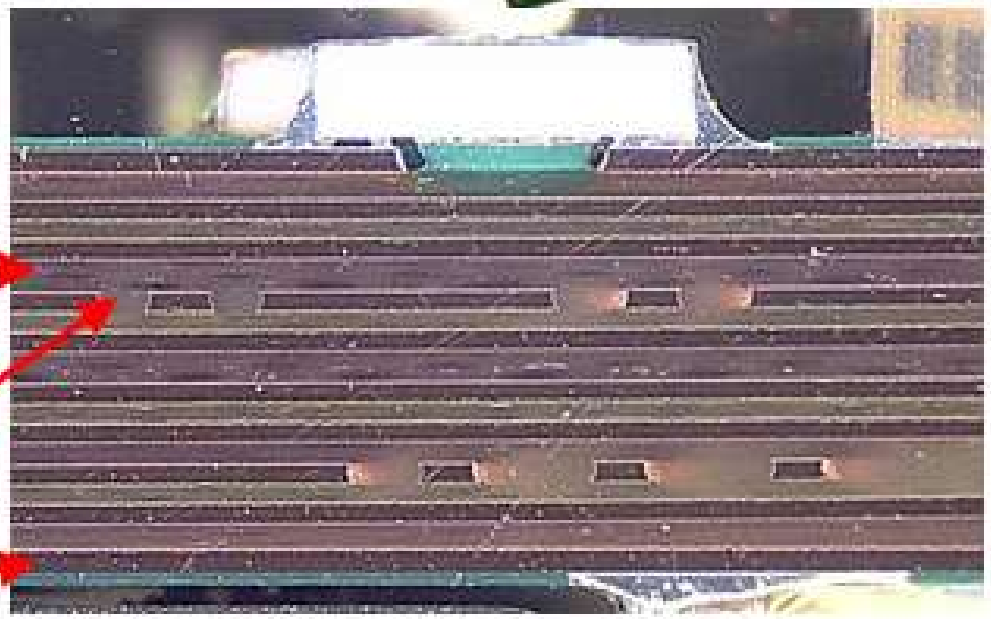




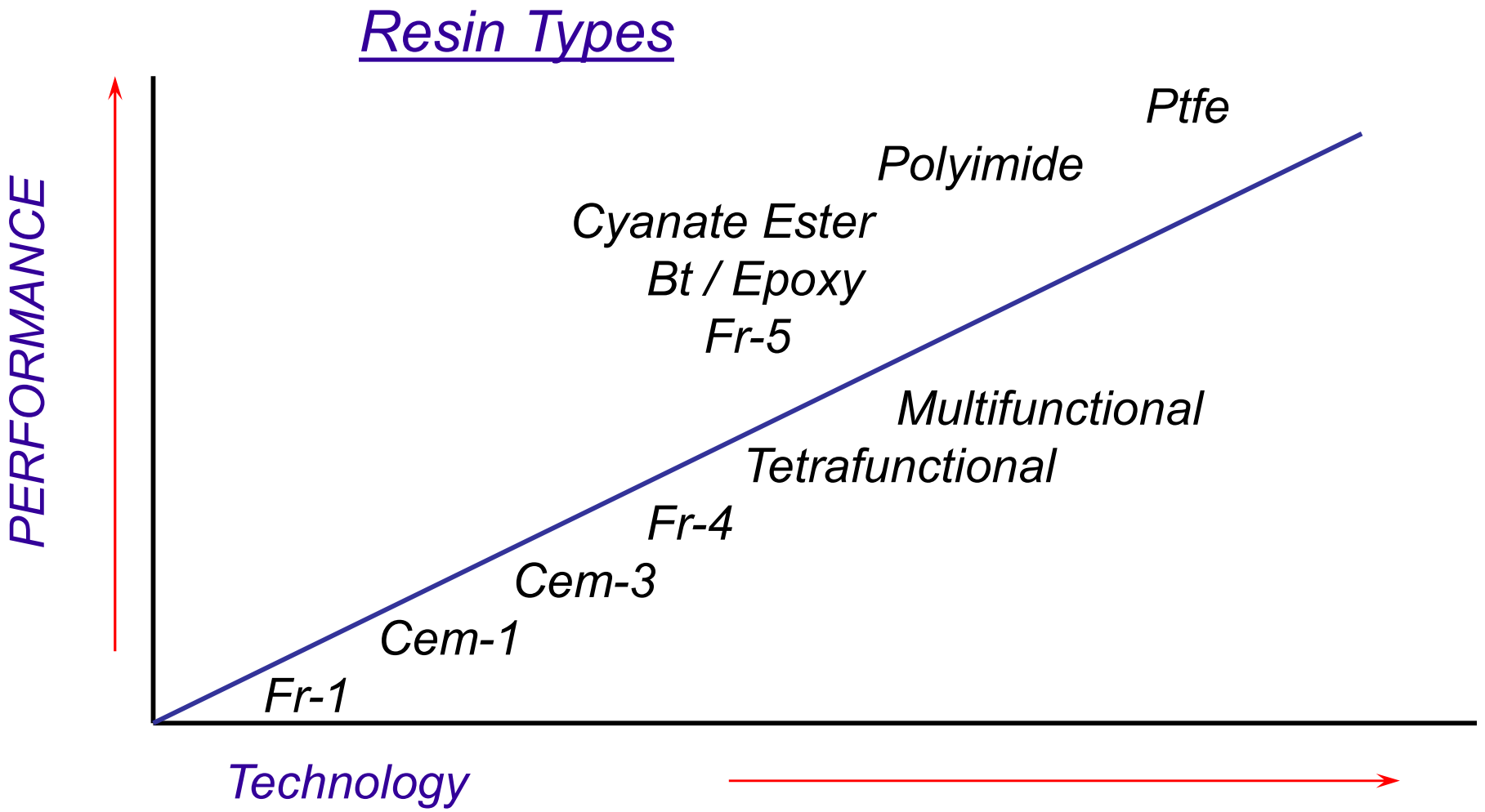
Materials

Printed Circuit Board

- Composite material
  - Reinforcement (glass cloth)
  - Polymer (resin)
  - Copper



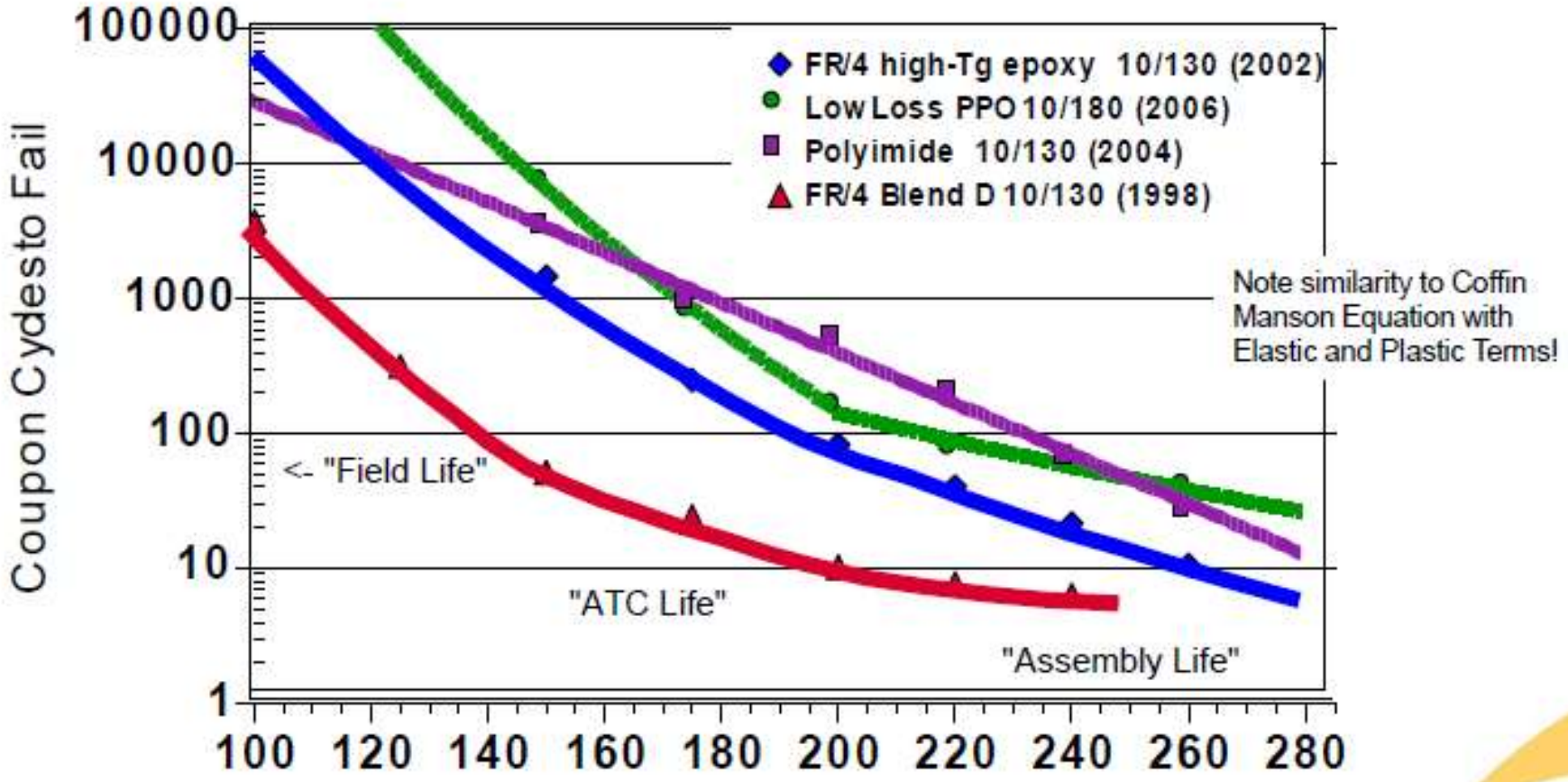
Evolution of Resin Based Materials

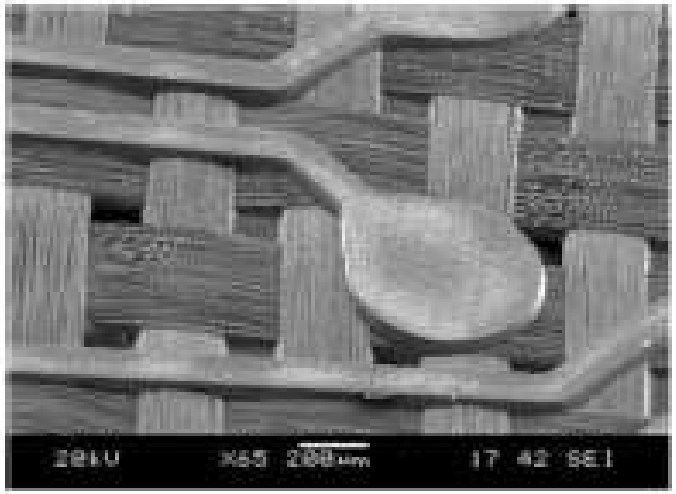


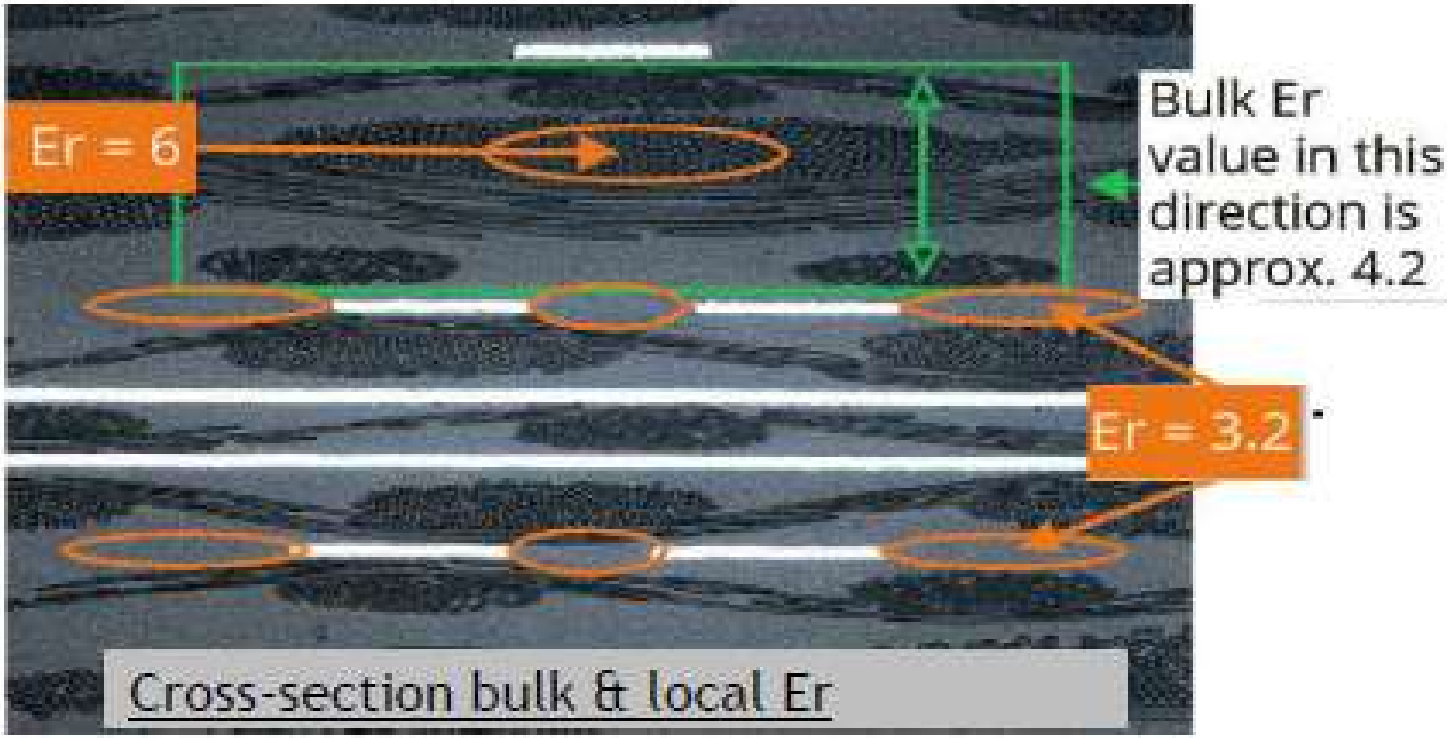
Reflow and The PTH Life Curve

CITC Life Curves at multiple temperatures, quick and effective way to:

- Evaluate and compare laminate materials
- Project via Life for any assembly/use temperatures (Cumulative Damage)
- Illustrate the importance of Reflow!

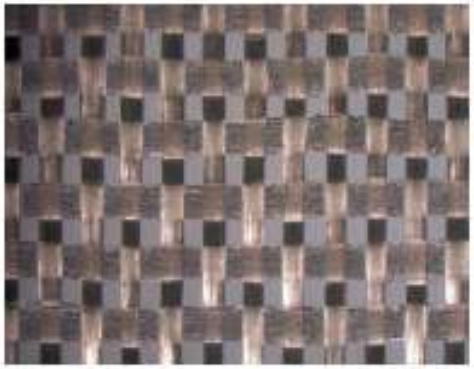



20kV
X65
17 42 SEI


Er = 6
Bulk Er value in this direction is approx. 4.2
Er = 3.2
Cross-section bulk & local Er

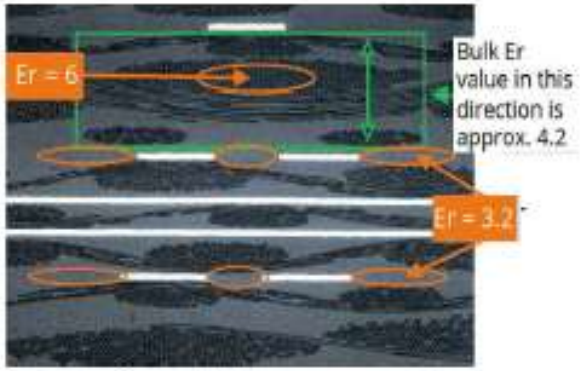
Glass styles

Material – glass style



Traditional glass cloth

Flattened glass cloth



Cross-section bulk & local Er

Flattened glass cloth:

- Achieved by mechanical or water jet blasting & "low twist"*
- **Good** for laser drilling and has a hidden side effect- signal integrity .
- **Better** control over finished thickness and thickness variation.
- **Risk** of resin starvation – choose optimal %RC** .

Glass styles

Material – *Electrical properties*

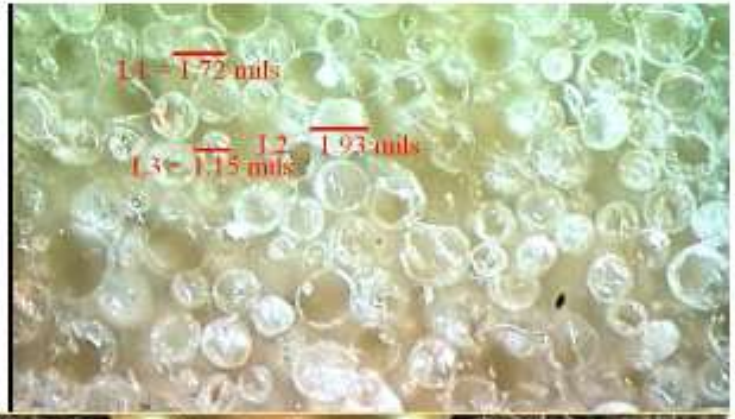
	Ref.	Standard		enhanced			
	FR4	FR408HR	RO4350 / ITERA	RO/3000 6000 / CLTE	FLEX PTFE	ASTRA MT	RO5880LZ
Dk @ 10 GHz	3.92	3.68	3.48	2.94-3.00	See next	3.00	1.96
Df	0.025	0.0092	0.0037	0.0013-0.0012	See next	0.0017	0.0019
Thermal Conductivity (W/m*K)	0.4	0.4	0.69	0.60-1.1	See next	0.45	0.33

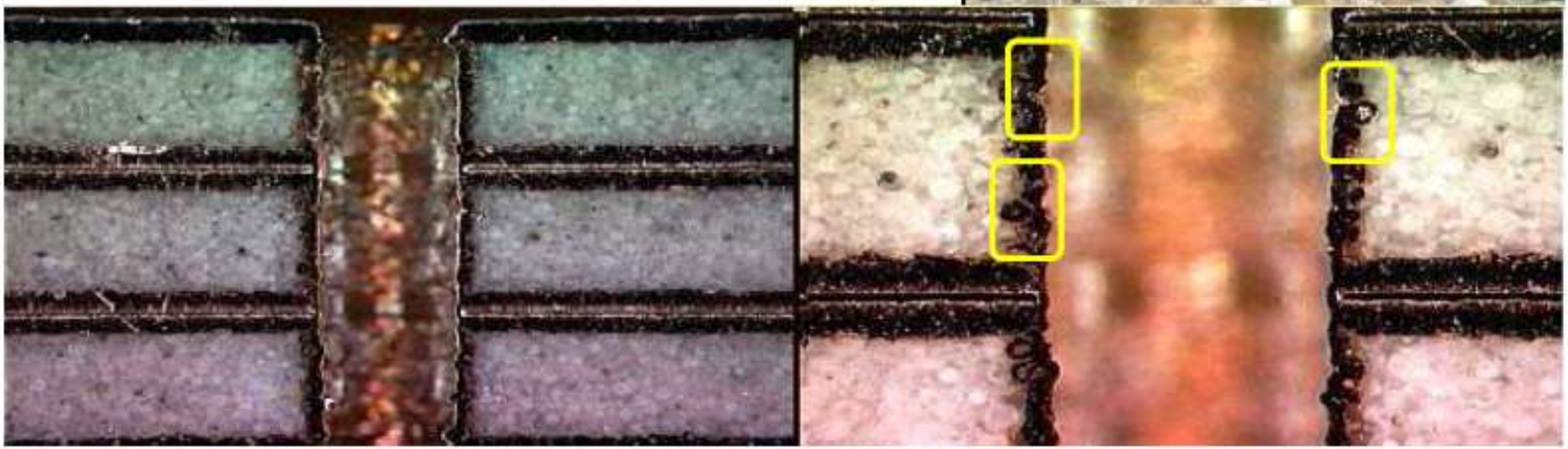
Glass styles

Material – fillers

RT/duroid® 5880LZ - unique filler system:

- Very low Dk
- Low Df
- Low weight
- Same Dk in all directions (as isotropic as it gets!)





Landless Vias

Landless Plated Through Holes – cont'd

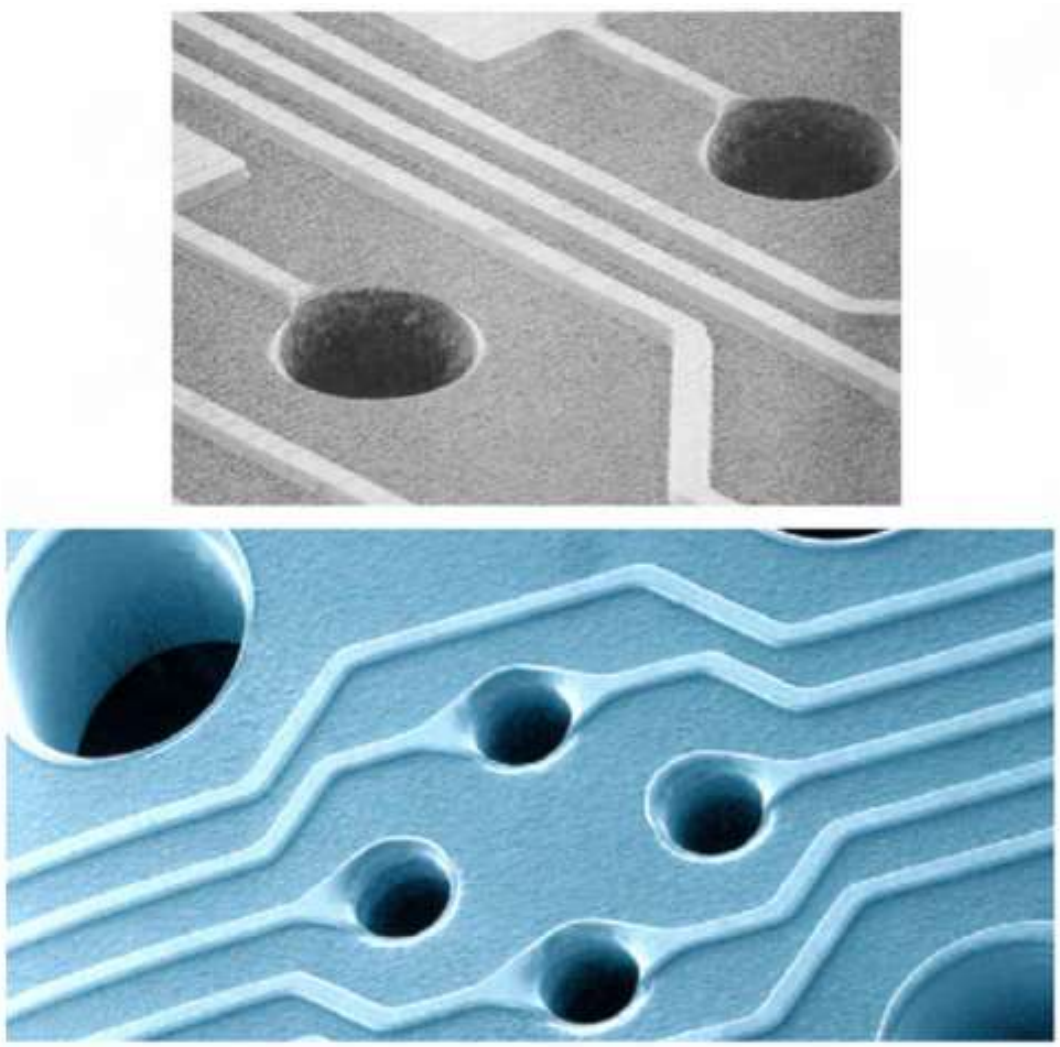
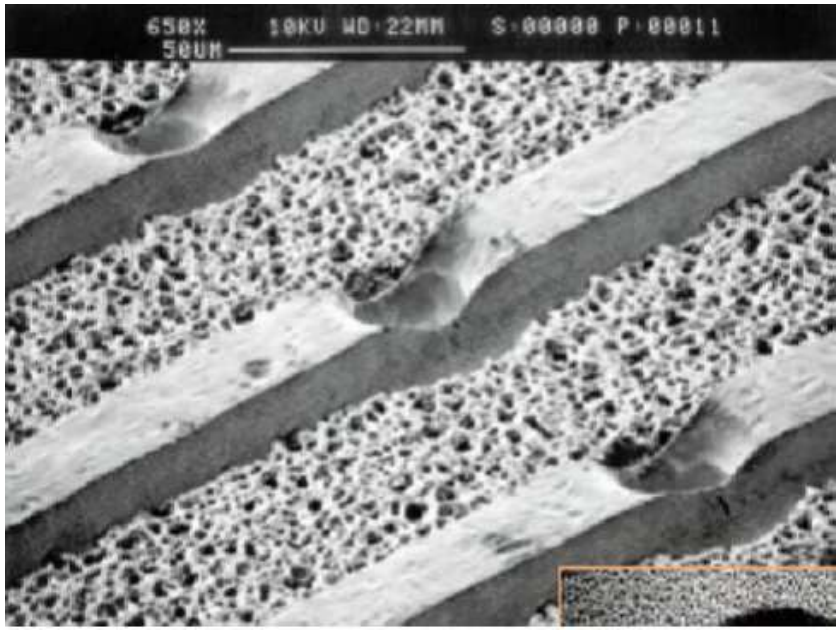


Figure 2: Typical landless vias on a Japanese multilayer from ~1985.



Courtesy – Happy Holden
The PCB Magazine

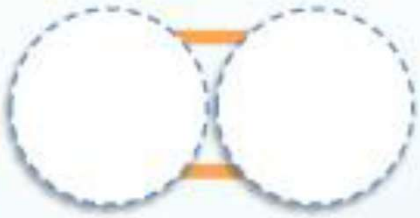
VeCS

VeCS process (D)

1. Rout slot, this can be done after lamination (at the drilling stage).

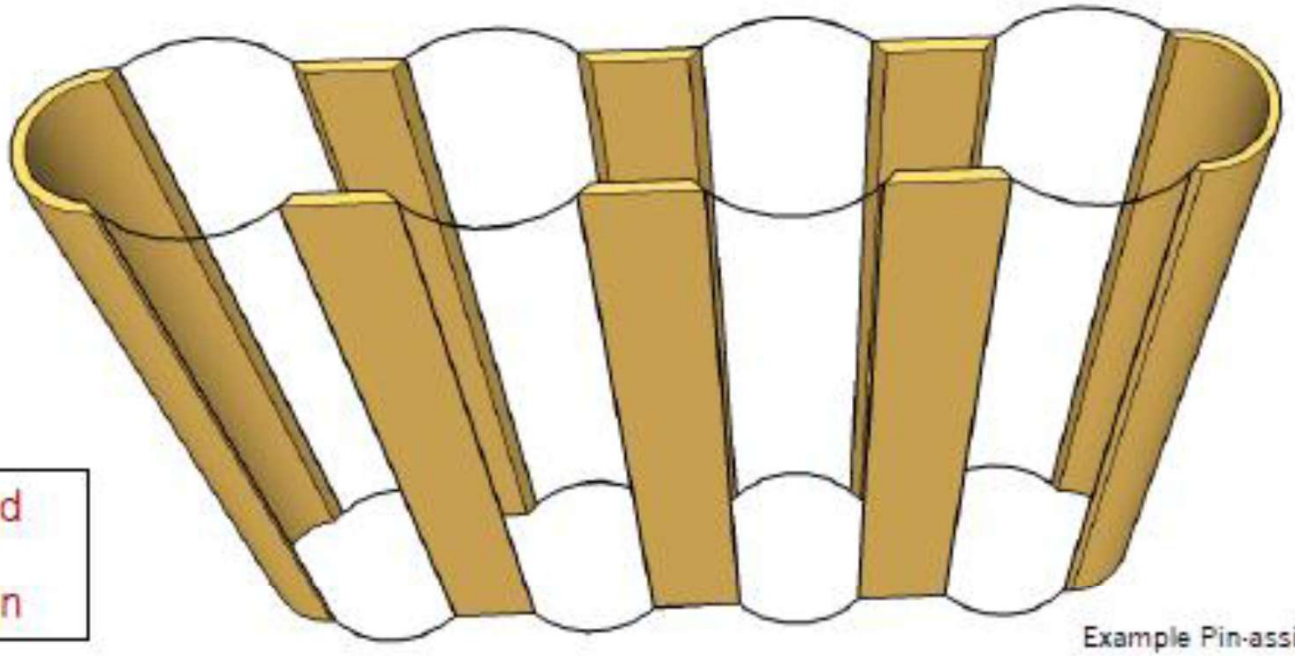
2. Apply seed layer and build up a conductive layer in de slot.

3. Remove plating plating creating two potentials. In this example it is done by using drilling or milling but it can be done by more advance techniques as photo definition and etching. As drilling and milling is known to the industry is the most logical to start with the existing process infrastructure.



VeCS

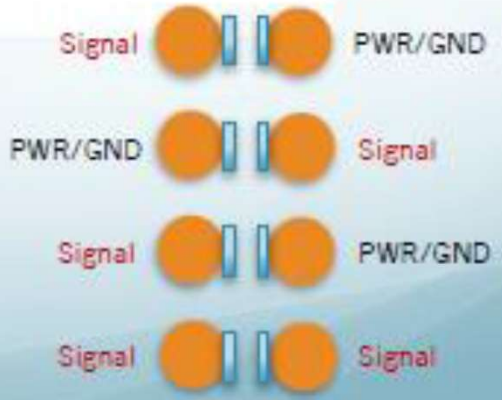
The hole is replaced by a vertical trace or half a sphere.
Preferred is the vertical trace from a signal integrity performance.

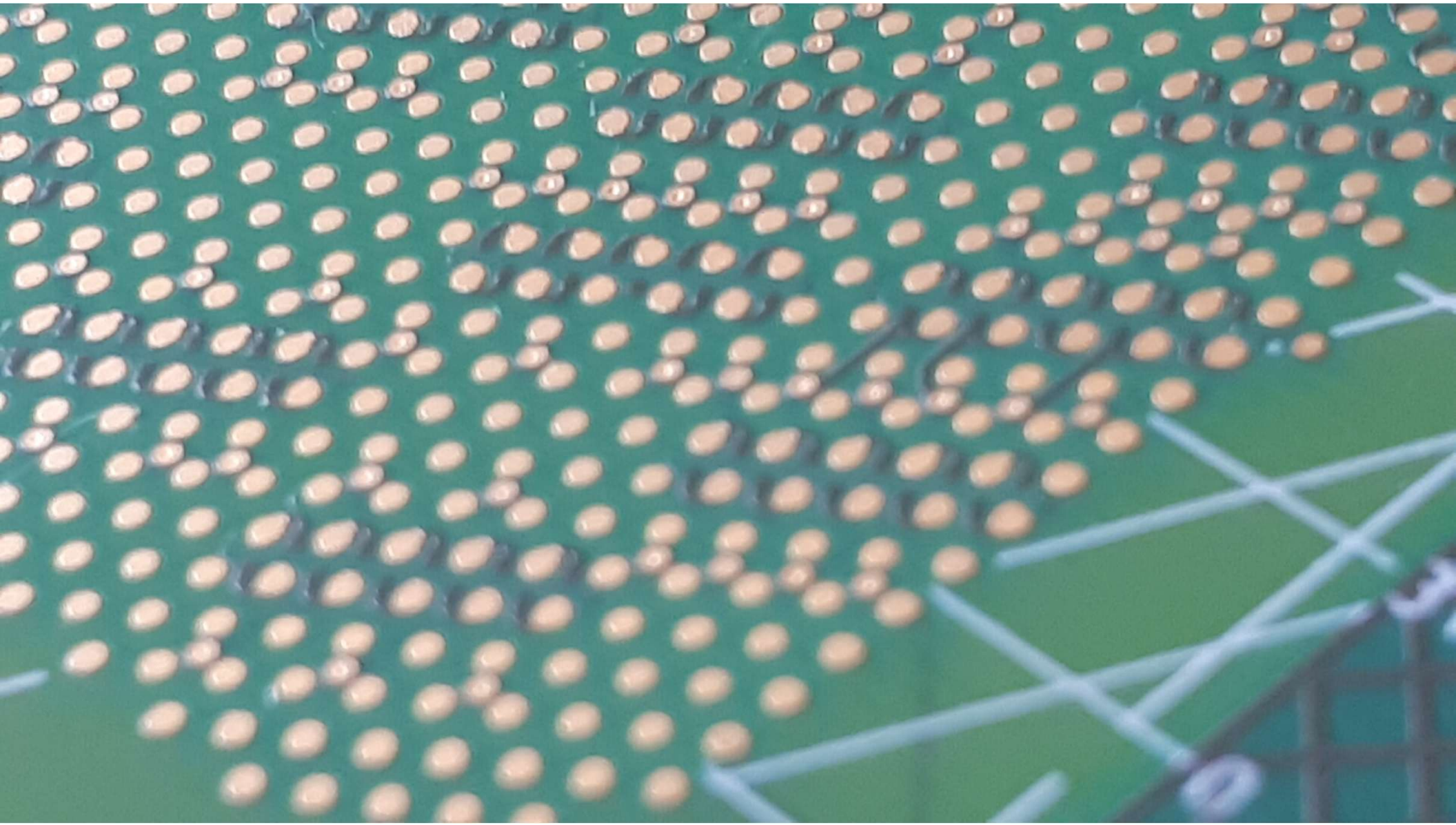


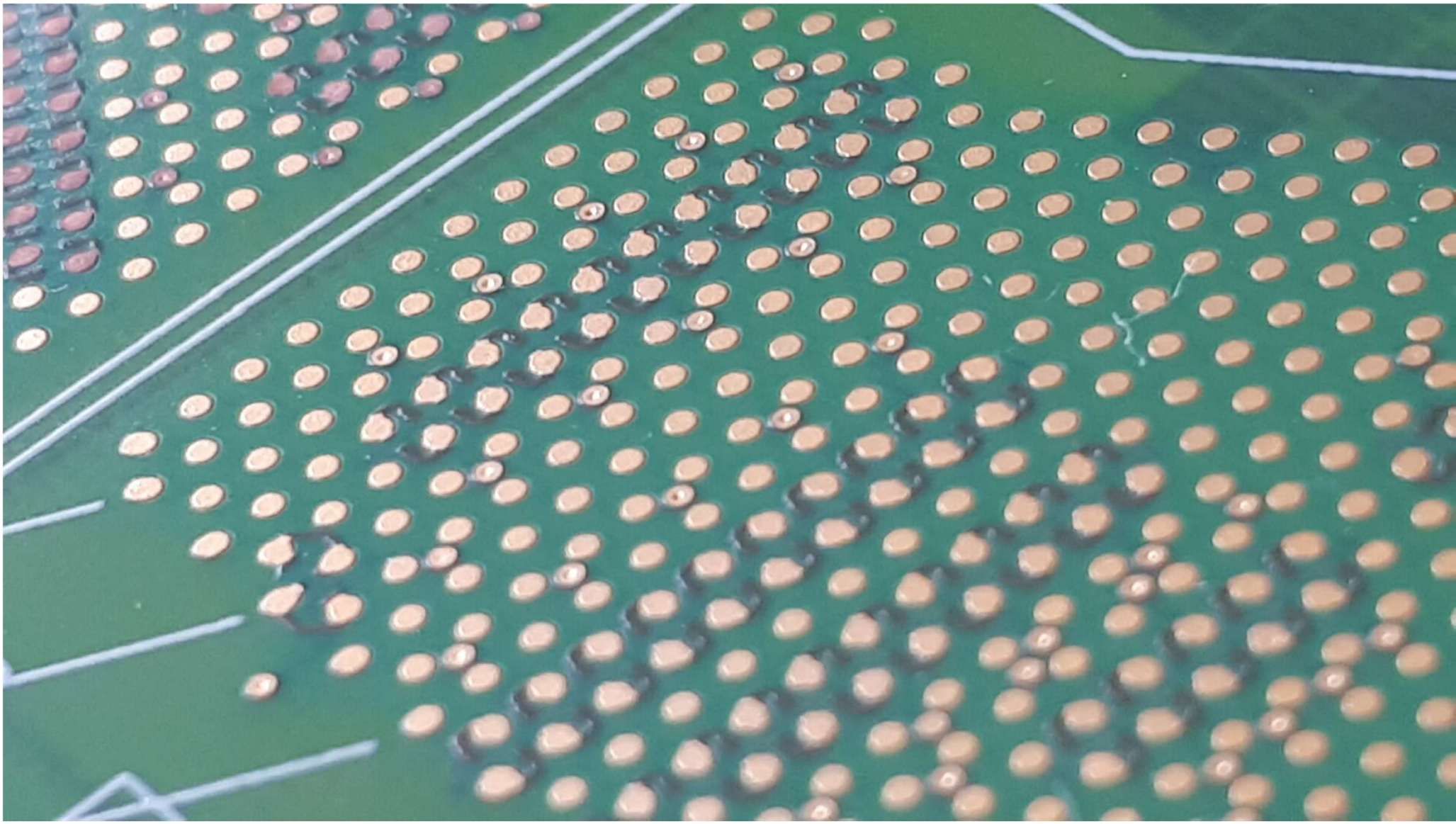
Structure can be filled and over-plated depending application

- More vertical connections per surface area
- No CAF path between vertical traces
- Coupling and Broad side coupling
- Thicker dielectrics, wider traces

Example Pin-assignment







Fine Line

Additive processing

Catalytic Precursor Ink

This ink controls the horizontal dimensions of line width and spacing

The vertical dimension of metal thickness is controlled

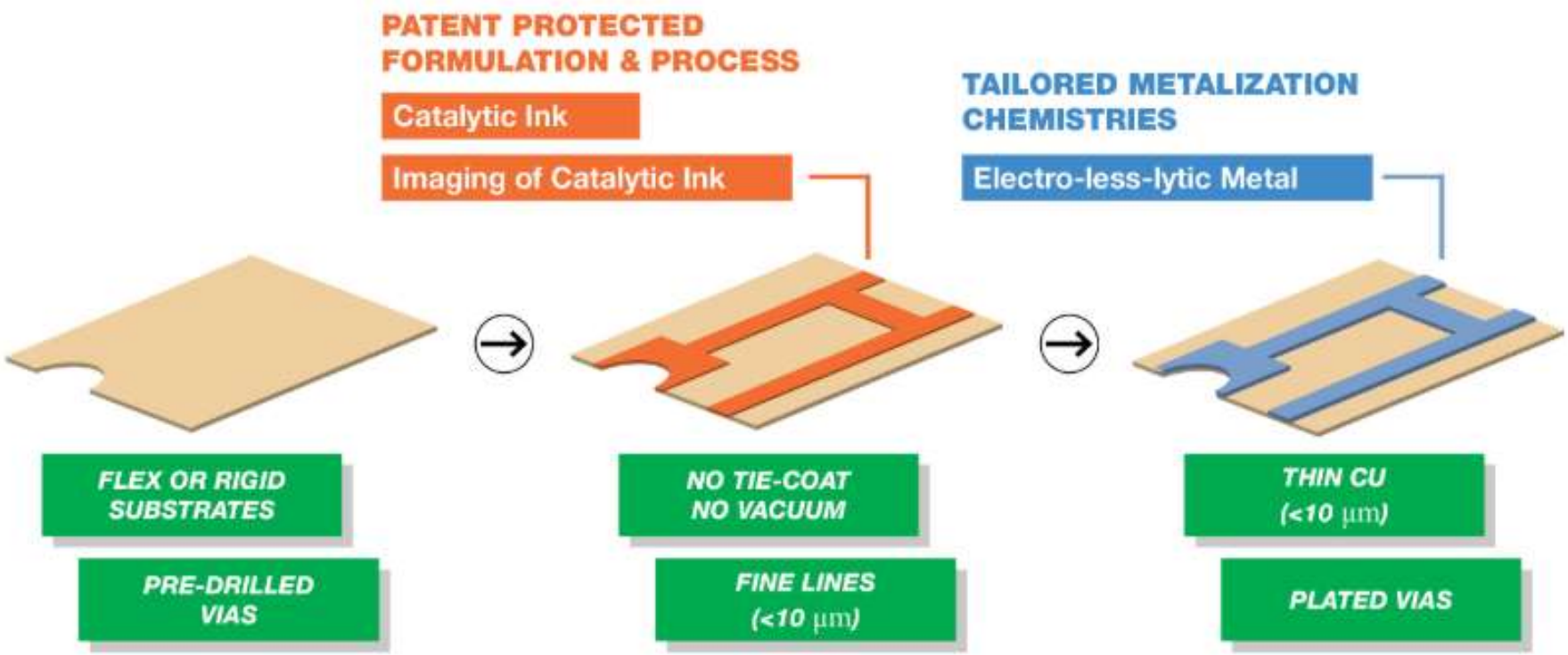
Interior of vias can be plated with metal using the same

The precursor ink promotes good bonding between the thin metal patterns and the substrate

Process

The technology can create metal lines/spacing widths below 5 microns and deposit copper to a thickness level from 0.1 micron up to 10 microns or more.

The additive feature of this technology allows the direct deposition of copper on a substrate in the pattern specified by the circuit design artwork without tie coat, adhesive, etching, or waste of copper.



STEP 1.

Substrate

STEP 2.

Drill vias in Substrate

STEP 3.

Coat/Cure Ink

STEP 4.

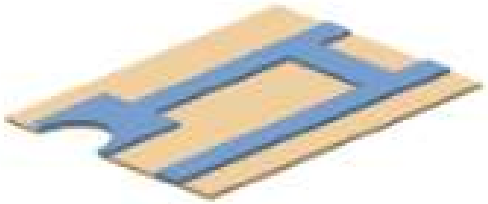
Make Ink Pattern

STEP 5.

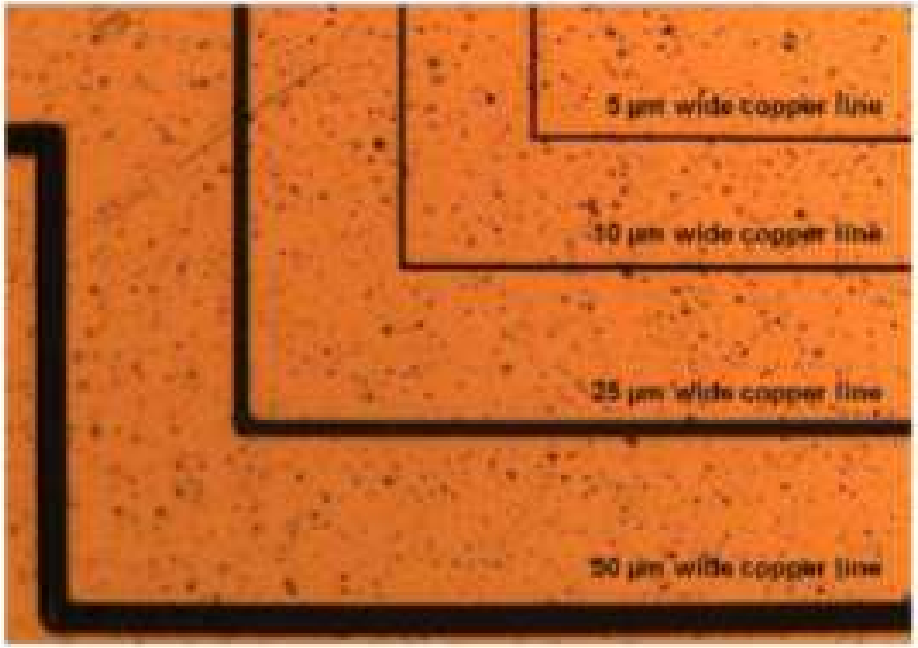
E-less Copper on Pattern

STEP 6.

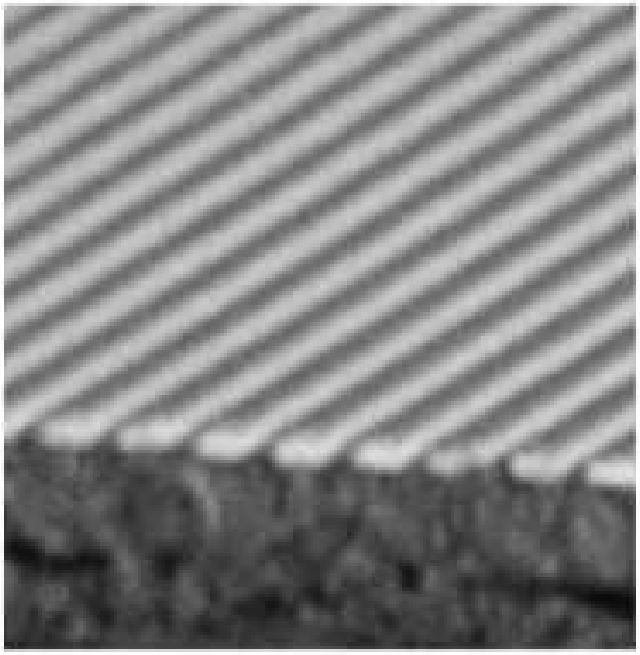
E-lytic Copper on Pattern

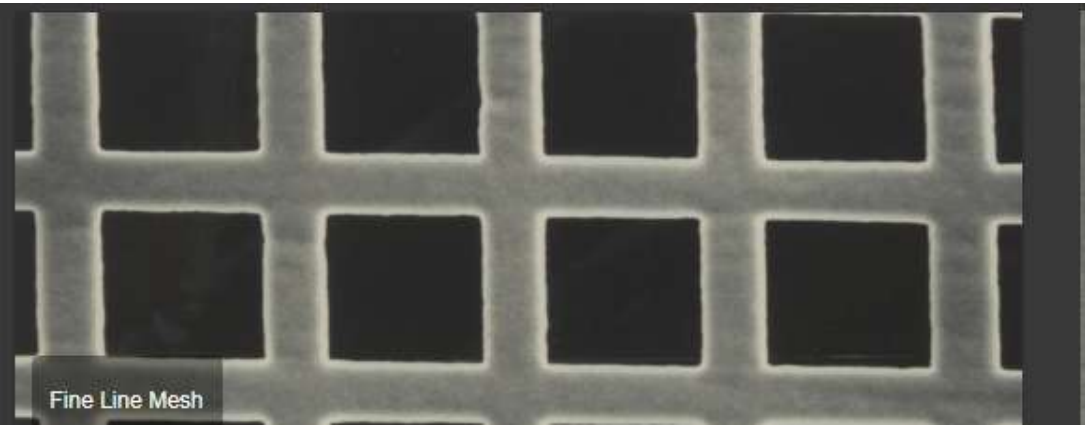


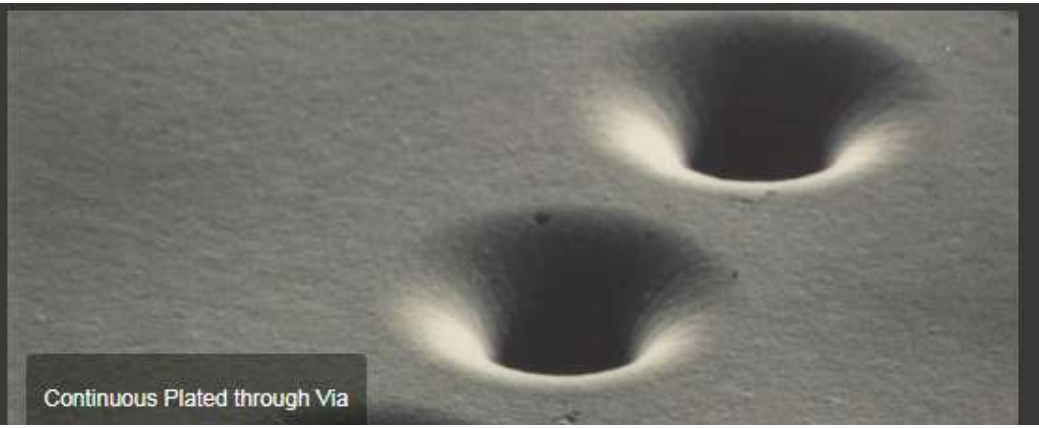
Fine LIne Samples On Polymide



SEM Image of 10 µm lines/ spaces





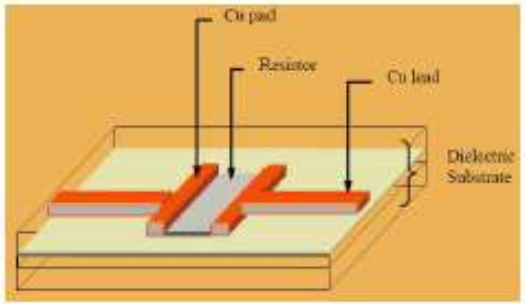


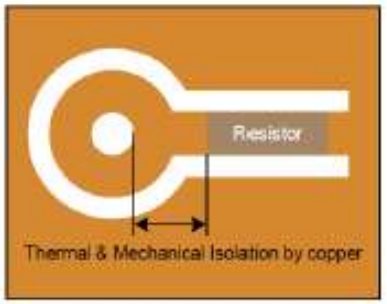
Thin cores

FRONT END

Buried Resistors: TICER & APR Resistors

laser direct imaging system can align with 0.06 mm (0.0025")



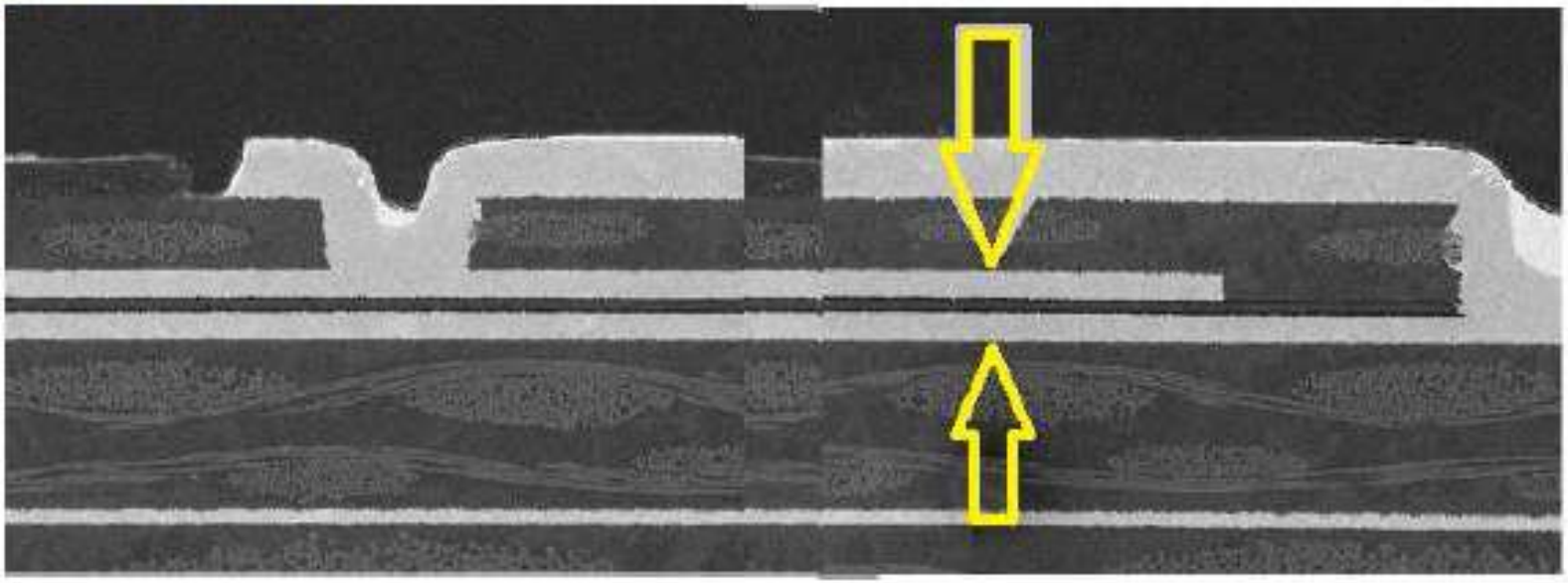


Ticer Technologies TCR® Foil Properties

Resistive Alloy	NiCr	NiCrAlSi
Sheet Resistance (Ohms/sq.)	25, 50, 100	25, 50, 100, 250
Material Tolerance (%)	+/- 5	+/- 5
Base Copper Foil thickness (um)	18, 35	18, 35
Recommended Etch Solution 1st Etch 2nd Etch 3rd Etch	 Cupric Chloride Ammoniacal N/A	 Ammoniacal* Acidic Permanganate Ammoniacal* *Cupric Chloride alternatively
Resistor Tolerances (%) Feature size 10 mil or greater	 +/- 10	 +/- 10

FRONT END

Buried Capacitors -



FARADFLEX
BC12

OAK-MITSUI

Fiberglass Comparison

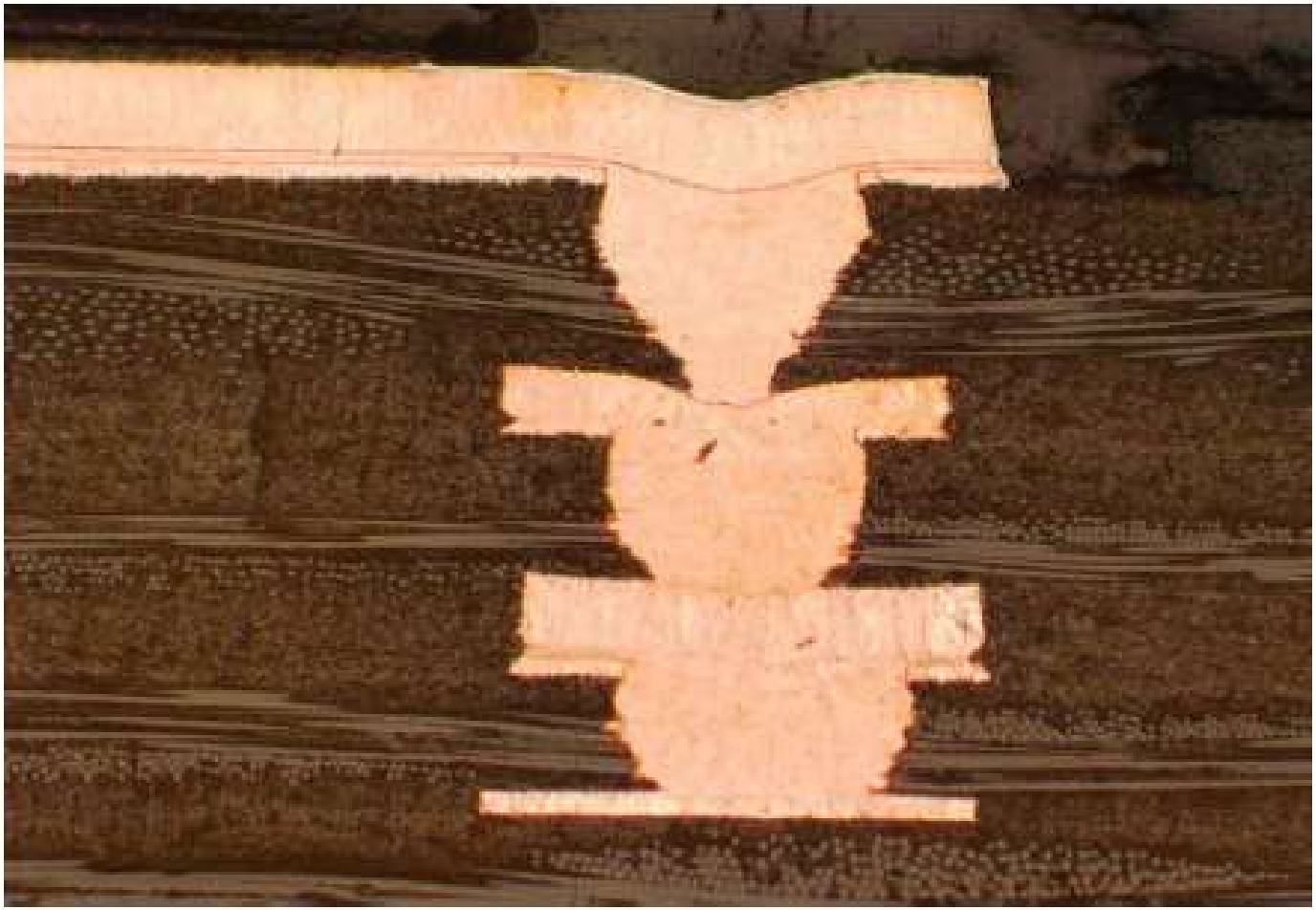
	E-glass	SI-glass	SI2-glass	SI-Q
Supplier / Grade Name	Grace Baotek Nittobo	NE-glass TD-glass	NER-glass L2-glass	TBA
Dielectric Constant, Dk (10GHz)	6.6	4.7	4.3	3.7
Dissipation Factor, Df (10GHz)	0.0060	0.0026	0.0018	0.0002
CTE (ppm/°C)	5.6	3.3	3.3	0.5-0.6
Density (g/cm^3)	2.6	2.3	2.3	2.2
Tensile Strength (GPa)	3.2	3.1	2.4	
Tensile Modulus (GPa)	75	64	53	74

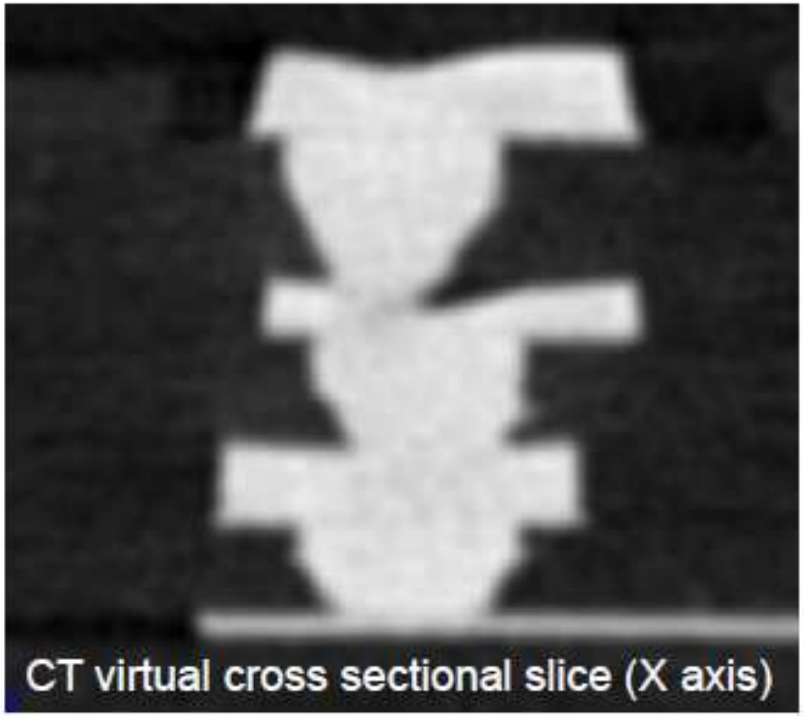
Ultra Thin Laminate & Prepreg

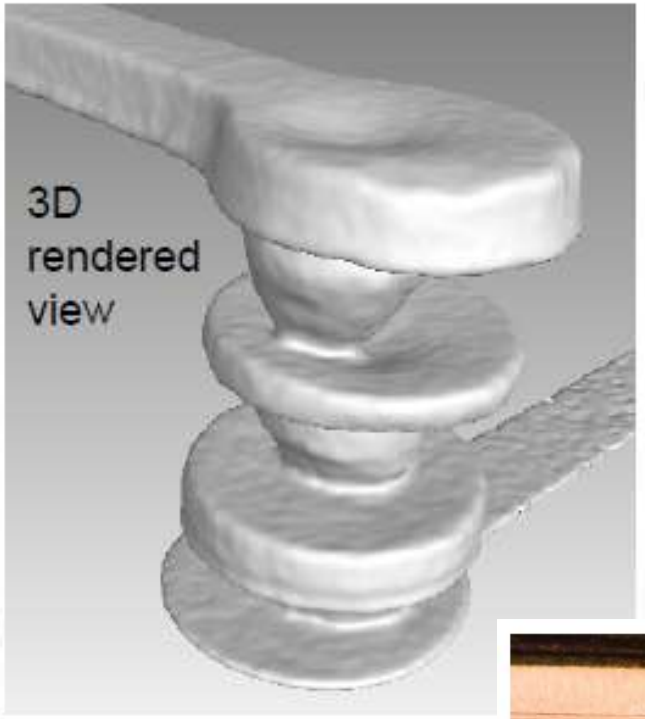
AGC
Your Dreams, Our Challenge

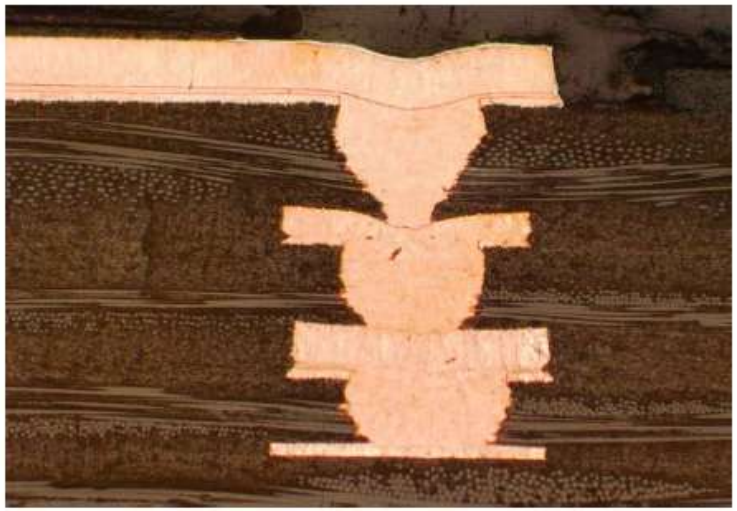
Thickness	Glass style	Status
40μm/1.6mil	1027	• Ready for mass production • Under Testing by customers
30μm/1.2mil	1027	• Ready for mass production • Under Testing by customers
25μm/1.0mil	1017	• Trial production in AMMS • Sample for testing available from 2025 Q1
20μm/0.8mil	1010	• Trial production in AMMS • Sample for testing available from 2025 Q1
<15μm/<0.6mil	1006	• Under evaluation

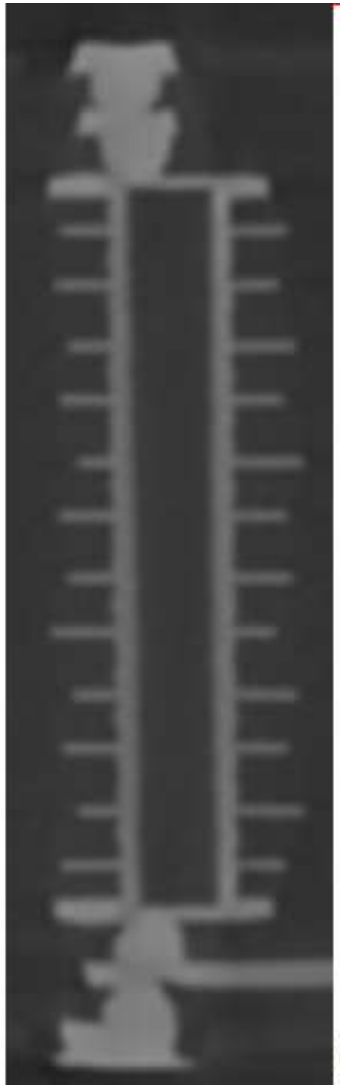
Microvia




CT virtual cross sectional slice (X axis)


3D
rendered
view

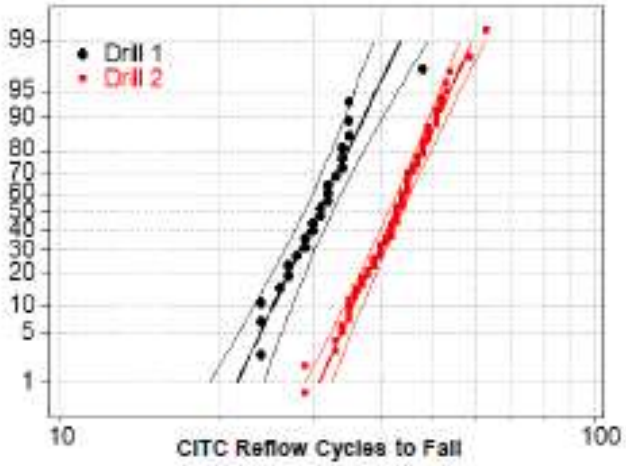




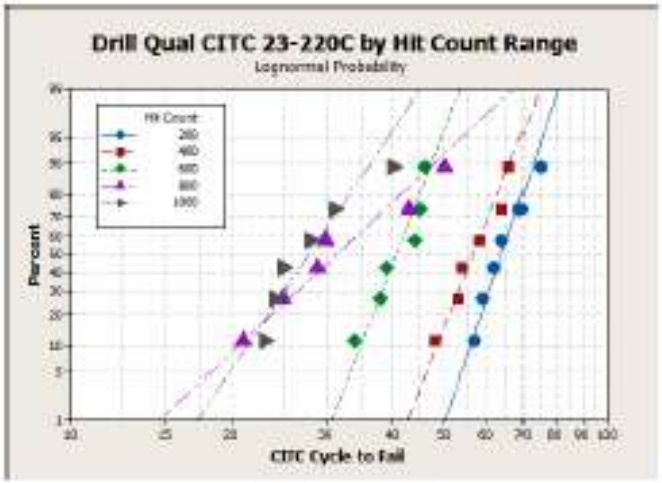
(X axis)

The failure can not be narrowed down to a specific via.

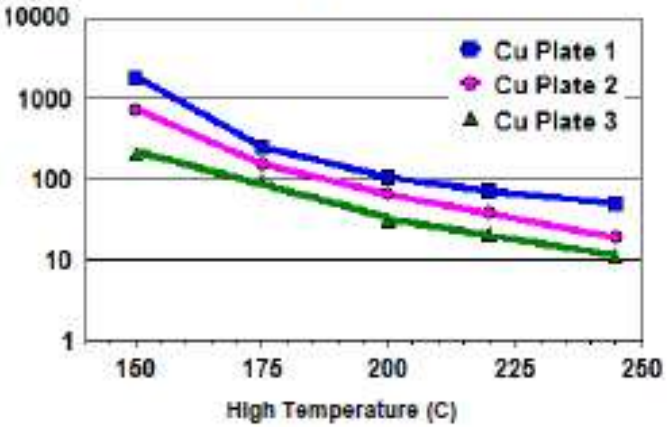
Drill Bit design



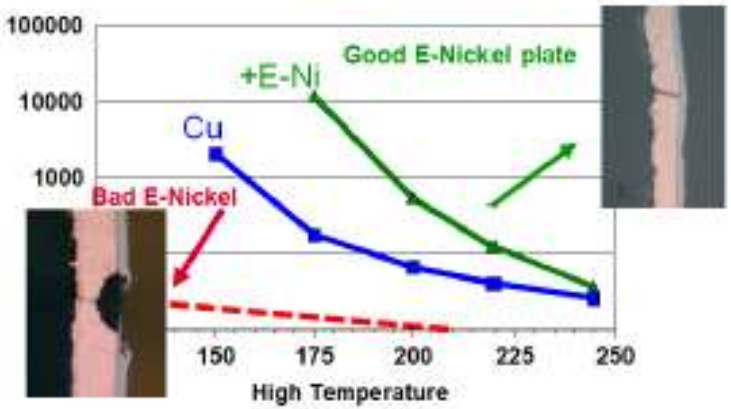
Drill Hit Count



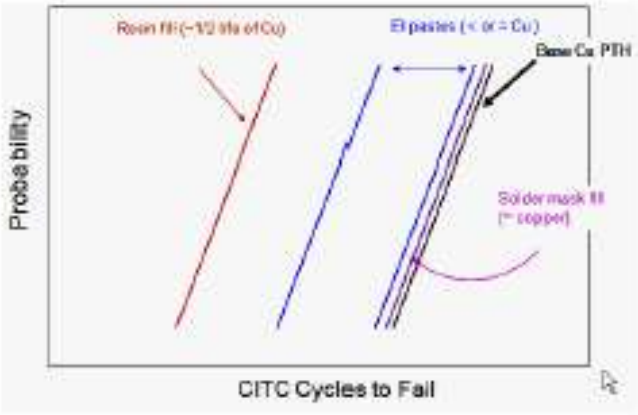
Cu Plate Chemistry



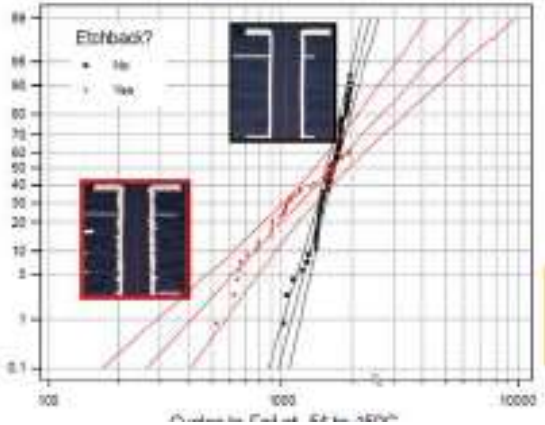
Nickel/Au Plate



Hole Fill



Etchback



Effect of Test Temperature

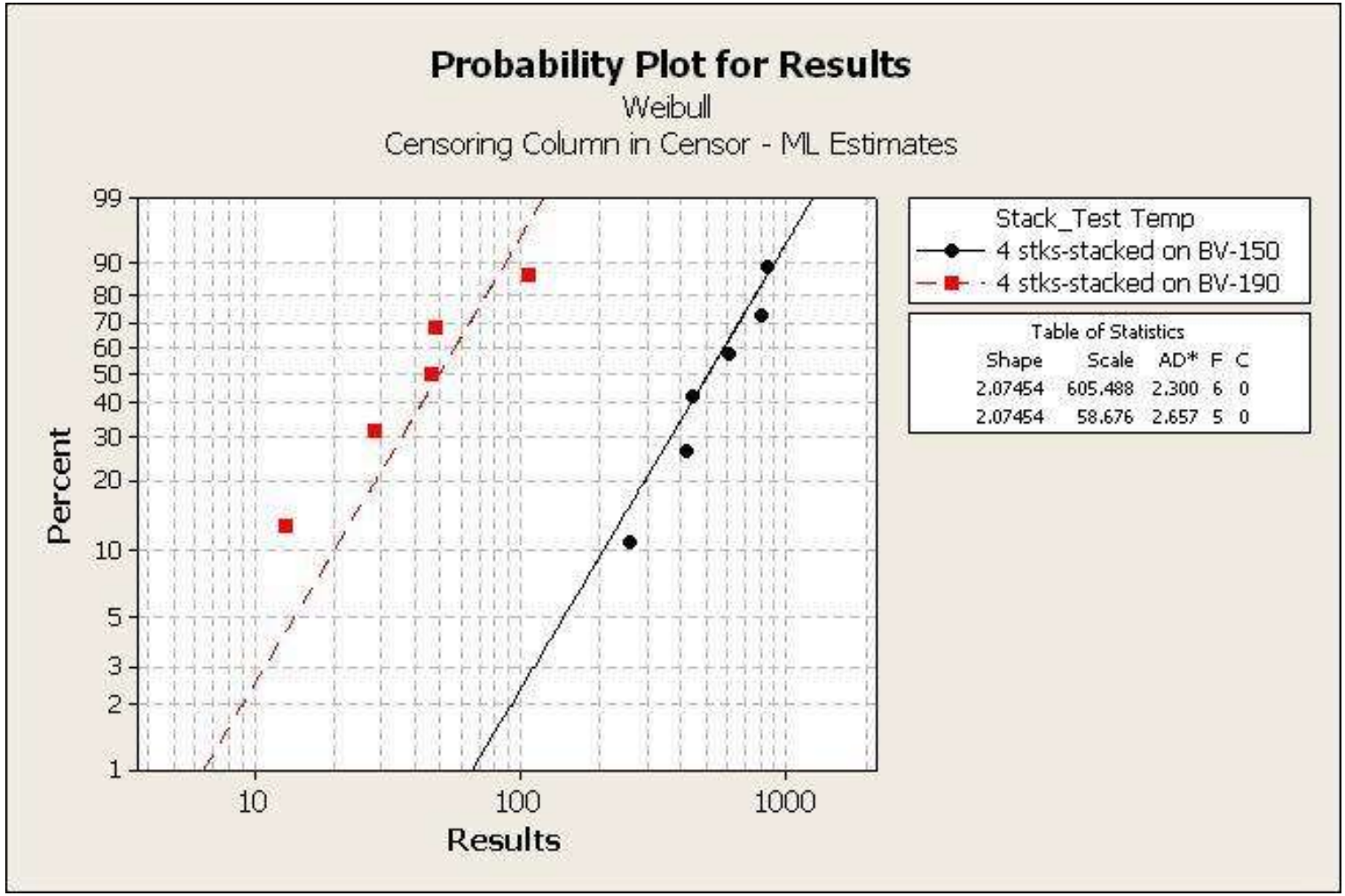


Chart / Data Courtesy PWB Interconnect

Stacked Micro-Via - Failures

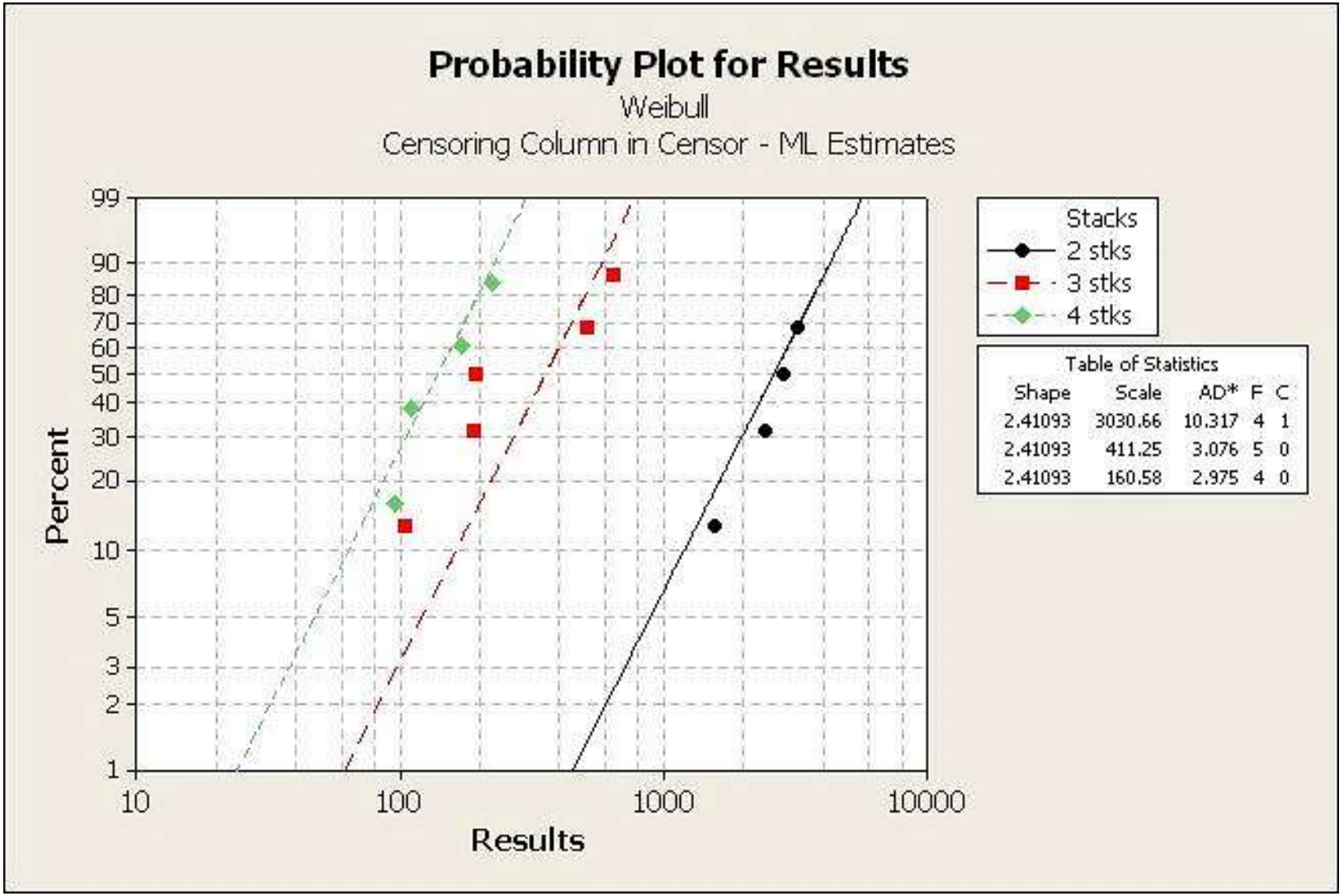


Chart / Data Courtesy PWB Interconnect

Staggered Micro-via Stresses

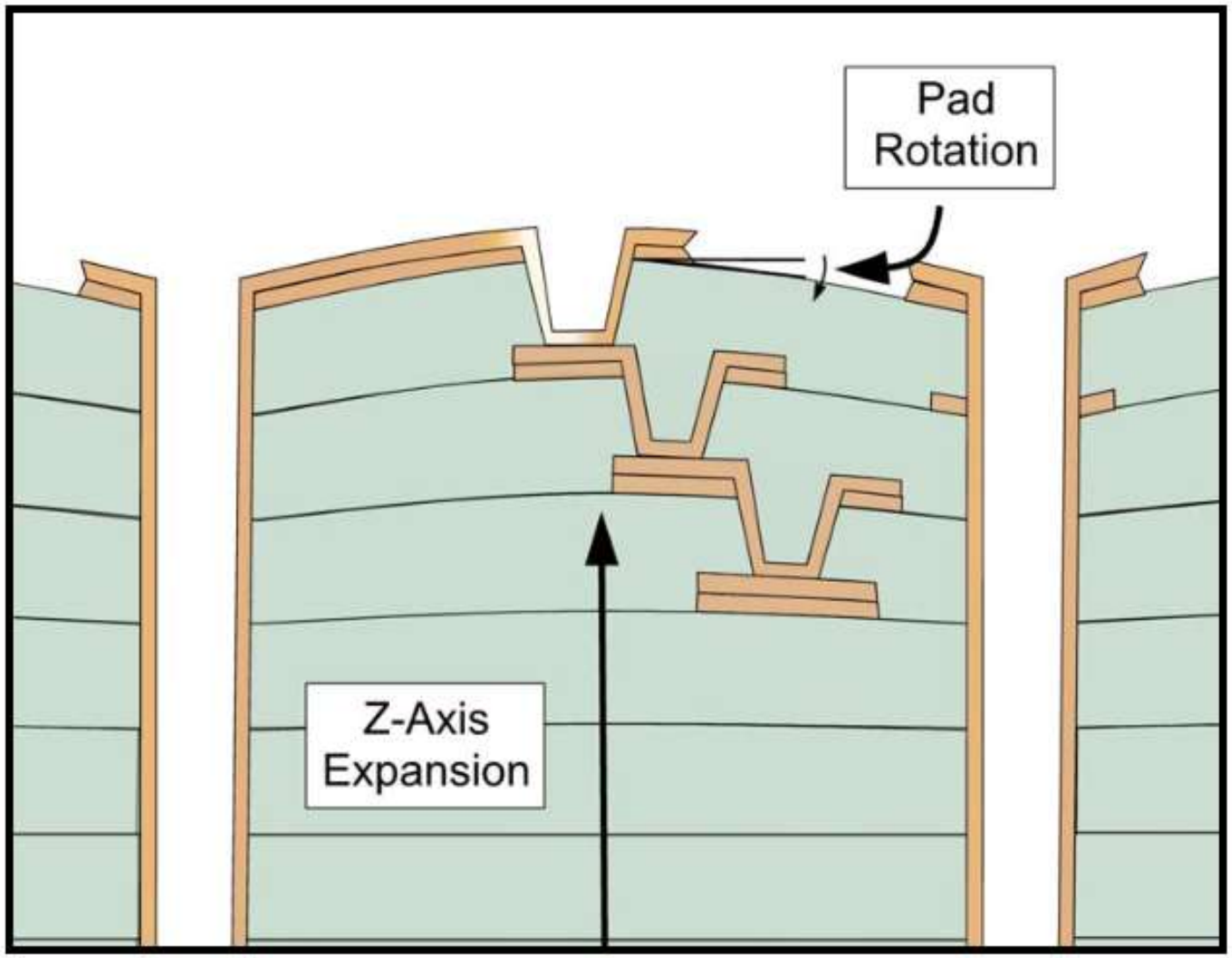


Chart / Data Courtesy PWB Interconnect

Stacked Micro-via Stresses

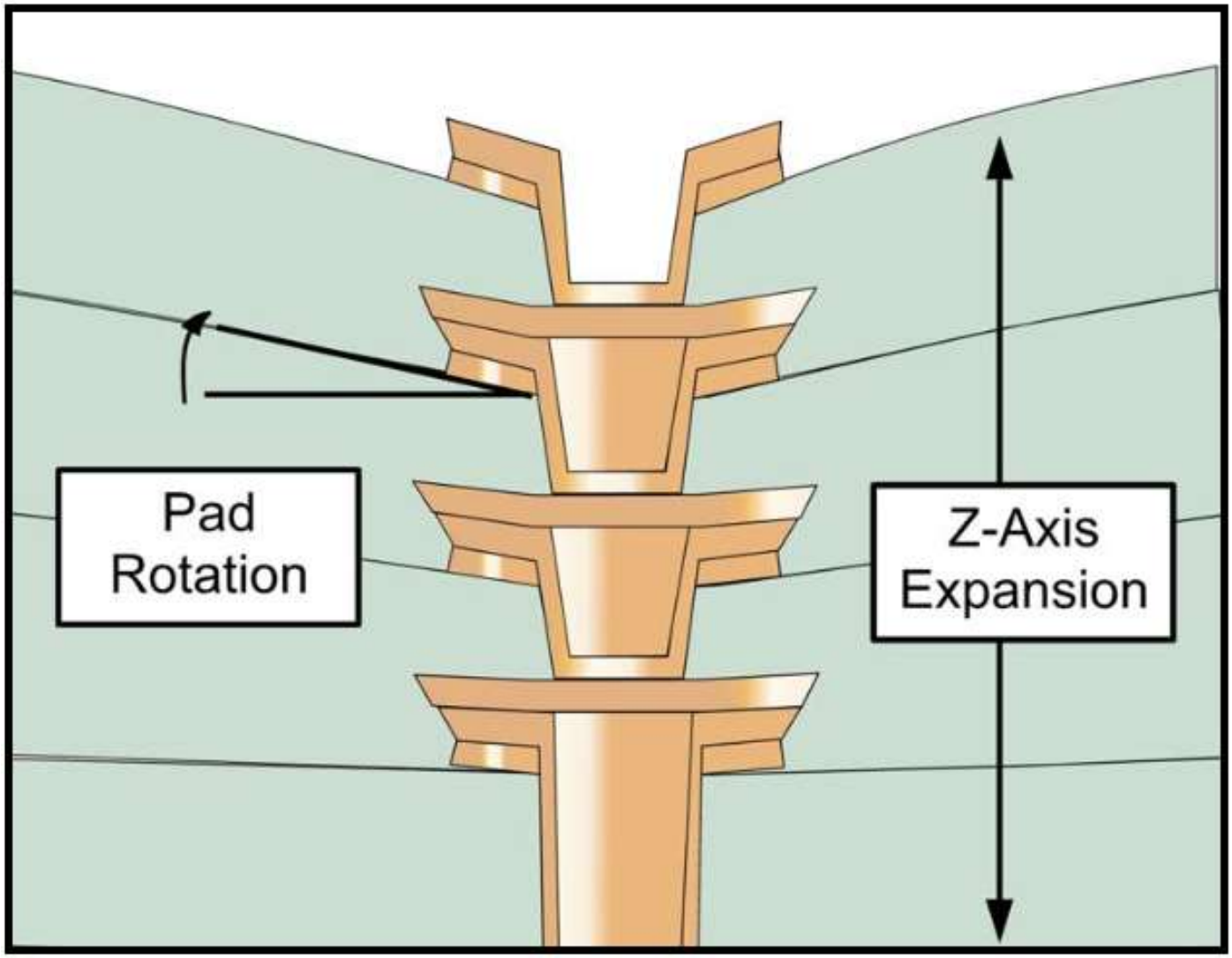
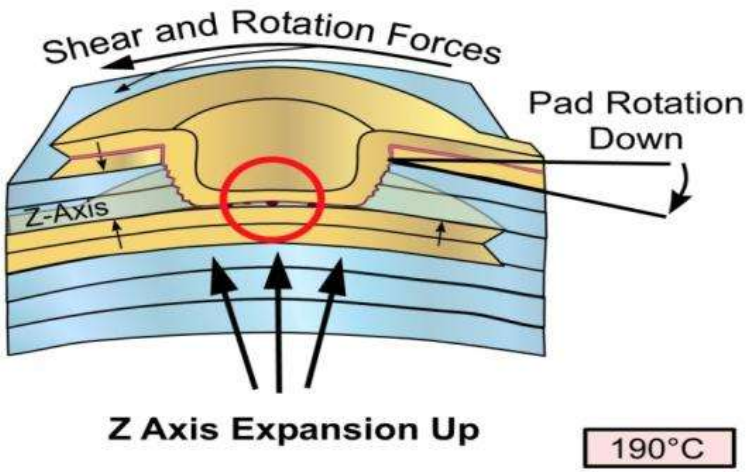
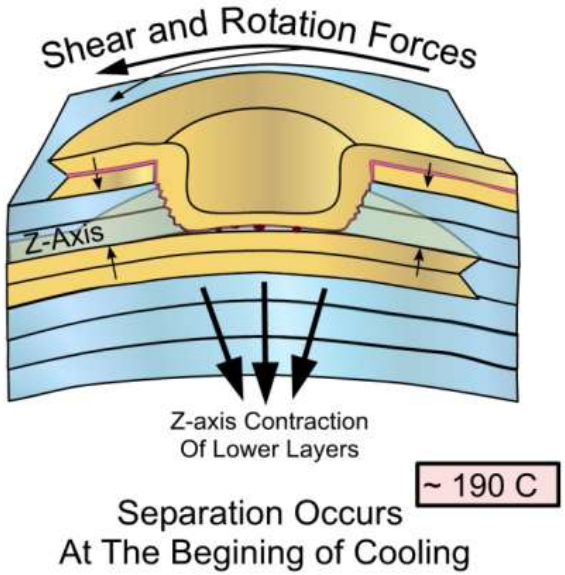
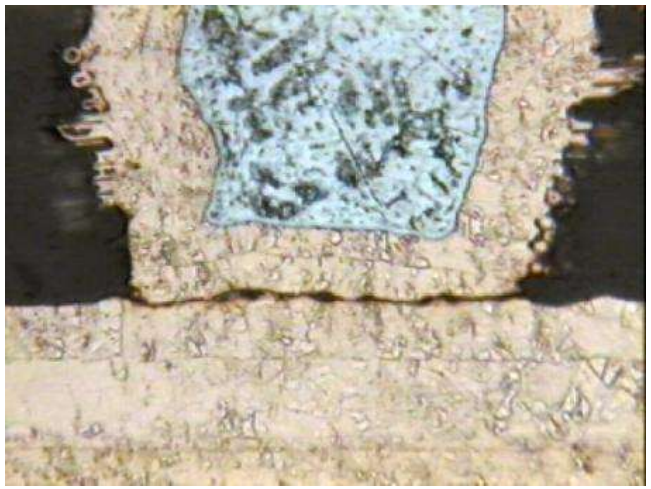


Chart / Data Courtesy PWB Interconnect

Micro Via – Pad Separation







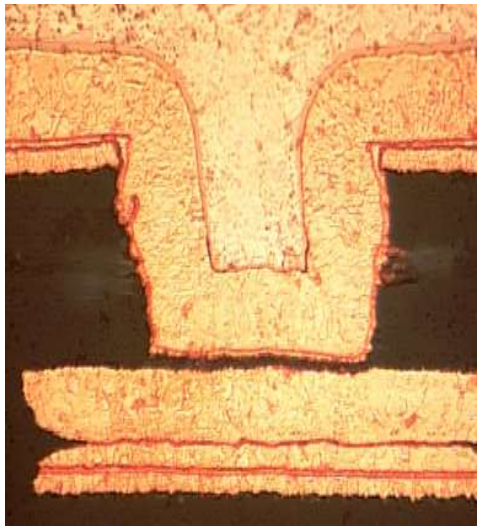
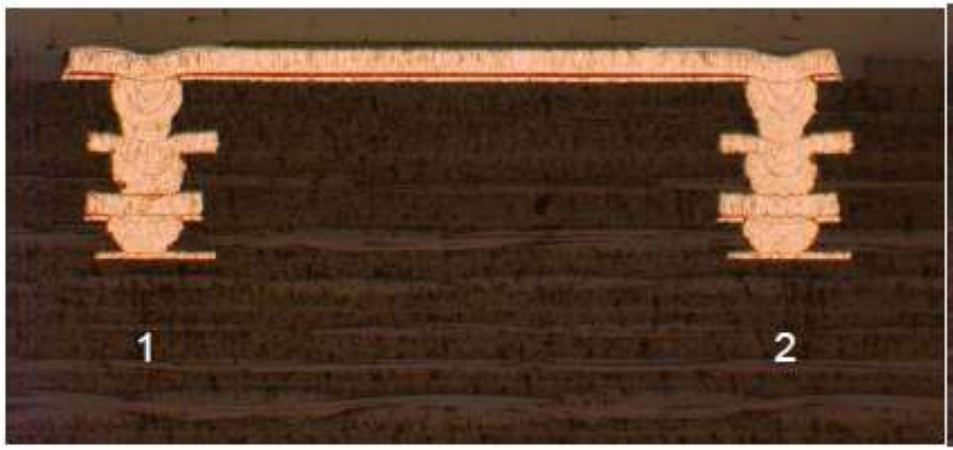
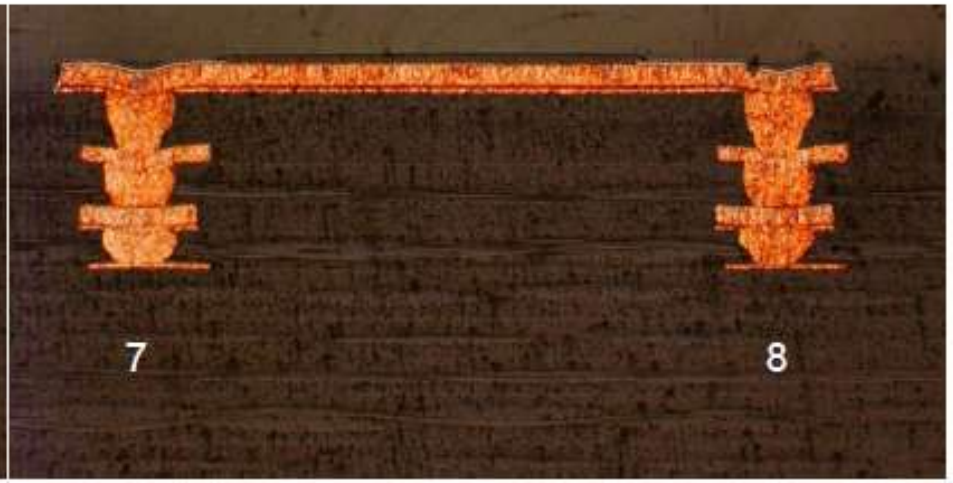


Chart / Data Courtesy PWB Interconnect


1
2

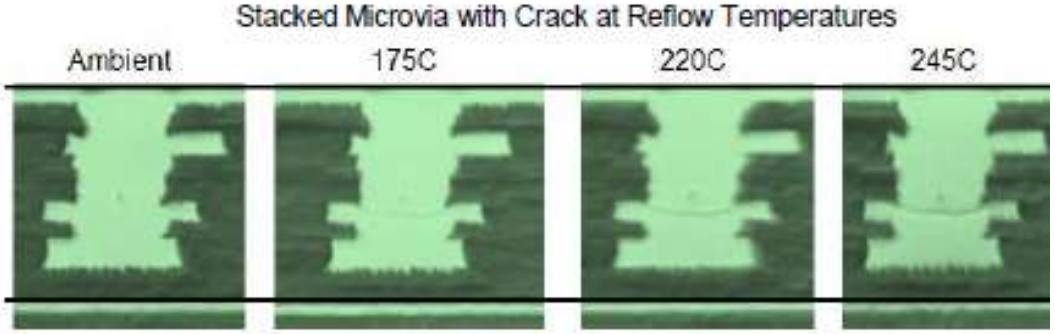

3
4


5
6


7
8

Stacked Microvias and Reflow

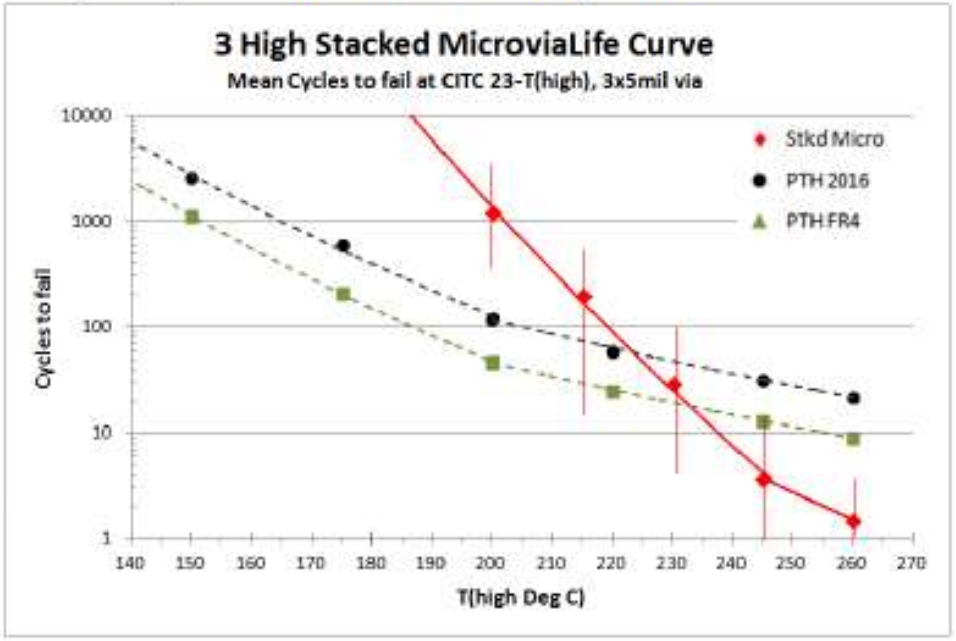
- Even more "Reflow driven" failure than PTH's: Steepest Life Curve!
- Failure rate strongly dependent on reflow temperature.
- Cracks are very fine; brittle like failure at low displacements.



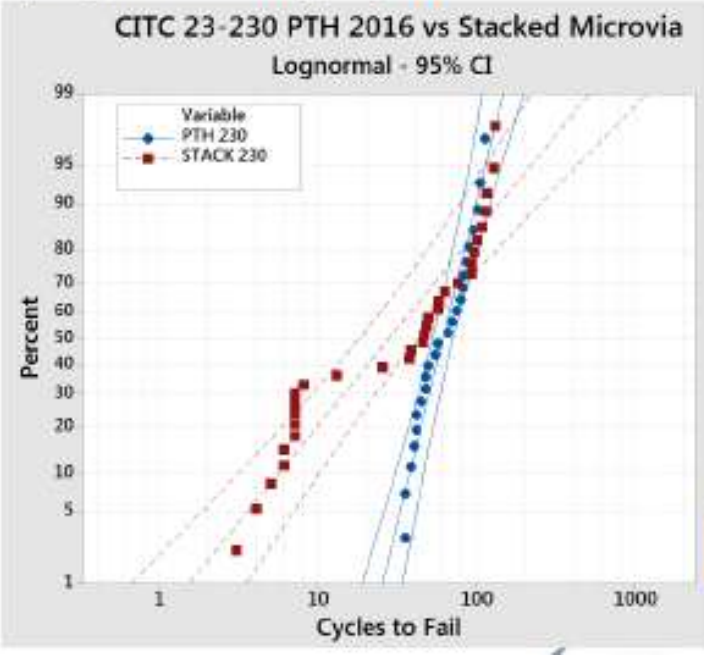
- Critical to test to failure at appropriate reflow temperature with sufficient sample size

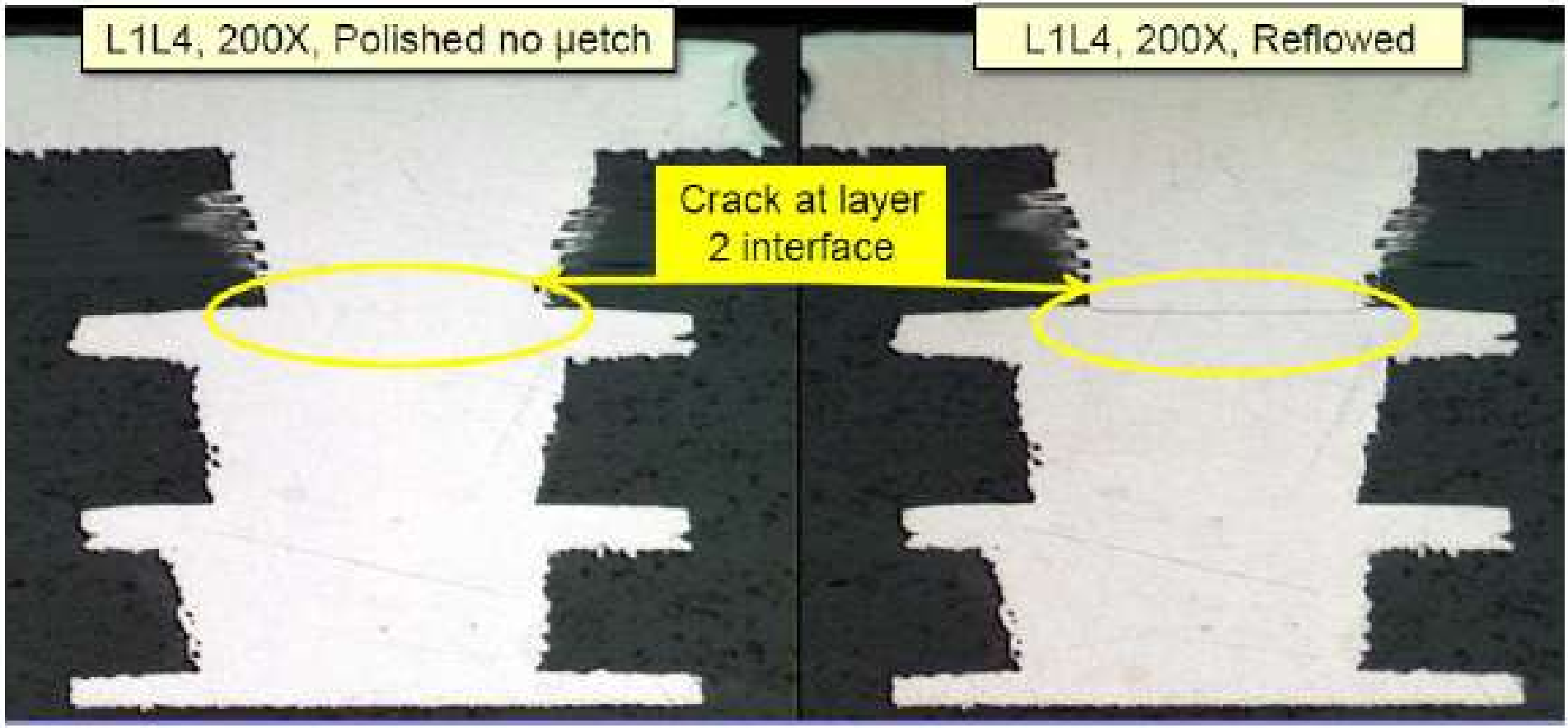
Stacked Microvias:

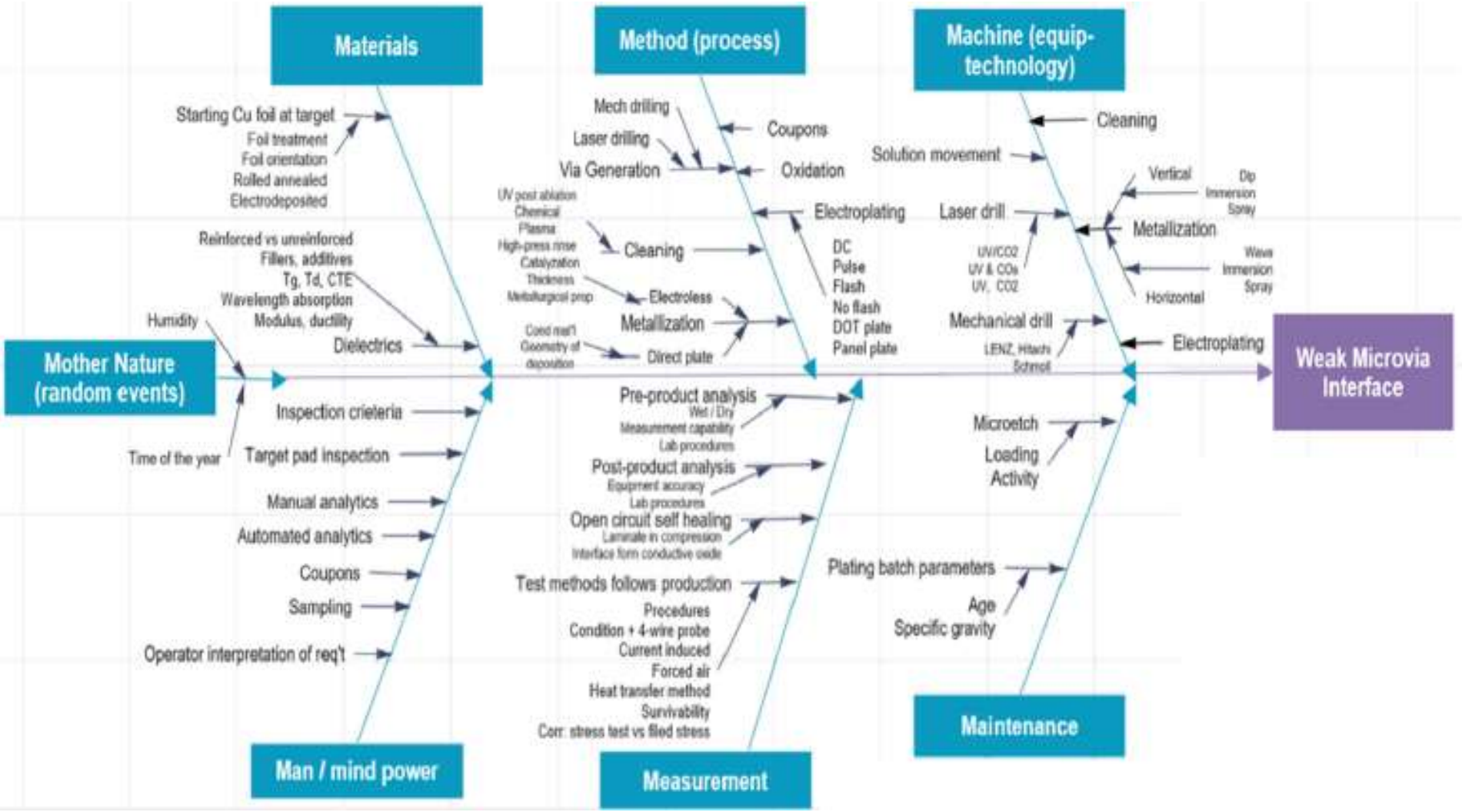
1) Steeper Failure Curve with temperature

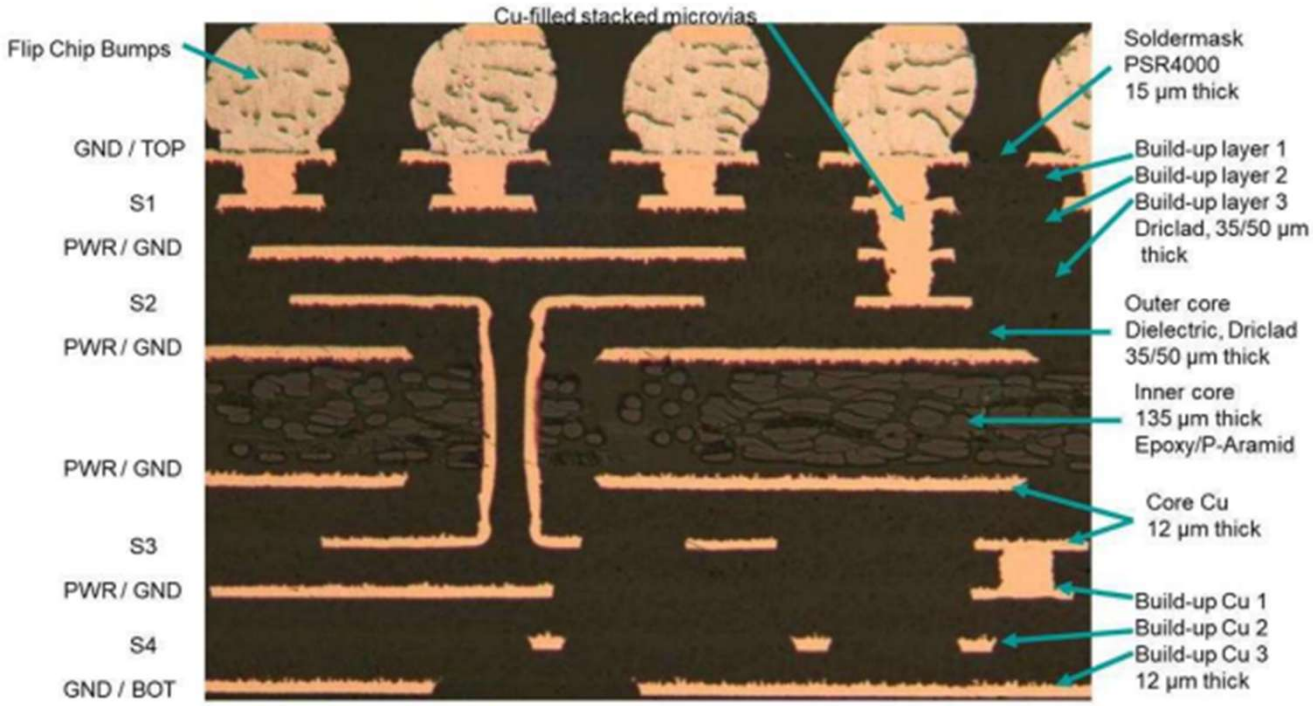


2) Higher variability, "sigma"

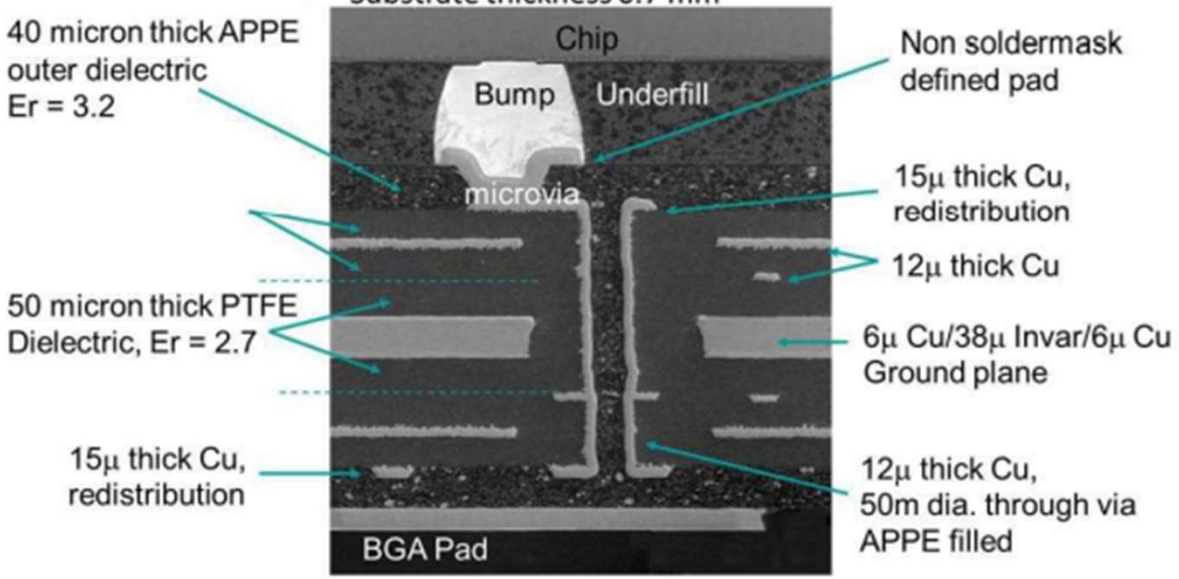


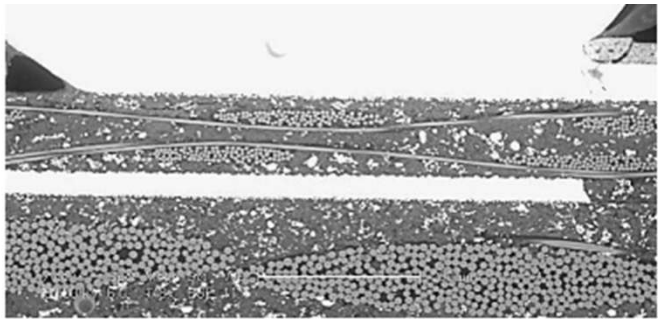

L1L4, 200X, Polished no µetch
L1L4, 200X, Reflowed
Crack at layer
2 interface


Materials
Method (process)
Machine (equip-technology)
Starting Cu foil at target
Foil treatment
Foil orientation
Rolled annealed
Electrodeposited
Reinforced vs unreinforced
Fillers, additives
Tg, Td, CTE
Wavelength absorption
Modulus, ductility
Dielectrics
Humidity
Mother Nature (random events)
Time of the year
Inspection crieteria
Target pad inspection
Manual analytics
Automated analytics
Coupons
Sampling
Operator interpretation of req't
Man / mind power
Mech drilling
Laser drilling
Via Generation
Coupons
Oxidation
UV post ablation
Chemical
Plasma
High-press rinse
Cleaning
Catalyzation
Thickness
Metallurgical prop
Electroless
Metallization
Cond met'l
Geometry of deposition
Direct plate
Electroplating
DC
Pulse
Flash
No flash
DOT plate
Panel plate
Pre-product analysis
Wet / Dry
Measurement capability
Lab procedures
Post-product analysis
Equipment accuracy
Lab procedures
Open circuit self healing
Laminate in compression
Interface form conductive oxide
Test methods follows production
Procedures
Condition + 4-wire probe
Current induced
Forced air
Heat transfer method
Survivability
Corr: stress test vs filed stress
Measurement
Cleaning
Solution movement
Laser drill
UV/CO2
UV & CO2
UV, CO2
Vertical
Dip
Immersion
Spray
Metallization
Wave
Immersion
Spray
Horizontal
Mechanical drill
LENZ, Hitachi
Schmoll
Electroplating
Microetch
Loading
Activity
Plating batch parameters
Age
Specific gravity
Maintenance
Weak Microvia Interface

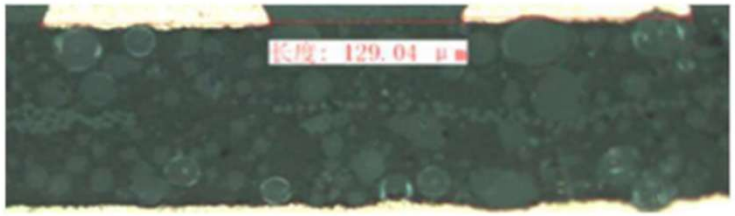


- 3-4-3 Stack up (10 copper layers)
- Substrate thickness 0.7 mm

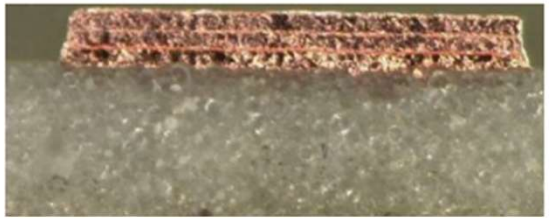




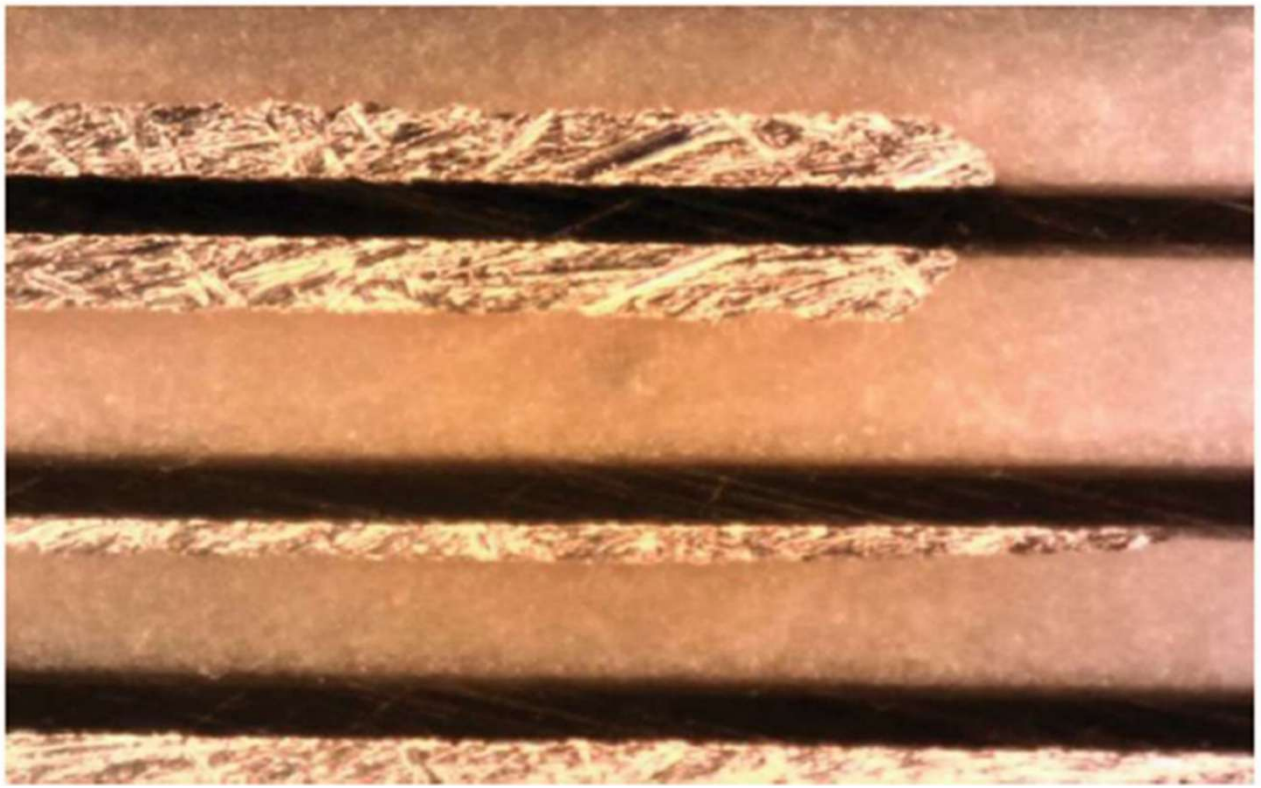
FR4 type woven
fiberglass
reinforced



Taconic
TSMDS3b
≈ 6% reinforced



Taconic
NF30



*fast*Rise™ EZ pure

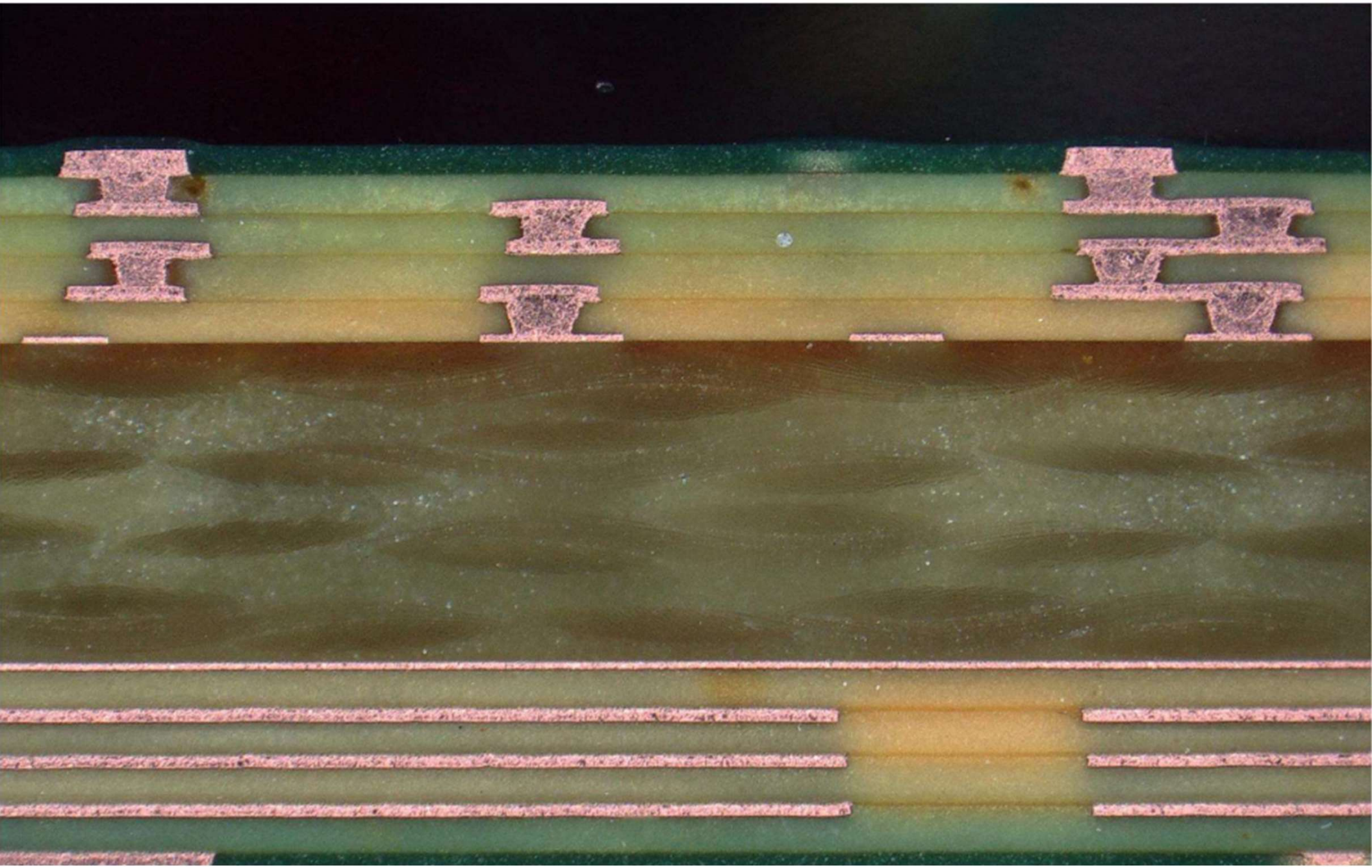
Pyralux® AP

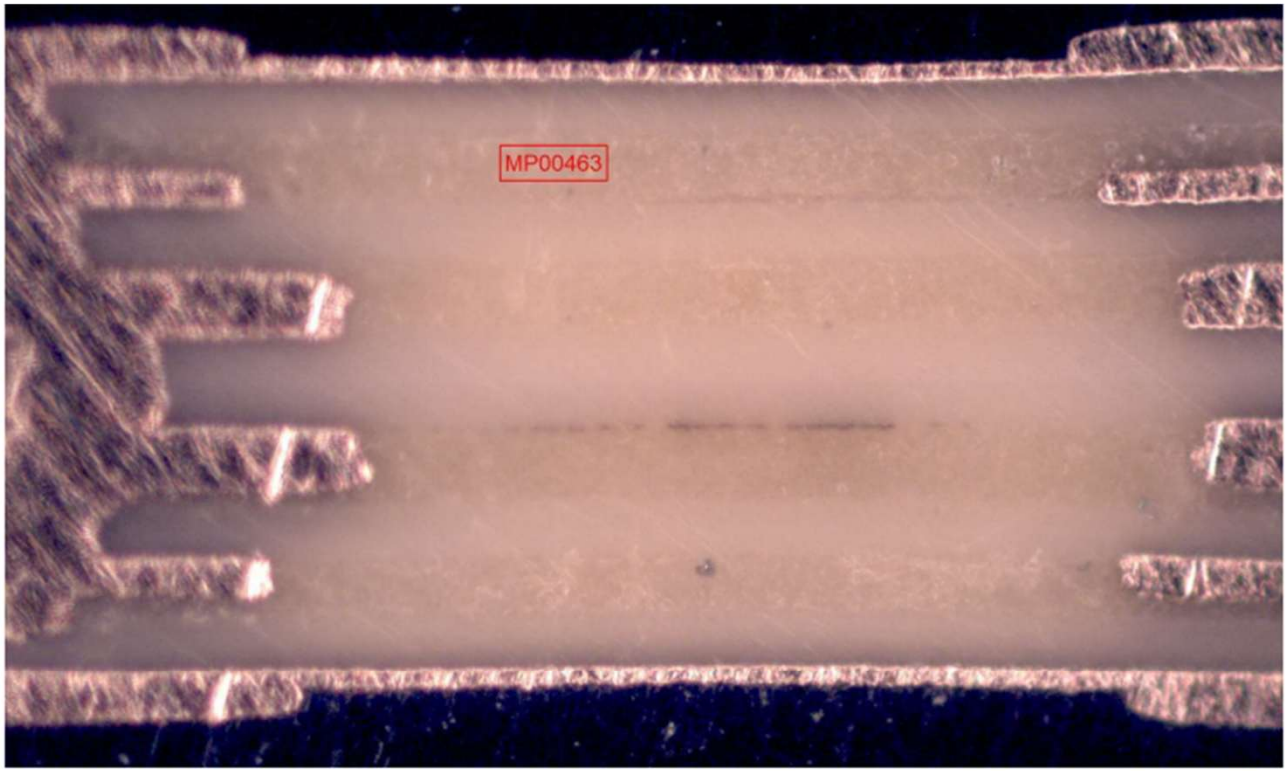
*fast*Rise™ EZ pure

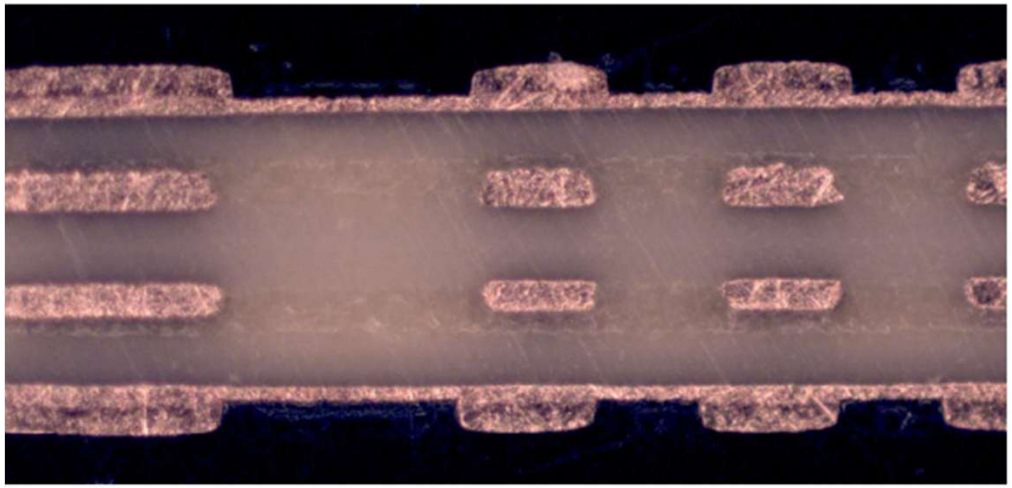
Pyralux® AP

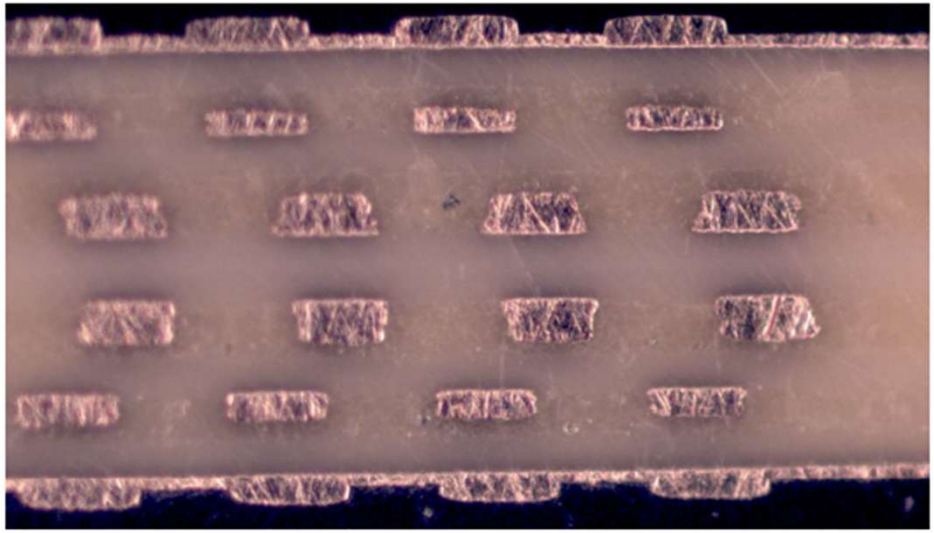
*fast*Rise™ EZ pure

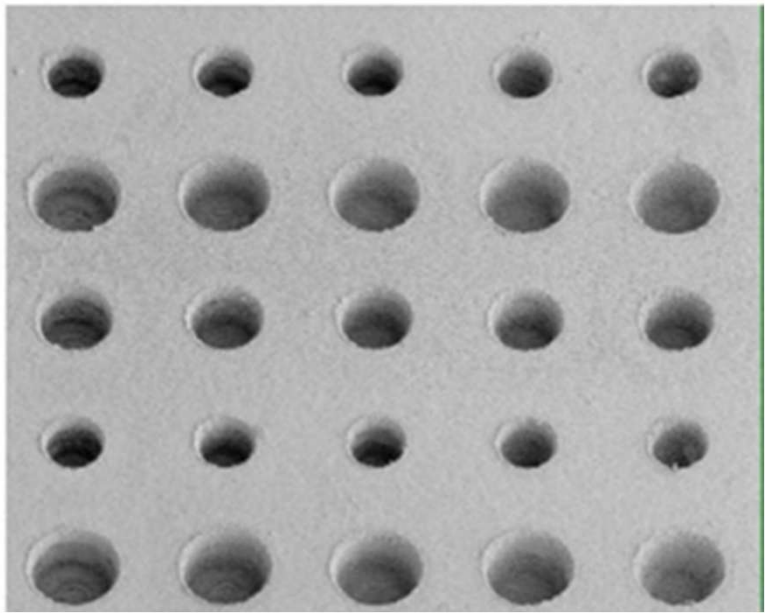
Pyralux® AP

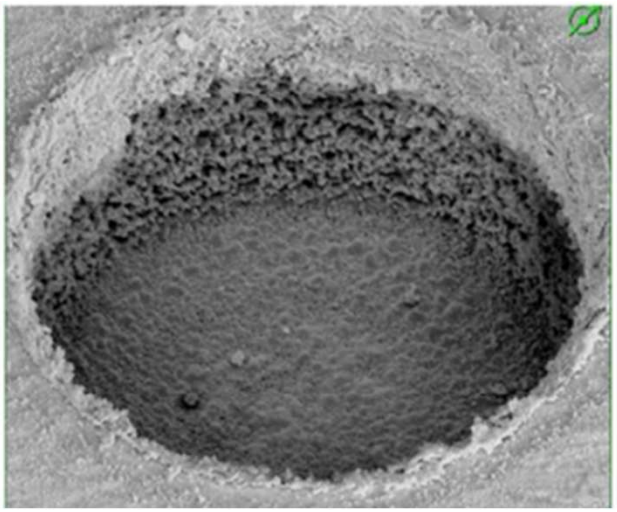


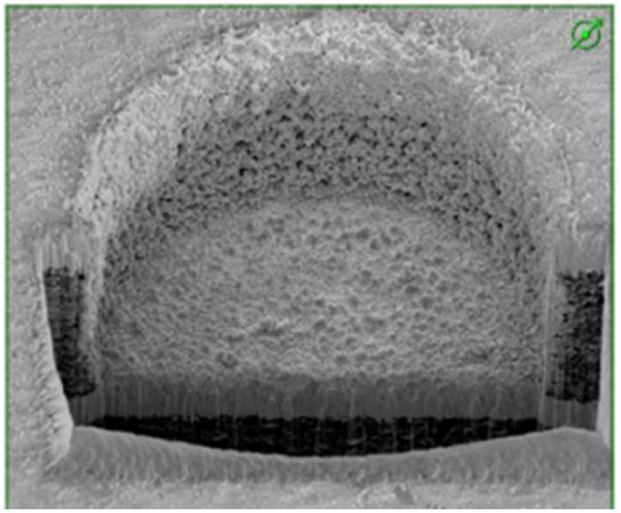

MP00463

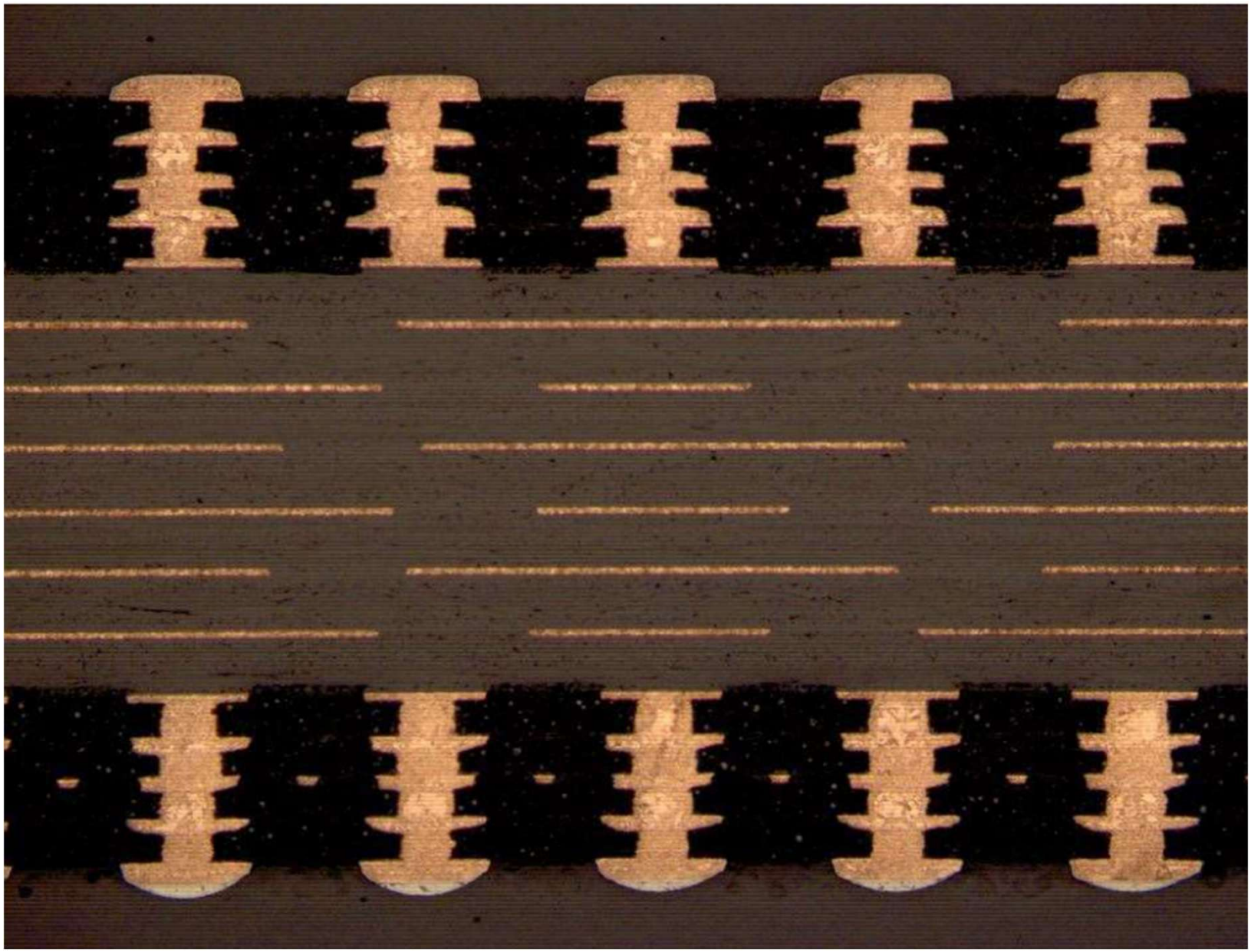


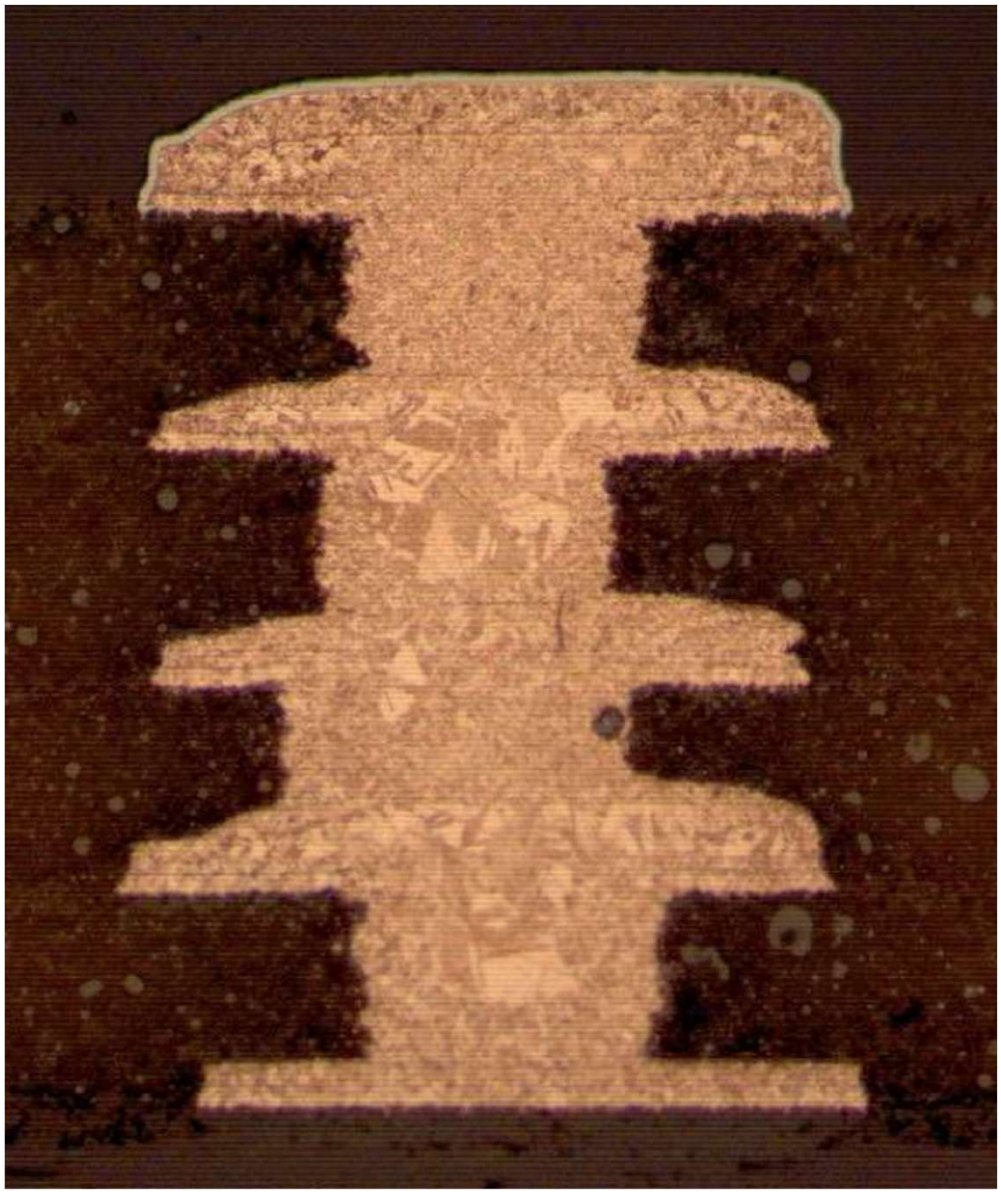










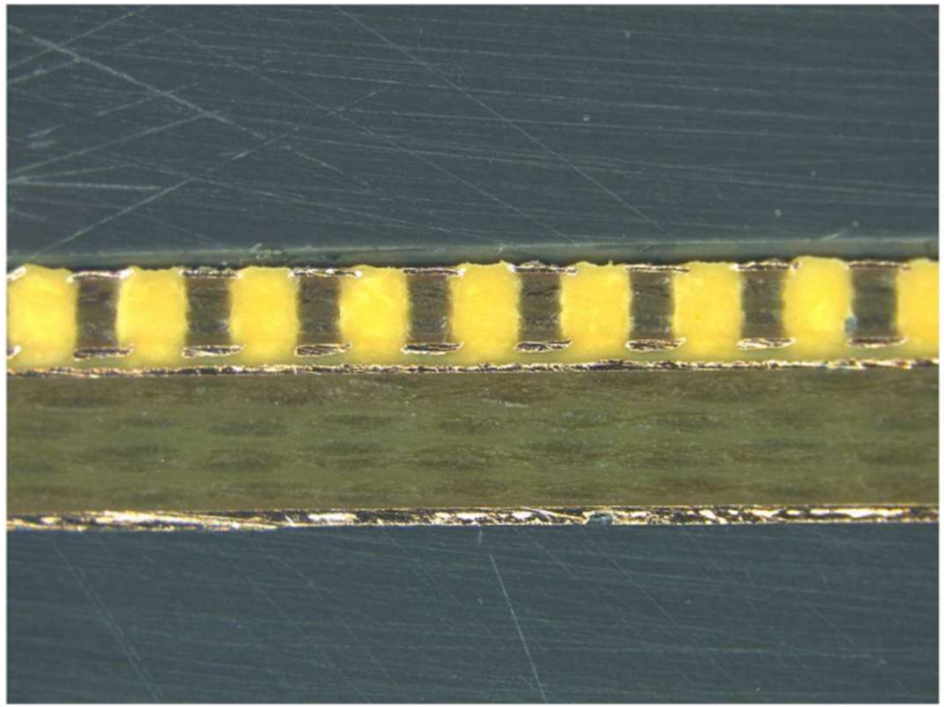


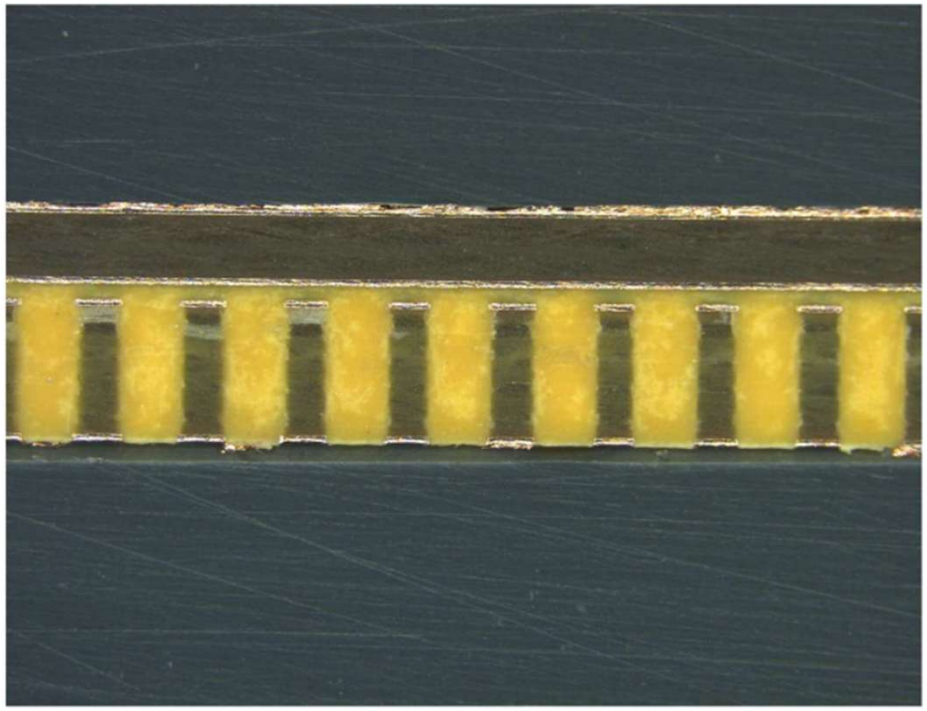
24 Panels Passed 24 cycles 35 to 235C
24 Panels Passed 24 cycles 35 to 260C

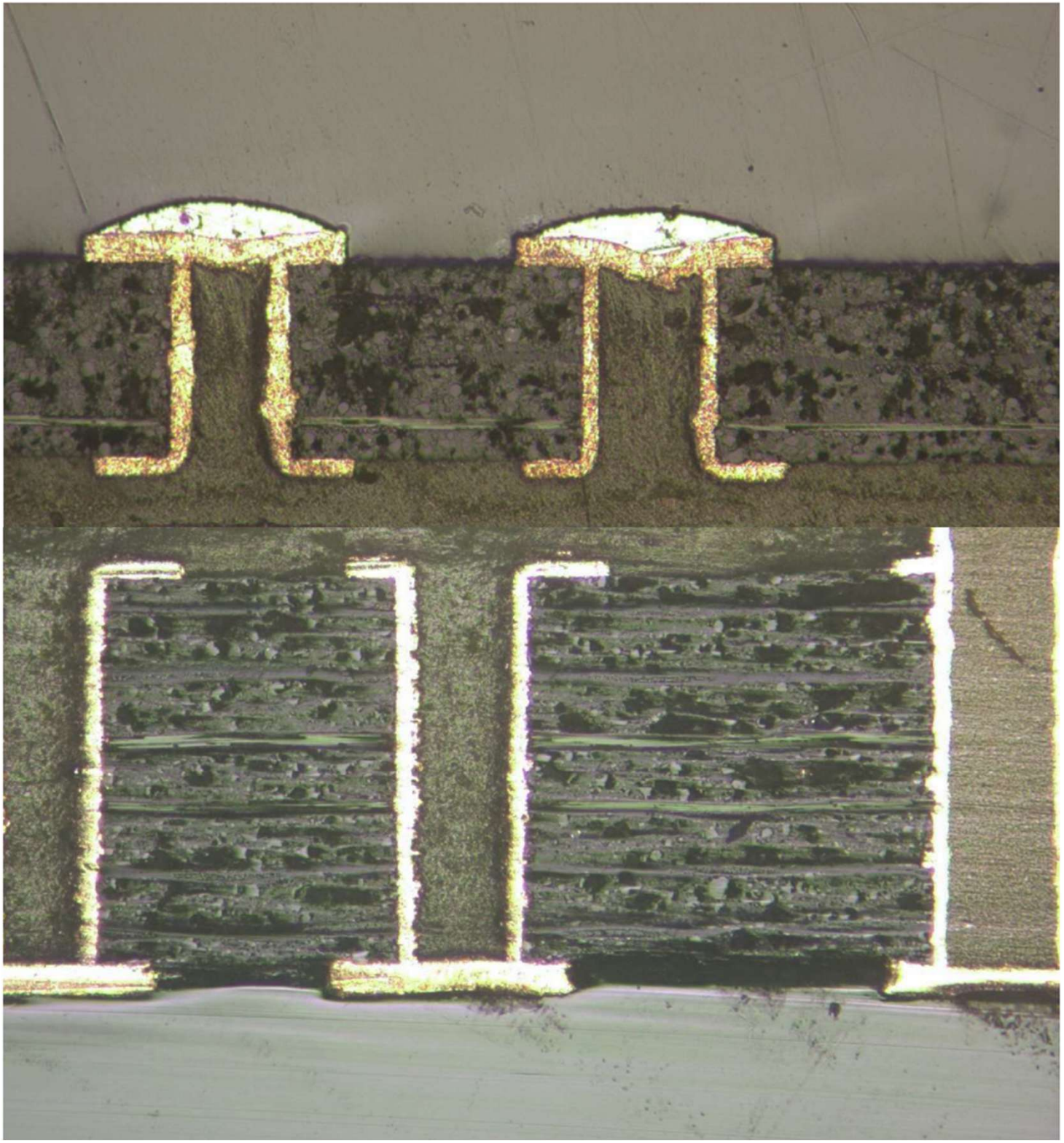
Took panels from sample lot exposed at 260C
Solder floated 8 of these at 270C
Solder floated 8 of these at 280C
Solderfloated 8 of these at 288C.
Retest 24 cycles, 35 to 260C

100% pass
24 panels passed 48 cycles 35 to 260C after exposure to 270, 280, and 288C
Panels tested by Kevin Knadle, **200** cycles RT to 260 had no failures

Property	*fast* Rise TC	Next Generation *fast* Rise TC
DK	4.8	3.5
Df	0.0023	0.0015 - 0.0020
CTE (X, Y, Z)	22	
Thermal Conductivity	0.94	
V - 0 Flammability	no	yes
Target Markets	Rigid/flex, conformable antenna, rigid mil/aero, via fill, heavy copper fill	High reliability, Mil/Aerospace, Telecom, Rigid PWBS







Thermal

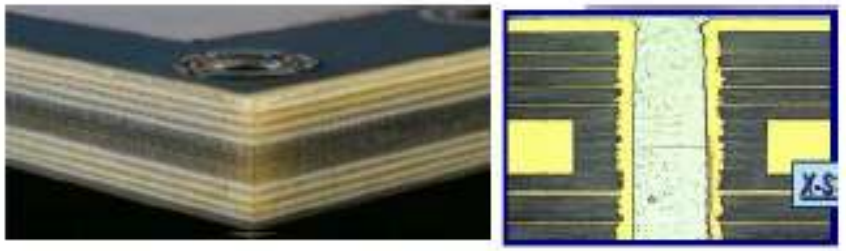
Thermal Relief

External Heat Sink

Aluminum

Copper

Internal Heat Sink



Carbon

Copper Invar Copper (C.I.C)

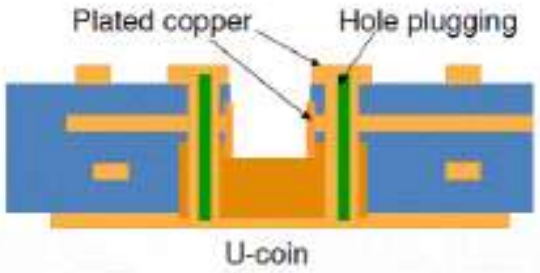
Copper

Thermal Relief

COIN Technology

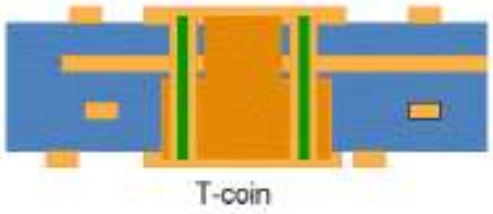
U-Coin

There will be cavity in each of the coin. The high power component can be placed into the cavity for heat dissipation. The grounding of coin can be done by plating of ground vias or cavity.



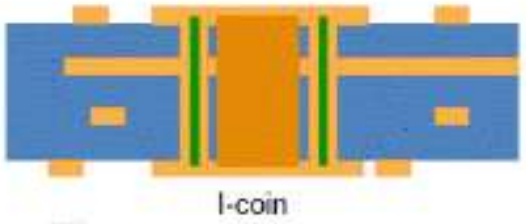
T-Coin

The coin embedded is T-shape.
There are plated ground via holes drilled through the ground plane and coin for ground connection.
The flat surface makes it better for surface mount components thermal dissipation.



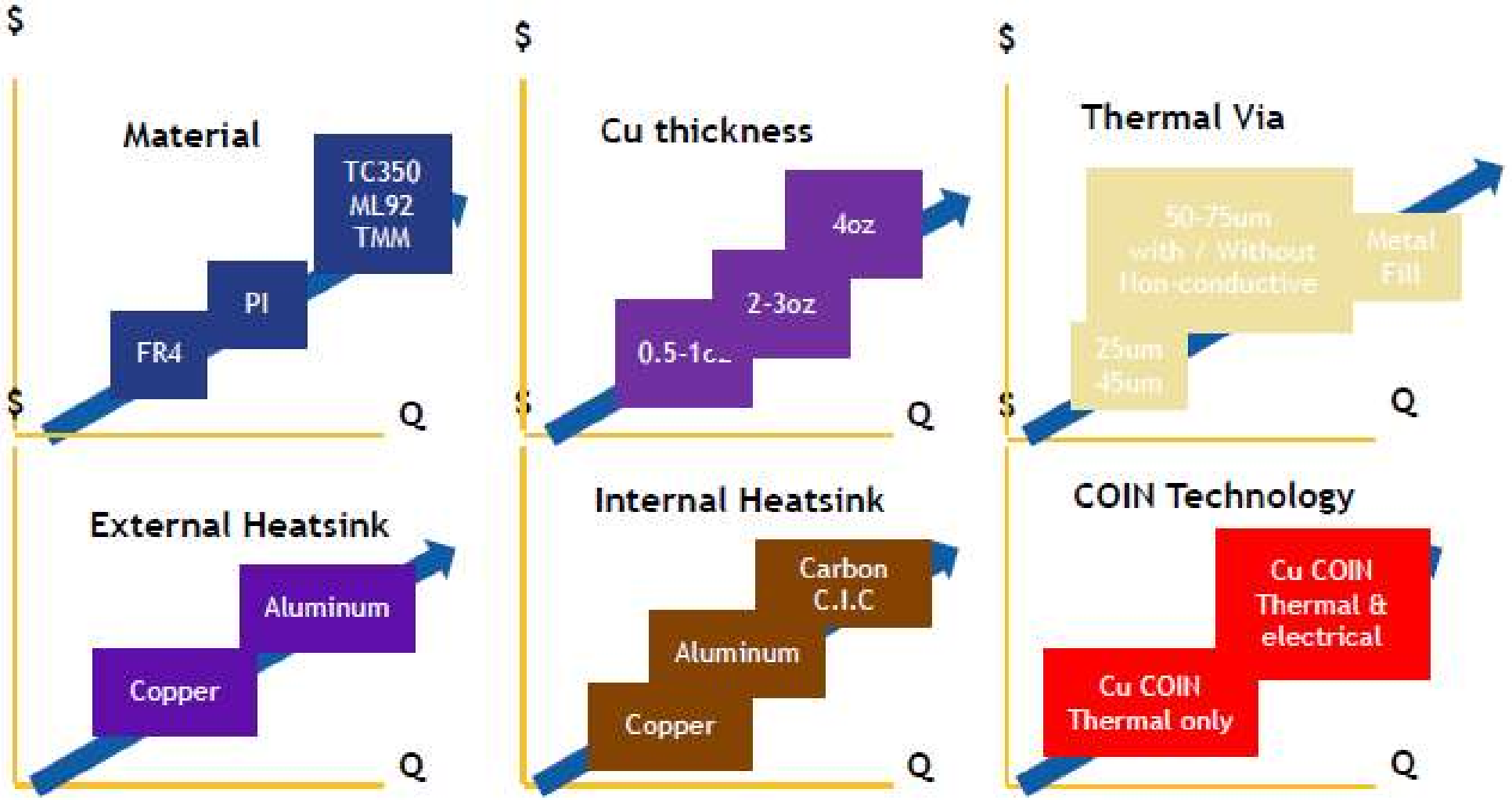
I-Coin

The shape of the coin is simply square. The ground via connected to the ground layer does not contact to the coin directly.

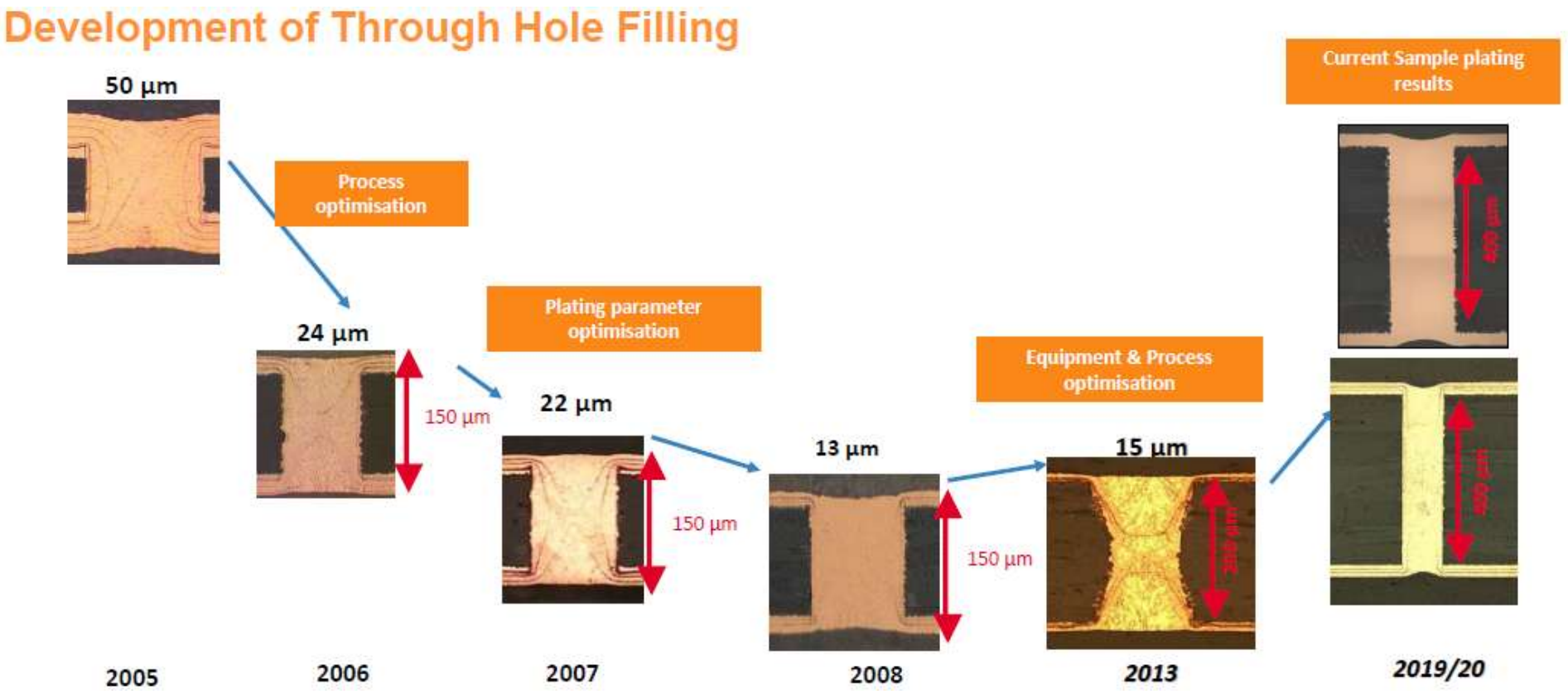


Thermal Relief

Thermal Relief



Thermal Relief



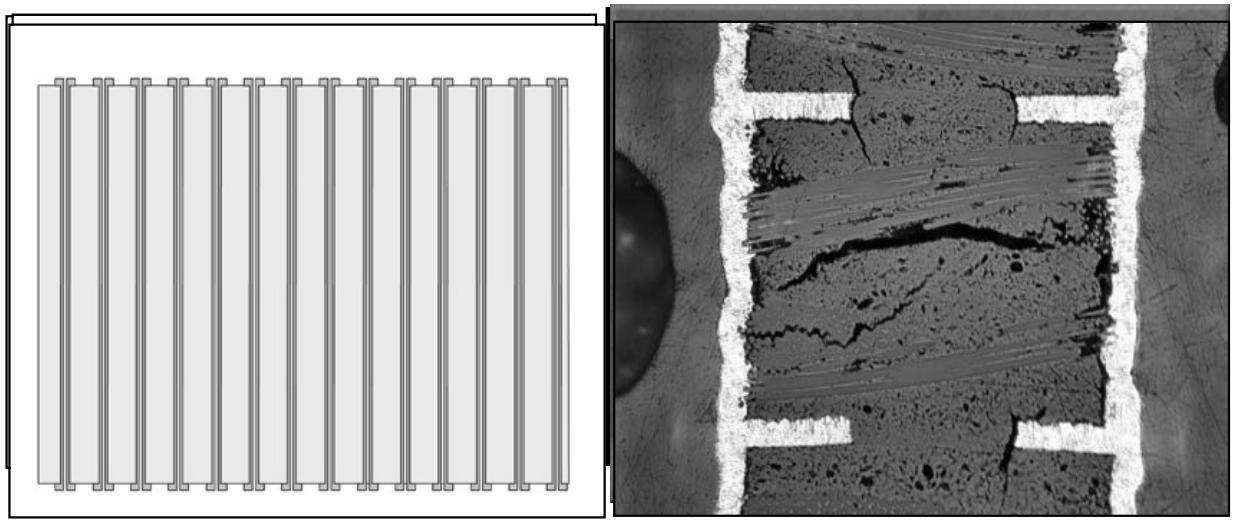
Grid size

The influence of grid size is based on failure of the laminate.

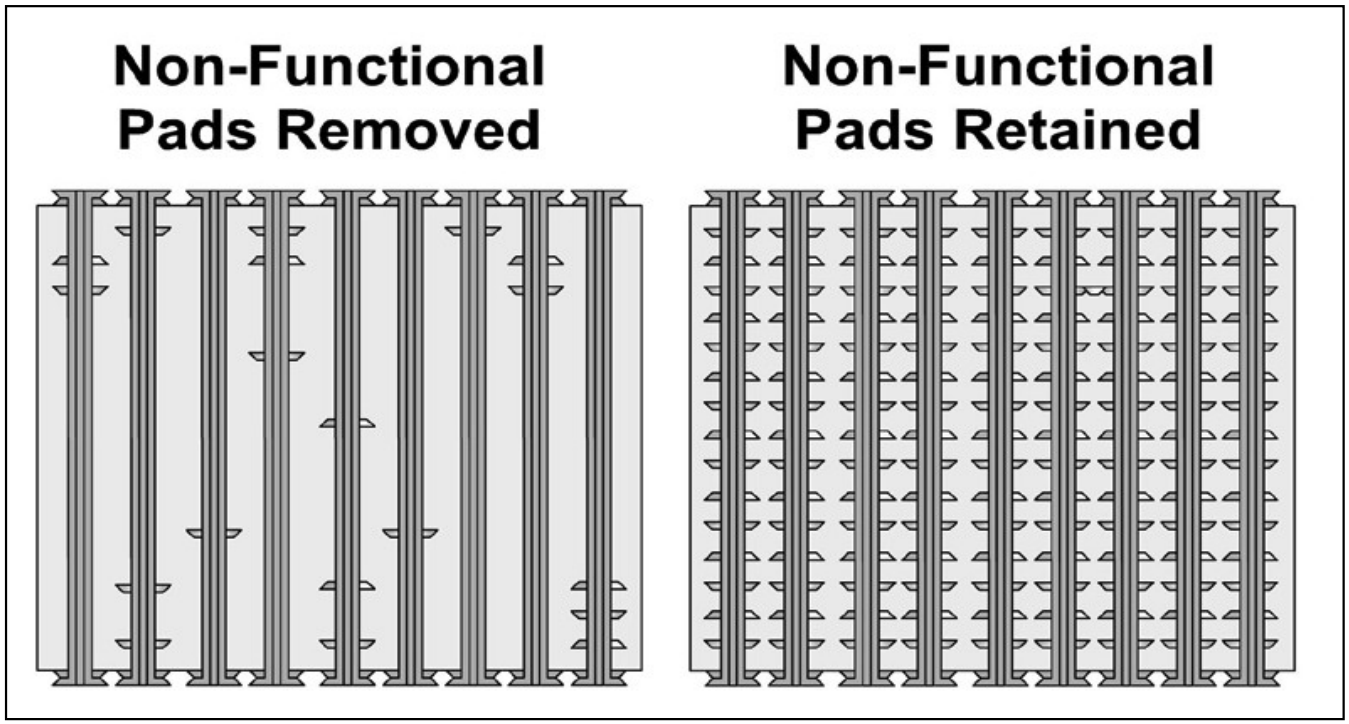
Grid sizes greater than 1.3mm (.050”) will have less delamination and more often they will exhibit material degradation.

With 1mm (.040”) we see delamination as the major material failure mode.

Grid sizes of .8mm (.032”) tend to have cohesive failures and grid sizes of .7mm (.020”) tend to have material failure due to crazing



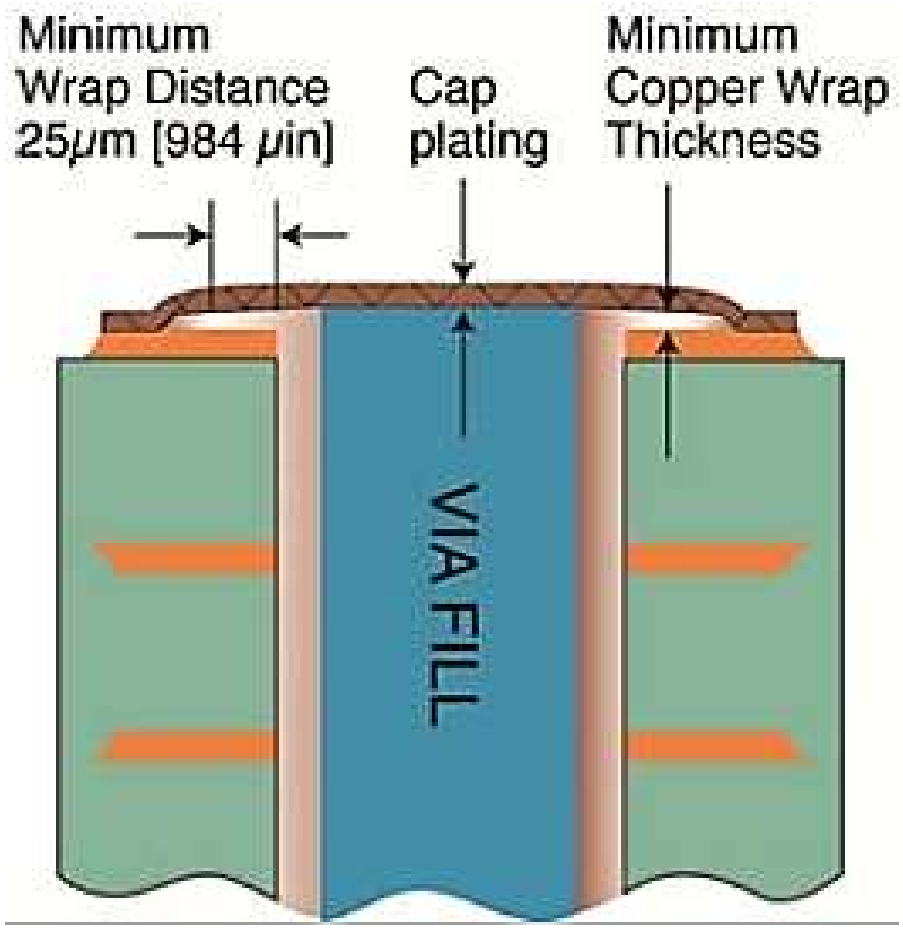
Non fuctional pads



Telegraphing
Low pressure areas
Dry weave/resin starvation

Wrap

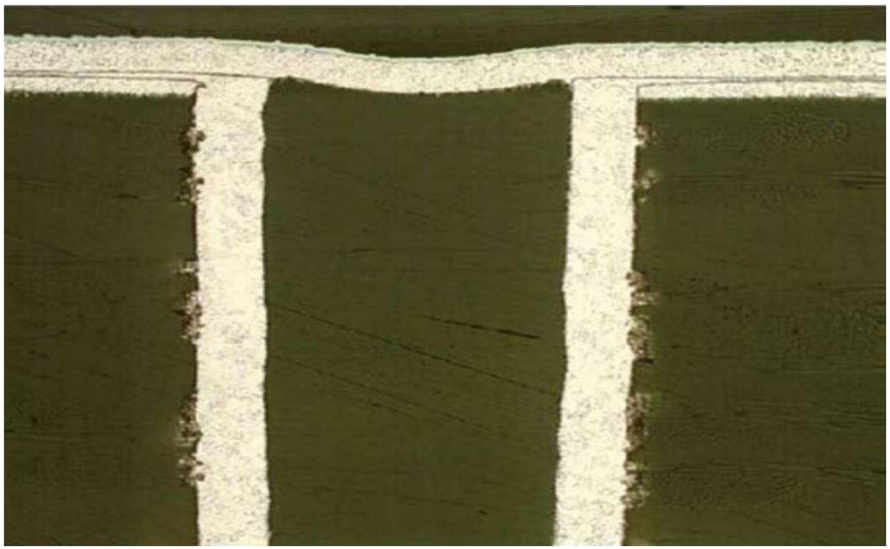
Copper Wrap

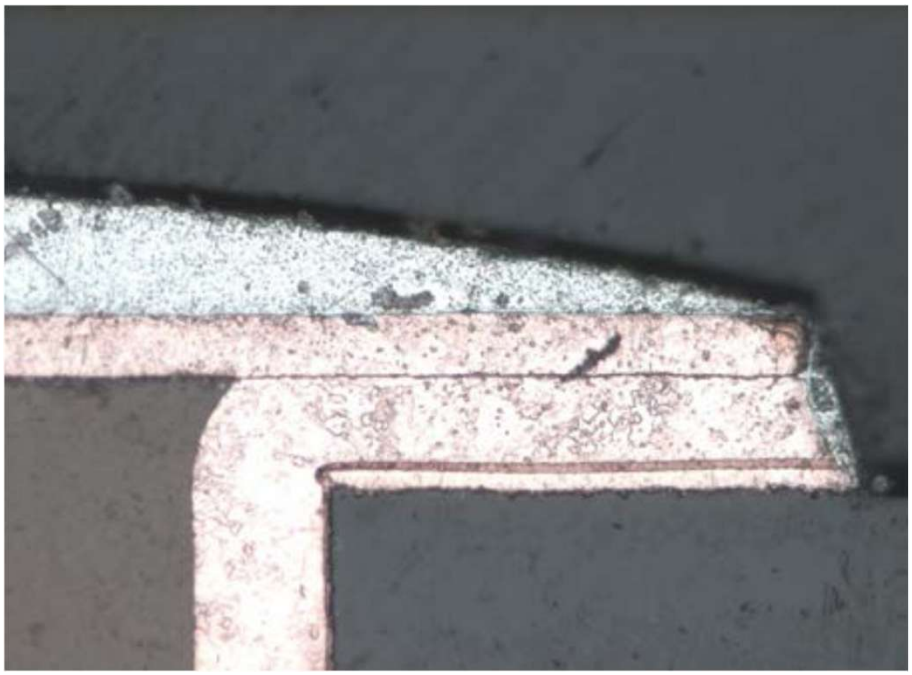

Minimum
Wrap Distance
25µm [984 µin]
Cap
plating
Minimum
Copper Wrap
Thickness
VIA FILL

Copper Wrap Plating

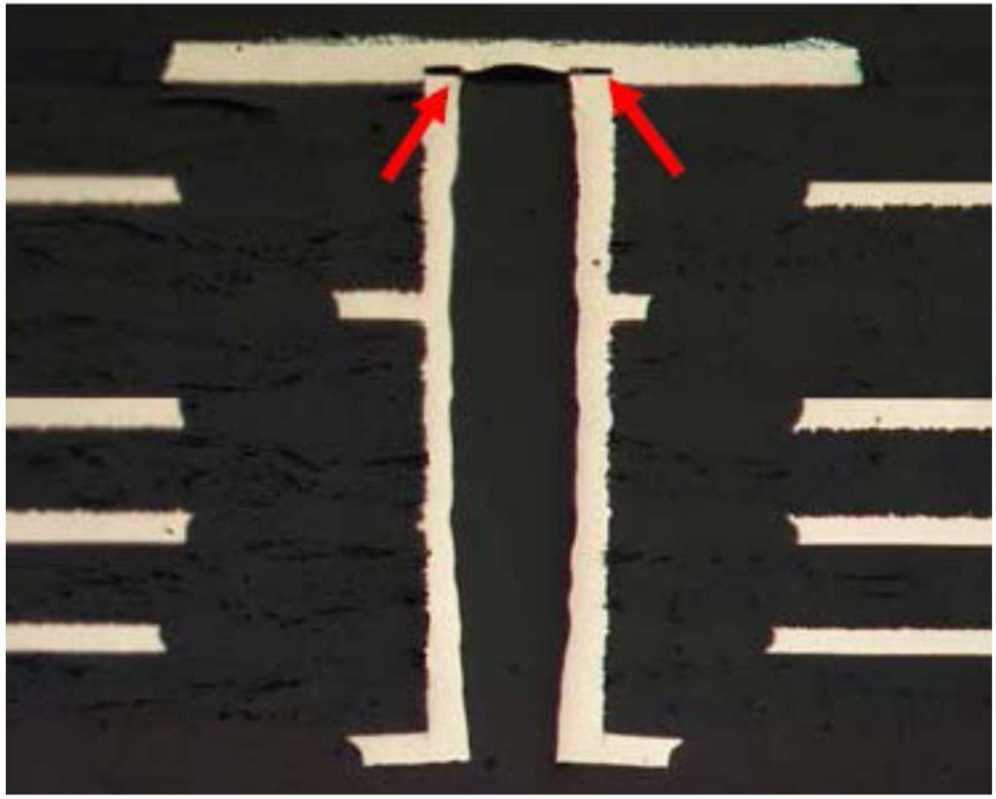
- Wrap plating is continuous from the filled plated hole onto the external surface and extends by a minimum of 25 µm [984 µin] where an annular ring is required

- Wrap thickness is not less than 7 µm [276 µin] for buried via cores (two layers)
- Reduction of surface wrap copper plating by processing (sanding, etching, planarization, etc.) does not result in insufficient wrap plating





Copper Wrap Plating

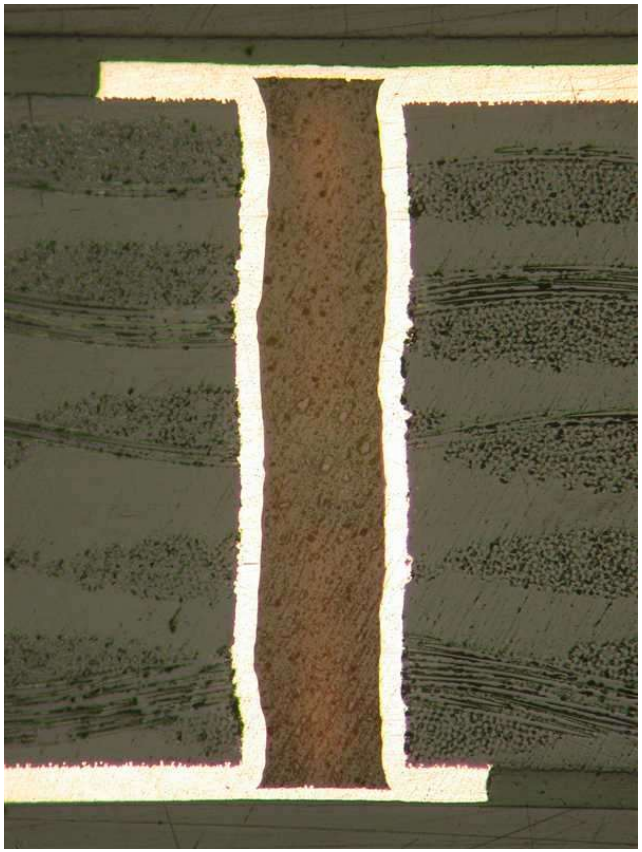


Copper Cap Plating of Filled Holes

When copper cap plating of filled holes (resin, conductive or non-conductive material, copper, etc.) for solderable lands (attachment of surface mount devices) is specified by the procurement documentation the following **shall** apply.

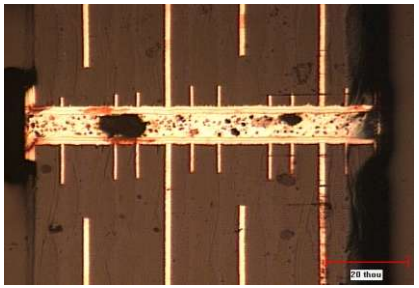
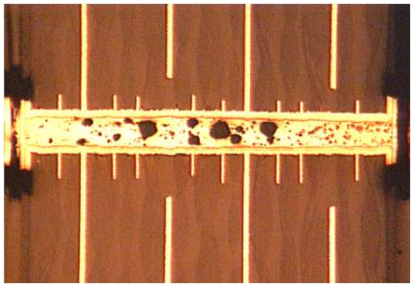
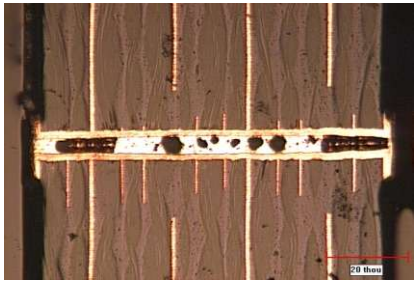
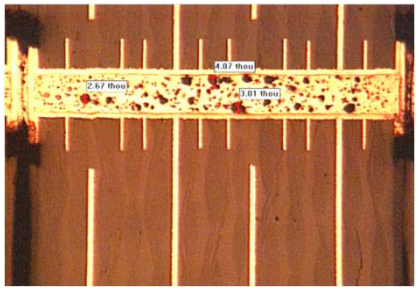
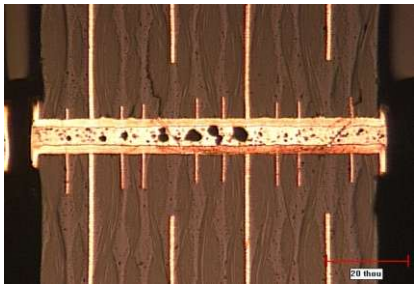
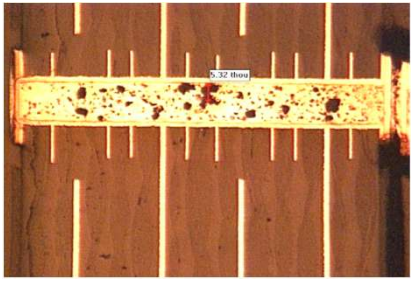
Target:

- Copper surface is planar with no protrusion (bump) and/or depression (dimple)

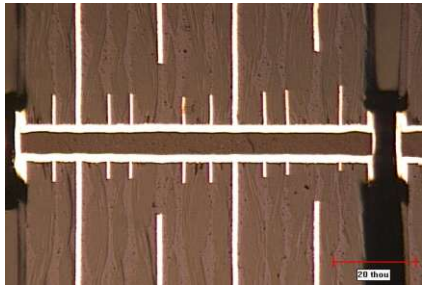
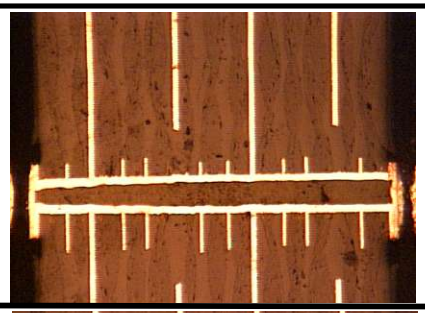
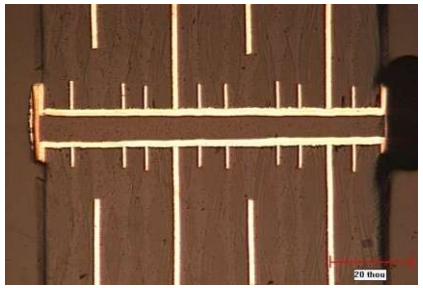
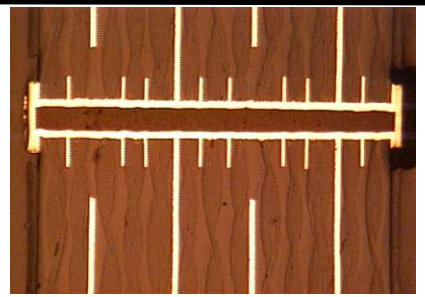


Via fill

Conductive Fill Results – DOE

Via Fill Material Supplier	Laminate Supplier A	Laminate Supplier B
Supplier A (Conductive)		
Supplier A (Conductive)		
Supplier A (Conductive)		

Non-Conductive Fill Results – DOE

Via Fill Material Supplier	Laminate Supplier A	Laminate Supplier B
Supplier E (Non-Conductive)		
Supplier E (Non-Conductive)		
Supplier E (Non-Conductive)